

# Using the i.MX RT FlexRAM

## 1. Introduction

This document describes the flexible memory array available on the i.MX RT MCUs. The first part of the document summarizes all features of the FlexRAM memory, including:

- Configuration of the bank array.
- Memory type size definition.
- Available memory controllers.
- Power domains and clocks.
- Interrupt request generation.

The second part of this document demonstrates the FlexRAM configuration usage on a specific application use case. It shows the things to consider in the application to fully utilize the FlexRAM memory in the i.MX RT1050 MCU. It focuses on the application memory capability from the performance point of view in a normal application runtime, as well as the low power feature implementation.

## Contents

1. Introduction .....	1
2. FlexRAM memory.....	2
2.1. FlexRAM configuration .....	3
2.2. FlexRAM memory controllers .....	6
2.3. FlexRAM module-related clocks and clock gates.....	8
2.4. FlexRAM power domains .....	8
2.5. FlexRAM interrupt .....	10
3. Using FlexRAM features in the application.....	12
3.1. FlexRAM configuration demonstration on iMX RT1050 devices .....	12
4. Revision history .....	22

## 2. FlexRAM memory

FlexRAM is a highly configurable and flexible RAM memory array. This memory array contains memory banks which can be independently configured to be accessed by different type of interfaces, such as I-TCM (Instruction-Tightly Coupled Memory), D-TCM (Data-Tightly Coupled Memory), or AXI (system). The memory bank can act as an ITCM, DTCM, or OCRM memory. There can also be up to three different power domains assigned to the dedicated bank or group of banks (PDRET, PDRAM0, PDRAM1) which can potentially reduce the power consumption in the low-power modes.

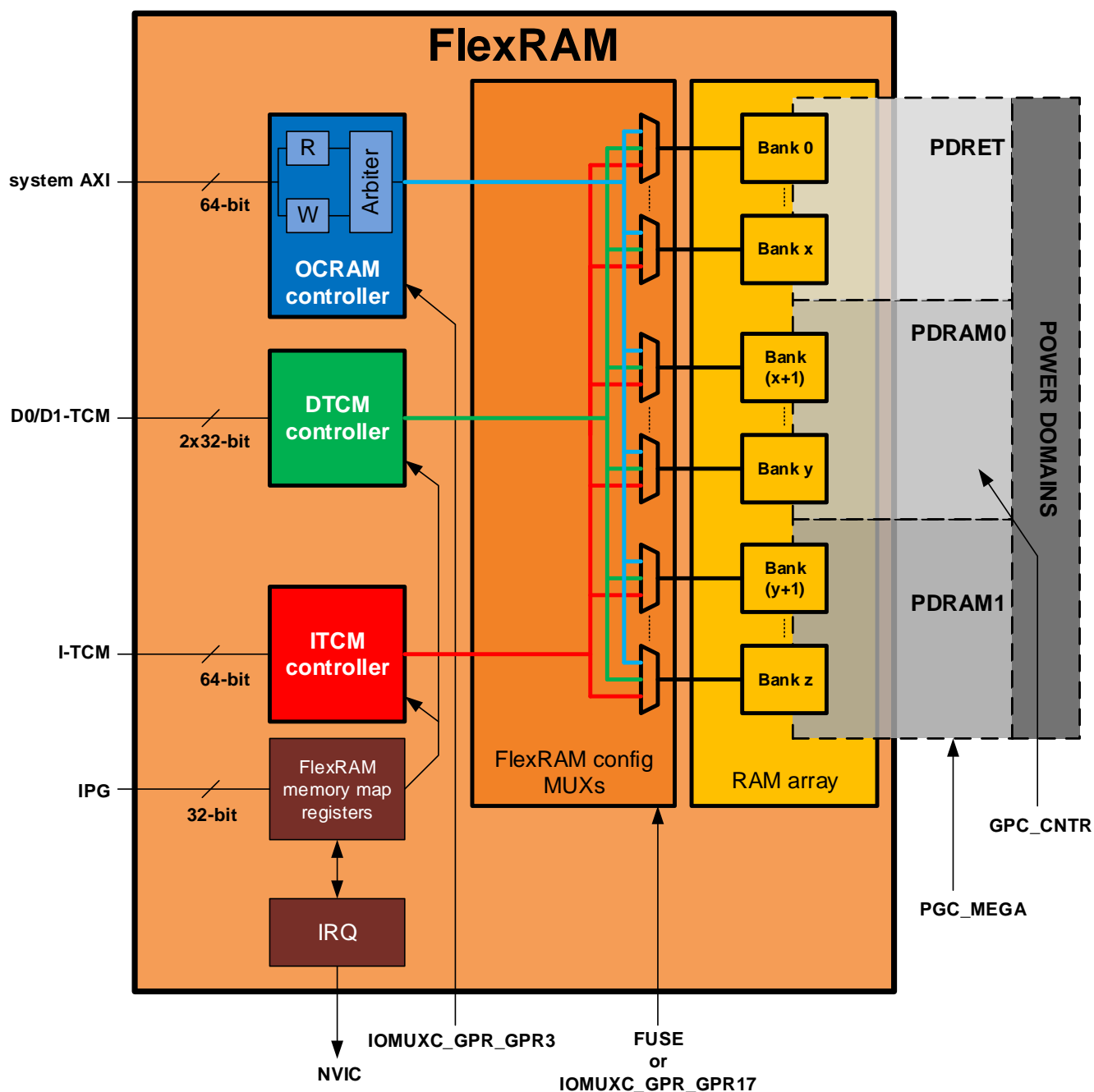


Figure 1. General block diagram of FlexRAM

**NOTE**

On some IMXRTxxxx devices, an additional OCRM (which is not part of the FlexRAM) can be found. It is used to increase the total on-chip memory size. This kind of memory is not considered in this document as it is not included in the FlexRAM array.

## 2.1. FlexRAM configuration

FlexRAM is a configurable memory RAM array which contains a number of banks.

### 2.1.1. FlexRAM memory bank configuration

Each bank in the FlexRAM array can be configured to act as:

- I-TCM (Instruction Tightly-Coupled Memory) accessed by the 64-bit I-TCM interface.
- D-TCM (Data Tightly-Coupled Memory) accessed by two 32-bit (D0 and D1) TCM interfaces in the interleaved fashion.
- OC RAM (On-Chip RAM memory) accessed by the 64-bit system AXI bus.

**NOTE**

All TCM interfaces run at the same frequency as the Arm® Cortex®-M7 core and are synchronous to each other.

The OCRM controller is connected through the 64-bit AXI bus to one slave port of the interconnect bus fabric (NIC). This slave port frequency is limited to ¼ of the core frequency. For example, if the Arm Cortex-M7 core runs at 528 MHz, then the AXI bus connected to the OCRM controller is limited to 132 MHz. Expect performance degradation in the data access to the OCRM in comparison to the xTCM memories. The L1 CACHE memory can help with that.

There are two sources to select the configuration of the FlexRAM banks:

- FUSE FlexRAM configuration value (default).
- FLEXRAM\_BANK\_CFG field value defined in the IOMUXC\_GPR\_GPR17 register.

The selection between these two sources is done by the value of the FLEXRAM\_BANK\_CFG\_SEL bit defined in the IOMUXC\_GPR\_PGR16 register. It is set to 0 by default and uses the fuse value for the FlexRAM configuration.

#### 2.1.1.1. Static configuration

The FUSE FlexRAM bank configuration value represents the static configuration of the FlexRAM banks because it cannot be changed after the device boots. The FUSE FlexRAM configuration value uses four fuses in the fusemap located at the 0x6D0 address in the [16-19]-bit position. [Table 1](#) shows an example of 16 possible configurations of the RT1050 FlexRAM banks based on a 4-bit fuse value. The default value is set to 0000, which represents the FlexRAM configuration 0 (see the example of iMXRT1050 in [Table 1](#)).

**NOTE**

The minimum configuration of OCRAM is 64 KB (see [Table 1](#)). This is required due to ROM code requires at least 64 KB of RAM for its execution. The minimum OCRAM requirements can be device dependent.

**Table 1. 16 possible configurations of FlexRAM banks using fuse value on i.MX RT1050**

	FUSE FlexRAM Configuration Value	IOMUXC_GPR_GPR17 (FLEXRAM_BANK_CFG) (binary)	Bank																OCRAM [kB]	DTCM [kB]	ITCM [kB]
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
0	0b0000	01010101101011111111101001010101	O	O	O	O	D	D	I	I	I	I	D	D	O	O	O	O	256	128	128
1	0b0001	01010101010110101111101001010101	O	O	O	O	D	D	I	I	D	D	O	O	O	O	O	O	320	128	64
2	0b0010	01011010111111111111111010010101	O	O	D	D	I	I	I	I	I	I	I	I	D	D	O	O	128	128	256
3	0b0011	01010101010101111010101001010101	O	O	O	D	D	D	I	O	O	O	O	O	O	O	O	O	352	128	32
4	0b0100	01010101010111111111101001010101	O	O	O	O	D	D	I	I	I	I	O	O	O	O	O	O	320	64	128
5	0b0101	01010101010101111110100101010101	O	O	O	O	D	D	I	I	O	O	O	O	O	O	O	O	384	64	64
6	0b0110	01010101111111111111111010010101	O	O	D	D	I	I	I	I	I	I	I	I	O	O	O	O	192	64	256
7	0b0111	111111111111111111111111111010101	O	O	I	I	I	I	I	I	I	I	I	I	I	I	I	I	64	0	448
8	0b1000	0101101010101111111110101010010101	O	O	D	D	D	D	I	I	I	I	D	D	D	D	O	O	128	256	128
9	0b1001	0101010110101010111110101010010101	O	O	D	D	D	D	I	I	D	D	D	D	O	O	O	O	192	256	64
10	0b1010	1010101011111111111111111010010101	O	O	D	D	I	I	I	I	I	I	I	I	D	D	D	D	64	192	256
11	0b1011	1010101010101010101010101010010101	O	O	D	D	D	D	D	D	D	D	D	D	D	D	D	D	64	448	0
12	0b1100	010101010101010111111111101010101	O	O	O	O	I	I	I	I	O	O	O	O	O	O	O	O	384	0	128
13	0b1101	0101010101010101010101111001010101	O	O	O	D	I	O	O	O	O	O	O	O	O	O	O	O	448	32	32
14	0b1110	010101010101111111111111111010101	O	O	I	I	I	I	I	I	I	I	O	O	O	O	O	O	256	0	256
15	0b1111	0101010101010101010101010101010101	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	512	0	0

O - OCRAM, D - DTCM, I - ITCM

**2.1.1.2. Runtime configuration**

The FlexRAM banks can be also configured at runtime by changing the value of the FLEXRAM\_BANK\_CFG field defined in the IOMUXC\_GPR\_GPR17 register. This is possible when the FLEXRAM\_BANK\_CFG\_SEL bit defined in the IOMUXC\_GPR\_GPR16 register is set to 1. In such case, the configuration of the FlexRAM banks is directly dependent on the value in the FLEXRAM\_BANK\_CFG field defined in the IOMUXC\_GPR\_GPR17 register and can be changed when the application runs.

The FlexRAM bank configuration value (FLEXRAM\_BANK\_CFG) is a 32-bit value. This 32-bit value includes the configuration values for each FlexRAM bank. Each FlexRAM bank uses two bits for the configuration:

- 00b—bank is not used.
- 01b—bank is configured for OCRAM.
- 10b—bank is configured for DTCM.
- 11b—bank is configured for ITCM.

The third column in [Table 1](#) shows the possible FLEXRAM\_BANK\_CFG field configuration values with respect to the static configuration done by the eFUSES.

**NOTE**

It is recommended to write the appropriate FlexRAM bank configuration value (FLEXRAM\_BANK\_CFG) into the IOMUXC\_GPR\_GPR17 register before switching from the bank configuration defined by fuses, that means before the FLEXRAM\_BANK\_CFG\_SEL bit is set to 1.

Configuring the memory in such way may potentially affect the application safety (stack overflow, invalid instruction execution, out of range access, and so on). Consider the code/data boundary locations properly to avoid application crashes. Also, the memory banks that are being re-configured are changing their access interfaces and still contain the same data. Consider at least 64 KB for the OCRAM configuration because the ROM code requires this portion of RAM for execution (stack/static data).

It is expected that:

- The part of code which performs the re-configuration is executed from a different kind of memory (for example, the QuadSPI flash accessed by the FlexSPI). The data accessed during FlexRAM re-configuration are also located in a different kind of memory (for example, SDRAM accessed by SEMC).
- The data/code in the re-configured banks are not required for the application program flow anymore.
- The re-configured banks should be re-filled with the initializer data/code before access (no stack/heap is expected there).
- The addressable memory spaces have changed (avoid potential application pointers to access that space).
- It is recommended to re-configure the FlexRAM array in the beginning of the start-up code (assembly code) executed from the external memory (FlexSPI/SEMC). It is expected that there will not be any access to the FlexRAM during this part of code execution. See [Section 3.1.3, “Software implementation”](#) for more details.

### 2.1.2. Definition of the memory type size

Each memory bank in the FlexRAM array has the same memory size which can be calculated as:

$$\text{bank size} = (\text{Total Flex RAM size}) / (\text{number of banks in FlexRAM array})$$

For example, the iMXRT1050 MCU has:

- A total FlexRAM size of 512 KB.
- 16 banks in the FlexRAM array (block0-block15).
- A bank size of  $512 \text{ KB} / 16 = 32 \text{ KB}$ .

The dedicated memory type (ITCM/DTCM/OCRAM) size can be easily calculated as:

$$\text{Memory type size} = (\text{number of banks configured to dedicated memory type}) * (\text{bank size})$$

The memory type size depends strictly on the application needs and, in total, can vary (based on the configuration) from 0 B to the total FlexRAM size. For example, on iMXRT1050, it can range from 0 to

512 KB. The specified memory type (ITCM/DTCM/OCRAM) does not have to be configured strictly in a continuous block of FlexRAM banks.

**Table 2. Example of non-continuous block of DTCM/OCRAM banks' configuration (i.MX RT1050)**

IOMUXC_GPR_GPR17 (FLEXRAM_BANK_CFG)	Bank																OCRAM	D-TCM	I-TCM
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
010110101111111111111111110100101	O	O	D	D	I	I	I	I	I	I	I	I	D	D	O	O	128	128	256

However, it still represents a continuous address space in the device memory map (see [Table 3](#)).

**Table 3. Example of memory type address space**

Memory type	Size [kB]	Address space	
		start	end
OCRAM	128	0x20200000	0x20220000
D-TCM	128	0x20000000	0x20020000
I-TCM	256	0x00000000	0x00040000

This feature enables you to configure the memory type and its size in accordance with the application needs from the power consumption aspect (see next part for more details).

### NOTE

The OCRAM cannot be configured to 0 kB due to the boot ROM code requirements. The 64 KB of OCRAM represents the minimum system requirement. The ITCM or DTCM can be configured to 0 KB (see also the possible static configuration shown in [Table 1](#)).

The Arm Cortex-M7 specifications require the size of ITCM/DTCM to be a power-of-two number, which can conflict with the FlexRAM configuration capability (see configurations 7, 10, 11 in [Table 1](#)). Avoid access to the empty RAM space configured by the corresponding FlexRAM configuration or use the recommended way, which defines the size of the TCM as a power-of-two number and reflect that by writing into the appropriate field in IOMUXC\_GPR\_GPR14->CM7\_CFGxTCMSZ (it will update the CM7\_xTCMCR accordingly).

If the requested ITCM/DTCM size is 0 Bytes, disable the corresponding TCM in IOMUXC\_GPR\_GPR16->INIT\_xTCM\_EN before configuring the size to 0 Bytes in IOMUXC\_GPR\_GPR14->CM7\_CFGxTCMSZ.

## 2.2. FlexRAM memory controllers

FlexRAM includes memory controllers responsible for converting the AXI (OCRAM) or TCM (I-TCM, D-TCM) interface signals into the RAM array interface signals. There are multiplexers between each memory controller (see FlexRAM config MUXs block in [Figure 1](#)) and each RAM array bank that are responsible for a proper connection of the memory controller and its RAM bank based on the FlexRAM configuration. These memory controllers also control the access to the memory.

### 2.2.1. TCM memories controllers

The TCM controller converts the TCM (64-bit I-TCM bus or 2x32-bit D-TCM buses) interface signals into an RAM array signal. The TCM interfaces are synchronized with the Cortex-M7 core and run at the same frequency. The TCM controller can also control the access to the RAM bank and affects the memory data access time (fetches the instructions on the I-TCM or accesses the data on the D-TCM). You may choose between two modes for both the read and write accesses:

- Fast access mode (default)—the access is expected to be done in one cycle.
- Wait access mode—the access is expected to be done in two cycles.

This can be done by enabling/disabling the appropriate access bit in the TCM control register (TCM\_CTRL) in the FlexRAM memory map:

- TCM\_RWAIT\_EN:
  - 0—fast mode selected.
  - 1—wait mode selected.
- TCM\_WWAIT\_EN:
  - 0—fast mode selected.
  - 1—wait mode selected.

The TCM controllers also include the dynamic clock gate control to reduce the power consumption when nothing is accessed.

### 2.2.2. OCRAM memory controller

The OCRAM memory acts as a slave port module connected to the 64-bit system AXI bus. It contains the OCRAM controller which handles the FlexRAM banks according to its configuration. The OCRAM controller converts the AXI interface signal to the RAM array signal. The read and write transactions are handled by two independent read and write control modules. The controller also contains an arbiter which takes control when two simultaneous requests come from both the read and write modules. The arbiter works in the round-robin scheme. The simultaneous read and write transactions are possible when targeted to different memory banks. When targeting the same bank, the read access gets a higher priority.

The OCRAM controller includes also features to avoid timing issues when the memory runs at a higher frequency. It supports adding the wait-states/pipeline into the memory access:

- Read/write address pipeline:
  - When enabled, this feature delays the reading/writing of an address from the AXI master by one cycle before it is accepted by the memory.
- Write data pipeline:
  - When enabled, this feature delays the writing of data from the AXI master by one cycle before it is accepted by the memory.
- Read data wait-state:
  - When enabled, this feature takes two cycles for each read access.

All previously mentioned features can be enabled/disabled by the corresponding OCRAM control bit (OCRAM\_CTL[3:0]) in the general-purpose register (IOMUXC\_GPR\_GPR3).

After performing any changes in the OCRAM control field (OCRAM\_CTL[3:0]) in the IOMUXC\_GPR\_GPR3 register, it is recommended to wait until the corresponded OCRAM status bit (OCRAM\_STATUS[19:16]) changes from 1 to 0 (1 means that the configuration is changed, but not applied yet).

### NOTE

The 64-bit AXI bus on the OCRAM controller slave port runs at one quarter of the Cortex-M7 core frequency. The interconnect bus fabric (NIC) runs at the same frequency. For example, if the Cortex-M7 core runs at 528 MHz, the OCRAM interface runs at 132 MHz. It is expected that the code which is changing and then checking the corresponding OCRAM status bit cannot be executed from the OCRAM.

## 2.3. FlexRAM module-related clocks and clock gates

The table below summarizes all clock related to FlexRAM module:

**Table 4. FlexRAM module**

Clock Name	Clock Source			peripheral interface / registers access clock			Clock gate
	Name	Default frequency	Maximum frequency	Name	Default frequency	Maximum frequency	
flexram_clk	module clock	6 MHz	600 MHz	ipg_clk_root	3 MHz	150 MHz	CCM_CCGR3[CG9] - flexram_clk_en
ocram_clk	ocram_exsc_aclk_exsc	3 MHz	150 MHz	ipg_clk_root	3 MHz	150 MHz	CCM_CCGR3[CG14] - ocram_clk_en

The FlexRAM clock (flexram\_clk) is the main clock the module is clocked by and is derived from the Arm core clock (core\_clk). The TCMs are fed by the same source clock. The on-chip RAM controller is fully synchronized to the system AXI interface and the clock for the OCRAM (ocram\_exsc\_clk) is derived from axi\_clk and further divided by 4. The last are the peripheral registers related to the FlexRAM module that are accessed by the peripheral bus (IPG interface). This part is clocked by the peripheral bus clock (ipg\_clk).

### NOTE

The interconnect bus fabric (NIC) is a bus matrix which interconnects the bus masters (like ARM AXIM, DMA, USB, ENET, uSDHC) with the bus slaves (OCRAM controller, ARM AHBS, FlexSPI module, SEMC, and so on). It runs at a quarter of the Arm Cortex-M7 core frequency. The OCRAM runs at the same frequency as the interconnect bus fabric.

## 2.4. FlexRAM power domains

The FlexRAM bank array can be partitioned into up to three different power sub-domains:

- PDRET domain.
- PDRAM0 domain.
- PDRAM1 domain.

Table 5 shows the state of the dedicated power domain in different low-power modes.



**Table 5. FlexRAM array power domains state in different low-power modes**

	System IDLE	Low Power IDLE	SUSPEND	SNVS
ARM core	WFI	WFI	power down	OFF
FlexRAM (PDRET)	ON	ON	ON	OFF
FlexRAM (PDRAM0)	ON	ON	ON/OFF	OFF
FlexRAM (PDRAM1)	ON/OFF	ON/OFF	Power Down	OFF

The main purpose to split the FlexRAM banks into different power domains is to save power when running in different power modes.

This power domain FlexRAM banks' assignment is device dependent, as shown in [Table 6](#).

**Table 6. Dedicated RT device power domain bank assignment**

RT device	Power domain bank assignment		
	PDRET	PDRAM0	PDRAM1
RT1050	Bank0	Bank1-Bank7	Bank8-Bank15
RT1020	Bank0-Bank7	-	-
RT1060/RT1064	-	Bank0-Bank15	-

### 2.4.1. PDRET power domain

This power domain is always on. It means that it is powered on down to the suspend mode. The only exception when the PDRET domain is powered off is the SNVS, which is a completely independent low-power domain usually supplied by a separate power supply (LiION battery).

### 2.4.2. PDRAM0 power domain

When the Arm core is powered off, this domain can be either powered on for data retention or powered off together with the core.

This feature is controllable via the FlexRAM PDRAM0 power gate enable (PDRAM0\_PGE) bit in the general power controller interface control (GPC\_CNTR) register. When this bit is set (default), the FlexRAM banks assigned to this domain keep their content even when the Arm core is powered down. When it is cleared, the PDRAM0 power domain is powered off when the Arm core is powered down.

### 2.4.3. PDRAM1 power domain

This domain's power gating is controlled via the power gate control mega (PGC\_MEGA) registers:

- Power sequence timing control:
  - Power-down sequence time (PGC\_MEGA\_PDNSCR):
    - Between the power-down request and asserting the isolation defined by the number of IPG cycles in the ISO value.
    - Between asserting the isolation and the negation of the power-toggle signal defined by

- the number of IPG cycles in the SW2ISO value.
- Power-up sequence time (PGC\_MEGA\_PUPSCR):
  - Between the power-up request and asserting the power-toggle signal defined by the number of IPG cycles in the ISO value.
  - Between asserting the power-toggle signal and the negation of isolation defined by the number of IPG cycles in the SW2ISO value.
- Power control (PGC\_MEGA\_CTRL):
  - Controls whether the power-down request signal switches the power for this domain on or off.

### NOTE

The critical data that are considered to be retained even in the suspend mode must be placed into the FlexRAM banks assigned to the PDRET power domain (if available).

## 2.5. FlexRAM interrupt

The FlexRAM module can generate interrupt requests based on two different events:

- Not allocated address access (address out of range).
- Magic address read/write access hit (not supported on all RT devices, see the corresponding reference manual for details).

The interrupt request signal is generated based on its configuration in the interrupt enable register (INT\_SIG\_EN). Each memory type (OCRAM/DTCM/ITCM) has its dedicated bit in this register for enabling the unallocated address access or the magic address access:

- OCRM\_ERR\_SIG\_EN/OCRAM\_MAM\_SIG\_EN – when set, it enables the generation of the OCRM out of address range/magic address access interrupt signal.
- DTCM\_ERR\_SIG\_EN/DTCM\_MAM\_SIG\_EN – when set, it enables the generation of the DTCM out of address range/magic address access interrupt signal.
- ITCM\_ERR\_SIG\_EN/ITCM\_MAM\_SIG\_EN – when set, it enables the generation of the ITCM out of address range/magic address access interrupt signal.

All these error signals are ORed (if enabled) and they generate one interrupt request to the NVIC with number 38.

Because there is just one interrupt vector for all these events, it is required to identify the dedicated source of event in the interrupt service routine by reading the appropriate bit in the interrupt status register (INT\_STATUS):

- OCRM\_ERR\_STATUS/OCRAM\_MAM\_STATUS – when set, it indicates that the OCRM out of address range/magic address access is generated.
- DTCM\_ERR\_STATUS DTCM\_MAM\_STATUS – when set, it indicates that the DTCM out of address range/magic address access is generated.
- ITCM\_ERR\_STATUS/ITCM\_MAM\_STATUS – when set, it indicates that the ITCM out of address range/magic address access is generated.

Each status bit can be cleared by writing a log. 1 into it.

The assertion of the status bits is conditioned by enabling the dedicated memory type bit in the interrupt status enable register (INT\_STAT\_EN):

- OCRM\_ERR\_STAT\_EN/OCRAM\_MAM\_STAT\_EN – when set, it indicates that the OCRM out of address range/magic address access interrupt status is granted.
- DTCM\_ERR\_STAT\_EN/DTCM\_MAM\_STAT\_EN – when set, it indicates that the DTCM out of address range/magic address access interrupt status is granted.
- ITCM\_ERR\_STAT\_EN/ITCM\_MAM\_STAT\_EN – when set, it indicates that the ITCM out of address range/magic address access interrupt status is granted.

Some of iMX RT devices can also generate a FlexRAM dedicated interrupt when there is a specific software defined address access hit.

The address and access type are user-defined in the magic address registers. A dedicated memory type (ITCM/DTCM/OCRAM) magic address register contains two fields; one for the magic address definition and one for the selection of the access type (read or write):

- OCRM\_MAGIC\_ADDR:
  - The OCRM\_MAGIC\_ADDR field represents a 16-bit address within the OCRM memory mapped address space.
  - OCRM\_WR\_RD\_SEL:
    - 0 – sets the interrupt generation for read access.
    - 1 – sets the interrupt generation for write access.
- DTCM\_MAGIC\_ADDR:
  - The DTCM\_MAGIC\_ADDR field represents a 16-bit address within the DTCM memory mapped address space.
  - DTCM\_WR\_RD\_SEL:
    - 0 – sets the interrupt generation for read access.
    - 1 – sets the interrupt generation for write access.
- ITCM\_MAGIC\_ADDR:
  - The ITCM\_MAGIC\_ADDR field represents a 16-bit address within the ITCM memory mapped address space.
  - ITCM\_WR\_RD\_SEL:
    - 0 – sets the interrupt generation for read access.
    - 1 – sets the interrupt generation for write access.

### 3. Using FlexRAM features in the application

The FlexRAM memory implemented on the i.MX RT devices provides a big advantage when compared to devices with single on-chip memories. Depending on the application memory footprint (code/constant data/static data/stack, and so on), it is possible to reconfigure the on-chip memory and make the device more suitable for the application. This can be very useful for different applications built on the same hardware platform (for example). This approach is very attractive nowadays because it saves the development time/cost/production time and rapidly reduces the time to market.

The next sub-sections describe the flexibility of the FlexRAM from the application point of view.

It focuses on one specific configuration technique from the time perspective. It demonstrates the combination of the static and dynamic configurations of the FlexRAM memory. It cannot be called a static configuration because it does not use the fuse default configuration, which happens immediately after the device boot. This approach cannot be used due to the unavailable configuration in the fuse table (see [Table 1](#)) required by the application use case. It is not truly dynamic because it does not change the configuration during application run-time. It configures the FlexRAM memory in the application startup (just before calling the static data and read-write code initialization) and it keeps the start-up setting after that. It is possible to make the FlexRAM configuration decision based on the memory footprint requirements which can be identified during the application building time.

#### 3.1. FlexRAM configuration demonstration on iMX RT1050 devices

The application use case of the FlexRAM configuration described here represents the case when the definition of a memory section size is more precisely identified according to the application code compiler/linker outputs. The size of the ITCM/DTCM/OCRAM memory depends on how much code/constant data/static data/stack memory the application requires. It is similar to the static configuration described at the beginning of this document.

##### 3.1.1. External memory versus FlexRAM memory access consideration

The i.MX RT10xx devices do not have embedded flash (RT1064 includes serial SPI flash as SIP). An unlimited size of code/data can be loaded into the external memory. It is limited only by the external RAM region (1 GB) defined by Arm (0x6000 0000 – 0x9FFF FFFF). On the i.MX RT devices, the external memory is accessible by the FlexSPI/SEMC interfaces (and other). These interfaces are not fast enough to execute the code/access the data without a penalty in the wait states when running at a maximum frequency (considering a case when the core runs at 600 MHz and the FlexSPI at a maximum of 166 MHz (DDR mode) or SEMC at 166 MHz and the L1 I/D cache cannot cover all the code/data). On the other hand, the execution of code/the access to data from the TCMs can be considered as a single cycle (see the exceptions in the above sections).

It is also important to consider what code/data can be placed into the external memory before the FlexRAM configuration. The most critical code to execute as fast as possible (without the wait states to fully utilize the super-scalar pipeline nature of Cortex-M7) must be placed into the ITCM (Harvard bus architecture nature is preferred in this consideration). The less important data (accessed sporadically) should be placed in the external memory. The data that is accessible only by the core (stack, static data, and so on) must be placed into the DTCM. The Cortex-M7 core also supports direct access to the TCM through the AHBS interface. The DMA master can still access the TCM through the AHBS. However,

the access is not as fast as the access by the core. It shall be used when the core is sleeping/powered down.

The data accessed by more than one bus master (for example; the core and DMA) should be placed in the OCRM, especially when it is accessed by the DMA in the low-power modes.

Consider all above-mentioned features in the application memory footprint before the FlexRAM configuration.

### 3.1.2. FlexRAM configuration

The FlexRAM configuration must take the linker-defined memory section sizes into account. The definition of section sizes can be adjusted according to the application needs during the application development. The FlexRAM configuration may reflect the linker sections definition.

Here are some application examples:

- Sensing the image from a camera (using the CSI module) with a resolution of 320x240 in the 5-6-5 RGB mode.
- Storing two raw-data images in the data buffers using the DMA module and displaying them dynamically using the DMA on the LCD module.
- Processing an image (only software-based) with the results of an image stored in a 30-KB data buffer.
- The image processing must be done as fast as possible.
- Store the last four images' processing data results (4 x 30-KB data buffers).
- The last processed image data results must be available in the memory after waking up from the stop mode.
- There are three additional data buffers in the same raw image data format which are displayed sporadically (application idle state).

Assumption: during the project development, the application software requires:

**Table 7. Requirements**

CODE	DATA
120 KB	889 KB

#### 3.1.2.1. Code memory footprint

The interrupt vector table and a couple of critical interrupt service routines must be placed in the ITCM (a 64-bit single-cycle access memory can pre-fetch 64-bit, 4 x 16-bit, or 2 x 32-bit instructions) to speed up its execution time. The interrupt vectors and corresponding interrupt service routines take 46 kB of memory.

### 3.1.2.2. Static data memory footprint

There are two 150-KB data buffers that contain the raw data from the image sensor (320x240 in the RGB 5-6-5 format).

#### NOTE

These buffers are considered critical data from the processing point of view. That kind of data are usually stored in the external SDRAM memory. There is a significantly faster access time to the OCRM than to the SDRAM and the cost efficiency from the customer point of view is considered. It is recommended to fully utilize the on-chip memory (if possible).

These buffers are filled by the DMA channel and triggered by the camera sensor interface module (in a ping-pong fashion). They are also read by the core and processed. It is convenient to place these data buffers into the OCRM which is accessed by the 64-bit system AXI bus.

#### NOTE

The OCRM is a cacheable memory. Care must be taken when both masters access the same memory region which is cacheable. It is recommended to disable the dedicated cache region in such case. If the cache is enabled, the software is responsible to ensure the synchronization of access for both masters.

The additional four data buffers are 30 KB in size and contain the resulting data of the image processing done by the core. These buffers are accessed only by the core and it is recommended to place these buffers into the DTCM memory that is accessed directly by the core data request. The remaining application static data (initialized, non-initialized, or initialized to zero) is handled only by the core and 15 KB in size. The best location for such data is the DTCM.

There are also three 150-KB constant data buffers (for example, static LCD images) which are displayed sporadically, based on the stand-by mode calling in the application. These buffers can be stored in an external type of memory.

Using the stack usage analyses (for example, [www.iar.com/support/resources/articles/mastering-stack-and-heap-for-system-reliability](http://www.iar.com/support/resources/articles/mastering-stack-and-heap-for-system-reliability)), the stack size is estimated to be 4 KB (10 % addition included). It is recommended to place the stack into the DTCM because it is accessed only by the core.

### 3.1.2.3. Total memory footprint (i.MX RT1050)

Considering the above assumptions when using the i.MX RT1050 device, it can be summarized:

**Table 8. Application memory section requirements**

	CODE		DATA			
	RO	RW	RO	RW	RW	RW
			constants	static (CPU only)	stack	static (all bus masters)
Memory size requirements	74	46	150	30	4	150
			150	30		150
			150	30		
				30		
				15		
In total	74	46	450	135	4	300

The total RAM memory requirement (in this case) is 483 KB. It fits into the i.MX RT1050 device with a 512-KB memory. However, when it is re-calculated into the 32-KB bank size, it is 544 kB, which means one more bank is required (see [Table 9](#)). According to the Arm TCM size configuration specification, the size of TCM can be the number of power of two (32 KB, 64 KB, 128 KB, 256 KB, or 512 KB).

**Table 9. Application memory section assignments based on previous table**

	External memory	ITCM	External memory	DTCM	OCRAM	In TOTAL memory / banks
Memory size requirements	74	46	450	139	300	485
Number of FlexRAM banks required		2		5	10	17
Total size of memory		64		160	320	544

In this case, it is considered to think about moving 15 KB of static data from the DTCM to the OCRAM (or ITCM). It depends on:

- OCRAM: the DMA channels loading the OCRAM controller write (CSI)/read (LCD) via the system AXI bus.
- ITCM: access to static data is not required in low-power modes.
- The effect on the overall performance.

If the approach of moving data from the DTCM to the OCRAM does not significantly affect the overall performance, then it can be done and fits into the FlexRAM memory configuration (see [Table 3](#)). If the approach cannot be applied due to performance degradation, then the solution of moving data to the ITCM can be applied.

[Table 10](#) shows the case when the application static data are moved from the DTCM memory to the OCRAM memory, considering no significant effect on performance.

**Table 10. Application memory section requirements when application static data moved to OCRAM**

	External memory	ITCM	External memory	DTCM	OCRAM	In TOTAL memory / banks
Memory size requirements	74	46	450	139-15	300+15	485
Number of FlexRAM banks required		2		4	10	16
Total size of memory		64		128	320	512

Both memory re-configurations (Table 10 and Table 11) fit into the i.MX RT1050 FlexRAM and all 16 banks are used.

**Table 11. Application memory section requirements when application static data moved to ITCM**

	External memory	ITCM	External memory	DTCM	OCRAM	In TOTAL memory / banks
Memory size requirements	74	46+15	450	139-15	300	485
Number of FlexRAM banks required		2		4	10	16
Total size of memory		64		128	320	512

The number of banks for each memory type configuration are known. However, it is still not clear what bank number uses what configuration. This depends on the application needs from the low-power view, because there are three different power domains used for the corresponding bank/bank groups. The features of the i.MX RT1050 FlexRAM power distribution (power sub-domains) can be utilized in the low-power modes of application. In this case, the application requires to retain the data of the last processed imaged data buffer. The size of this buffer (30 KB) fits into the size of one bank (32 KB). The FlexRAM bank 0 is in the PDRET power domain and keeps the data content down to the suspend mode. The FlexRAM bank 0 can be used to store the last image processed result data buffer content. The remaining memory is used only in the normal run power mode.

Table 12 shows detailed configuration of FlexRAM bank for this example. The figures 2-4 shows also the starting addresses and the content of the individual memory configuration.



Table 12. Application example of FlexRAM banks configuration

FlexRAM bank	Configuration	Size	Power domain
Bank0	DTCM	128 KB	PDRET
Bank1	DTCM		PDRAM0
Bank2	DTCM		
Bank3	DTCM		
Bank4	ITCM	64 KB	
Bank5	ITCM		
Bank6	OCRAM	320 KB	PDRAM1
Bank7	OCRAM		
Bank8	OCRAM		
Bank9	OCRAM		
Bank10	OCRAM		
Bank11	OCRAM		
Bank12	OCRAM		
Bank13	OCRAM		
Bank14	OCRAM		
Bank15	OCRAM		

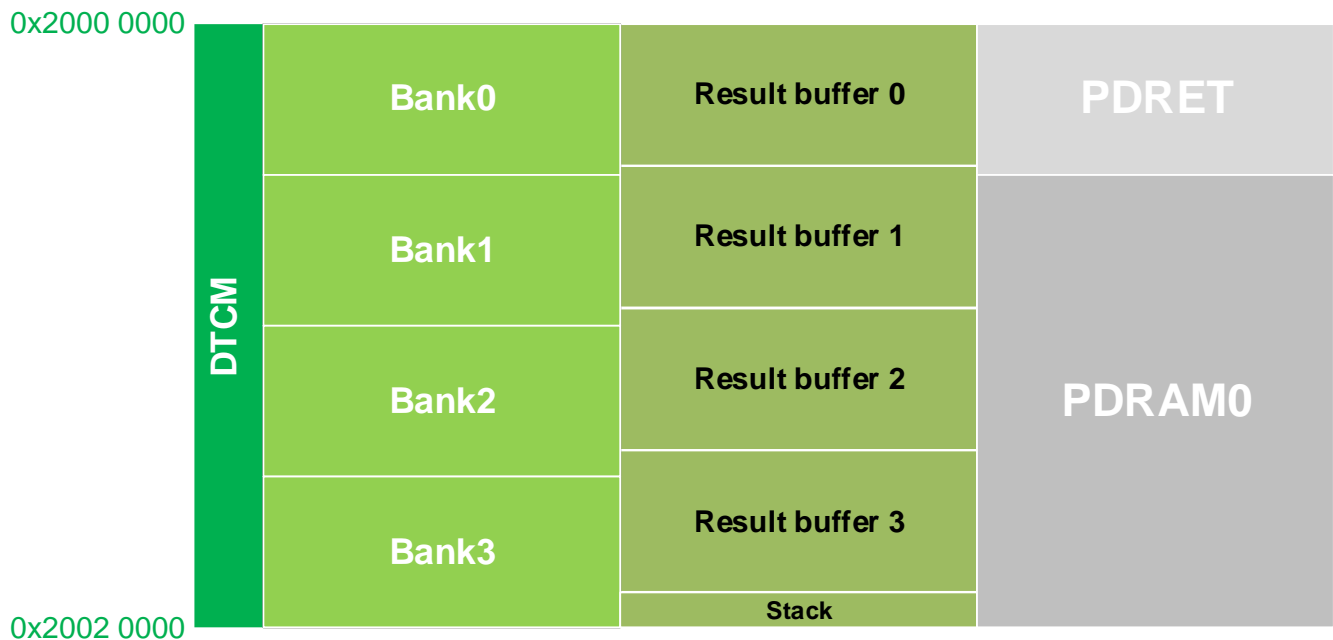


Figure 2. DTCM memory addresses, configuration, content, and appropriate power domain

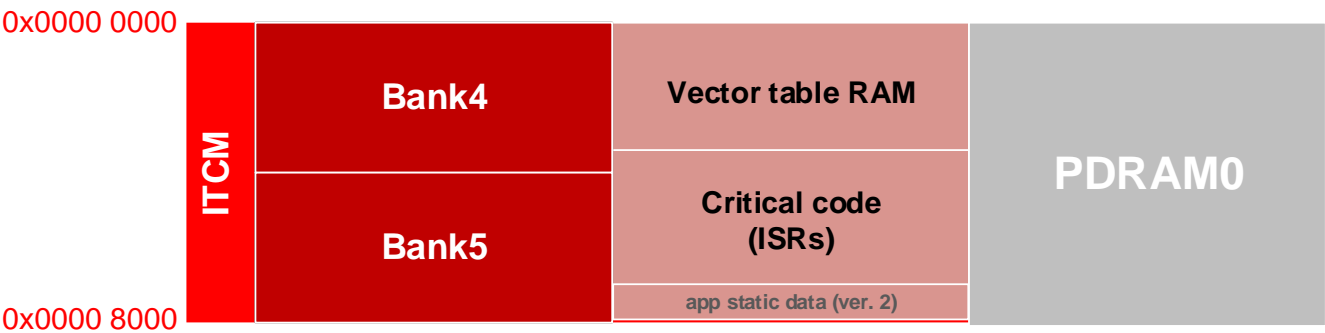


Figure 3. ITCM memory addresses, configuration, content, and appropriate power domain

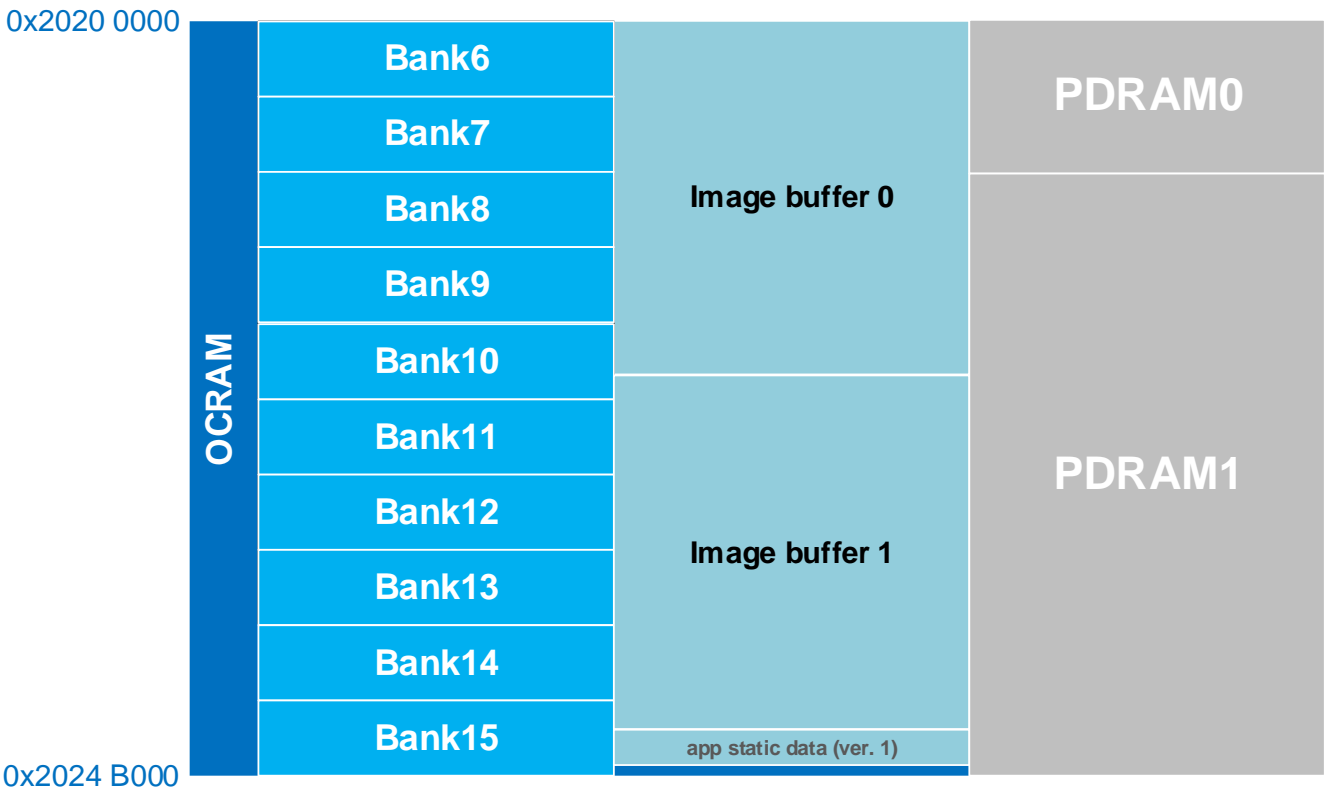


Figure 4. OCRM memory addresses, configuration, content, and appropriate power domain

As shown in [Table 1](#), there is no valid FlexRAM configuration available in the fuse default setting aligned with the configuration required by this use case. The static configuration cannot be utilized here. However, it is possible to configure the FlexRAM by the run-time configuration approach defined in [Section 2.1, “FlexRAM configuration”](#). This configuration must be done before the start-up code calls the static data and r/w code initialization.

The final FlexRAM configuration value will be 0x55555FAA:

IOMUXC_GPR_GPR17 (FLEXRAM_BANK_CFG)	Bank																OCRAM	D-TCM	I-TCM
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
01010101010101010101111110101010	D	D	D	D	I	I	O	O	O	O	O	O	O	O	O	O	320	128	64

**NOTE**

Consider the release (no debug) target configuration of the application project when compiling.

**3.1.3. Software implementation**

The best place for FlexRAM configuration in the application software is the start-up code before the execution of static variable initialization, RW code initialization (if considered in TCM/OCRAM), vector table relocation, any stack access (PUSH/POP), and so on. The start-up code shall be executed from a different kind of memory; for example, external serial flash. During the FlexRAM configuration code execution, the ITCM/DTCM/OCRAM memory cannot be accessed and the interrupts shall be disabled (to avoid stacking/unstacking).

**NOTE**

It is possible to process the FlexRAM reconfiguration in the application run-time; for example, code located in the external serial flash (FlexSPI) or all data including the stack/heap in the external SDRAM (SEMC). Make sure to avoid data overlapping, access mismatch, and so on after the FlexRAM release. It is not recommended to reconfigure the FlexRAM memory using DCD (Device Configuration Data) due to a potential conflict with the ROM code memory allocation.

**3.1.3.1. Considering Cortex-M7 TCM size limitations**

The TCM-size Arm specification considers the size of TCM in a power-of-two number (in case of iMXRTxxxx FlexRAM, it is 0 k/32 k/64 k/128 k/256 k/512 k). The application use case mentioned above considers these limitations. In this case, the application software after the power-on reset event performs these steps:

1. Ensure that there is no access to any of the banks in the FlexRAM array during its reconfiguration code execution:
  - Execute the code from memory outside the FlexRAM array (OCRAM not included in FlexRAM, QSPI, SDRAM, and so on).
  - Disable the interrupts.
2. Configure the FlexRAM bank array according to application needs:
  - Use the FLEXRAM\_BANK\_CFG field in the IOMUXC\_GPR\_GPR17 register.
3. Switch from eFuse-defined FlexRAM configuration to user-defined FlexRAM configuration:
  - Use the FLEXRAM\_BANK\_CFG\_SEL field in the IOMUXC\_GPR\_GPR16 register.
4. If there is a request to have 0 kB of any TCM memory, disable the corresponding TCM before setting the size to 0 kB. If not, omit this step:
  - Use the INT\_xTCM\_EN fields in the IOMUXC\_GPR\_GPR16 register to disable the corresponding xTCM memory before configuring it to 0 kB.
5. Configure the dedicated TCM memory size to the application-required size in a power-of-two number according to the Arm specification.

- Use the CM7\_CFGxTCMSZ fields in the IOMUXC\_GPR\_GPR14 registers to configure the size to 0 k/32 k/64 k/128 k/256 k/512 k.

#### **NOTE**

It is possible to configure the TCM size into a lower size (4 k/8 k/16 k). The FlexRAM bank has a higher size (32 k). In such case, the FlexRAM is not utilized effectively because there is a part of available memory not accessible by the core. A bus fault is generated when accessing (read/write) unallocated memory space. The Cortex-M7 base register CM7\_xTCMCR is updated according to this setting.

6. Run/Jump into the full memory-defined application code.

```

__iomux_gpr14_adr EQU 0x400AC038
__iomux_gpr16_adr EQU 0x400AC040
__iomux_gpr17_adr EQU 0x400AC044
__flexram_bank_cfg EQU 0x55555FAA
__flexram_itcm_size EQU 0x7 ; 64kB
__flexram_dtcn_size EQU 0x8 ; 128k

Reset_Handler
    CPSID I ; Mask interrupts

#ifdef FLEXRAM_CFG_ENABLE
    LDR R0,=__iomux_gpr17_adr ; load IOMUXC_GPR17 register address to R0
    MOV32 R1,__flexram_bank_cfg ; move FlexRAM configuration value to R1
    STR R1,[R0]
    LDR R0,__iomux_gpr16_adr ; load IOMUXC_GPR16 register address to R0
    LDR R1,[R0] ; load IOMUXC_GPR16 register value to R0
    ORR R1, R1, #4 ; set corresponding FLEXRAM_BANK_CFG_SEL bit
    STR R1,[R0] ; store the value to IOMUXC_GPR16 (user defined FlexRAM cfg enabled)
#endif

#ifdef FLEXRAM_ITCM_ZERO_SIZE
    LDR R0,__iomux_gpr16_adr ; load IOMUXC_GPR16 register address to R0
    LDR R1,[R0] ; load IOMUXC_GPR16 register value to R0
    AND R1, R1, #0xFFFFF0 ; clear corresponding INIT_ITCM_EN bit
    STR R1,[R0] ; store the value to IOMUXC_GPR16 (disable ITCM)
#endif

#ifdef FLEXRAM_DTCM_ZERO_SIZE
    LDR R0,__iomux_gpr16_adr ; load IOMUXC_GPR16 register address to R0
    LDR R1,[R0] ; load IOMUXC_GPR16 register value to R0
    AND R1, R1, #0xFFFFF0 ; clear corresponding INIT_DTCM_EN bit
    STR R1,[R0] ; store the value to IOMUXC_GPR16 (disable DTCM)
#endif

    LDR R0,__iomux_gpr14_adr ; load IOMUXC_GPR16 register address to R0
    LDR R1,[R0] ; load IOMUXC_GPR16 register value to R0
    MOVT R1, #0x0000 ; clear upper halfword of IOMUXC_GPR16 register
    MOV R2, #__flexram_itcm_size
    MOV R3, #__flexram_dtcn_size
    LSL R2, R2, #16
    LSL R3, R3, #20
    ORR R1, R2, R3
    STR R1,[R0] ; store the value to IOMUXC_GPR16 (disable DTCM)

#ifdef
    LDR R0,=0xE000ED08
    LDR R1,=__vector_table
    STR R1,[R0]
    LDR R2,[R1]
    MSR MSP, R2
    LDR R0,=SystemInit
    BLX R0
    CPSIE I ; Unmask interrupts
    LDR R0,=__iar_program_start
    BX R0

```

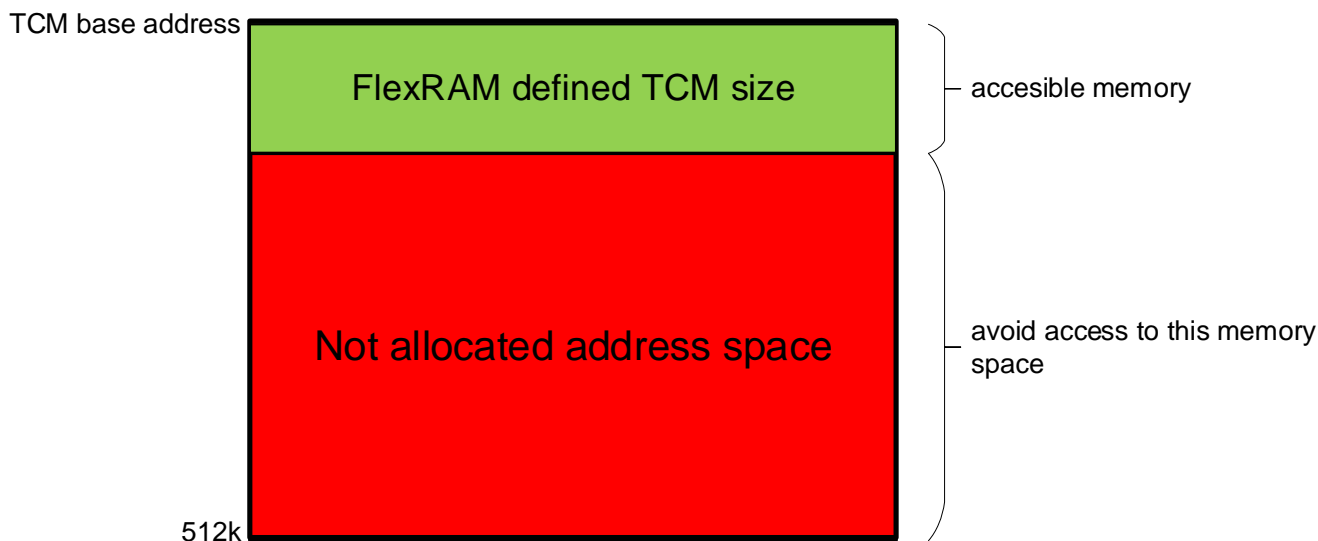
Figure 5. Example of the assembly code following previous rules

### 3.1.3.2. Ignoring Cortex-M7 TCM size limitations

This approach considers that the application software is aware of unallocated address space and avoids access to that space. The advantage of this approach is that the TCM memory does not need to consider the size in a power-of-two number.

Considerations:

- It is required to keep the default TCM size setting in the CM7\_CFGxTCMSZ fields in the IOMUXC\_GPR\_GPR14 register (it considers the value of the whole FlexRAM size).
- The software must avoid accessing unallocated address space.



**Figure 6. Example of accessible and non-accessible address space**

The software implementation can be similar to the previous case, excluding point 5 and the power-of-two size consideration.

## 4. Revision history

Table summarizes the changes done to this document since the initial release.

**Table 13. Revision history**

Revision number	Date	Substantive changes
0	10/2017	Initial release
1	08/2018	Added <a href="#">Section 3.1.3, "Software implementation"</a> . Added support for additional RT10xx devices.

**How to Reach Us:**

**Home Page:**

[www.nxp.com](http://www.nxp.com)

**Web Support:**

[www.nxp.com/support](http://www.nxp.com/support)

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address:

[www.nxp.com/SalesTermsandConditions](http://www.nxp.com/SalesTermsandConditions).

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C 5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. Arm, AMBA, Arm Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and  $\mu$ Vision are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. Arm7, Arm9, Arm11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, Mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2018 NXP B.V.

Document Number: AN12077

Rev. 1

08/2018

