Schematic: RT-M7

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03	Main Power
04	MCU Power
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07	Boot CFG / LCD / LED / BUT
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Revision History

DATE	REVISION	DESCRIPTION
2018/04/19	RT-M7 SCH v1.0 180419	Initial Release

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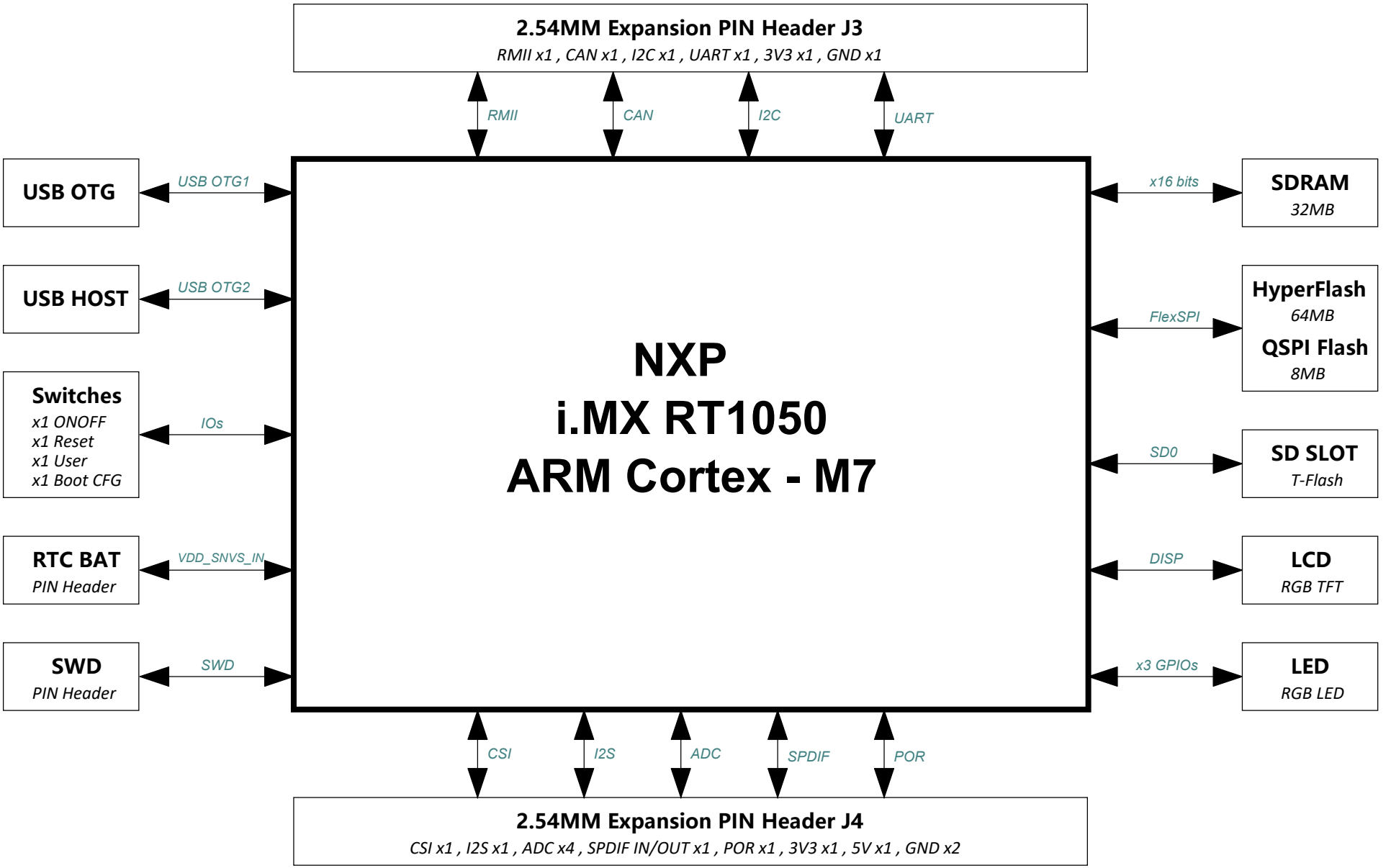
RT-M7 Blcok Diagram



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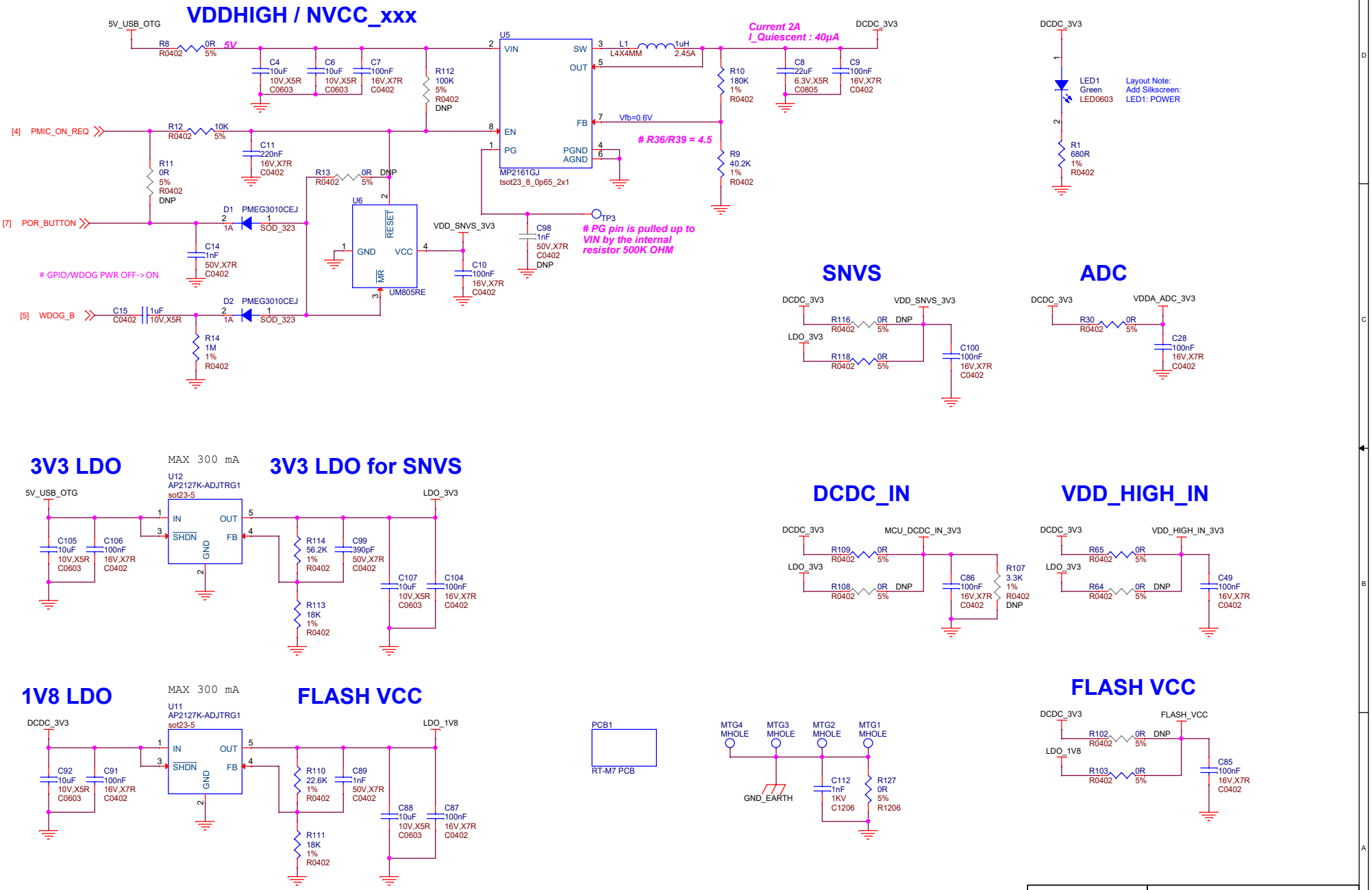

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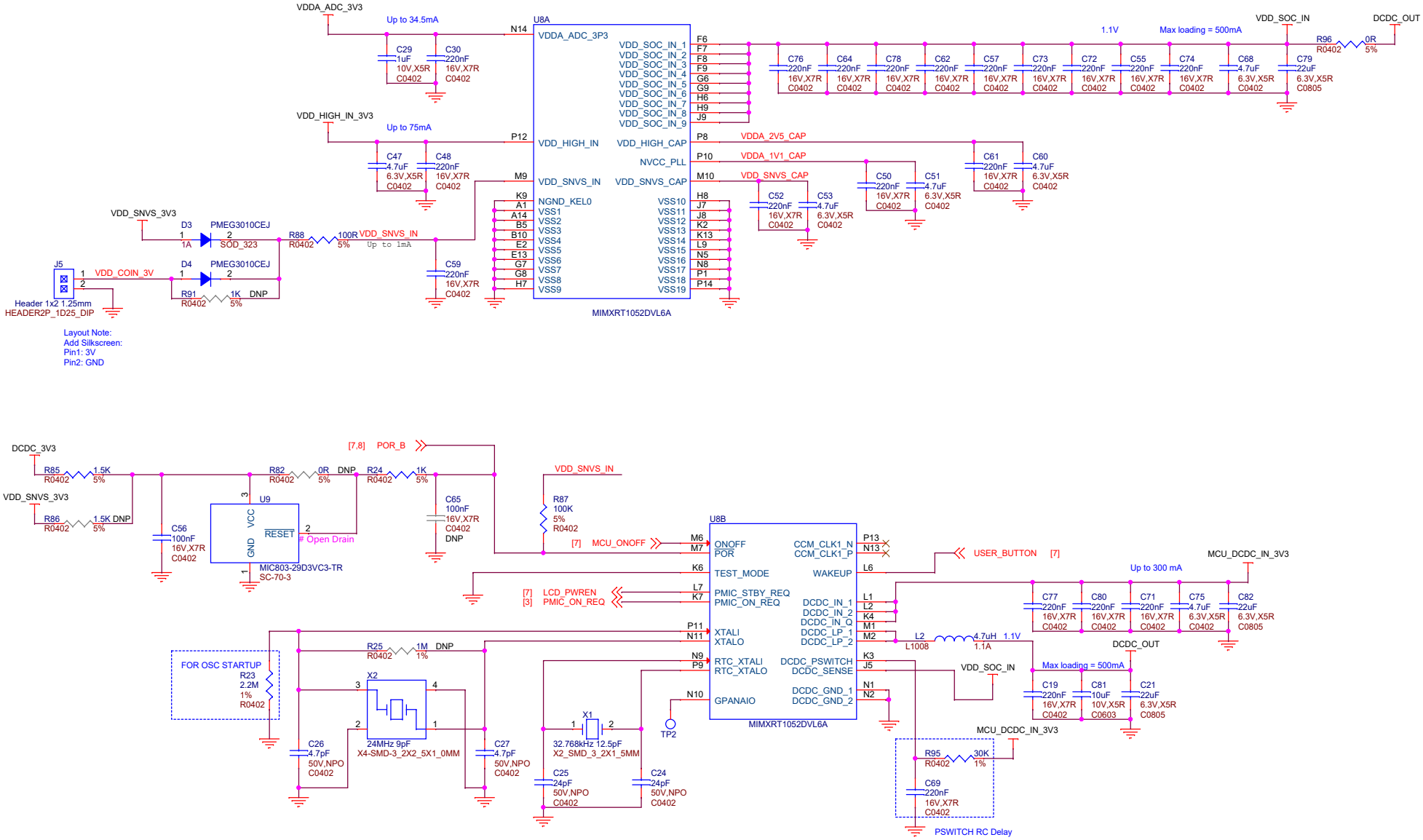

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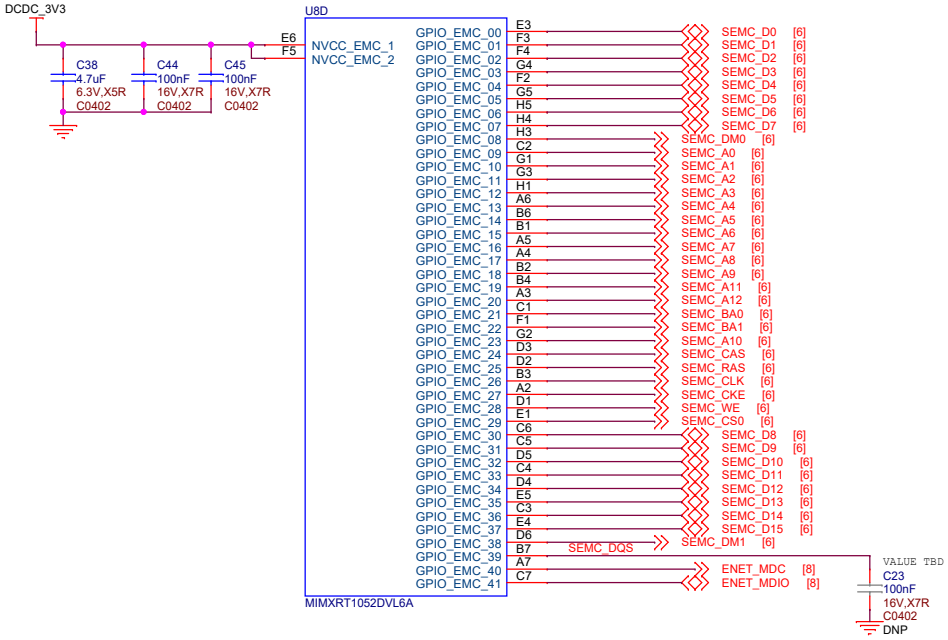
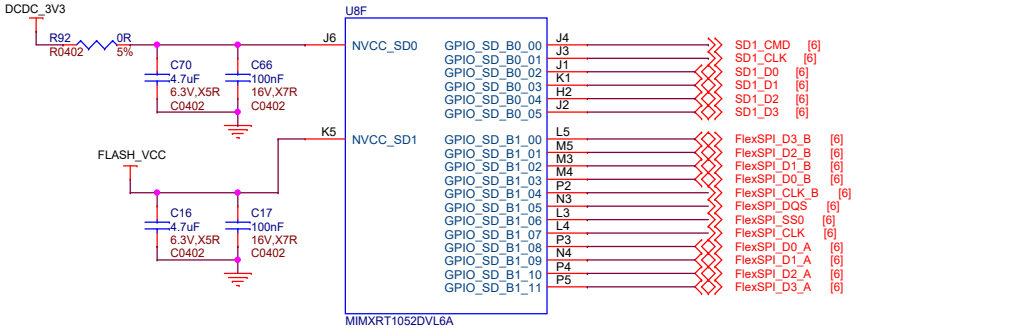
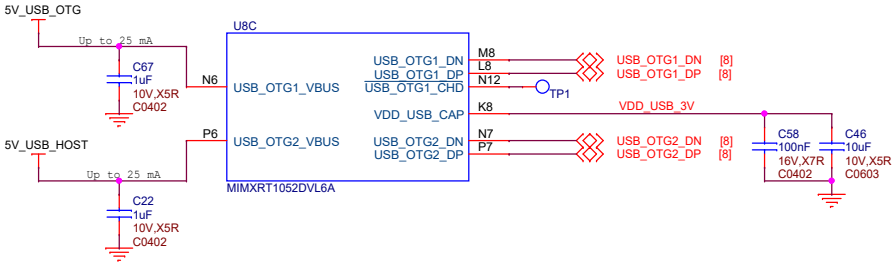
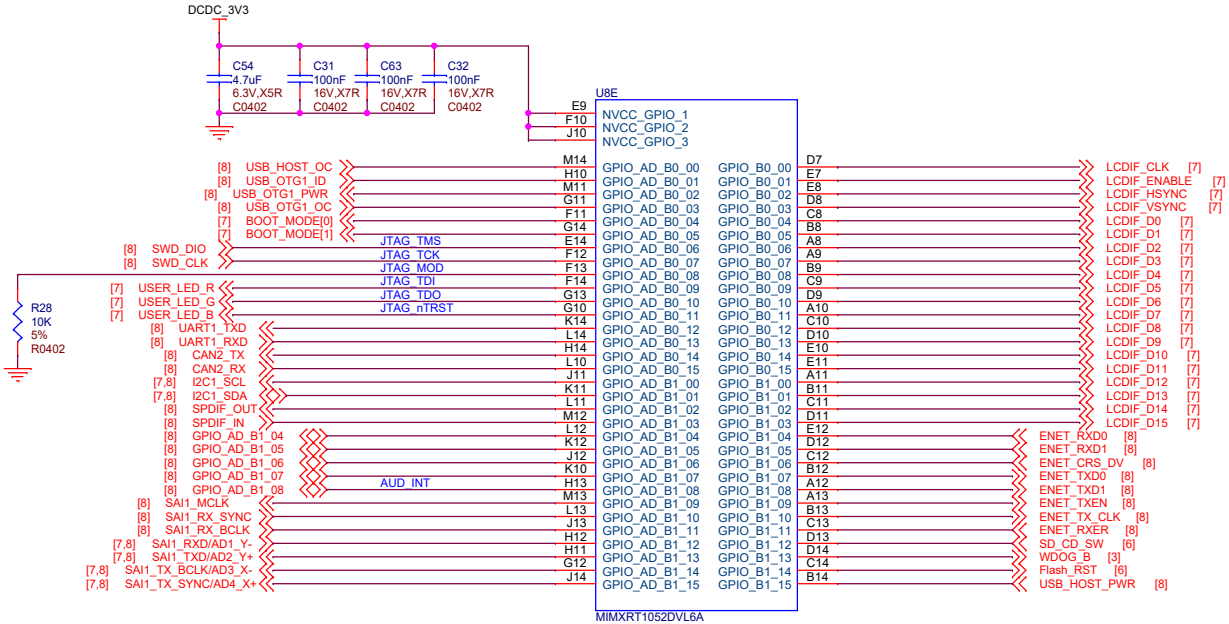






MCU PINOUT



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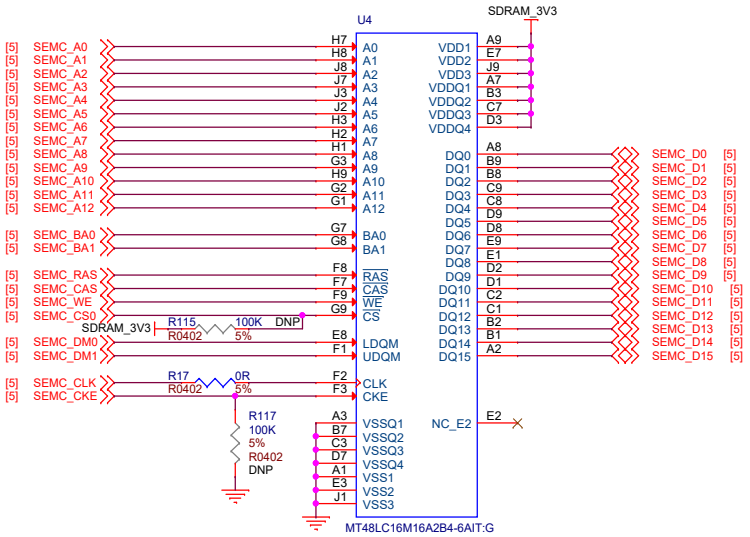


SDRAM

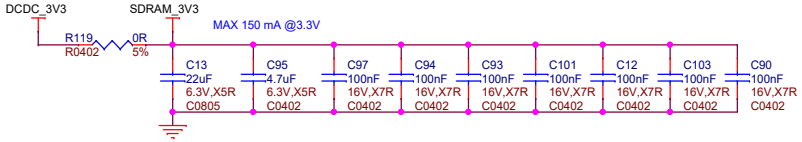
Layout Note:

The SDRAM interface (running at up to 166 MHz):

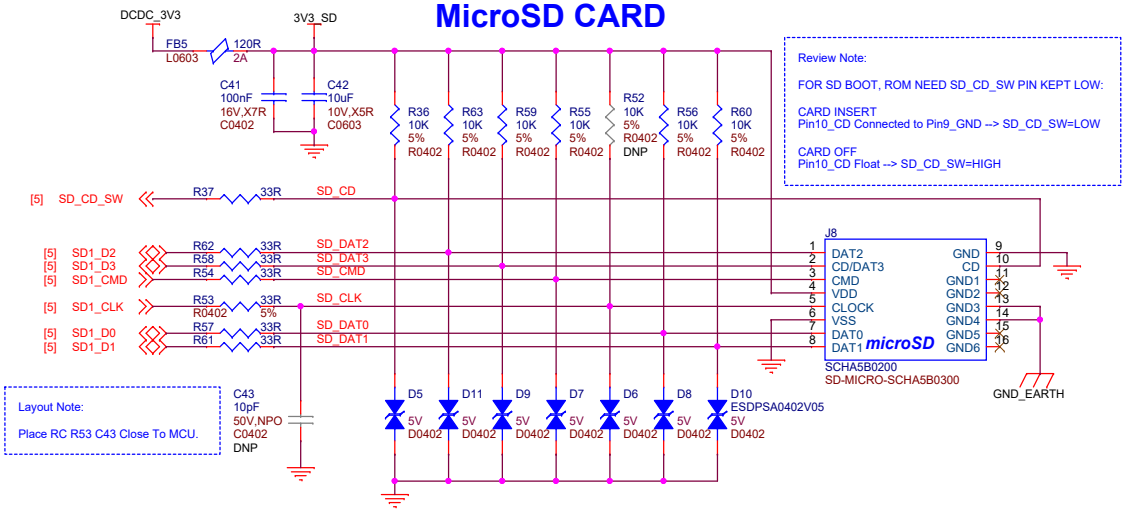
1. The SDRAM routing must be separated into three groups: data, address, and control.
2. Route all signals at the same length within 100 Mils.
3. The controlled impedance for the single-ended traces must be 50 Ω.

The FlexSPI interface (HyperFlash, QSPI Flash, running at up to 166 MHz):
The SD module interfaces (running at up to 50 MHz):

1. Follow similar SDRAM rules for data, address, and control as for the FlexSPI and SD interfaces.

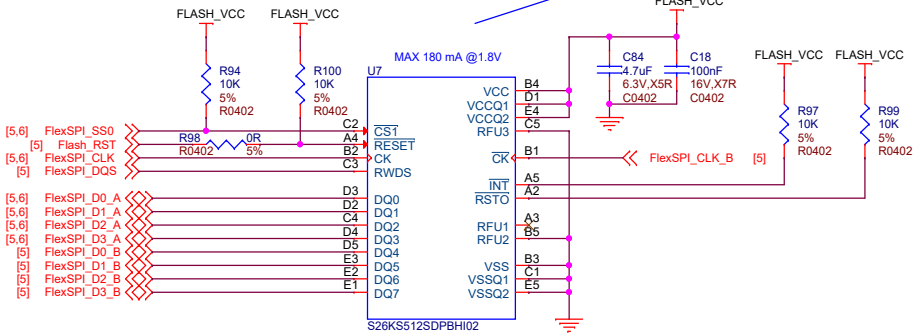


MicroSD CARD

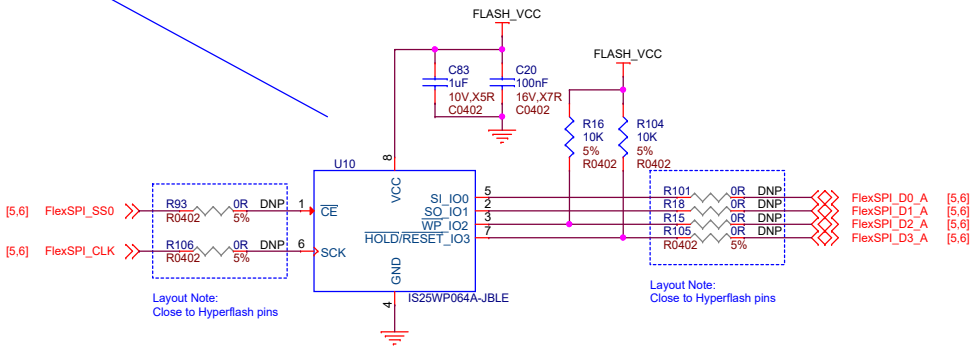


OPTION1: USE Hyperflash(DNP U33)
OPTION2: USE QSPI FLASH(DNP U19)

1V8 HyperFlash



1V8 QSPI Flash



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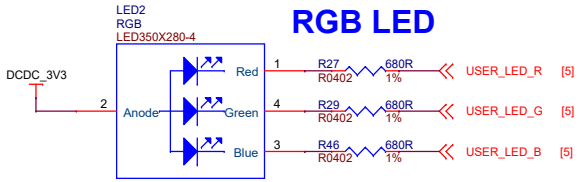
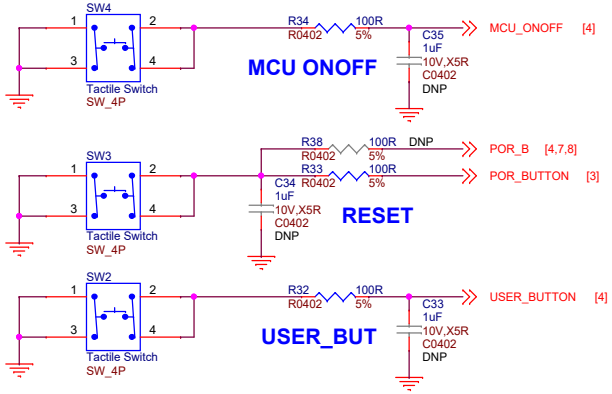
FUSE MAP

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 (Serial NOR)	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*

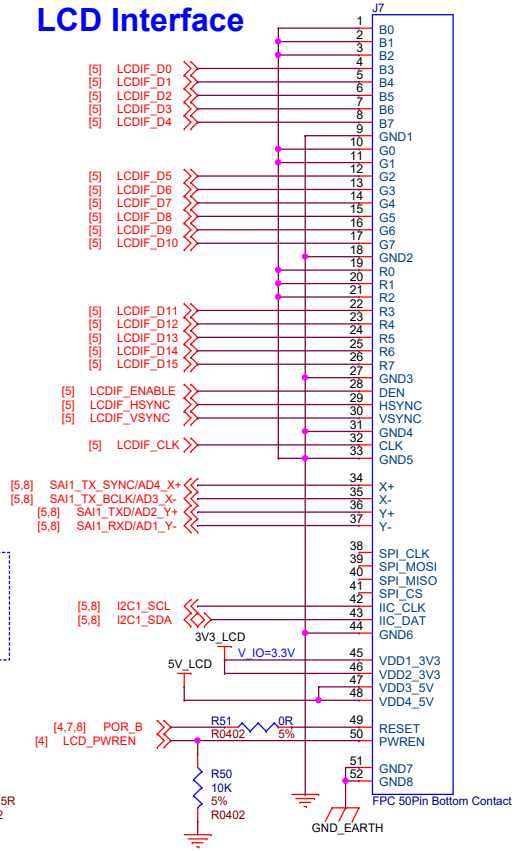
RGB LED



Button



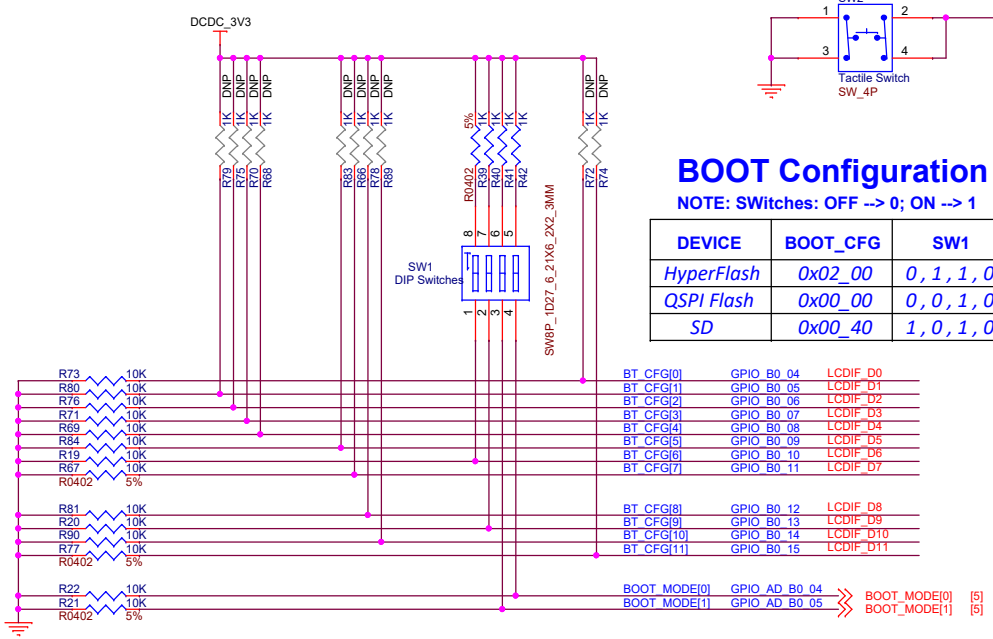
LCD Interface



BOOT Configuration

NOTE: SWitches: OFF --> 0; ON --> 1

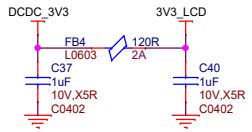
DEVICE	BOOT_CFG	SW1
HyperFlash	*0x02_00*	*0,1,1,0*
QSPI Flash	*0x00_00*	*0,0,1,0*
SD	*0x00_40*	*1,0,1,0*

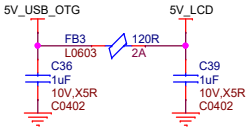


Layout Note:

The LCD interface (running at up to 75 MHz):

1. Route all signals at the same length within 100 Mils.
2. The controlled impedance for the single-ended traces must be 50 Ω.





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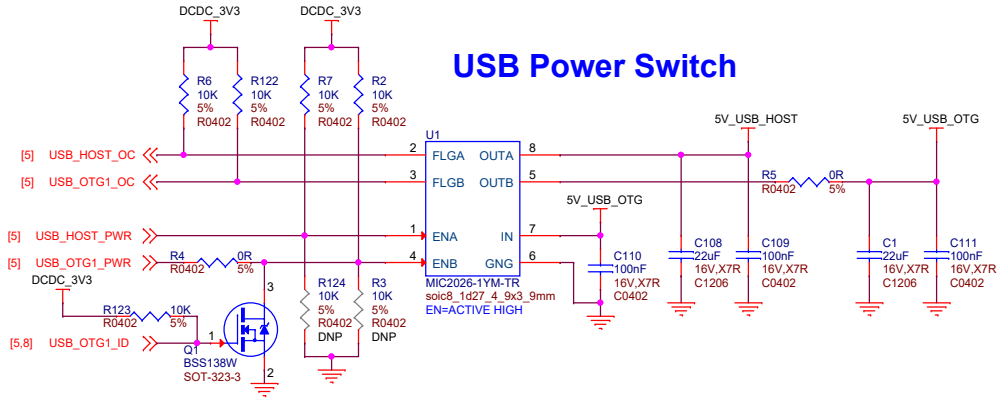

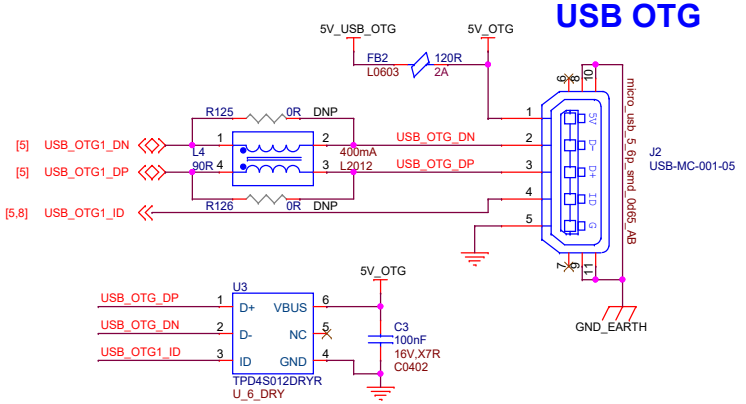

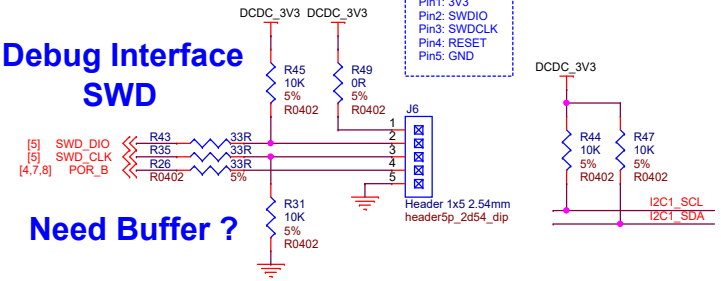

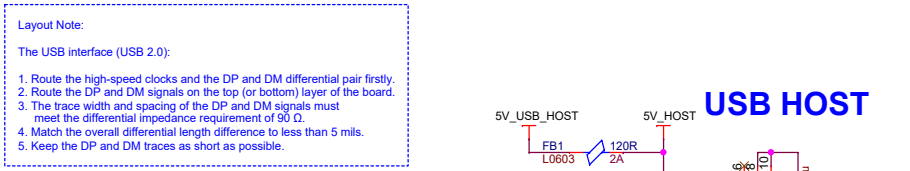

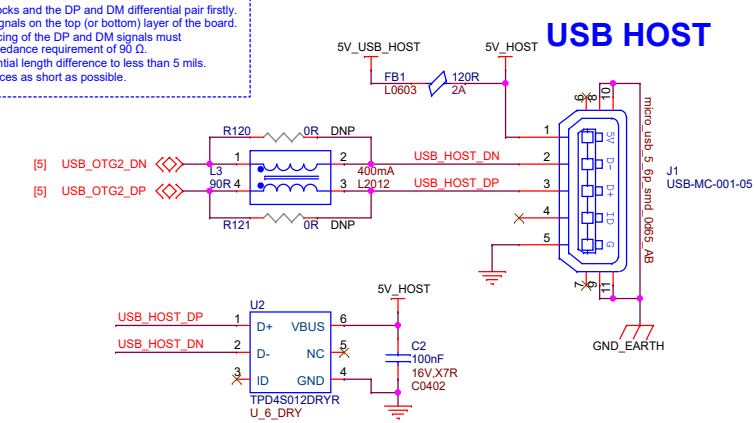

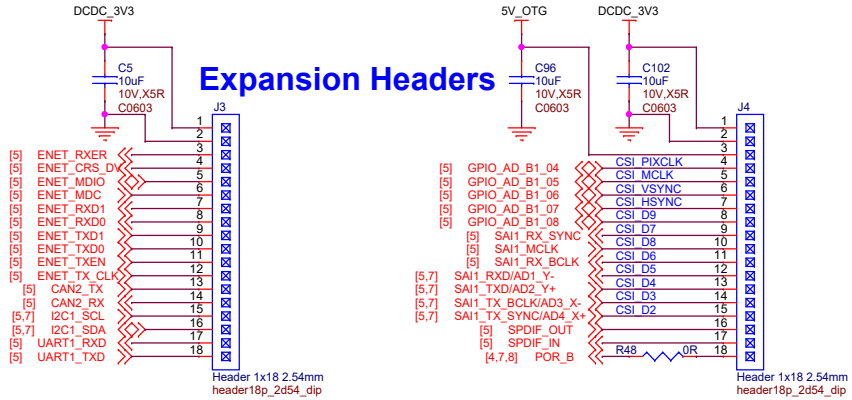

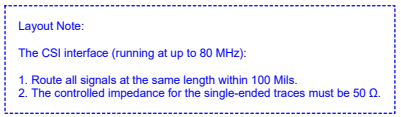

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