Implementation of 2-Bit Magnitude Comparator Circuit in FPGA

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Download the LaTex source code from:

https://github.com/balapriyac/EE5811−FPGA−lab/Project/latex_code

Download the Verilog code and configuration files from:

https://github.com/balapriyac/EE5811−FPGA−lab/Project/code

1 Introduction

This report goes over the implementation details of the 2-bit magnitude comparator.

- Hardware Used: Vaman LC
- Programming Language: Verilog

2 What is a Magnitude Comparator?

An N-bit magnitude comparator is a logical circuit that takes in two N-bit binary inputs A and B, and outputs one of the following three: $A > B$, $A < B$, or $A = B$.

In this report, let's go over the implementation of a 2-bit magnitude comparator that takes 2-bit inputs A and B, and outputs the result depending on whether or not the magnitude of A is greater than, less than, or equal to the magnitude of B.

3 Applications of Magnitude Comparators

The following are some applications of magnitude comparators:

- Magnitude comparators are widely used in circuits in control applications.
- In control circuits, inputs can be binary equivalent of the values of physical quantities or variables of interest temperature, humidity, pressure, and so on.
- In such control applications, the output of the comparator often triggers a specific sequence of actions.

4 Truth Table of 2-Bit Magnitude Comparator

The truth table for the 2-bit magnitude comparator is shown in the table below:

A_1	A_0	B_1	B_0	A > B	A < B	A = B
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

5 Simplification Using Karnaugh Map

This section will go over the simplification of the expressions for the output of the magnitude comparator using Karnaugh map.

5.1 Boolean Expression for $A > B$

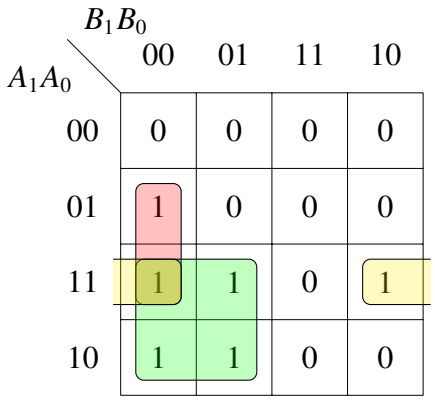


Fig. 1: K-Map for $A > B$

Upon simplification using the K-map, the Boolean expression for $A > B$ is as follows:

$$(A > B) = A_1B_1' + A_0B_1'B_0' + A_1A_0B_0'$$

5.2 Boolean Expression for $A < B$

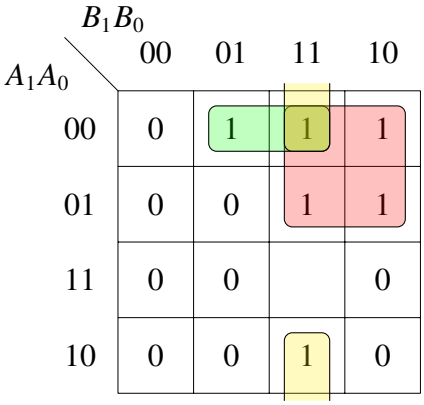


Fig. 2: K-Map for $A < B$

The simplified expression for $A < B$ is:

$$(A < B) = A_1'B_1 + A_0'B_1B_0 + A_1'A_0'B_0$$

5.3 Boolean Expression for $A = B$

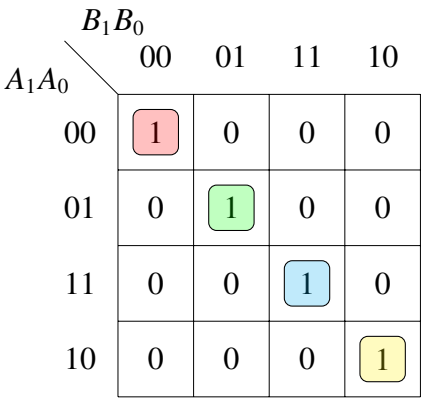


Fig. 3: K-Map for $A = B$

The Boolean expression for $A = B$ is:

$$A = B = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0'B_1B_0' + A_1B_1A_0B_0$$

This can be simplified as:

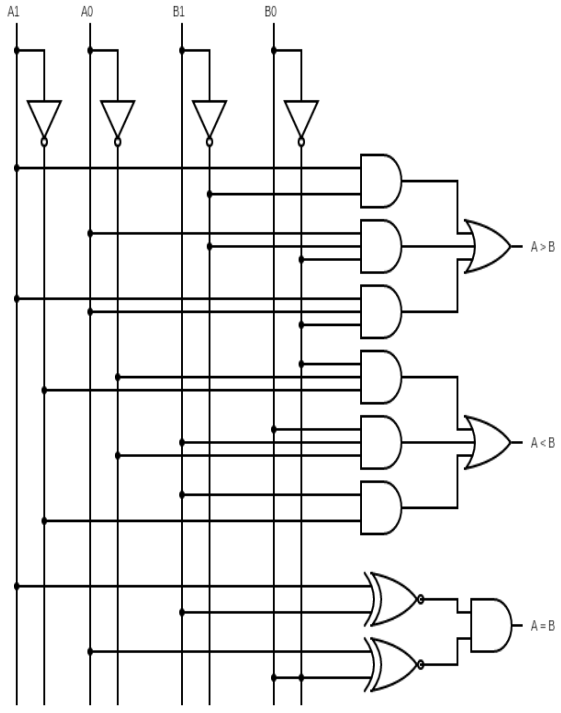
$$(A = B) = (A_1 \odot B_1).(A_0 \odot B_0)$$

6 Code Execution

- The file `twobitcomparator.v` contains the definition of the Verilog module for the 2-bit comparator circuit.
- The file `quickfeather.pcf` contains the pin configurations
- Provide inputs as needed to the Vaman LC board, compile and run the source code files in the `code` folder in the above-mentioned GitHub repository.

7 Logic Circuit

Using the Boolean expressions for the output of the comparator, we can draw the equivalent logic circuit as shown below. (Figure generated using the open-source tool `Circuit Diagram`)



8 Conclusion

In this report, we've discussed what magnitude comparators are, their applications, Boolean expressions for output, and implementation in FPGA.