

Implementation of 2-Bit Magnitude Comparator in FPGA

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Introduction

Implementation details of the project for FPGA Lab: 2-Bit Magnitude Comparator

- Hardware Used: Vaman LC
- Programming Language: Verilog

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Magnitude Comparator Circuit

An N-bit magnitude comparator is a logical circuit that takes in two N-bit binary inputs A and B , and outputs one of the following three:

- $A > B$
- $A < B$
- $A = B$

This presentation goes over the implementation details of the 2-bit magnitude comparator.

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Applications of Magnitude Comparator

- Circuits in control applications
- Inputs: binary equivalent of the values of physical quantities like temperature, humidity, pressure, etc.
- Output of the comparator: often triggers a specific sequence of actions
- Analog-to-Digital Converter circuits, ALUs, and more

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2-Bit Magnitude Comparator: Truth Table

The truth table for the 2-bit magnitude comparator is shown in the table below:

A_1	A_0	B_1	B_0	$A > B$	$A < B$	$A = B$
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

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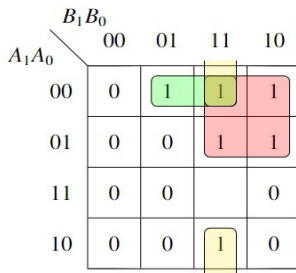
Boolean Expression for $A > B$

		B_1B_0			
		00	01	11	10
A_1A_0	00	0	0	0	0
	01	1	0	0	0
	11	1	1	0	1
	10	1	1	0	0

Fig. 1: K-Map for $A > B$

$$(A > B) = A_1B'_1 + A_0B'_1B'_0 + A_1A_0B'_0$$

Boolean Expression for $A < B$



A 4x4 Karnaugh Map for the Boolean expression $A < B$. The vertical axis is labeled A_1A_0 with values 00, 01, 11, 10. The horizontal axis is labeled B_1B_0 with values 00, 01, 11, 10. The map contains 1s in the following cells: (00, 01), (00, 11), (00, 10), (01, 11), (01, 10), (11, 11), and (10, 11). Three groups of 1s are highlighted: a green group of two cells (00, 01) and (00, 11), a red group of four cells (00, 11), (00, 10), (01, 11), and (01, 10), and a yellow group of two cells (11, 11) and (10, 11).

$A_1A_0 \backslash B_1B_0$	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0		0
10	0	0	1	0

Fig. 2: K-Map for $A < B$

$$(A < B) = A'_1B_1 + A'_0B_1B_0 + A'_1A'_0B_0$$

Boolean Expression for $A = B$

A_1A_0	B_1B_0			
	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

Fig. 3: K-Map for $A = B$

$$A = B = A_1'A_0'B_1'B_0' + A_1'A_0B_1'B_0 + A_1A_0'B_1B_0' + A_1B_1A_0B_0$$

$$(A = B) = (A_1 \odot B_1).(A_0 \odot B_0)$$

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Implementation

- The file `twobitcomparator.v` contains the definition of the Verilog module for the 2-bit comparator circuit.
- The file `quickfeather.pcf` contains the pin configurations
- Provide inputs as needed to the Vaman LC board, compile and run the source code files in the code folder in the above-mentioned GitHub repository.

Thank You!