EE5811 - FPGA Lab Assignment 1

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Download the LaTex code from:

https://github.com/balapriyac/EE5811−FPGA−lab/tree/main/Assignment−1

1 Question

[CBSE 2013 Q6 (b)] Obtain the Boolean expression for the logic circuit shown below:

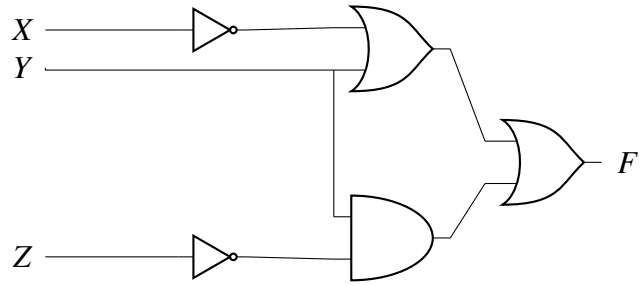

Fig. 1: Logic circuit

2 Solution

The algebraically simplified Boolean expression for F is shown below.

$$F = (X' + Y) + YZ' \quad (2.1)$$
$$= X' + (Y + YZ') \quad (2.2)$$
$$= X' + Y(1 + Z') \quad (2.3)$$
$$= X' + Y(1 + Z') \quad (2.4)$$
$$= X' + Y \quad since\ 1 + Z' = 1 \quad (2.5)$$
$$\implies F = X' + Y \quad (2.6)$$

3 Truth Table

The truth table corresponding to F for various choices of input X, Y, Z is shown below:

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

4 Simplification Using Karnaugh Map

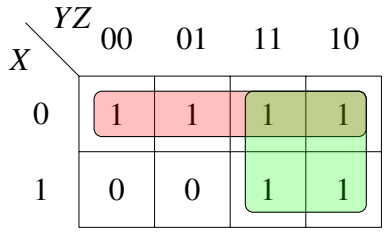

Fig. 2: K-Map for $F = X' + Y$

5 Implementation Using NAND Logic

$$F = X' + Y \quad (5.1)$$
$$= (X.Y')' \quad (5.2)$$
$$since\ \ (A.B)' = A' + B' \quad (5.3)$$
$$\implies F = (X.Y')'\ (using\ NAND\ logic) \quad (5.4)$$

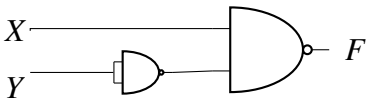

Fig. 3: Logic circuit using NAND logic