EE5811 - FPGA Lab Assignment 1

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Download the LaTex code from:

https://github.com/balapriyac/EE5811-FPGA-lab/tree/main/Assignment-1

1 Question

[CBSE 2013 Q6 (b)] Obtain the Boolean expression for the logic circuit shown below:

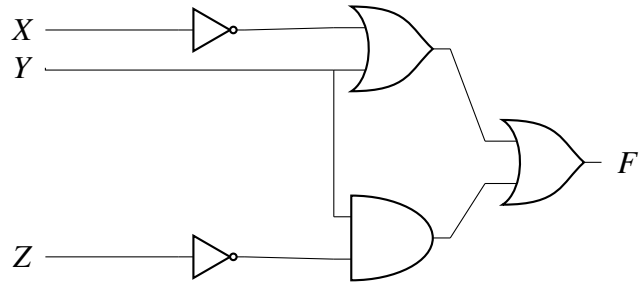

Fig. 1: Logic circuit

2 Solution

The algebraically simplified Boolean expression for F is shown below.

$$F = (X' + Y) + YZ' \tag{2.1}$$
$$= X' + (Y + YZ') \tag{2.2}$$
$$= X' + Y(1 + Z') \tag{2.3}$$
$$= X' + Y(1 + Z') \tag{2.4}$$
$$= X' + Y \quad since\ 1 + Z' = 1 \tag{2.5}$$
$$\implies F = X' + Y \tag{2.6}$$

3 Truth Table

The truth table corresponding to F for various choices of input X, Y, Z is shown below:

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

4 Simplification Using Karnaugh Map

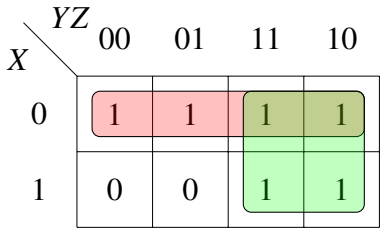

Fig. 2: K-Map for $F = X' + Y$