Rahulgandhi Parasuraman

Synopsis

A postgraduate in Electronics Design Technology with 3 years of hands-on design verification experience. Passionate about working with team and challenging environment.

Experience:

Design verification Engineer in Excelmax technologies pvt ltd, Bangalore March'20 – till date.

Client Company : Mavenir Systems private limited, Banglaore.

Projects Handled : 5G- Oran router, ETAP module, Top level verification.

Job Profile:

- Test case and testbench development.
- Sequences Scoreboard development.
- Module level verification.
- Top level verification.
- Running regression and debugging at top level in UL and DL Path.

Educational Qualifications

- M.Tech in Electronics design technology (EDT) from National Institute of Electronics and information Technology [NIELIT] Calicut, 2017-2019 with 6.925 CGPA.
- P.G Diploma in VLSI and embedded hardware design, NIELIT, Calicut, 2015.
- B. E. (ECE) from Adhiyamaan Engineering College in 2014 with 8.35 CGPA.
- HSC from Wisdom matric Hr sec School with 80.6%.
- SSLC from Wisdom vidyashram Matric School with 90%.

Technical Skills

- Languages/scripts : Verilog, System Verilog
- Methodologies : UVM
- Protocols : AXI,GIC,SIPIF.
- Tools : Questasim, ModelSim, Cadence, Xilinx ISE.
- FPGA Boards : Altera, Spartan, Xilinx ZYNQ.
- Operating System : linux, windows
- Radio Knowledge : ETAP, DFE, Oran Router.
- CPU Knowledge : ARM Cortex M3, sound knowledge of RISC-V

Experience in detail:

Project Name: Block Level verification of ORAN Router of Remote Radio Head

Client Name: Mavenir Systems pvt ltd March'2022 to present

Languages: System Verilog.

Methodology: UVM

Description:

The ORAN_Router module will receive UL packets from UL processing chain and s-plane module via AXI streaming slave port. The UL packets will be routed to Ethernet interface via AXI streaming master port. In UL path ORAN_Router module will receive DL packets from UL processing chain, it will perform arbitration, packetization of incoming packets as per ORAN standard and route the UL packets to DU via Ethernet interface.

In DL path ORAN_Router module will receive DL packets from DU via Four Ethernet interface, it will perform packet filtering and routing of packets to downlink processing chain C-plane module & m-plane DMA module based on the ORAN standard.

Responsibilities:

- Creation of verification plan and testcase scenarios with respect to verification plan.
- Involved in development of scoreboard, sequences and maintaining testbench as well.
- Involved in running regression and publishing report.
- Analysis of code coverage and publishing report.

Project Name: Top level verification of Radio Unit

Client Name: Mavenir systems pvt ltd March'2021 – Feb'2022

Languages: Verilog, System Verilog

Methodologies: UVM

Description:

Top level subsystem includes Clock subsystem, TDD, ADC, DFE, L1Phy, Mailbox, Oran router, Ethernet subsystem in Uplink [UL] path and Downlink [DL] Path. All these blocks are connected and checked for its data path correctness and header correctness from end to end.

Responsibilities:

- Creation of tasks which configure DFE for different carrier components.
- Development of RAL model for Oran router at top level verification.
- Involved in running regression and debugging of data path in UL and DL for various builds.

- Creation of regression analysis report.

Project Name: Module level verification of ETAP [Enhanced Test Access Port]

Client Name: Mavenir Systems pvt ltd June'2020 – Feb'2021

Languages: Verilog, System Verilog

Methodology: UVM

Description:

The ETAP block is a form of integrated logic analyzer and data injection block which is used for debugging/verifying blocks using SW stimulus from the Ethernet port of the Main board. Its main functionalities include capturing data from selected tap points in the design and injecting samples to the inputs/outputs of selected blocks in the design. It shall be used for testing and verification of the hardware in the radio.

Responsibilities:

- Involved in creation of testcases for different capture and injection scenarios.
- Involved in running and debugging the different ETAP scenarios for different builds.
- Configuring ETAP module to work on different modes with different data formats.
- Involved in creating and publishing ETAP regression analysis report.

Internship Project:

Design and verification of AMBA AXI Bus protocol using SV/UVM [Duration : 6 months]

Advanced Microcontroller Bus Architecture (AMBA) protocol family provides metric-driven verification of protocol compliance, enabling comprehensive testing of interface intellectual property (IP) blocks and system-on-chip (SoC) designs. This AMBA bus protocol is customized to advanced extensible interface which includes the following: support for burst lengths up to 24 beats, updated write response requirements and supports ordering model.