ANUPRIYA MISHRA

M.Tech in Electronics and Communication Engineering

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Objective

Seeking a position with an organization where I can contribute my skills for organization's success and synchronize with new technology while being resourceful, innovative and flexible.

SKILl Set

- EDA Tools : Mentor Graphics, Vivado, Model Sim, Spyglass.
- Hardware Description Languages : Verilog, System Verilog.
- Software Skills : TCL, Perl.
- Platforms : Windows, Linux.

Technical Expertise

Digital Electronics, Analog & Digital Communication, Electronic Device and Circuit, Low Power CMOS VLSI Design, Microelectronics.

Academic Profile

Degree	Board / University	Year	CGPA / Percentage
M.Tech [ECE]	GGSIPU	2018	**75.10%**
B.Tech [ECE]	UPTU	2013	**66.66%**
Higher Secondary	CBSE	2009	**74%**
Secondary	CBSE	2007	**69%**

WORK EXPERIENCE

- RTL Design Engineer, June 2022- Present, Capgemini
  - Working for INTEL Client.
  - Performs logic design, Register transfer level coding.
  - Simulation to generate cell libraries, functional units, and subsystems for inclusion in full chip designs.
  - Participates in the development of Architecture and Microarchitecture specifications for the Logic components. Provides IP integration support to SoC customers and represents RTL team.
- Validation Engineer (Contractor), February 2019 –April 2022 Xilinx Hyderabad
  - Hands on experience on Xilinx's FPGAs from design bring up to implementationphase.
  - Skilled in debugging FPGA flow related issues and Vivado Tool relatedissues.

- Skilled in running Lint and debugging all Lint related issues
- Working on the Verification Infra for the Vivado IPI/IP verification.
- Developed Various New Features for the Automation Infrastructure. Enhanced the Automation Environment itself.
- Regression flow automation wherever required.
- IP packaging, Design Bring Up/Debug and Automation Verification Infrastructure
- Verification of Different DRAM Memory Controllers which Include

  - DDR4, DDR3, RLDRAM3, RLDRAM2, LPDDR3, QDR2PLUS
- Hands on work experience in handling variety of tools which include.
  - Vivado Synthesis and Implementation.
  - ModelSim/Questa, IES for Simulation.
  - Spyglass Lint for Linting RTL code.

- Project Mentor, July 2017-April 2018
  Bibox Banglore
  - Worked on sensors & microcontrollers.
  - Projects design and Testing.
  - Worked on two live projects.

PROjects

M.Tech Final Year Project

1) Title: **Design of Low Power Dynamic Comparator and Full Adder in 180 nm CMOS Technology**

Abstract: I have successfully design Dynamic CMOS comparator in 180nm CMOS technology. Comparator is proposed using circuit level techniques LECTOR, GALEOR, ONOFIC, LCNT & LCMT in which two leakage transistors are added between pull up and pull-down network of logic circuit in different styles and are used to design circuit with no critical path. Proposed comparator circuit performance analysis is done in respect of power dissipation and delay**.**

M.Tech Semester projects

2) Millimeter Wave Mobile communication for 5G Cellular.
3) A Massive MIMO using Millimeter Wave
4) WIMAX Technology.
5) Design and Analysis of Dynamic Comparator using stacking low power technique.

Communicated ReSearch PAPER

- ANUPRIYA Mishra and Manoj Kumar, "**Design of Low Power Dynamic Comparator in 180 nm CMOS Technology**", IEEE International Conference on Advances in Computing, Communication Control and Networking.

Personal Strengths

- Hard working and good at team work.
- Rapid at learning things.

Declaration

I hereby declare that all the information provided here is correct to the best of my knowledge and belief and I promise to abide all the norms laid down by your esteemed organization.
Anupriya Mishra