Frequency (MHz)	**20**
Clock Divider	**10**

Sync-Seg	1
Prop-Seg	7
Phase-Seg1	**4**
Phase-Seg2	**4**
SJW	**3**
Bit Length (TQ)	16

TQ (ns)	500
Baud (kbps)	125
TQ/Bit	16
prop-delay/meter (ns)	5
Max Bus Length required (m)	300
Bus prop-delay (ns)	3400
Oscillator Tolerance 1	0.980%
Oscillator Tolerance 2	0.938%
Oscillator Tolerance Absolute	**0.938%**
Max Bus Length Supported (m)	**310**
Sample Point	**75.00%**

Input Frequency to the CAN Controller

The clock divider for the incoming CAN controller frequency

Phase-Seg2 must be less than or equal to **Prop-Seg** + **Phase-Seg1**

SJW must be less than or equal to both **Phase-Seg1** and **Phase-Seg2**. Some CAN controllers require **SJW** to be less than **Phase-Seg2** to allow for processing time

The sum of **Sync-Seg** + **Prop-Seg** + **Phase-Seg1** + **Phase-Seg2**, must be equal to **TQ/bit**

Timing parameters should be chosen to maximize this value while meeting the 300m bus length requirement

This is the maximum theoretical bus length supported by the timing parameters, must be greater than or equal to 300, determined by **Prop-Seg**

This is the point within the bit where the data will be sampled, sane values are typically between 60% and 80%