# 1. General Description

The Realtek RTD2717Q-CG monitor controller combines the multiple DP1.4 digital input interfaces with HDCP1.4/HDCP2.2 and multiple HDMI2.0 digital input interfaces with HDCP1.4/HDCP2.2,. The embedded MCU is based on an industrial standard 8051 core with external serial flash.

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The RTD2717Q-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.



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# 2. Features

**General**

- RTD2717Q-CG supports input format up to 2560 x 1440 @ 165Hz via signal DP1.4 port
- Support multiple panel interfaces like V-by-1, and eDP
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency

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**Crystal**

- Support 14.318MHz crystal type

**Ultra-High Speed Receiver**

- RTD2717Q-CG supports 2 ports of Ultra-High Speed Receiver can support DisplayPort1.4
- In DisplayPort mode, four link layer speed HBR3 (8.1GHz), HBR2 (5.4GHz), HBR (2.7GHz), RBR (1.62GHz) are supported

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- In DisplayPort mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In DisplayPort mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.2) is supported
- In DisplayPort mode, DisplayPort audio is allowed to transmit to I2S/SPDIF output
- In DisplayPort mode, VESA Adaptive Sync technology is supported

**Ultra-High Speed Receiver**

- RTD2717Q-CG supports 2 ports of Ultra-High Speed Receiver can support HDMI2.0
- In HDMI mode, the latest HDMI2.0 (6GHz) is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.2) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In HDMI mode, AMD HDMI Freesync technology is supported



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**Embedded MCU**

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

**Auto Detection /Auto Calibration**

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

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**Audio**

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

**Scaling**

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

**Color Processor**

- True 12-bit color processing engine
- Programmable 14-bit gamma support
- Programmable 12-bit 3D gamma support
- xvYCC supported
- Adobe/sRGB compliance
- Advanced dithering logic for the fewer panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Peaking/Coring function for video sharpness
- Support UltraVivid III function to enhance image quality with minimal artificial effect on productivity applications
- Panel Uniformity (Brightness and color uniformity)
- Support EOTF(electro-optical transfer function): 10 bits SMPTE 2084
- Support Adaptive Tone-Mapping
- Support segmented backlight control to enhance HDR performance
- Support BT 2020



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**VividColorTM**

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- 2nd generation of Precise color mapping (PCM)
- Image Adaptive Power Saving (IAPS)
- Support ADC Noise Reduction
- Support Realtek Owl Sight Technology

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**Output Interface**

- Support 8-bit / 10-bit output through either V-by-1 and eDP
- Supports 8-lane V-by-One or 8-lane eDP HBR2 with the output format up to 2560*1440 @ 165Hz.
- Flexible data pair swapping for easier system design.
- Fixed Last Line output for perfect panel capability

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**Embedded OSD**

- Embedded 64K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2, 4 and 4-bit per pixel
- 64 color palette
- Maximum 26 window with alpha-blending /gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering
- Rotate 90,180,270 degree
- OSD-made internal pattern generator for factory mode
- Support 12x18 proportional font
- Hardware decompression for OSD font
- Support factor scale up
- Support 2 independent font based OSD

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**Frame Buffer Support**

- LiveShow™ Function, High-performance RTC (response time compensation).
- Frame Rate Control Function
- Embedded frame buffer

**Power Supply**

- 3.3V / 1.5V / 1.1V power supply



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# 3. System Applications

- Display System on Motherboard, Monitor

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- Display System for All in One PCs and embedded applications



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# 4. Block Diagram

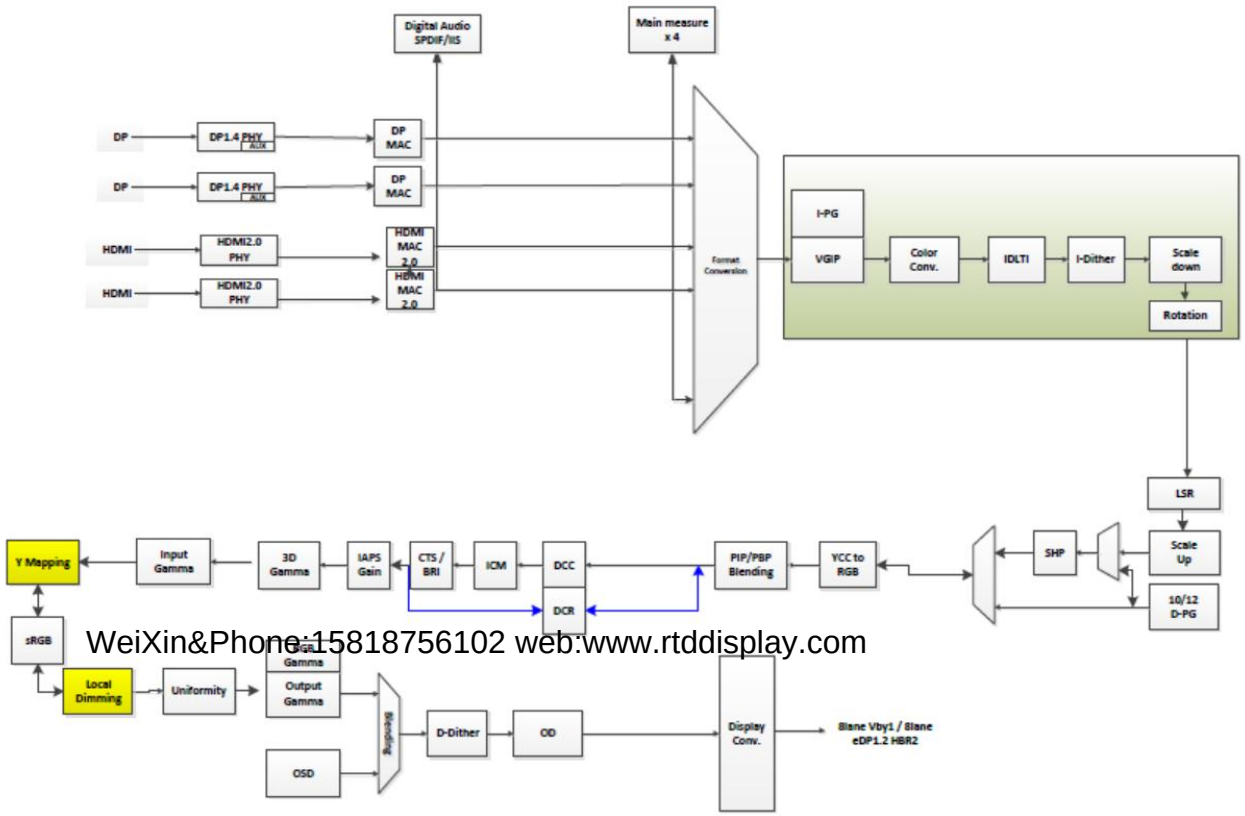


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**Figure 1. Block Diagram**



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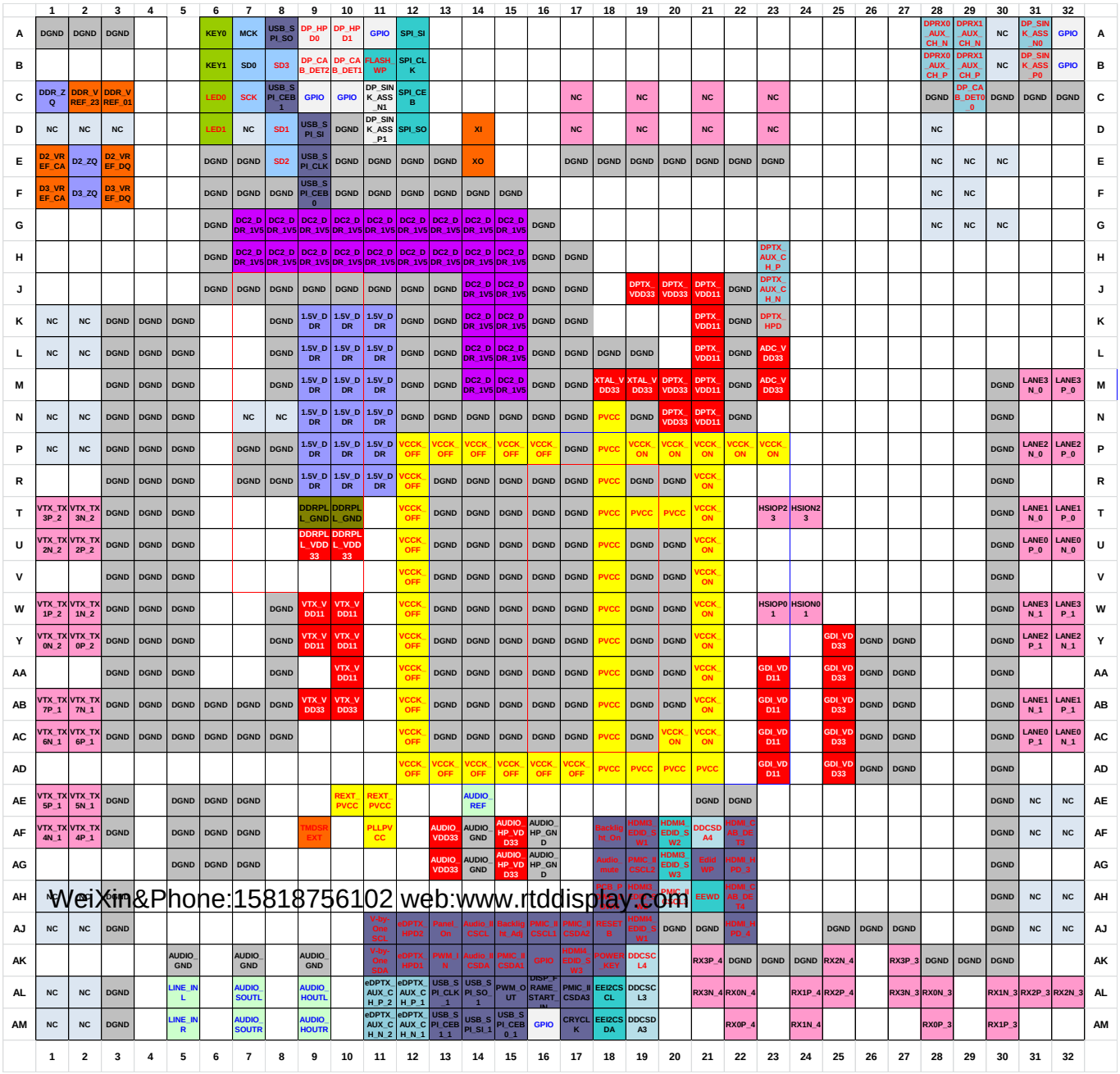
# 5. Pin Assignments

## HSBGA



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DGND | DGND | DGND | | | KEY0 | MCK | USB_SPI_SO | DP_HPD0 | DP_HPD1 | GPIO | SPI_SI | | | | | | | | | | | | | | | | DPRX0_AUX_CH_N | DPRX1_AUX_CH_N | NC | DP_SINK_ASS_N0 | GPIO | A |
| B | | | | | | KEY1 | SD0 | SD3 | DP_CAB_DET2 | DP_CAB_DET1 | FLASH WP | SPI_CLK | | | | | | | | | | | | | | | | DPRX0_AUX_CH_P | DPRX1_AUX_CH_P | NC | DP_SINK_ASS_P0 | GPIO | B |
| C | DDR_ZQ | DDR_VREF_23 | DDR_VREF_01 | | | LED0 | SCK | USB_SPI_CEB1 | GPIO | GPIO | DP_SINK_ASS_N1 | SPI_CEB | | | | | NC | | NC | | NC | | NC | | | | | DGND | DP_CAB_DET0_0 | DGND | DGND | DGND | C |
| D | NC | NC | NC | | | LED1 | NC | SD1 | USB_SPI_SI | DGND | DP_SINK_ASS_P1 | SPI_SO | | XI | | | NC | | NC | | NC | | NC | | | | | NC | | | | | D |
| E | D2_VREF_CA | D2_ZQ | D2_VREF_DQ | | | DGND | DGND | SD2 | USB_SPI_CLK | DGND | DGND | DGND | DGND | XO | | | DGND | DGND | DGND | DGND | DGND | DGND | DGND | | | | | NC | NC | NC | | | E |
| F | D3_VREF_CA | D3_ZQ | D3_VREF_DQ | | | DGND | DGND | DGND | USB_SPI_CEB0 | DGND | DGND | DGND | DGND | DGND | DGND | | | | | | | | | | | | | NC | NC | | | | F |
| G | | | | | | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | | | | | | | | | | | NC | NC | NC | | | G |
| H | | | | | | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | DGND | | | | | DPTX_AUX_CH_P | | | | | | | | | H |
| J | | | | | | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | DGND | | DPTX_VDD33 | DPTX_VDD33 | DPTX_VDD11 | DGND | DPTX_AUX_CH_N | | | | | | | | | J |
| K | NC | NC | DGND | DGND | DGND | | | DGND | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | DGND | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | DGND | | | | DPTX_VDD11 | DGND | DPTX_HPD | | | | | | | | | K |
| L | NC | NC | DGND | DGND | DGND | | | DGND | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | DGND | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | DGND | DGND | DGND | | DPTX_VDD11 | DGND | ADC_VDD33 | | | | | | | | | L |
| M | | | DGND | DGND | DGND | | | DGND | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | DGND | DGND | DC2_DDR_1V5 | DC2_DDR_1V5 | DGND | DGND | XTAL_VDD33 | XTAL_VDD33 | DPTX_VDD33 | DPTX_VDD11 | DGND | ADC_VDD33 | | | | | | | DGND | LANE3N_0 | LANE3P_0 | M |
| N | NC | NC | DGND | DGND | DGND | | NC | NC | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | DGND | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DPTX_VDD33 | DPTX_VDD11 | DGND | | | | | | | | DGND | | | N |
| P | NC | NC | DGND | DGND | DGND | | DGND | DGND | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | VCCK_OFF | VCCK_OFF | VCCK_OFF | VCCK_OFF | VCCK_OFF | DGND | PVCC | VCCK_ON | VCCK_ON | VCCK_ON | VCCK_ON | VCCK_ON | | | | | | | | DGND | LANE2N_0 | LANE2P_0 | P |
| R | | | DGND | DGND | DGND | | DGND | DGND | 1.5V_DDR | 1.5V_DDR | 1.5V_DDR | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | | | | | | | | | DGND | | | R |
| T | VTX_TX3P_2 | VTX_TX3N_2 | DGND | DGND | DGND | | | | DDRPLL_GND | DDRPLL_GND | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | PVCC | PVCC | VCCK_ON | | HSIOP23 | HSION23 | | | | | | | DGND | LANE1N_0 | LANE1P_0 | T |
| U | VTX_TX2N_2 | VTX_TX2P_2 | DGND | DGND | DGND | | | | DDRPLL_VDD33 | DDRPLL_VDD33 | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | | | | | | | | | DGND | LANE0P_0 | LANE0N_0 | U |
| V | | | DGND | DGND | DGND | | | | | | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | | | | | | | | | DGND | | | V |
| W | VTX_TX1P_2 | VTX_TX1N_2 | DGND | DGND | DGND | | | DGND | VTX_VDD11 | VTX_VDD11 | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | HSIOP01 | HSION01 | | | | | | | DGND | LANE3N_1 | LANE3P_1 | W |
| Y | VTX_TX0N_2 | VTX_TX0P_2 | DGND | DGND | DGND | | | DGND | VTX_VDD11 | VTX_VDD11 | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | | | GDI_VDD33 | DGND | DGND | | | | DGND | LANE2P_1 | LANE2N_1 | Y |
| AA | | | DGND | DGND | DGND | | | DGND | | VTX_VDD11 | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | GDI_VDD11 | | GDI_VDD33 | DGND | DGND | | | | DGND | | | AA |
| AB | VTX_TX7P_1 | VTX_TX7N_1 | DGND | DGND | DGND | DGND | DGND | DGND | VTX_VDD33 | VTX_VDD33 | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | DGND | VCCK_ON | | GDI_VDD11 | | GDI_VDD33 | DGND | DGND | | | | DGND | LANE1N_1 | LANE1P_1 | AB |
| AC | VTX_TX6N_1 | VTX_TX6P_1 | DGND | DGND | DGND | DGND | DGND | DGND | | | | VCCK_OFF | DGND | DGND | DGND | DGND | DGND | PVCC | DGND | VCCK_ON | VCCK_ON | | GDI_VDD11 | | GDI_VDD33 | DGND | DGND | | | | DGND | LANE0P_1 | LANE0N_1 | AC |
| AD | | | | | | | | | | | | VCCK_OFF | VCCK_OFF | VCCK_OFF | VCCK_OFF | VCCK_OFF | VCCK_OFF | PVCC | PVCC | PVCC | PVCC | | GDI_VDD11 | | GDI_VDD33 | DGND | DGND | | | | DGND | | | AD |
| AE | VTX_TX5P_1 | VTX_TX5N_1 | DGND | | DGND | DGND | DGND | | | REXT_PVCC | REXT_PVCC | | | AUDIO_REF | | | | | | | DGND | DGND | | | | | | | | | DGND | NC | NC | AE |
| AF | VTX_TX4N_1 | VTX_TX4P_1 | DGND | | DGND | DGND | DGND | | TMDSREXT | | PLLPVCC | | AUDIO_VDD33 | AUDIO_GND | AUDIO_HP_VDD33 | AUDIO_HP_GND | | Backlight_On | HDMI2_EDID_SW1 | HDMI4_EDID_SW2 | DDCSDA4 | HDMI_HAD_DET3 | | | | | | | | DGND | NC | NC | AF |
| AG | | | | | DGND | DGND | DGND | | | | | | AUDIO_VDD33 | AUDIO_GND | AUDIO_HP_VDD33 | AUDIO_HP_GND | | Audio_mute | PMIC_ICSCL2 | HDMI3_EDID_SW3 | EdidWP | HDMI_HPD_3 | | | | | | | | DGND | | | AG |
| AH | NC | NC | DGND | | | | | | | | | | | | | | | PCB_PWEN_KEY | HDMI3_EDID_SW4 | PMIC_IICSDA2 | EEWD | HDMI_CAB_DET4 | | | | | | | | DGND | NC | NC | AH |
| AJ | NC | NC | DGND | | | | | | | | V-by-One SCL | eDPTX_HPD2 | Panel_On | Audio_IICSCL | Backlight_Adj | PMIC_IICSCL3 | PMIC_IICSDA2 | RESETB | HDMI4_EDID_SW1 | DGND | DGND | HDMI_HPD_4 | | | DGND | DGND | DGND | | | DGND | NC | NC | AJ |
| AK | | | | | AUDIO_GND | | AUDIO_GND | | AUDIO_GND | | V-by-One SDA | eDPTX_HPD1 | PWM_IN | Audio_IICSDA | PMIC_IICSDA1 | GPIO | HDMI5_EDID_SW3 | POWEN_KEY | DDCSCL4 | | RX3P_4 | DGND | DGND | DGND | RX2N_4 | | RX3P_3 | DGND | DGND | DGND | | | AK |
| AL | NC | NC | DGND | | LINE_INL | | AUDIO_SOUTL | | AUDIO_HOUTL | | eDPTX_AUX_CH_P_2 | eDPTX_AUX_CH_P_1 | USB_SPI_CLK_1 | USB_SPI_SO_1 | PWM_OUT | DISP_FRAME_START_IN | PMIC_IICSDA3 | EEI2CSCL | DDCSCL3 | | RX3N_4 | RX0N_4 | | RX1P_4 | RX2P_4 | | RX3N_3 | RX0N_3 | | RX1N_3 | RX2P_3 | RX2N_3 | AL |
| AM | NC | NC | DGND | | LINE_INR | | AUDIO_SOUTR | | AUDIO_HOUTR | | eDPTX_AUX_CH_N_2 | eDPTX_AUX_CH_N_1 | USB_SPI_CEB1_1 | USB_SPI_SI_1 | USB_SPI_CEB0_1 | GPIO | CRYCLK | EEI2CSDA | DDCSDA3 | | | RX0P_4 | | RX1N_4 | | | | RX0P_3 | | RX1P_3 | | | AM |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | |

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**Figure 2. Pin Diagram of HSBGA**



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# 8. Mechanical Specifications

HSBGA

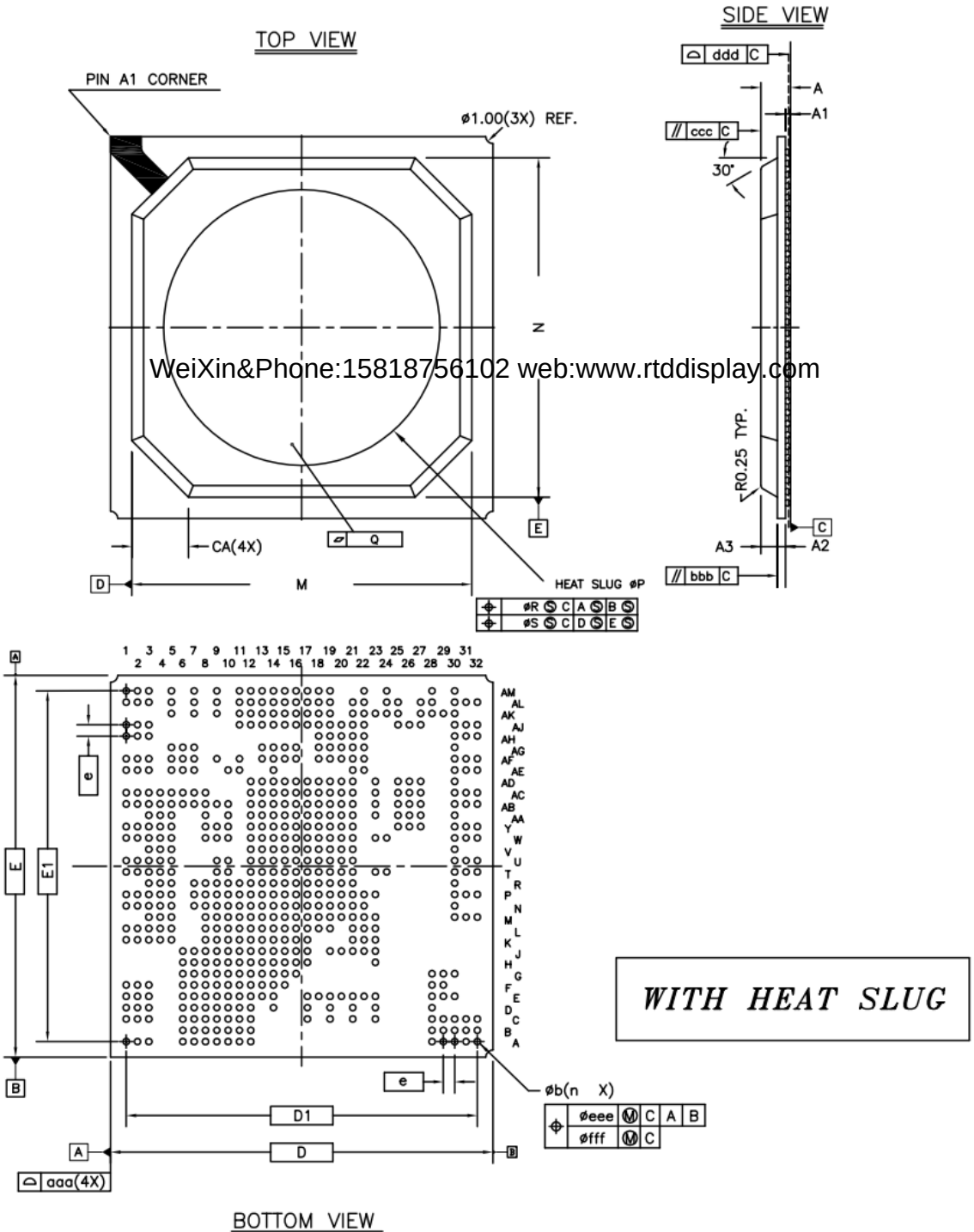


**Figure 3. Mechanical Specification of HSBGA**

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| | | Symbol | Common Dimensions | | |
|---|---|---|---|---|---|
| | | | MIN. | NOM. | MAX. |
| Package : | | | HSTK FBGA | | |
| Body Size: | X | D | 27.000 | | |
| | Y | E | 27.000 | | |
| Ball Pitch : | | e | 0.800 | | |
| Total Thickness : | | A | 1.982 | 2.100 | 2.218 |
| Mold Thickness : | | A3 | 1.170 Ref. | | |
| Substrate Thickness : | | A2 | 0.560 Ref. | | |
| Ball Diameter : | | | 0.450 | | |
| Stand Off : | | A1 | 0.320 | – | 0.420 |
| Ball Width : | | b | 0.375 | – | 0.525 |
| Mold Area : | X | M | 24.000 | | |
| | Y | N | 24.000 | | |
| H/S Exposed Size: | | P | 19 ~ 20 | | |
| H/S Flatness | | Q | 0.100 | | |
| H/S Shift With Substrate Edge: | | R | 0.300 | | |
| H/S Shift With Mold Area: | | S | 0.500 | | |
| Chamfer | | CA | 4.000 Ref. | | |
| Package Edge Tolerance : | | aaa | 0.150 | | |
| Substrate Parallelism : | | bbb | 0.100 | | |
| Mold Parallelism : | | ccc | 0.200 | | |
| Coplanarity: | | ddd | 0.150 | | |
| Ball Offset (Package) : | | eee | 0.150 | | |
| Ball Offset (Ball) : | | fff | 0.080 | | |
| Ball Count : | | n | 602 | | |
| Edge Ball Center to Center : | X | D1 | 24.800 | | |
| | Y | E1 | 24.800 | | |

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**Figure 4. Mechanical Specification of HSBGA**



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# 9. Ordering Information

**Table 6. Ordering Information**

| Part No. | Max. Resolution | Input : VGA | Input : DP1.4 HBR3 | Input : HDMI2.0 | Output : eDP | Output : Vby1 | FRC | OD | PKG |
|---|---|---|---|---|---|---|---|---|---|
| RTD2717Q-CG | 2560x1440 @165Hz | N/A | 2 Ports | 2 Ports | ● | ● | ● | ● | PBGA |

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