RTD2797UPM-CG

MULTI-FUNCTION DISPLAY CONTROLLER

DATASHEET

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2016/03/10	First release.
1.01	2016/05/10	DP version upgrade

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1. General Description

The Realtek RTD2797UPM-CG monitor controller combines an analog RGB input interface, multiple HDMI 2.0 compliant digital input interfaces with HDCP1.4/HDCP2.2, multiple DP1.4 digital input interfaces with HDCP1.4/HDCP2.2, multiple HDMI 1.4 compliant digital input interfaces with HDCP1.4, and multiple MHL2.2 digital input interfaces with HDCP1.4. The embedded MCU is based on an industrial standard 8051 core with external serial flash.

The RTD2797UPM-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.

2. Features

General

- RTD2797UPM-CG supports input format up to 3440x1440 @60Hz and 4096x2160 @ 60Hz.
- Supports one analog RGB input and six multiple-digital-interface combo inputs
- Support multiple panel interfaces like, V-by-One, and eDP
- Support DisplayPort 1.4 HBR2 MST daisy-chaining
- Supports PIP / PBP and 4P function
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.

Crystal

- Support 14.318MHz crystal type

Analog RGB Input Interface

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

Ultra-High Speed Receiver

- 4 ports of Ultra-High Speed Combo Receivers.
- Support two HDMI2.0 (6GHz), and two DisplayPort1.4 (5.4GHz, HBR2).
- In HDMI mode, the latest HDMI2.0 is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.2) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In DisplayPort mode, the latest DisplayPort 1.4 is supported
- In DisplayPort mode, three link layer speed HBR2 (5.4GHz), HBR (2.7GHz), RBR (1.62GHz) are supported

- In DisplayPort mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In DisplayPort mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.2) is supported
- In DisplayPort mode, DisplayPort audio is allowed to transmit to I2S/SPDIF output

High Speed Combo Receiver

- RTD2797UPM-CG supports 2 ports of High Speed Combo Receivers.
- Each port can be configured as HDMI1.4 (3GHz), MHL2.2 (3GHz), or DVI as desired
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In MHL mode, MHL2.2 is supported
- In MHL mode, High-Bandwidth Digital Content Protection (HDCP 1.4) is supported
- In MHL mode, packet pixel mode is supported
- In DVI mode, Digital Content Protection (HDCP 1.4) is supported
- In DVI mode, two adjacent receivers to support dual-link DVI with HDCP

Embedded MCU

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Audio

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- True 12-bit color processing engine
- Programmable 14-bit gamma support

- Programmable 12-bit 3D gamma support
- xvYCC supported
- Adobe/sRGB compliance
- Advanced dithering logic for the fewer panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Peaking/Coring function for video sharpness
- Support Ultra-Vivid III function to enhance image quality with minimal artificial effect on productivity applications
- Panel Uniformity (Brightness and color uniformity)
- Support 17x17x17 3D Gamma LUT
- Support EOTF(electro-optical transfer function): 10 bits SMPTE 2084
- Support Adaptive Tone-Mapping
- Support BT 2020

VividColor™

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- 2nd generation of Precise color mapping (PCM)
- Image Adaptive Power Saving Tech. (IAPS)
- Support ADC Noise Reduction

Embedded DDR3 Controller

- RTD2797UPM-CG support maximal 2 external 16-bit DDR3 DRAM
- Support DDR3 speed up to 1.6GHz
- Support 90 degree image rotation: Portrait-to-Landscape or Landscape-to-Portrait
- LiveShow™ Function, High-performance RTC (response time compensation).
- Frame Rate Control Function
- RTD2797UPM-CG supports PIP / PBP and 4P function

Output Interface

- RTD2797UPM-CG supports 8-lane V-by-One or 8-lane eDP (HBR) with the output format up to 4096x2160 @ 60Hz.
- Support 4-lane eDP (HBR2) with the output format up to 4096x2160 @ 60Hz.
- Support DisplayPort 1.4 HBR2 Multi-stream Transport (MST) with 3 maximal downstream capability.
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 64K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel

- 64 color palette
- Maximum 26 window with alpha-blending /
- gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow
- Rotate 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18 ~ 4x18 proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Power Supply

- 3.3V / 1.5V / 1.1V power supply

3. System Applications

- Display System on Motherboard, Monitor
- Display System for All in One PCs and embedded applications

4. Block Diagram

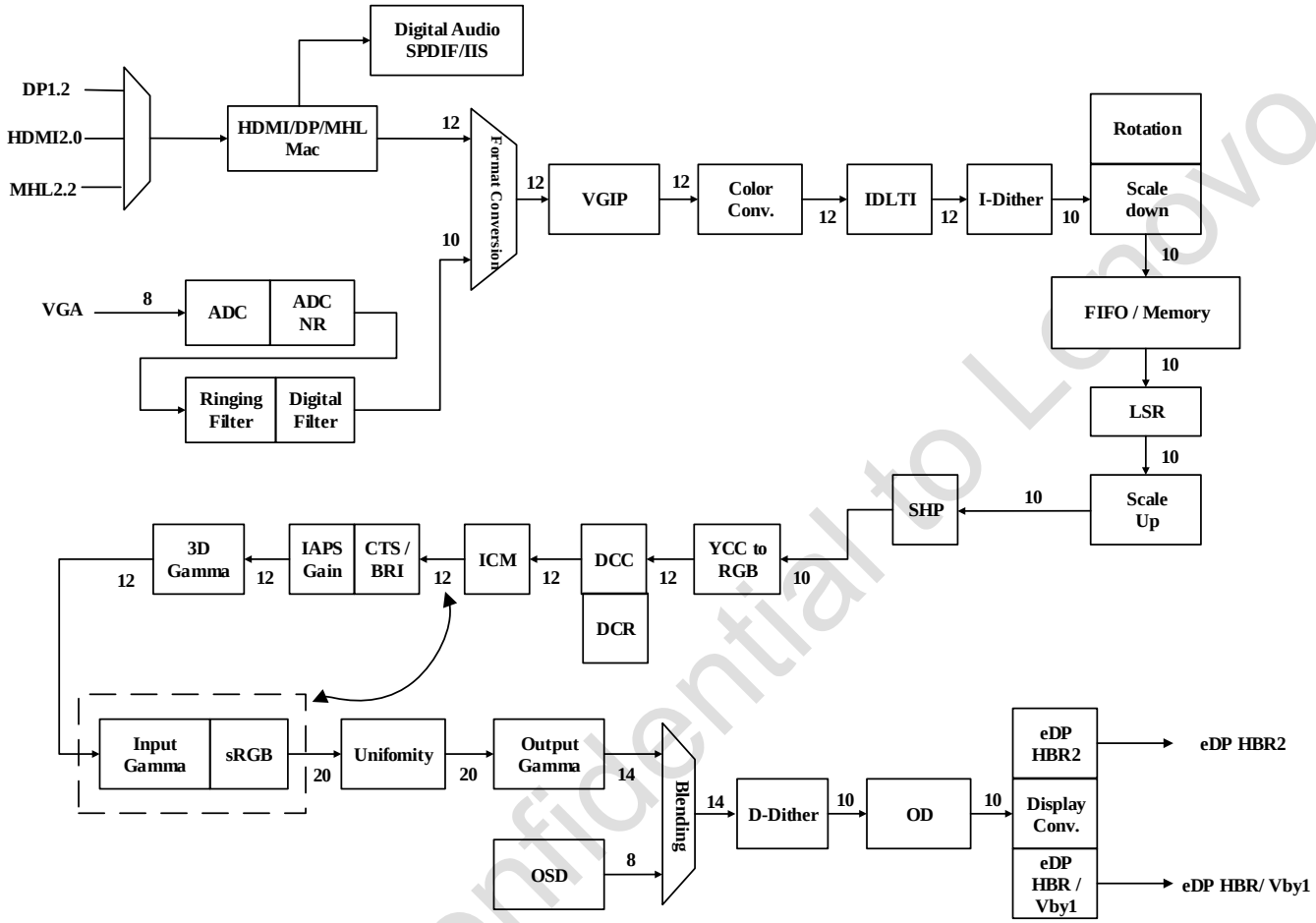
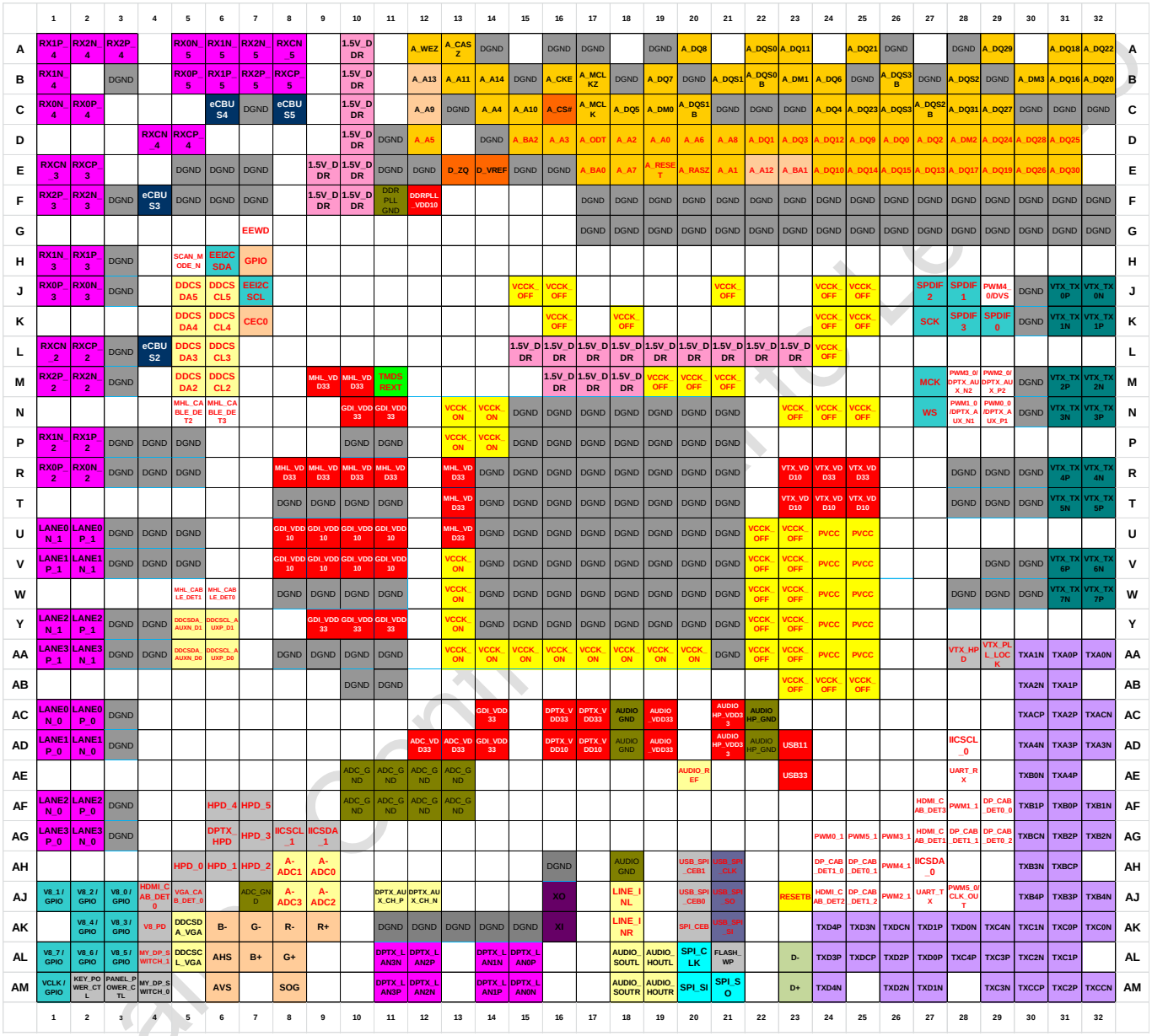


Figure 1. Data Path

5. Pin Assignments

640 Ball EDHS BGA



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
A	RX1P_4	RX2N_4	RX2P_4		RX0N_5	RX1N_5	RX2N_5	RXCN_5		1.5V_DDR		A_WEZ	A_CASZ	DGND		DGND	DGND		DGND	A_DQ8		A_DQS0	A_DQ11		A_DQ21	DGND		DGND	A_DQ29		A_DQ18	A_DQ22	A
B	RX1N_4		DGND		RX0P_5	RX1P_5	RX2P_5	RXCP_5		1.5V_DDR		A_A13	A_A11	A_A14	DGND	A_CKE	A_MCLKZ	DGND	A_DQ7	DGND	A_DQS1	A_DQS0B	A_DM1	A_DQ6	DGND	A_DQS3B	DGND	A_DQS2	DGND	A_DM3	A_DQ16	A_DQ20	B
C	RX0N_4	RX0P_4				eCBUS4	DGND	eCBUS5		1.5V_DDR		A_A9	DGND	A_A4	A_A10	A_CS#	A_MCLK	A_DQ5	A_DM0	A_DQS1B	DGND	DGND	DGND	A_DQ4	A_DQ23	A_DQS3	A_DQS2B	A_DQ31	A_DQ27	DGND	DGND	DGND	C
D				RXCN_4	RXCP_4					1.5V_DDR	DGND	A_A5		DGND	A_BA2	A_A3	A_ODT	A_A2	A_A0	A_A6	A_A8	A_DQ1	A_DQ3	A_DQ12	A_DQ9	A_DQ0	A_DQ2	A_DM2	A_DQ24	A_DQ28	A_DQ25		D
E	RXCN_3	RXCP_3			DGND	DGND	DGND		1.5V_DDR	1.5V_DDR	DGND	DGND	D_ZQ	D_VREF	DGND	DGND	A_BA0	A_A7	A_RESET	A_RASZ	A_A1	A_A12	A_BA1	A_DQ10	A_DQ14	A_DQ15	A_DQ13	A_DQ17	A_DQ19	A_DQ26	A_DQ30		E
F	RX2P_3	RX2N_3	DGND	eCBUS3	DGND	DGND	DGND		1.5V_DDR	1.5V_DDR	DDR PLL GND	DDRPLL VDD10					DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	F
G							EEWD										DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	G
H	RX1N_3	RX1P_3	DGND		SCAN_MODE_N	EEI2C SDA	GPIO																										H
J	RX0P_3	RX0N_3	DGND		DDCSDA5	DDCSCL5	EEI2C SCL								VCCK_OFF	VCCK_OFF					VCCK_OFF			VCCK_OFF	VCCK_OFF		SPDIF2	SPDIF1	PWM4_0/DVS	DGND	VTX_TX0P	VTX_TX0N	J
K					DDCSDA4	DDCSCL4	CEC0									VCCK_OFF		VCCK_OFF						VCCK_OFF	VCCK_OFF		SCK	SPDIF3	SPDIF0	DGND	VTX_TX1N	VTX_TX1P	K
L	RXCN_2	RXCP_2	DGND	eCBUS2	DDCSDA3	DDCSCL3									1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	1.5V_DDR	VCCK_OFF									L
M	RX2P_2	RX2N_2	DGND		DDCSDA2	DDCSCL2			MHL_VDD33	MHL_VDD33	TMDS REXT					1.5V_DDR	1.5V_DDR	1.5V_DDR	VCCK_OFF	VCCK_OFF	VCCK_OFF						MCK	PWM3_0/DPTX_AUX_N2	PWM2_0/DPTX_AUX_P2	DGND	VTX_TX2P	VTX_TX2N	M
N					MHL_CABLE_DET2	MHL_CABLE_DET3				GDI_VDD33	GDI_VDD33		VCCK_ON	VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	DGND		VCCK_OFF	VCCK_OFF	VCCK_OFF		WS	PWM1_0/DPTX_AUX_N1	PWM0_0/DPTX_AUX_P1	DGND	VTX_TX3N	VTX_TX3P	N
P	RX1N_2	RX1P_2	DGND	DGND	DGND					DGND	DGND		VCCK_ON	VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	DGND												P
R	RX0P_2	RX0N_2	DGND	DGND	DGND			MHL_VDD33	MHL_VDD33	MHL_VDD33	MHL_VDD33		MHL_VDD33	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND		VTX_VDD10	VTX_VDD33	VTX_VDD33			DGND	DGND	DGND	VTX_TX4P	VTX_TX4N	R
T								DGND	DGND	DGND	DGND		MHL_VDD33	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND		VTX_VDD10	VTX_VDD10	VTX_VDD10			DGND	DGND	DGND	VTX_TX5N	VTX_TX5P	T
U	LANE0N_1	LANE0P_1	DGND	DGND	DGND			GDI_VDD10	GDI_VDD10	GDI_VDD10	GDI_VDD10		MHL_VDD33	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF	VCCK_OFF	PVCC	PVCC							U
V	LANE1P_1	LANE1N_1	DGND	DGND	DGND			GDI_VDD10	GDI_VDD	GDI_VDD10	GDI_VDD10		VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF	VCCK_OFF	PVCC	PVCC				DGND	DGND	VTX_TX6P	VTX_TX6N	V
W					MHL_CABLE_DET1	MHL_CABLE_DET0		DGND	DGND	DGND	DGND		VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF	VCCK_OFF	PVCC	PVCC			DGND	DGND	DGND	VTX_TX7N	VTX_TX7P	W
Y	LANE2N_1	LANE2P_1	DGND	DGND	DDCSDA_AUXN_D1	DDCSCL_AUXP_D1			GDI_VDD33	GDI_VDD33	GDI_VDD33		VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF	VCCK_OFF	PVCC	PVCC							Y
AA	LANE3P_1	LANE3N_1	DGND	DGND	DDCSDA_AUXN_D0	DDCSCL_AUXP_D0		DGND	DGND	DGND	DGND		VCCK_ON	VCCK_ON	VCCK_ON	VCCK_ON	VCCK_ON	VCCK_ON	VCCK_ON	VCCK_ON	DGND	VCCK_OFF	VCCK_OFF	PVCC	PVCC			VTX_HPD	VTX_PLL_LOCK	TXA1N	TXA0P	TXA0N	AA
AB										DGND	DGND													VCCK_OFF	VCCK_OFF	VCCK_OFF					TXA2N	TXA1P		AB
AC	LANE0N_0	LANE0P_0	DGND											GDI_VDD33		DPTX_VDD33	DPTX_VDD33	AUDIO GND	AUDIO_VDD33		AUDIO HP_VDD33	AUDIO HP_GND									TXACP	TXA2P	TXACN	AC
AD	LANE1P_0	LANE1N_0	DGND									ADC_VDD33	ADC_VDD33	GDI_VDD33		DPTX_VDD10	DPTX_VDD10	AUDIO GND	AUDIO_VDD33		AUDIO HP_VDD33	AUDIO HP_GND	USB11					IICSCL_0		TXA4N	TXA3P	TXA3N	AD
AE										ADC_GND	ADC_GND	ADC_GND	ADC_GND							AUDIO_REF			USB33					UART_RX		TXB0N	TXA4P		AE
AF	LANE2N_0	LANE2P_0	DGND			HPD_4	HPD_5			ADC_GND	ADC_GND	ADC_GND	ADC_GND														HDMI_CAB_DET3	PWM1_1	DP_CAB_DET0_0	TXB1P	TXB0P	TXB1N	AF
AG	LANE3P_0	LANE3N_0	DGND			DPTX_HPD	HPD_3	IICSCL_1	IICSDA_1															PWM0_1	PWM5_1	PWM3_1	HDMI_CAB_DET1	DP_CAB_DET1_1	DP_CAB_DET0_2	TXBCN	TXB2P	TXB2N	AG
AH					HPD_0	HPD_1	HPD_2	A-ADC1	A-ADC0							DGND		AUDIO GND		USB_SPI_CEB1	USB_SPI_CLK			DP_CAB_DET1_0	DP_CAB_DET0_1	PWM4_1	IICSDA_0			TXB3N	TXBCP		AH
AJ	V8_1 / GPIO	V8_2 / GPIO	V8_0 / GPIO	HDMI_CAB_DET0	VGA_CAB_DET_0		ADC_GND	A-ADC3	A-ADC2		DPTX_AUX_CH_P	DPTX_AUX_CH_N				XO		LINE_INL		USB_SPI_CEB0	USB_SPI_SO		RESETB	HDMI_CAB_DET2	DP_CAB_DET1_2	PWM2_1	UART_TX	PWM5_0/CLK_OUT		TXB4P	TXB3P	TXB4N	AJ
AK		V8_4 / GPIO	V8_3 / GPIO	V8_PD	DDCSDA_VGA	B-	G-	R-	R+		DGND	DGND	DGND	DGND	DGND	XI		LINE_INR		SPI_CEB	USB_SPI_SI			TXD4P	TXD3N	TXDCN	TXD1P	TXD0N	TXC4N	TXC1N	TXC0P	TXC0N	AK
AL	V8_7 / GPIO	V8_6 / GPIO	V8_5 / GPIO	MY_DP_SWITCH_1	DDCSCL_VGA	AHS	B+	G+			DPTX_LAN3N	DPTX_LAN2P		DPTX_LAN1N	DPTX_LAN0P			AUDIO_SOUTL	AUDIO_HOUTL	SPI_CLK	FLASH_WP		D-	TXD3P	TXDCP	TXD2P	TXD0P	TXC4P	TXC3P	TXC2N	TXC1P		AL
AM	VCLK / GPIO	KEY_POWER_CTL	PANEL_POWER_CTL	MY_DP_SWITCH_0		AVS		SOG			DPTX_LAN3P	DPTX_LAN2N		DPTX_LAN1P	DPTX_LAN0N			AUDIO_SOUTR	AUDIO_HOUTR	SPI_SI	SPI_SO		D+	TXD4N		TXD2N	TXD1N		TXC3N	TXCCP	TXC2P	TXCCN	AM
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

Figure 2. Ball Diagram of EDHS BGA

6. Pin Assignments Table

EDHS BGA Pin Table

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Signals Total : 318 balls

Table 1. Signals Pin Assignment of EDHS BGA

Pin Name	I/O	Pin #	Description	Note
TMDS REXT	AI	M11	Impedance Match Reference Resistor For Scan mode,it should be pulled high	Ref value: 12 K ohm (Reference to GND)
eCBUS5 / HPD_5 / GPIO	AIO	C8	MHL eCBUS 5 / Hot Plug Detect 5 / MCU GPIO	5V tolerance even when power-off
RXCP_5	AI	B8	TMDS Differential Signal Input	3.3V tolerance
RXCN_5	AI	A8	TMDS Differential Signal Input	3.3V tolerance
RX2P_5	AI	B7	TMDS Differential Signal Input	3.3V tolerance
RX2N_5	AI	A7	TMDS Differential Signal Input	3.3V tolerance
RX1P_5	AI	B6	TMDS Differential Signal Input	3.3V tolerance
RX1N_5	AI	A6	TMDS Differential Signal Input	3.3V tolerance
RX0P_5 / MHLP	AI	B5	TMDS Differential Signal Input	3.3V tolerance
RX0N_5 / MHLN	AI	A5	TMDS Differential Signal Input	3.3V tolerance
eCBUS4 / HPD_4 / GPIO	AIO	C6	MHL eCBUS 4 / Hot Plug Detect 4 / MCU GPIO	5V tolerance even when power-off
RXCP_4	AI	D5	TMDS Differential Signal Input	3.3V tolerance
RXCN_4	AI	D4	TMDS Differential Signal Input	3.3V tolerance
RX2P_4	AI	A3	TMDS Differential Signal Input	3.3V tolerance
RX2N_4	AI	A2	TMDS Differential Signal Input	3.3V tolerance
RX1P_4	AI	A1	TMDS Differential Signal Input	3.3V tolerance
RX1N_4	AI	B1	TMDS Differential Signal Input	3.3V tolerance
RX0P_4 / MHLP	AI	C2	TMDS Differential Signal Input	3.3V tolerance
RX0N_4 / MHLP	AI	C1	TMDS Differential Signal Input	3.3V tolerance
eCBUS3 / HPD_3 / GPIO	AIO	F4	MHL eCBUS 3 / Hot Plug Detect 3 / MCU GPIO	5V tolerance even when power-off
RXCP_3	AI	E2	TMDS Differential Signal Input	3.3V tolerance
RXCN_3	AI	E1	TMDS Differential Signal Input	3.3V tolerance
RX2P_3	AI	F1	TMDS Differential Signal Input	3.3V tolerance
RX2N_3	AI	F2	TMDS Differential Signal Input	3.3V tolerance
RX1P_3	AI	H2	TMDS Differential Signal Input	3.3V tolerance
RX1N_3	AI	H1	TMDS Differential Signal Input	3.3V tolerance
RX0P_3 / MHLP	AI	J1	TMDS Differential Signal Input	3.3V tolerance
RX0N_3 / MHLP	AI	J2	TMDS Differential Signal Input	3.3V tolerance
eCBUS2 / HPD_2 / GPIO	AIO	L4	MHL eCBUS 2 / Hot Plug Detect 2 / MCU GPIO	5V tolerance even when power-off
RXCP_2	AI	L2	TMDS Differential Signal Input	3.3V tolerance
RXCN_2	AI	L1	TMDS Differential Signal Input	3.3V tolerance
RX2P_2	AI	M1	TMDS Differential Signal Input	3.3V tolerance

RX2N_2	AI	M2	TMDS Differential Signal Input	3.3V tolerance
RX1P_2	AI	P2	TMDS Differential Signal Input	3.3V tolerance
RX1N_2	AI	P1	TMDS Differential Signal Input	3.3V tolerance
RX0P_2 / MHLP	AI	R1	TMDS Differential Signal Input	3.3V tolerance
RX0N_2 / MHLP	AI	R2	TMDS Differential Signal Input	3.3V tolerance
LANE0P_1	AI	U2	DP Input : LANE0P / TMDS Differential Signal Input	3.3V tolerance
LANE0N_1	AI	U1	DP Input : LANE0N / TMDS Differential Signal Input	3.3V tolerance
LANE1P_1	AI	V1	DP Input : LANE1P / TMDS Differential Signal Input	3.3V tolerance
LANE1N_1	AI	V2	DP Input : LANE1N / TMDS Differential Signal Input	3.3V tolerance
LANE2P_1	AI	Y2	DP Input : LANE2P / TMDS Differential Signal Input	3.3V tolerance
LANE2N_1	AI	Y1	DP Input : LANE2N / TMDS Differential Signal Input	3.3V tolerance
LANE3P_1	AI	AA1	DP Input : LANE3P / TMDS Differential Signal Input	3.3V tolerance
LANE3N_1	AI	AA2	DP Input : LANE3N / TMDS Differential Signal Input	3.3V tolerance
LANE0P_0	AI	AC2	DP Input : LANE0P / TMDS Differential Signal Input	3.3V tolerance
LANE0N_0	AI	AC1	DP Input : LANE0N / TMDS Differential Signal Input	3.3V tolerance
LANE1P_0	AI	AD1	DP Input : LANE1P / TMDS Differential Signal Input	3.3V tolerance
LANE1N_0	AI	AD2	DP Input : LANE1N / TMDS Differential Signal Input	3.3V tolerance
LANE2P_0	AI	AF2	DP Input : LANE2P / TMDS Differential Signal Input	3.3V tolerance
LANE2N_0	AI	AF1	DP Input : LANE2N / TMDS Differential Signal Input	3.3V tolerance
LANE3P_0	AI	AG1	DP Input : LANE3P / TMDS Differential Signal Input	3.3V tolerance
LANE3N_0	AI	AG2	DP Input : LANE3N / TMDS Differential Signal Input	3.3V tolerance
MHL_CABLE_DET1 / GPIO / Test4b	IO	W5	MHL Cable Detect 1 / MCU GPIO	5V tolerance even when power-off
MHL_CABLE_DET0 / GPIO / Test4b	IO	W6	MHL Cable Detect 0 / MCU GPIO	5V tolerance even when power-off
DDCSCL_AUXP_D1 / GPIO	IO	Y6	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSDA_AUXN_D1 / GPIO	IO	Y5	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSCL_AUXP_D0 / GPIO	IO	AA6	AUX-CH 1 / DDC1 (Open drain I/O) / MCU GIPO	5V tolerance even when power-off
DDCSDA_AUXN_D0 /	IO	AA5	AUX-CH 1 / DDC1 (Open drain I/O) /	5V tolerance

GPIO			MCU GIPO	even when power-off
GPIO / Test4b	IO	AJ3	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AJ1	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AJ2	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AK3	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AK2	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AL3	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AL2	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AL1	MCU GPIO	5V tolerance even when power-off
GPIO / Test4b	IO	AM1	MCU GPIO	5V tolerance even when power-off
AVS	I	AM6	ADC vertical sync input	5V tolerance even when power-off
AHS	I	AL6	ADC horizontal sync input	5V tolerance even when power-off
B-	AI	AK6	Negatice Blue analog input (Pb-)	3.3V tolerance
B+	AI	AL7	Positive Blue analog input (Pb+)	3.3V tolerance
G-	AI	AK7	Negatice Green analog input (Y-)	3.3V tolerance
G+	AI	AL8	Positive Green analog input (Y+)	3.3V tolerance
SOG	AI	AM8	Sync-On-Green	3.3V tolerance
R-	AI	AK8	Negative RED analog input (Pr-)	3.3V tolerance
R+	AI	AK9	Positive RED analog input (Pr+)	3.3V tolerance
DDCSDA_VGA / GPIO	IO	AK5	DDC(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSCL_VGA / GPIO	IO	AL5	DDC(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
MY_DP_SWITCH_0 / PWM3 / TCON[8] / GPIO	IO	AM4	My DP Switch 0 / PWM / TCON / MCU GPIO	5V tolerance even when power-off
MY_DP_SWITCH_1 / PWM2 / TCON[7] / GPIO	IO	AL4	My DP Switch 1 / PWM / TCON / MCU GPIO	5V tolerance even when power-off

PWM1 / TCON[5] / INT0 / GPIO	IO	AK4	PWM / TCON / INT / MCU GPIO	5V tolerance even when power-off
VGA_CAB_DET_0 / PWM0 / TCON[4] / GPIO	IO	AJ5	VGA Cable Detect 0 / PWM / TCON / MCU GPIO	5V tolerance even when power-off
PANEL_POWER_CTL / PWM5 / TCON[12] / GPIO	IO	AM3	Panel Power Control / PWM / TCON / MCU GPIO	5V tolerance even when power-off
KEY_POWER_CTL / PWM4 / TCON[10] / INT1 / GPIO	IO	AM2	Key Power Control / PWM / TCON / MCU GPIO	5V tolerance even when power-off
IICSDA_1 / PWM0 / TCON[3] / GPIO	IO	AG9	IIC BUS / PWM / TCON / MCU GPIO	5V tolerance even when power-off
IICSCL_1 / PWM1 / TTCON[7] / GPIO	IO	AG8	IIC BUS / PWM / TCON / MCU GPIO	5V tolerance even when power-off
DP_HOT_PLUG_0 / GPIO / Test4b	IO	AH5	Hot Plug Detect 0 / MCU GPIO	5V tolerance even when power-off
DP_HOT_PLUG_1 / GPIO / Test4b	IO	AH6	Hot Plug Detect 1 / MCU GPIO	5V tolerance even when power-off
MHL_SEL_2 / GPIO / Test4b	IO	AH7	HDMI_MHL_SEL_2 / MCU GPIO	5V tolerance even when power-off
MHL_SEL_3 / GPIO / Test4b	IO	AG7	HDMI_MHL_SEL_3 / MCU GPIO	5V tolerance even when power-off
MHL_SEL_4 / GPIO / Test4b	IO	AF6	HDMI_MHL_SEL_4 / MCU GPIO	5V tolerance even when power-off
MHL_SEL_5 / GPIO / Test4b	IO	AF7	HDMI_MHL_SEL_5 / MCU GPIO	5V tolerance even when power-off
HDMI_CAB_DET0 / GPIO / Test4b	IO	AJ4	HDMI Cable Detect 0 / MCU GPIO	5V tolerance even when power-off
DPTX_HPD / GPIO	IO	AG6	DP Hot Plug Detect / MCU GPIO	5V tolerance even when power-off
A-ADC0 / INT0 / GPIO	IO	AH9	8-bit MCU ADC Input / INT /MCU GPIO	5V tolerance even when power-on
A-ADC1 / INT1 / GPIO	IO	AH8	8-bit MCU ADC Input / INT /MCU GPIO	5V tolerance even when power-on
A-ADC2 / GPIO	IO	AJ9	8-bit MCU ADC Input / MCU GPIO	5V tolerance even when power-on
A-ADC3 / GPIO	IO	AJ8	8-bit MCU ADC Input / MCU GPIO	5V tolerance even when power-on

DPTX_AUX_CH_P	IO	AJ11	DPTX_AUX_CH_P / GPIO	3.3V tolerance
DPTX_AUX_CH_N	IO	AJ12	DPTX_AUX_CH_N / GPIO	3.3V tolerance
DPTX_LAN3N	AO	AL11	DP Output : LANE3N	3.3V tolerance
DPTX_LAN3P	AO	AM11	DP Output : LANE3P	3.3V tolerance
DPTX_LAN2N	AO	AM12	DP Output : LANE2N	3.3V tolerance
DPTX_LAN2P	AO	AL12	DP Output : LANE2P	3.3V tolerance
DPTX_LAN1N	AO	AL14	DP Output : LANE1N	3.3V tolerance
DPTX_LAN1P	AO	AM14	DP Output : LANE1P	3.3V tolerance
DPTX_LAN0N	AO	AM15	DP Output : LANE0N	3.3V tolerance
DPTX_LAN0P	AO	AL15	DP Output : LANE0P	3.3V tolerance
XI	AI	AK16	Crystal Input	3.3V tolerance
XO	AO	AJ16	Crystal Output	3.3V tolerance
LINE_INL	AI	AJ18	LINE-IN / IIS-WS / MCU GPIO	3.3V tolerance
LINE_INR	AI	AK18	LINE-IN / IIS-SCK / MCU GPIO	3.3V tolerance
AUDIO_REF	I	AE20	Audio Reference Resustance / IIS-MCK / MCU GPIO	3.3V tolerance
AUDIO_SOUTL / SD0 / SPDIF0 / GPIO	AO	AL18	Audio Speaker Output / IIS-SD0 / SPDIF 0 / MCU GPIO	3.3V tolerance
AUDIO_SOUTR / SD1 / SPDIF1 / GPIO	AO	AM18	Audio Speaker Output / IIS-SD1 / SPDIF 1 / MCU GPIO	3.3V tolerance
AUDIO_HOUTL / SD2 / SPDIF2 / GPIO	AO	AL19	Audio Headphone Output / IIS-SD2 / SPDIF 2 / MCU GPIO	3.3V tolerance
AUDIO_HOUTR / SD3 / SPDIF3 / GPIO	AO	AM19	Audio Headphone Output / IIS-SD3 / SPDIF 3 / MCU GPIO	3.3V tolerance
SPI_SI	IO	AM20	SPI flash serial data input	3.3V tolerance
SPI_CLK	IO	AL20	SPI flash serial clock	3.3V tolerance
SPI_CEB	IO	AK20	SPI flash chip enable bar	3.3V tolerance
SPI_SO	IO	AM21	SPI flash serial data output	3.3V tolerance
USB_SPI_CLK / CLKO / GPIO	IO	AH21	Serial clock / CLKO /MCU GPIO	5V tolerance even when power-off
FLASH_WP / GPIO	IO	AL21	FLASH Write Protect / MCU GPIO	3.3V tolerance
USB_SPI_SO / INT1 / GPIO	IO	AJ21	Serial data output / INT /MCU GPIO	5V tolerance even when power-off
USB_SPI_SI / INT0 / GPIO	IO	AK21	Serial data input / INT / MCU GPIO	5V tolerance even when power-off
USB_SPI_CEB1 / T2EX/ GPIO	IO	AH20	SPI chip enable bar 1 /T2EX/ MCU GPIO	5V tolerance even when power-off
USB_SPI_CEB0 / IRQB / GPIO	IO	AJ20	SPI chip enable bar 0 /IRQB / MCU GPIO	5V tolerance even when power-off
RESETB	I	AJ23	Chip reset bar	3.3V tolerance
HDMI_CAB_DET2 / SCK / GPIO / Test4b	IO	AJ24	HDMI Cable Detect 2/ IIS-SCK / MCU GPIO	5V tolerance even when power-off
HDMI_CAB_DET1 / WS / GPIO / Test4b	IO	AG27	HDMI Cable Detect 1 / IIS-WS / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET1_0 / TCON[8] / GPIO /	IO	AH24	DP Cable Detect 1_0/ TCON / MCU GPIO	5V tolerance even when

Test4b				power-off
HDMI_CAB_DET3 / MCK / GPIO / Test4b	IO	AF27	HDMI Cable Detect 3/ IIS-MCK / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET1_2 / SD1 / SPDIF1 / TCON[10] / GPIO	IO	AJ25	DP Cable Detect 1_2 / IIS-SD1 / SPDIF1 / TCON / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET1_1 / SD0 / SPDIF0 / TCON[9] / GPIO	IO	AG28	DP Cable Detect 1_1 / IIS-SD0 / SPDIF0 / TCON / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET0_1 / SD3 / SPDIF3 / TCON[12] / GPIO	IO	AH25	DP_CAB_DET0_1 / SD3 / SPDIF3 / TCON / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET0_0 / SD2 / SPDIF2 / TCON[11] / GPIO	IO	AF29	DP_CAB_DET0_0 / SD2 / SPDIF2 / TCON / MCU GPIO	5V tolerance even when power-off
UART_TX/ TCON[0] / GPIO / Test4b	IO	AJ27	UART TX / TCON / MCU GPIO	5V tolerance even when power-off
DP_CAB_DET0_2 / TCON[13] / GPIO / Test4b	IO	AG29	DP_CAB_DET0_2/ TCON / MCU GPIO / Test4b	5V tolerance even when power-off
PWM0_1 / TCON[2] / GPIO / PCB_POWE_DOWN / Test4b	IO	AG24	PWM / TCON / MCU GPIO / PCB Power Down	5V tolerance even when power-off
UART_RX / TCON[1] / GPIO / Test4b	IO	AE28	UART RX / TCON/ MCU GPIO	5V tolerance even when power-off
PWM2_1 / TCON[4] / IR_RECEIVER / GPIO	IO	AJ26	PWM / TCON / IR Receiver / MCU GPIO	5V tolerance even when power-off
PWM1_1 / TCON[3] / GPIO / Test4b	IO	AF28	PWM / TCON / MCU GPIO	5V tolerance even when power-off
PWM4_1 / TCON[6] / T1 / GPIO	IO	AH26	PWM / TCON / T1 / MCU GPIO	5V tolerance even when power-off
PWM3_1 / TCON[5] / T2 / GPIO	IO	AG26	PWM / TCON / T2/ MCU GPIO	5V tolerance even when power-off
PWM5_0 /XTAL_CLK_OUT / TCON[11] / GPIO	IO	AJ28	PWM / XTAL_CLK_OUT / TCON / MCU GPIO	5V tolerance even when power-off
PWM5_1 / TCON[7] / T0 / GPIO	IO	AG25	PWM / TCON / T0 / MCU GPIO	5V tolerance even when power-off
IICSDA_0 / TCON[5] / GPIO / Test4b	IO	AH27	IIC BUS / TCON / MCU GPIO	5V tolerance even when power-off
IICSCL_0 / TCON[4] / GPIO / Test4b	IO	AD28	IIC BUS / TCON / MCU GPIO	5V tolerance even when power-off
VTX_HPD / DP	IO	AA28	V-by-One Hot Plug Detect / DPTX Hot	5V tolerance

TX_HPD_1 / GPIO / Test4b			Plug Detect 1 / MCU GPIO	even when power-off
VTX_PLL_LOCK / DP TX_HPD_2 / GPIO / Test4b	IO	AA29	V-by-One PLL Lock / DPTX Hot Plug Detect 2 / MCU GPIO	5V tolerance even when power-off
NA	-	AL23	NA	
NA	-	AM23	NA	
NA	-	AK24	NA	
NA	-	AM24	NA	
NA	-	AL24	NA	
NA	-	AK25	NA	
NA	-	AL25	NA	
NA	-	AK26	NA	
NA	-	AL26	NA	
NA	-	AM26	NA	
NA	-	AK27	NA	
NA	-	AM27	NA	
NA	-	AL27	NA	
NA	-	AK28	NA	
NA	-	AL28	NA	
NA	-	AK29	NA	
NA	-	AL29	NA	
NA	-	AM29	NA	
NA	-	AM30	NA	
NA	-	AM32	NA	
NA	-	AM31	NA	
NA	-	AL30	NA	
NA	-	AL31	NA	
NA	-	AK30	NA	
NA	-	AK31	NA	
NA	-	AK32	NA	
NA	-	AJ30	NA	
NA	-	AJ32	NA	
NA	-	AJ31	NA	
NA	-	AH30	NA	
NA	-	AH31	NA	
NA	-	AG30	NA	
NA	-	AG31	NA	
NA	-	AG32	NA	
NA	-	AF30	NA	
NA	-	AF32	NA	
NA	-	AF31	NA	
NA	-	AE30	NA	
NA	-	AE31	NA	
NA	-	AD30	NA	

NA	-	AD31	NA	
NA	-	AD32	NA	
NA	-	AC30	NA	
NA	-	AC32	NA	
NA	-	AC31	NA	
NA	-	AB30	NA	
NA	-	AB31	NA	
NA	-	AA30	NA	
NA	-	AA31	NA	
NA	-	AA32	NA	
VTX_TX7N / DPTX_LANE3N_1	AO	W31	V-by-One Output : 7N / DP Output :LANE3N	3.3V tolerance
VTX_TX7P / DPTX_LANE3P_1	AO	W32	V-by-One Output : 7P / DP Output :LANE3P	3.3V tolerance
VTX_TX6N / DPTX_LANE2N_1	AO	V32	V-by-One Output : 6N / DP Output :LANE2N	3.3V tolerance
VTX_TX6P / DPTX_LANE2P_1	AO	V31	V-by-One Output : 6P / DP Output :LANE2P	3.3V tolerance
VTX_TX5N / DPTX_LANE1N_1	AO	T31	V-by-One Output : 5N / DP Output :LANE1N	3.3V tolerance
VTX_TX5P / DPTX_LANE1P_1	AO	T32	V-by-One Output : 5P / DP Output :LANE1P	3.3V tolerance
VTX_TX4N / DPTX_LANE0N_1	AO	R32	V-by-One Output : 4N / DP Output :LANE0N	3.3V tolerance
VTX_TX4P / DPTX_LANE0P_1	AO	R31	V-by-One Output : 4P / DP Output :LANE0P	3.3V tolerance
VTX_TX3N / DPTX_LANE3N_2	AO	N31	V-by-One Output : 3N / DP Output :LANE3N	3.3V tolerance
VTX_TX3P / DPTX_LANE3P_2	AO	N32	V-by-One Output : 3P / DP Output :LANE3P	3.3V tolerance
VTX_TX2N / DPTX_LANE2N_2	AO	M32	V-by-One Output : 2N / DP Output :LANE2N	3.3V tolerance
VTX_TX2P / DPTX_LANE2P_2	AO	M31	V-by-One Output : 2P / DP Output :LANE2P	3.3V tolerance
VTX_TX1N / DPTX_LANE1N_2	AO	K31	V-by-One Output : 1N / DP Output :LANE1N	3.3V tolerance
VTX_TX1P / DPTX_LANE1P_2	AO	K32	V-by-One Output : 1P / DP Output :LANE1P	3.3V tolerance
VTX_TX0N / DPTX_LANE0N_2	AO	J32	V-by-One Output : 0N / DP Output :LANE0N	3.3V tolerance
VTX_TX0P / DPTX_LANE0P_2	AO	J31	V-by-One Output : 0P / DP Output :LANE0P	3.3V tolerance
WS / TCON[12] / GPIO / Test4b	IO	N27	IIS-WS / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
SCK / TCON[13] / GPIO / Test4b	IO	K27	IIS-SCK / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
MCK / GPIO / Test4b	IO	M27	IIS-MCK / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off

SPDIF0 / SD0 / TCON[0] /GPIO / Test4b	IO	K29	SPDIF0 / IIS-SD0 / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
SPDIF1 / SD1 / TCON[1] / GPIO / Test4b	IO	J28	SPDIF1 / IIS-SD1 / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
SPDIF2 / SD2 / TCON[2] / GPIO / Test4b	IO	J27	SPDIF2 / IIS-SD2 / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
SPDIF3 / SD3 / TCON[3] / GPIO / Test4b	IO	K28	SPDIF3 / IIS-SD2 / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
PWM4_0 / DVS / TCON[10] / GPIO	IO	J29	PWM / DVS / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
PWM0_0 / DPTX_AUX_CH_P_1 / TCON[6] / GPIO	IO	N29	PWM / DPTX AUX-CH / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
PWM1_0 / DPTX_AUX_CH_N_1 / TCON[7] / GPIO	IO	N28	PWM / DPTX AUX-CH / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
PWM2_0 / DPTX_AUX_CH_P_2 / TCON[8] / GPIO	IO	M29	PWM / DPTX AUX-CH / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
PWM3_0 / DPTX_AUX_CH_N_2 / TCON[9] / GPIO	IO	M28	PWM / DPTX AUX-CH / TCON / MCU GPIO (This pin can not work when power saving & power Down.)	5V tolerance even when power-off
D_VREF	I	E14	Reference Voltage	
A_BA0	IO	E17	Bank Address Input	
A_BA1	IO	E23	Bank Address Input	
A_BA2	IO	D15	Bank Address Input	
A_A0	IO	D19	Address Input	
A_A1	IO	E21	Address Input	
A_A2	IO	D18	Address Input	
A_A3	IO	D16	Address Input	
A_A4	IO	C14	Address Input	
A_A5	IO	D12	Address Input	
A_A6	IO	D20	Address Input	
A_A7	IO	E18	Address Input	
A_A8	IO	D21	Address Input	
A_A9	IO	C12	Address Input	
A_A10	IO	C15	Address Input	
A_A11	IO	B13	Address Input	
A_A12	IO	E22	Address Input	
A_A13	IO	B12	Address Input	
A_A14	IO	B14	Address Input	
A_DM0	IO	C19	Input Data Mask	
A_DM1	IO	B23	Input Data Mask	
A_DM2	IO	D28	Input Data Mask	

A_DM3	IO	B30	Input Data Mask	
A_DQ0	IO	D26	Data Input / Output	
A_DQ1	IO	D22	Data Input / Output	
A_DQ2	IO	D27	Data Input / Output	
A_DQ3	IO	D23	Data Input / Output	
A_DQ4	IO	C24	Data Input / Output	
A_DQ5	IO	C18	Data Input / Output	
A_DQ6	IO	B24	Data Input / Output	
A_DQ7	IO	B19	Data Input / Output	
A_DQ8	IO	A20	Data Input / Output	
A_DQ9	IO	D25	Data Input / Output	
A_DQ10	IO	E24	Data Input / Output	
A_DQ11	IO	A23	Data Input / Output	
A_DQ12	IO	D24	Data Input / Output	
A_DQ13	IO	E27	Data Input / Output	
A_DQ14	IO	E25	Data Input / Output	
A_DQ15	IO	E26	Data Input / Output	
A_DQ16	IO	B31	Data Input / Output	
A_DQ17	IO	E28	Data Input / Output	
A_DQ18	IO	A31	Data Input / Output	
A_DQ19	IO	E29	Data Input / Output	
A_DQ20	IO	B32	Data Input / Output	
A_DQ21	IO	A25	Data Input / Output	
A_DQ22	IO	A32	Data Input / Output	
A_DQ23	IO	C25	Data Input / Output	
A_DQ24	IO	D29	Data Input / Output	
A_DQ25	IO	D31	Data Input / Output	
A_DQ26	IO	E30	Data Input / Output	
A_DQ27	IO	C29	Data Input / Output	
A_DQ28	IO	D30	Data Input / Output	
A_DQ29	IO	A29	Data Input / Output	
A_DQ30	IO	E31	Data Input / Output	
A_DQ31	IO	C28	Data Input / Output	
A_DQS0	IO	A22	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS0B	IO	B22	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS1	IO	B21	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS1B	IO	C20	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS2	IO	B28	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS2B	IO	C27	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_DQS3	IO	C26	Data strobe : Output with read data. Edge-aligned with read data. Input with	

			write data. Center-aligned to write data	
A_DQS3B	IO	B26	Data strobe : Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data	
A_CASZ	IO	A13	Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to VREFCA.	
A_CKE	IO	B16	Clock enable	
A_CS#	IO	C16	Chip select	
A_MCLK	IO	C17	Clock : A_ MCLK and A_ MCLKZ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of A_MCLK and negative edge of A_MCLKZ.	
A_MCLKZ	IO	B17	Clock : A_ MCLK and A_ MCLKZ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of A_MCLK and negative edge of A_MCLKZ.	
A_ODT	IO	D17	On-die termination : ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM.	
A_RASZ	IO	E20	Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to VREFCA.	
A_RESET	IO	E19	Reset : A_RESET is an active LOW CMOS input referenced to VSS.	
A_WEZ	IO	A12	Command inputs : A_RASZ, A_CASZ, and A_WEZ (along with A_CS#) define the command being entered and are referenced to VREFCA.	
D_ZQ	I	E13	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (1%), which is tied to VSSQ.	
GPIO / Test4b	IO	H7	MCU GPIO	5V tolerance even when power-off
CEC0 / GPIO	IO	K7	CEC 0 / MCU GPIO	5V tolerance even when power-off
EEWD / PWM2 / Tcon[3] / GPIO	IO	G7	EEWD / PWM / Tcon / MCU GPIO	3.3V tolerance
EEI2CSCL / PWM0 / TCON[1] / GPIO	IO	J7	EEI2CSCL / PWM / TCON / MCU GPIO	3.3V tolerance

EEI2CSDA / PWM1 / TCON[2] / GPIO	IO	H6	EEI2CSDA / PWM / TCON / MCU GPIO	3.3V tolerance
SCAN_MODE_N	IO	H5	When AC power is turned on, this ball must be pull “High”.	3.3V tolerance
DDCSCL5 / GPIO	IO	J6	DDC5(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSDA5 / GPIO	IO	J5	DDC5(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSCL4 / GPIO	IO	K6	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSDA4 / GPIO	IO	K5	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSCL3 / GPIO	IO	L6	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSDA3 / GPIO	IO	L5	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSCL2 / GPIO	IO	M6	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
DDCSDA2 / GPIO	IO	M5	DDC4(Open drain I/O) / MCU GPIO	5V tolerance even when power-off
MHL_CABLE_DET2 / GPIO / Test4b	IO	N5	MHL Cable Detect 2 / MCU GPIO	5V tolerance even when power-off
MHL_CABLE_DET3 / GPIO / Test4b	IO	N6	MHL Cable Detect 3 / MCU GPIO	5V tolerance even when power-off

Power / Ground Pin Assigment

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Total : 322 balls

Table 2. Power / Ground Pin Assignment of EDHS BGA

P/G Pin Name	I/O	Pin #	Description	Note
GDI_VDD33	AP	N10, N11, Y9, Y10, Y11, AC14, AD14	3.3V Analog Power	7 balls
GDI_VDD11	AP	U8, U9, U10, U11, V8, V9, V10, V11	1.1V Analog Power	8 balls
MHL_VDD33	AP	R8, R9, R10, R11, T13, U13, M9, M10, R13	3.3V Analog Power	9 balls
ADC_VDD33	AP	AD12, AD13	3.3V ADC Power	2 balls
ADC_GND	AG	AJ7, AE11, AF11, AE10, AF10, AE12, AF12, AE13, AF13	ADC Gound	9 balls
DPTX_VDD11	AP	AD16, AD17	1.1V DPTx Power	2 balls
DPTX_VDD33	AG	AC16, AC17	3.3V DPTx Power	2 balls

AUDIO_VDD33	AP	AC19, AD19	3.3V Audio Power	2 balls
AUDIO_GND	AG	AC18, AD18, AH18	Audio Gound	3 balls
AUDIO HP _VDD33	AP	AC21, AD21	3.3V Audio HP Power	2 balls
AUDIO HP_GND	AG	AC22, AD22	Audio HP Ground	2 balls
USB11	AP	AD23	USB 1.1V	1 ball
USB33	AP	AE23	USB 3.3V	1 ball
VTX_VDD10	AP	R23, T23, T24, T25	1.1V Analog Power	4 balls
VTX_VDD33	AP	R24, R25	3.3V Analog Power	2 balls
PVCC	P	U25, V24, V25, W24, U24, W25, Y24, Y25, AA24, AA25	Pad Power	10 balls
1.5V_DDR	P	A10, B10, C10, D10, E9, E10, F9, F10, L15, L16, L17, L18, L19, L20, M16, M17, M18, L21, L22, L23	1.5V DDR3 Power	20 balls
VCCK_ON	P	AA18, AA17, AA16, AA13, Y13, W13, P13, N14, N13, P14, V13, AA14, AA15, AA19, AA20	1.1V Core Power	15 balls
VCCK_OFF	P	L24, M21, M19, M20, K24, K25, K16, K18, J15, J16, J21, J24, J25, N23, N24, N25, U22, U23, V22, V23, W22, W23, Y22, Y23, AA22, AA23, AB23, AB24, AB25	1.1V Core Power	29 balls
DDRPLL_VDD10	P	F12	1.1V DDR PLL Power	1 ball
DDR PLL GND	G	F11	DDR PLL Ground	1 ball
DGND	G	A14, A16, A17, A19, A26, A28, B15, B18, B20, B25, B27, B29, C13, C21, C22, C23, C30, C31, C32, D11, D14, E11, E12, E15, E16, F17, F18, F19, F20, F21, F22, F23, F25, F26, F27, F28, G17, G18, G20, G21, G22, G23, G24, G25, G26, G27, G28, H3, J3, J30, T8, T9, T10, T11, U3, U4, U5, V14, V15, V16, V17, V18, V19, V20, V21, W14, W15, W16, W17, W18, W19, W20, W21, W28, W29, Y14, Y15, Y16, Y17, Y18, Y19, Y20, Y21, AA3, AA4, AA8, AA9, AA10, AA11, AA21, N20, P3, P4, P5, P10, P11, P15, P16, P17, P18, P20, P21, R3, R4, R14, R15, P19, R5, R16, B3, C7, E5, E6, E7, F3, F5, F6, F7, F24, F29, F30, F31, F32, G19, G29, G30, G31, G32, K30, L3, M3, M30, N15, N16, N17, N18, N19, N30, R17, R18, R19, R20, R21, R28, R29, R30, T14, T15, T16, T17, T18, T19, T20, T21, T28,	Digital Ground	190 balls

		T29, T30, U14, U15, U16, U17, U18, U19, U20, U21, V3, V4, V5, V29, V30, W8, W9, W10, W11, W30, Y3, Y4, AB10, AB11, AC3, AD3, AF3, AG3, AH16, AK11, AK12, AK13, AK14, AK15, N21		

7. Register Description

8. Electrical Specifications

PBGA DC Characteristics

8.1. Recommended Operating Conditions

Table 3. Recommended Operating Conditions of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	V_{IN}	-1		5.3	V
Supply Voltage	PVCC	3.14	3.30	3.47	V
DDR Voltage	1.5V_DDR	1.43	1.5	1.57	V
Core Power On Voltage	VCCK_ON	1.05	1.1	1.15	V
Core Power Off Voltage	VCCK_OFF	1.05	1.1	1.15	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage Temperature (plastic)	T_{STG}	-55		110	ºC
Thermal Resistance (Junction to Air)	θ_{JA}		18.05		ºC/W
Thermal Resistance (Junction to Case)	θ_{JC}		6.61		ºC/W
Junction Acceptable Temperature	T_j			125	ºC

8.2. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	PVCC			3.6	V
Storage Temperature (plastic)	T_{STG}			150	ºC
Junction Acceptable Temperature	T_j			125	ºC

Note : Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

8.3. Reset Period

Table 5. Reset Period of PBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en[1]	1120			ns
Power-on-Reset Period	Tpor-rst[2]	145	146.5	148	ms

1. 16 * Xtal_cycle(1/14.3Mhz)
2. 65536*16*2*Xtal_cycle(1/14.3Mhz)

9. Mechanical Specifications

PBGA

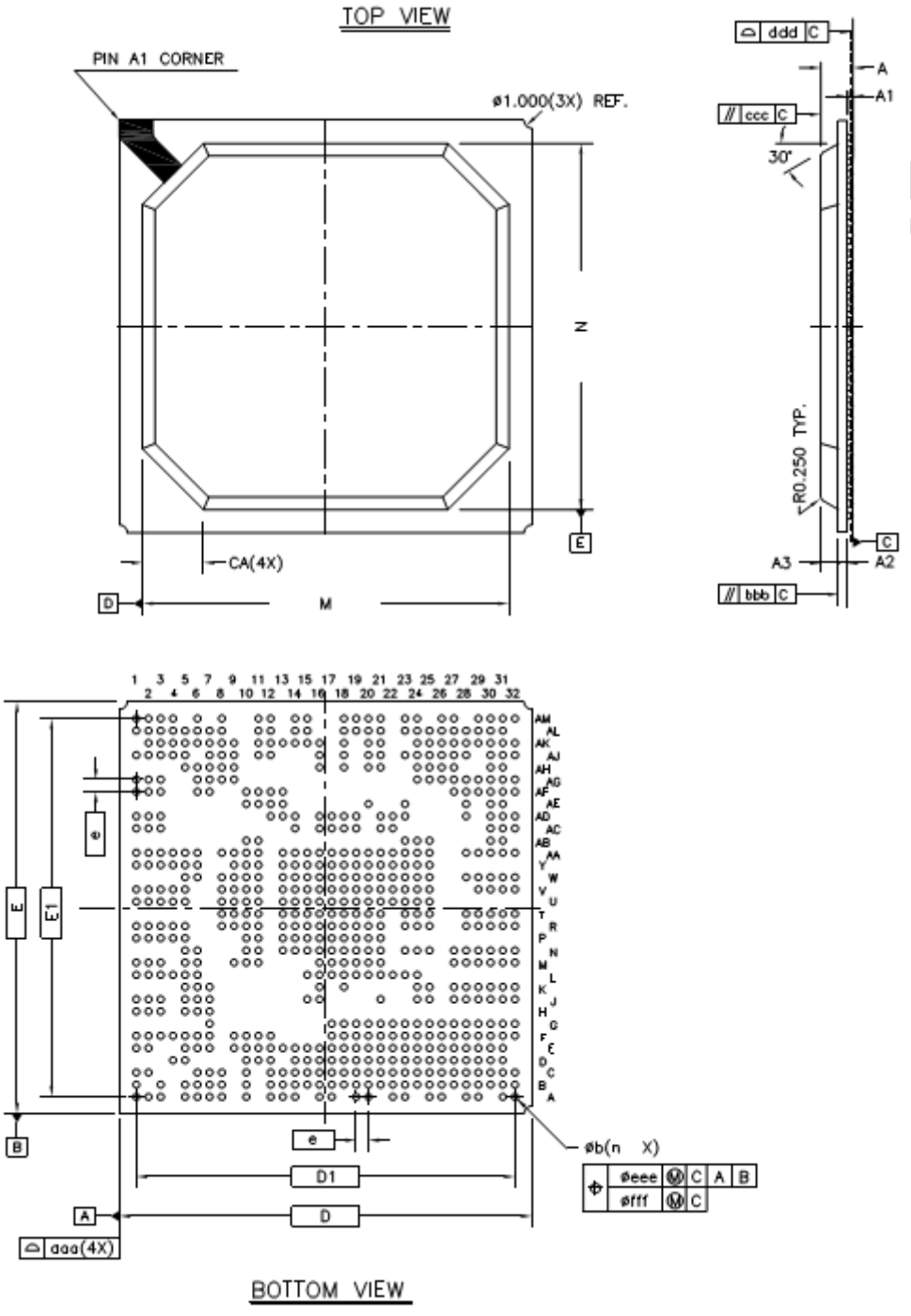


Figure 3. Mechanical Specification of PBGA (1)

		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			HS FBGA		
Body Size:	X	D	27.000		
	Y	E	27.000		
Ball Pitch :		e	0.800		
Total Thickness :		A	1.982	2.100	2.218
Mold Thickness :		A3	1.170 Ref.		
Substrate Thickness :		A2	0.560 Ref.		
Ball Diameter :			0.450		
Stand Off :		A1	0.320	–	0.420
Ball Width :		b	0.375	–	0.525
Mold Area :	X	M	24.000		
	Y	N	24.000		
H/S Exposed Size:		P	19 ~ 20		
H/S Flatness		Q	0.100		
H/S Shift With Substrate Edge:		R	0.300		
H/S Shift With Mold Area:		S	0.500		
Chamfer		CA	4.000 Ref.		
Package Edge Tolerance :		aaa	0.150		
Substrate Parallelism :		bbb	0.100		
Mold Parallelism :		ccc	0.200		
Coplanarity:		ddd	0.150		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	640		
Edge Ball Center to Center :	X	D1	24.800		
	Y	E1	24.800		

Unit: mm

Figure 4. Mechanical Specification of PBGA (2)

10. Ordering Information

Table 6. Ordering Information

Part No.	Max. Resolution / Timing	Input: VGA	Input: HDMI2.0	Input DP1.2 HBR2	Input: HDMI1.4/ MHL2/DVI	Output: DP1.2 MST out	Output: Vx1 / eDP HBR/ eDP HBR2	PIP/ PBP	4P	FRC	OD	Max number of DDR3 support	Package
RTD2797UPM-CG	4096x2160 @60Hz	●	2 Port	2 Port	2 Port	●	●	●	●	●	●	2	640-ball PBGA

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