

RTD2486VTD**Multi-Function Display Controller****Specification**

Version 3.1
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1. Features

General

- Embedded 3 DDC with DDC1/2B/CI
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.
- Support input format up to FHD
- Embedded 1.2V LDO for ADC

Crystal

- Support 27MHz/24MHz/14.318MHz crystal type

Analog RGB Input Interface

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

HDMI 1.4 Compliant Digital Input Interface with HDCP

- HDMI Input with embedded high speed switch
- Single link on-chip TMDS receiver up to 225MHz.
- Support long cable
- Adaptive algorithm for TMDS capability
- Data enable only mode support
- High-Bandwidth Digital Content Protection (HDCP 1.4)
- Enhanced protection of HDCP secret key
- Capable of 8-channel I2S/SPDIF output in HDMI application
- ATC Lab certification pass HDMI1.4a compliance test
- Support DVI 1.0 with HDCP 1.1
- CEC

DisplayPort 1.2 Digital Input Interface with HDCP 1.4

- Support 4 lanes digital input, each lanes speed up to 1.62Gbps and 2.7Gbps
- Support 6-bit, 8-bit, 10-bit, and 12-bit color depth transport
- High-Bandwidth Digital Content Protection (HDCP 1.4)
- Capable of 8-channel I2S/SPDIF output in DP

application

Embedded MCU

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master hardware supported

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Audio

- Output: IIS , SPDIF
- Embedded 2ch Audio DAC
- Embedded headphone amp
- DVC(Digital Volume Control)

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- True 10 bits color processing engine
- xvYCC supported
- sRGB compliance
- Advanced dithering logic for 18-bit panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support
- Peaking/Coring function for video sharpness
- Support UltraVivid function to enhance image quality

VividColor™

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- Precise color mapping (PCM)
- Image Adaptive Power Saving Tech. (IAPS)
- Support UltraVivid function to enhance image quality

LiveShow™ Function

- High-performance RTC (response time compensation).

Frame Rate Control Function**Output Interface**

- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- 1 and 2 pixel/clock panel support and up to FHD resolution(option). 93MHz for single LVDS. 186MHz for dual LVDS.
- LVDS -output interface on single PCB
- Support 8-bit LVDS output and 10-bit LVDS output
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 20K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 18 window with alpha-blending/ gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Power Supply

- 3.3V / 1.2V power supply
- Low standby current (Power Saving < 9mA, Power Down < 9mA @25°C)

2. Ordering Information

Part No.	VGA	DVI	HDMI	DP	HDCP	Audio DAC	OD	FRC	Max. Resolution	Output	PKG
RTD2486VTD-CG	Yes (210MHz)	No	Yes	Yes	Yes	Yes	Yes	Yes	1920*1200 2048*1152 (1:1)	Dual-LVDS	LQFP128 (green package)

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3. Chip Data Path Block Diagram

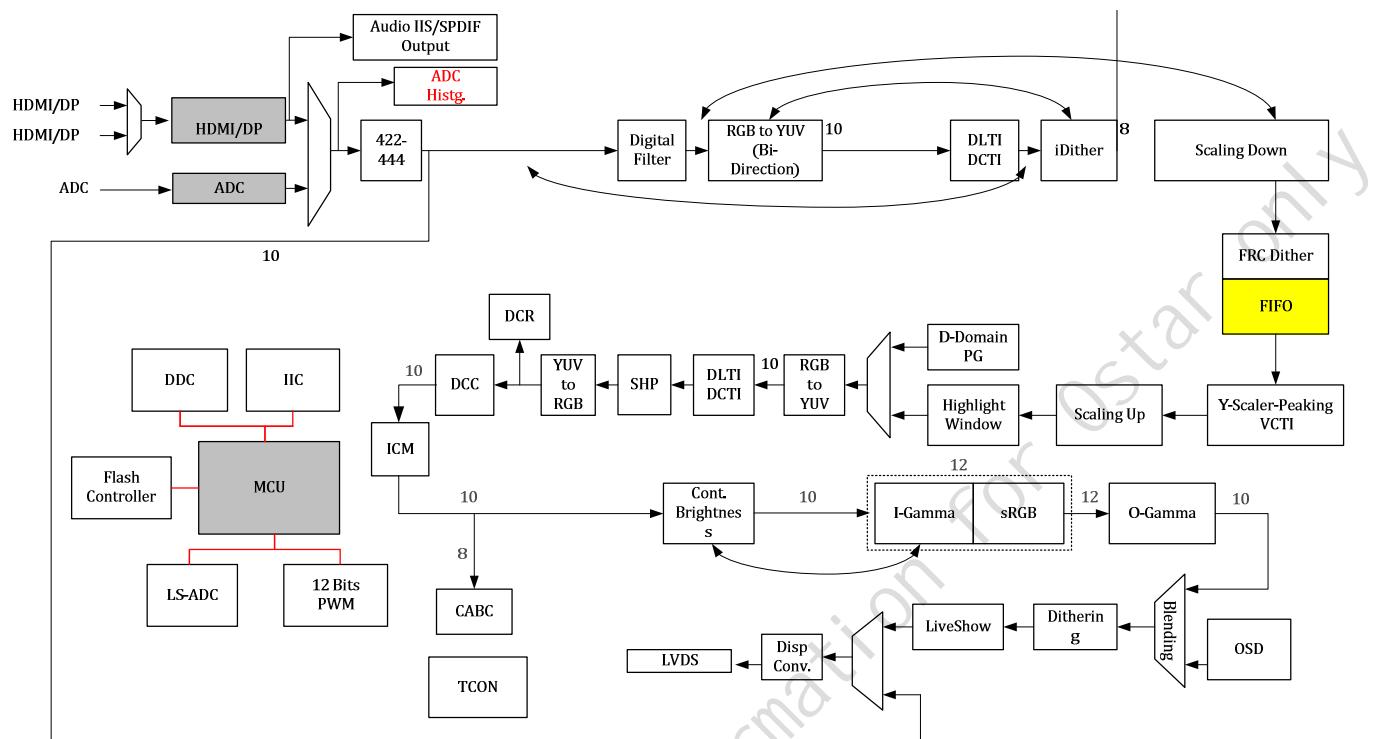
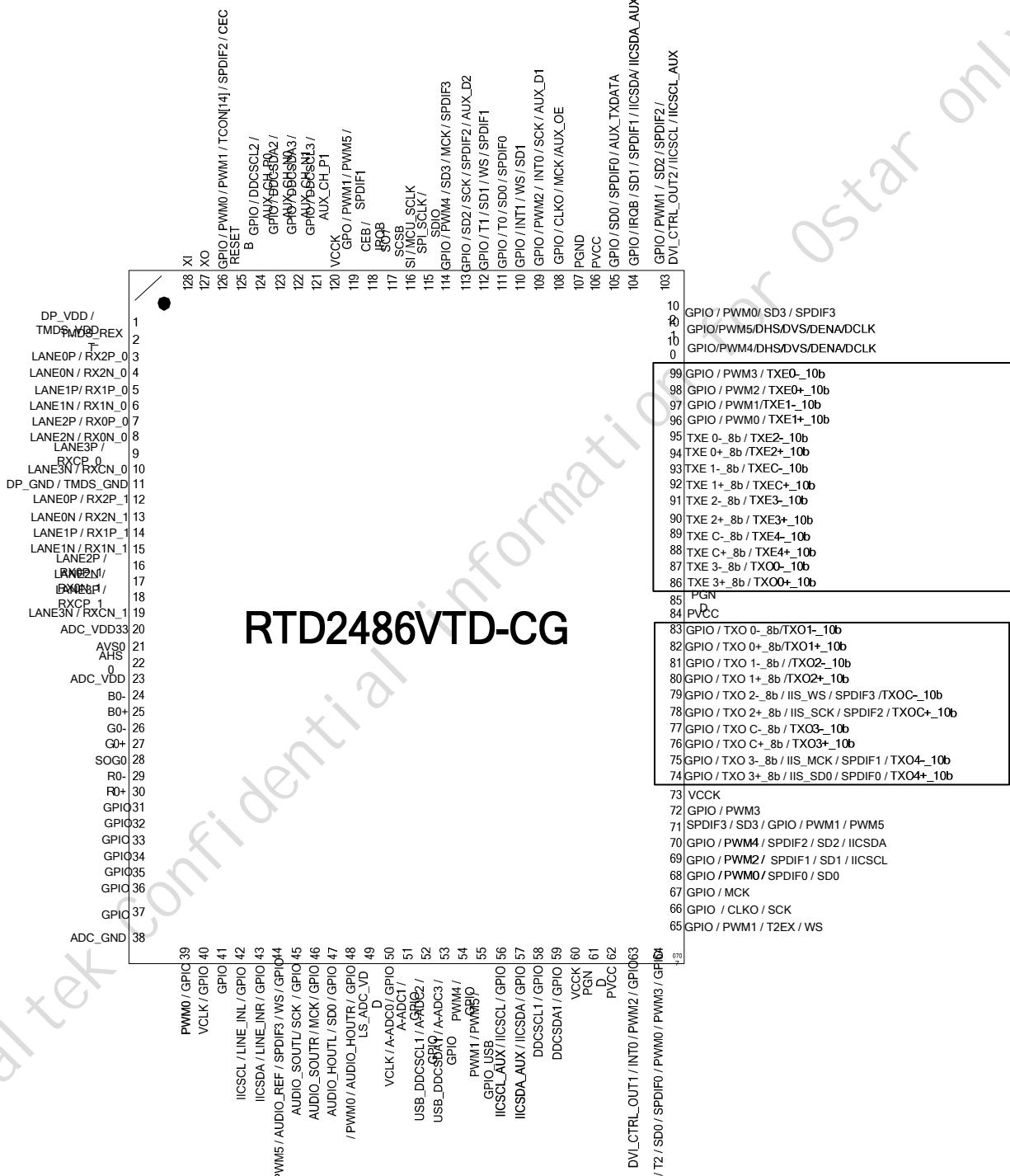


Figure1

4. Pin Diagram 128 Pin LQFP



RTD2486VTD-CG

(Pin 119 : Power on latch Pin)
 (when AC Power On , Power on latch pin must be “High”)

Table of Pin Assignment

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Name	I/O	Pin #	Description	Note
TMDS_VDD/DP_VDD	AP	1	TMDS power/Display Port Power	(3.3 V)
TMDS_REXT	AI	2	Impedance Match Reference Resistor For Scan mode,it should be pulled high Scan mode: SI[7:0] is assigned to {124~121,114~111} SO[7:0] is assigned to {110~108,105~101} SE is assigned to 100.	Ref value: 6.2 K ohm (Reference to VCC)
RX2P_0/LANE0P	AI	3	TMDS Differential signal Input/LANE0P	
RX2N_0/LANE0N	AI	4	TMDS Differential signal Input/LANE0N	
RX1P_0/LANE1P	AI	5	TMDS Differential signal Input/LANE1P	
RX1N_0/LANE1N	AI	6	TMDS Differential signal Input/LANE1N	
RX0P_0/LANE2P	AI	7	TMDS Differential signal Input/LANE2P	
RX0N_0/LANE2N	AI	8	TMDS Differential signal Input/LANE2N	
RXCP_0/LANE3P	AI	9	TMDS Differential signal Input/LANE3P	
RXCN_0/LANE3N	AI	10	TMDS Differential signal Input/LANE3N	
TMDS_GND/DP_GND	AG	11	TMDS ground/Display Port Ground	
RX2P_1/LANE0P	AI	12	TMDS Differential signal Input/LANE0P	
RX2N_1/LANE0N	AI	13	TMDS Differential signal Input/LANE0N	
RX1P_1/LANE1P	AI	14	TMDS Differential signal Input/LANE1P	
RX1N_1/LANE1N	AI	15	TMDS Differential signal Input/LANE1N	
RX0P_1/LANE2P	AI	16	TMDS Differential signal Input/LANE2P	
RX0N_1/LANE2N	AI	17	TMDS Differential signal Input/LANE2N	
RXCP_1/LANE3P	AI	18	TMDS Differential signal Input/LANE3P	
RXCN_1/LANE3N	AI	19	TMDS Differential signal Input/LANE3N	
ADC_VDD33	AP	20	ADC Power	(3.3 V)
AVS0	I	21	ADC vertical sync input	5V tolerance even when power-off
AHS0	I	22	ADC horizontal sync input AVS0 and AHS0 could be used to select one of three scan chain. AHS0/AVS0: 2'b00: {i_chain[2:0], mcu_chain[1:0], vbi_chain[2:0]} 2'b01: d_chain 2'b10: vdec_chain Other are reserved	5V tolerance even when power-off
ADC_VDD	AP	23	ADC Power	(1.2V)
B0-	AI	24	Negative BLUE analog input (Pb-)	
B0+	AI	25	Positive BLUE analog input (Pb+)	
G0-	AI	26	Negative GREEN analog input (Y-)	
G0+	AI	27	Positive GREEN analog input (Y+)	
SOG0	AI	28	Sync-On-Green	
R0-	AI	29	Negative RED analog input (Pr-)	
R0+	AI	30	Positive RED analog input (Pr+)	
GPIO/TCON[6]	IO	31	MCU GPIO/TCON	3.3V tolerance
GPIO/TCON[7]	IO	32	MCU GPIO/TCON	3.3V tolerance
GPIO/TCON[8]	IO	33	MCU GPIO/TCON	3.3V tolerance
GPIO/TCON[9]	IO	34	MCU GPIO/TCON	3.3V tolerance
GPIO/TCON[0]	IO	35	MCU GPIO/TCON	3.3V tolerance



GPIO/TCON[10]	IO	36	MCU GPIO/TCON	3.3V tolerance
GPIO/TCON[4]/FIELD/L_R	IO	37	MCU GPIO/TCON/Field signal/L_R signal	3.3V tolerance
ADC_GND	AG	38	ADC ground	
GPIO/PWM0/TCON[14]	IO	39	MCU GPIO/PWM /TCON	5V tolerance even when power-off
GPIO/VCLK	IO	40	MCU GPIO/VCLK	5V tolerance even when power-off
GPIO/TCON[5]	IO	41	MCU GPIO/TCON	5V tolerance even when power-off
GPIO/LINE_INL/IICSL/IICSL_AUX	IO	42	MCU GPIO/LINE-IN/IIC BUS/IIC over AUX	3.3 V tolerance
GPIO/LINE_INR/IICSDA/IICSDA_AUX	IO	43	MCU GPIO/LINE-IN/IIC BUS/IIC over AUX	3.3 V tolerance
GPIO/PWM5/WS/SPDIF3/AUDIO_REF	IO	44	MCU GPIO/PWM/IIS-WS/SPDIF3/Audio Reference Resistance	3.3 V tolerance
GPIO/SCK/AUDIO_SOUTL	IO	45	MCU GPIO/IIS-SCK/Speaker Output	3.3 V tolerance
GPIO/MCK/AUDIO_SO_UTR	IO	46	MCU GPIO/IIS-MCK/Speaker Output	3.3 V tolerance
GPIO/SD0/AUDIO_HOUTL	IO	47	MCU GPIO/IIS-SD0/ Audio Headphone Output	3.3 V tolerance
GPIO/PWM0/AUDIO_H_OUTR	IO	48	MCU GPIO/PWM/ Audio Headphone Output	3.3 V tolerance
LS_ADC_VDD	AP	49	Low Speed ADC POWER	(3.3V)
A-ADC0/GPIO/VCLK	IO	50	8-bit MCU ADC Input/MCU GPIO/VIDEO clock	5 V tolerance
A-ADC1/GPIO	IO	51	8-bit MCU ADC Input/MCU GPIO	5V tolerance
A-ADC2/GPIO/USB_DDCSCL1	IO	52	8-bit MCU ADC Input/MCU GPIO/USB_DDCSCL1 When (Page 10, 0xD6[0] = 1) && (pin55 = 1), disable DDC function of pin 58, 59 and swap to pin 52, 53	5V tolerance
ADC3/GPIO/USB_DDCSDA1	IO	53	8-bit MCU ADC Input/MCU GPIO/USB_DDCSDA1 When (Page 10, 0xD6[0] = 1) && (pin55 = 1), disable DDC function of pin 58, 59 and swap to pin 52, 53	5V tolerance
GPIO/PWM4	IO	54	MCU GPIO/PWM	5V tolerance even when power-off
GPIO_USB/PWM1/PWM5/TCON[0][5]	IO	55	MCU GPIO_USB Ctrl/PWM/TCON	5V tolerance even when power-off
GPIO/TCON[1][4]/IICSL /IICSL_AUX	IO	56	MCU GPIO/TCON/IIC BUS/IIC over AUX	5V tolerance even when power-off
GPIO/TCON[9][11]/IICSDA /IICSDA_AUX	IO	57	MCU GPIO/TCON/IIC BUS/IIC over AUX	5V tolerance even when power-off
DDCSCL1/GPIO/TCON[7][10]	IO	58	DDC1(Open drain I/O)/MCU GPIO/TCON	5V tolerance even when power-off
DDCSDA1/GPIO/TCON[3][5]	IO	59	DDC1(Open drain I/O)/MCU GPIO/TCON	5V tolerance even when power-off



VCCK	P	60	Digital Power	(1.2V)
PGND	G	61	Pad ground	
PVCC	P	62	Pad power	(3.3V)
GPIO/PWM2/ TCON[1][8][16]/ DVI_CTRL_OUT1	IO	63	MCU GPIO/PWM/TCON/ DVI Control Output	5V tolerance even when power-off
GPIO/PWM0/PWM3/ TCON[0][6][7][15]/SD0/ SPDIF0	IO	64	MCU GPIO/PWM/TCON/IIS-SD0/SPDIF0	5V tolerance even when power-off
GPIO/PWM1/ TCON[7][1]/WS	IO	65	MCU GPIO/PWM/TCON/IIS-WS	5V tolerance even when power-off
GPIO/TCON[2][4][16]/ SCK	IO	66	MCU GPIO/TCON/IIS-SCK	5V tolerance even when power-off
GPIO/TCON[5][9][12]/ MCK	IO	67	MCU GPIO/TCON/IIS-MCK	5V tolerance even when power-off
GPIO/PWM0/ TCON[14][15]/ SD0/SPDIF	IO	68	MCU GPIO/PWM/TCON/IIS-SD0/SPDIF0	5V tolerance even when power-off
GPIO/PWM2/ TCON[3][7]/SD1/ SPDIF1/IICSCL	IO	69	MCU GPIO/PWM/TCON/IIS-SD1/SPDIF1/ IIC BUS	5V tolerance even when power-off
GPIO/PWM4/ TCON[9][11]/SD2/ SPDIF2/IICSDA	IO	70	MCU GPIO/PWM/TCON/IIS-SD2/SPDIF2/ IIC BUS	5V tolerance even when power-off
GPIO/PWM1/PWM5/ TCON[8][10]/SD3/ SPDIF3	IO	71	MCU GPIO/PWM/TCON/IIS-SD3/SPDIF3	5V tolerance even when power-off
GPIO/PWM3/ TCON[6][12]	IO	72	MCU GPIO/PWM/TCON	5V tolerance even when power-off
VCCK	P	73	Digital Power	(1.2V)
TXO3+_8b(GPIO/IIS_SD 0/SPDIF0	IO	74	LVDS 8bit/MCU GPIO/IIS_SD0/SPDIF0/LVDS 10bit	3.3 V tolerance
TXO3-_8b(GPIO/IIS_MC K/SPDIF1	IO	75	LVDS 8bit/MCU GPIO/IIS_MCK/SPDIF1	3.3 V tolerance
TXOC+_8b(GPIO	IO	76	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXOC-_8b(GPIO	IO	77	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO2+_8b(GPIO/IIS_SC K/SPDIF2	IO	78	LVDS 8bit/MCU GPIO/IIS_SCK/SPDIF2	3.3 V tolerance
TXO2-_8b(GPIO/IIS_WS /SPDIF3	IO	79	LVDS 8bit/MCU GPIO/IIS_WS/SPDIF	3.3 V tolerance
TXO1+_8b(GPIO	IO	80	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO1-_8b(GPIO	IO	81	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0+_8b(GPIO	IO	82	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0-_8b(GPIO	IO	83	LVDS 8bit/MCU GPIO	3.3 V tolerance
PVCC	P	84	Pad power	3.3V
PGND	G	85	Pad ground	
TXE3+_8b	O	86	LVDS 8bit	3.3 V tolerance
TXE3-_8b	O	87	LVDS 8bit	3.3 V tolerance

Table of Pin Assignment



TXEC+_8b	O	88	LVDS 8bit	3.3 V tolerance
TXEC-_8b	O	89	LVDS 8bit	3.3 V tolerance
TXE2+_8b	O	90	LVDS 8bit	3.3 V tolerance
TXE2-_8b	O	91	LVDS 8bit	3.3 V tolerance
TXE1+_8b	O	92	LVDS 8bit	3.3 V tolerance
TXE1-_8b	O	93	LVDS 8bit	3.3 V tolerance
TXE0+_8b	O	94	LVDS 8bit	3.3 V tolerance
TXE0-_8b	O	95	LVDS 8bit	3.3 V tolerance
GPIO/PWM0	IO	96	MCU GPIO/PWM	3.3 V tolerance
GPIO/PWM1/TCON[S0]	IO	97	MCU GPIO/PWM/TCON	3.3 V tolerance
GPIO/PWM2/TCON[13][15]	IO	98	MCU GPIO/PWM/TCON	3.3 V tolerance
GPIO/PWM3/TCON[0][6][11]	IO	99	MCU GPIO/PWM/TCON	3.3 V tolerance
GPIO/PWM4/TCON[S1][3][12]/FIELD/DHS/DVS/DENA/DCLK/L_R	IO	100	MCU GPIO/PWM/TCON/Field signal/Display H-sync/Display V-sync/Data Enable/Display Clock/L_R signal	5V tolerance even when power-off
GPIO/PWM5/TCON[14]/FIELD/DHS/DVS/DENA/DCLK	IO	101	MCU GPIO/PWM/TCON/Field signal/Display H-sync/Display V-sync/Data Enable/Display Clock	5V tolerance even when power-off
GPIO/PWM0/TCON[10]/SD3/SPDIF3	IO	102	MCU GPIO/PWM/TCON/IIS-SD3/SPDIF3	5V tolerance even when power-off
GPIO/PWM1/TCON[8]/SD2/SPDIF2/DVI_CTRL_OUT2/IICSL/IICSL_AUX	IO	103	MCU GPIO/PWM/TCON/IIS-SD2/SPDIF2/DVI Control Output/IICSL/IIC over AUX	5V tolerance even when power-off (GPIO open-drain)
GPIO/TCON[5]/SD1/SPDIF1/IRQB/IICSDA/IICSDA_AUX	IO	104	MCU GPIO/TCON[5]/IIS-SD1/SPDIF1/IRQ Bar/IICSDA/IIC over AUX	5V tolerance even when power-off
GPIO/TCON[6][9]/SD0/SPDIF0/AUX_TXDATA	IO	105	MCU GPIO/TCON/IIS-SD0/SPDIF0/AUX_TXDATA	5V tolerance even when power-off
PVCC	P	106	Pad 3.3V power	3.3V
PGND	G	107	Pad 3.3V GND	
GPIO/TCON[7]/MCK/AUX_OE	IO	108	MCU GPIO/TCON/IIS-MCK/AUX_OE	5V tolerance even when power-off
GPIO/PWM2/TCON[3]/SCK/AUX_D1	IO	109	MCU GPIO/PWM/TCON/IIS-SCK/AUX_D1	5V tolerance even when power-off
GPIO/TCON[2][6][7]/WS/SD1	IO	110	MCU GPIO/TCON/IIS-WS/IIS-SD1	5V tolerance even when power-off
GPIO/TCON[4][7]/SD0/SPDIF0	IO	111	MCU GPIO/TCON/IIS-SD0/SPDIF0	5V tolerance even when power-off



GPIO/TCON[5][9]/SD1/ WS/SPDIF1	IO	112	MCU GPIO/TCON/IIS-SD1/IIS-WS/SPDIF1	5V tolerance even when power-off
GPIO/TCON[1][11]/SD2/ SCK/SPDIF2/AUX_D2	IO	113	MCU GPIO/TCON/IIS-SD2/IIS-SCK/SPDIF2/ AUX_D2	5V tolerance even when power-off
GPIO/PWM4/ TCON[0][13]/SD3/MCK/ SPDIF3	IO	114	MCU GPIO/PWM/TCON/IIS-SD3/IIS-MCK/ SPDIF3	5V tolerance even when power-off
SPI_SCLK/SDIO	IO	115	SPI flash serial clock /external MCU serial control I/F data in	3.3 V tolerance
SI/MCU_SCLK	IO	116	SPI flash serial data input /external MCU serial control I/F clock	3.3 V tolerance
SO/SCSB	IO	117	SPI flash serial data output /external MCU serial control I/F chip select	3.3 V tolerance
CEB/IRQB	IO	118	SPI flash chip enable bar/IRQ Bar Note:It should be pulled down to 0 v or pulled up to 3.3 v in order to designate the MCU type(Internal MCU(3.3 volts) or External MCU(0 volts)).	3.3 V tolerance
GPO/PWM1/PWM5/ SPDIF1	IO	119	MCU GPO/PWM/SPDIF1 (Power on latch Pin .) (when AC Power On , Power on latch Pin must be “High”)	5V tolerance even when power-off
VCCK	P	120	Digital 1.2V Power	1.2V
DDCSCL3/GPIO/ AUX_CH_P1	IO	121	DDC3(Open drain I/O)/MCU GPIO/ DP AUX_CH_P1	5V tolerance even when power-off
DDCSDA3/GPIO/ AUX_CH_N1	IO	122	DDC3(Open drain I/O)/MCU GPIO/ DP AUX_CH_N1	5V tolerance even when power-off
DDCSDA2/GPIO/ AUX_CH_N0	IO	123	DDC2(Open drain I/O)/MCU GPIO/ DP AUX_CH_N0	5V tolerance even when power-off
DDCSCL2/GPIO/ AUX_CH_P0	IO	124	DDC2(Open drain I/O)/MCU GPIO/ DP AUX_CH_P0	5V tolerance even when power-off (GPIO open-drain)
RESETB	I	125	Chip Reset Bar	Low active; 5V tolerance even when power-off
GPIO/PMW0/PWM1/ TCON[14]/SPDIF2/CEC	I/O	126	MCU GPIO/PWM/TCON/SPDIF2/CEC	5V tolerance
XO	AO	127	Crystal Output	
XI	AI	128	Crystal Input	

MCU GPIO Assignment

PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name
31	PD.7	70	P1.6	122	P7.2
32	PD.6	71	P1.7	123	P7.1
33	PD.5	72	PC.2	124	P7.0
34	PD.4	74	P9.0	126	PC.0
35	PD.3	75	P9.1		
36	PD.2	76	P9.2		
37	PD.1	77	P9.3		
39	PD.0	78	P9.4		
40	PC.4	79	PA.0		
41	PB.7	80	PA.1		
42	PB.6	81	PA.2		
43	PB.5	82	PA.3		
44	PB4	83	PA.4		
45	PB.3	94	P5.0 (removed)		
46	PB.2	95	P5.1 (removed)		
47	PB.1	96	P5.2		
48	PB.0	97	P5.3		
50	P6.0	98	P5.4		
51	P6.1	99	P5.5		
52	P6.2	100	P5.6		
53	P6.3	101	P5.7		
54	P6.4	102	P7.6		
55	P6.5	103	P7.5		
56	P6.6	104	P7.4		
57	P6.7	105	P8.0		
58	P3.0/RXD(I/O)	108	P8.1/CLKO1(O)		
59	P3.1/TXD(O)	109	P3.2/INT0(I)		
63	PC.3 /INT0(I)	110	P3.3/INT1(I)		
64	P1.0/T2(I) /INT1(I)	111	P3.4/T0		
65	P1.1/T2EX(I)	112	P3.5(BS)/T1		
66	P1.2/CLKO2(O)	113	P3.6		
67	P1.3	114	P3.7		
68	P1.4	119	PC.1		
69	P1.5	121	P7.3		

5. Register Description

Global Event Flag

Register::ID_Reg_01						0x00
Name	Bit	R/W	Default	Description	Config	
ID	7:0	R	0xF0	MSB 4 bits: 1111 product code LSB 4 bits: 0000 rev. code		

Register:: Host_ctrl						0x01
Name	Bit	R/W	Default	Description	Config.	
XTAL_PWDN	7	R/W	0	Power Gated XTAL (active high)		
Reset_chk	6	R/W	0	Reset Check Once scalar is reset, this value will be cleared to 0. The purpose of it is to check if LVR has been triggered. It should be written to 1 ahead, then read it. LVR has been triggered if the value is 0, else LVR has not.		
Rev	5:3	---	---	Reserved		
PD_EN	2	R/W	1	Power Down Mode Enable 0: Normal 1: Enable power down mode(Default) Turn off ADC RGB Channel/ ADC Band gap/ SOG/ DPLL/ LVDS/ ADC PLL/ SYNC PROC/ TMDS / HDMI Audio PLL/AUTO SOY ADC/m2pll Note: For LVDS Power Control, refer to following table. Turn off LVDS even port(as 0x8C-A0[5])/LVDS odd port(as 0x8C-A0[4])/APLL gbl pwdn sav/ ADC_GLPOW. Display Clock gated and Display timing disable(0x28[0]=0). Disable Xtal clock to APLL/DDS/ZCD(DAC)/OSD/adc auto_adj Disable Xtal clock to APLL/DDS/ZCD(DAC)/OSD/adc auto_adj HDMI/DP digital power down/OSD Clock EN/Sync_pro Xtal clock gated		
PS_EN	1	R/W	1	Power Saving Mode Enable 0: Normal 1: Enable power saving mode (Default) Turn off ADC RGB channel/ DPLL/ LVDS/ ADC PLL/ m2pll When power down or power saving function is enabled, internal meu clock is forced to crystal clock. Note: For LVDS Power Control, refer to following table. Turn off LVDS even port(as 0x8C-A0[5])/LVDS odd port(as 0x8C-A0[4])/APLL gbl pwdn sav/ ADC_GLPOW.		

				Display Clock gated and Display timing disable(0x28[0]=0). Disable Xtal clock to APLL/DDS/ZCD(DAC)/OSD/adc auto_adj Internal emcu clock can't from m2pll.	
Sft_Reset	0	R/W	0	Software Reset Whole Chip (Low pulse at least 8ms) 0: Normal (Default) 1: Reset All registers are reset to default except HOST_CTRL and power-on-latch.	

- Power Down/Power Saving control only effective when LVDS Display Output is double.

DISP_TYPE CR 8C-00[1:0]	DATA_TYPE CR 28[2]	Port	Power Control
LVDS [01]	Double [1]	LVDS Even	Power Down/Power Saving CR01 [2]/CR 01[1]
LVDS [01]	Double [1]		
LVDS [01]	Single [0]	LVDS Even	Power Up LVDS Even-Port CR8C-A0 [5]
LVDS [01]	Single [0]	LVDS Odd	Power Up LVDS Odd-Port CR8C-A0 [4]

Register:: STATUS0					0x02
Name	Bit	R/W	Default	Description	Config.
ADCPLL_nonlock	7	R	0	ADC_PLL Non-Lock If the ADC_PLL non-lock occurs, this bit is set to "1".	
IVS_error	6	R	0	Input VSYNC Error If the input vertical sync occurs within the programmed active period, this bit is set to "1".	
IHS_error	5	R	0	Input HSYNC Error If the input horizontal sync occurs within the programmed active period, this bit is set to "1".	
ODD_Occur	4	R	0	Input ODD Toggle Occur (For internal field odd toggle, refer to CR1A[5]) If the ODD signal (From SAV/EAV or V16_ODD) toggle occurs, this bit is set to "1".	
V8HV_Occur	3	R	0	Video8 Input Vertical/Horizontal Sync Occurs If the YUV input V or H sync edge occurs, this bit is set to "1".	
ADCHV_Occur	2	R	0	ADC Input Vertical/Horizontal Sync Occurs Input V or H sync edge occurs; this bit is set to "1".	
Buffer_Ovfl	1	R	0	Input Overflow Status (Frame Sync Mode) * ¹ If an overflow in the input data capture buffer occurs, this bit is set to "1".	
Buffer_Udf1	0	R	0	Line Buffer Underflow Status (Frame Sync Mode)	

*¹Only first event of input overflow/underflow is recorded if both of them occurs.

				If an underflow in the line-buffer occurs, this bit is set to “1”.	
--	--	--	--	--	--

Write to clear status.

Register:: STATUS1					0x03
Name	Bit	R/W	Default	Description	Config.
Buffer_Ovf2	7	R	0	Line Buffer Overflow Status 1: Line Buffer overflow has occurred since the last status cleared	
Buffer_Udf2	6	R	0	Line Buffer Underflow Status 1: Line Buffer underflow has occurred since the last status cleared	
DENA_Stop	5	R	0	DENA Stop Event Status 1: If the DENA stop event occurred since the last status cleared	
DENA_Start	4	R	0	DENA Start Event Status 1: If the DENA start event occurred since the last status cleared as an interrupt source	
DVS_Start	3	R	0	DVS Start Event Status 1: If the DVS start event occurred since the last status cleared	
IENA_Stop	2	R	0	IENA Stop Event Status 1: If the IENA stop event occurred since the last status cleared	
IENA_Start	1	R	0	IENA Start Event Status 1: If the IENA start event occurred since the last status cleared	
IVS_Start	0	R	0	IVS Start Event Status 1: If the IVS start event occurred since the last status cleared	

Write to clear status.

Register::IRQ_CTRL0					0x04
Name	Bit	R/W	Default	Description	Config.
IRQ_EN	7	R/W	0	Internal IRQ Enable: (Global) 0: Disable these interrupt. 1: Enable these interrupt.	
IRQ_ADCPLL	6	R/W	0	IRQ (ADC_PLL Non-Lock) 0: Disable the ADC_PLL non-lock error event as an interrupt source 1: Enable the ADC_PLL non-lock error event as an interrupt source	
IRQ_IHV	5	R/W	0	IRQ (Input VSYNC/HSYNC Error) (DEN across Vsync or Hsync) 0: Disable the Input VSYNC/HSYNC error event as an interrupt source 1: Enable the Input VSYNC/HSYNC error event as an interrupt source	
IRQ_ODD	4	R/W	0	IRQ (Input ODD Toggle Occur) (EAV/SAV from Video8) 0: Disable Input ODD toggle event as an interrupt source 1: Enable the Input ODD toggle event as an interrupt source	
IRQ_V8_HV	3	R/W	0	IRQ (Video8 Input Hsync/Vertical Sync Occurs) 0: Disable the Video8 Input Hsync or	

				Vsync event as an interrupt source 1: Enable the Video8 Input Hsync or Vsync event as an interrupt source	
IRQ_ADC_HV	2	R/W	0	IRQ (ADC Input Hsync/Vertical Sync Occurs) 0: Disable the ADC Input Hsync or Vsync event as an interrupt source 1: Enable the ADC Input Hsync or Vsync event as an interrupt source	
IRQ_Buffer	1	R/W	0	IRQ (Line Buffer Underflow/Overflow Status) 0: Disable the Line Buffer underflow/overflow event as an interrupt source 1: Enable the Line Buffer underflow/overflow event as an interrupt source	
IRQ_IENA	0	R/W	0	IRQ (Input ENA Start Event Occurred Status) 0: Disable IENA start as interrupt source 1: Enable IENA start as interrupt source	

Register:: HDMI_STATUS0 0x05					
Name	Bit	R/W	Default	Description	Config.
HDMI status 0	7:0	R	---	Reference to CRCB for HDMI Function (Page 2)(write 1 clear)	

Register:: HDMI_STATUS1 0x06					
Name	Bit	R/W	Default	Description	Config.
HDMI status 1	7:0	R	---	Reference to CRCC for HDMI Function (Page 2)(write 1 clear)	

Register:: New_added_status0 0x07					
Name	Bit	R/W	Default	Description	Config.
Wstate	7	R	---	Wait state status	
New_m_state	6	R	---	New mode state	
Change_m_happen	5	R	---	Change mode happen (it will not be triggered while VGIP active signal is low)	
Wstate_IRQ_en	4	R/W	0	IRQ enable of Wait state status 0:disable 1:enable	
New_m_state_IRQ_en	3	R/W	0	IRQ enable of New mode status 0:disable 1:enable	
Change_m_happen_IRQ_en	2	R/W	0	IRQ enable of change mode happen status 0:disable 1:enable	
DP_IRQ	1	R	--	Display port IRQ status	
HDMI_IRQ	0	R	---	HDMI port IRQ status(reference P2_CA-60[7])	

Register::: New_added_status1					0x08
Name	Bits	R/W	Default	Description	Config
IVS_IRQ_EN	7	R	0	IVS IRQ enable: 0:disable 1:enable	
IVS_IRQ	6	R/W	0	IVS IRQ flag(Write 1 clear)	
DVS_IRQ_EN	5	R	0	DVS IRQ enable 0:disable 1:enable	
DVS_IRQ	4	R/W	0	DVS IRQ flag(Write 1 clear)	
Frame_start_IRQ_EN	3	R	0	DEN start IRQ enable 0:disable 1:enable	
Frame_start_IRQ	2	R/W	0	DEN start flag(Write 1 clear)	
ihvs_timeout_IRQ_en	1	R/W	0	(Input HSYNC/VSYNC overflow or Input VSYNC Time-Out) detected IRQ enable 0: disable 1: enable	
ihvs_timeout_IRQ	0	R	0	(Input HSYNC/VSYNC overflow or Input VSYNC Time-Out) detected IRQ status	Wclr_out

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Power Control

Register:: Power_Ctrl0					0x09
Name	Bit	R/W	Default	Description	Config.
Powoff_EO	7	R	-	Top power off block power cut cell strong control signal flag. When all power cut strong control enable, the flag will be 0.	
Powoff_EWO	6	R	-	Top power off block power cut cell weak control signal flag. When all power cut weak control enable, the flag will be 0.	
Powoff_EI_FW	5	R/W	1	Top power off block power cut cell strong control enable by F/W. Not control power cut cell directly, decided by 0x0B[7]	
Powoff_EWI	4	R/W	1	Top power off block power cut cell weak control enable.	
Xtal clock select	3	R/W	0	X'tal clock select 0: external xtal 1: internal OSC	
Xtal power off	2	R/W	0	0: normal mode 1: disable xtal	
Top_Pwr_off_blk_iso_ctrl	1	R/W	0	Top power off block isolation control 0: normal mode 1: isolation mode	
Top_pwr_off_blk_soft_rst	0	R/W	0	0: normal 1: reset	

Register:: Power_Ctrl1					0x0A
Name	Bit	R/W	Default	Description	Config.
GDIoff_EO	7	R	-	GDI power off block power cut cell strong control signal flag. When all power cut strong control enable, the flag will be 0.	
GDIoff_EWO	6	R	-	GDI power off block power cut cell weak control signal flag. When all power cut weak control enable, the flag will be 0.	
GDIoff_EI_FW	5	R/W	1	GDI power off block power cut cell strong control enable by F/W. Not control power cut cell directly, decided by 0x0B[6]	
GDIoff_EWI	4	R/W	1	GDI power off block power cut cell weak control enable.	
Reserved	3	R/W	0	Reserved	
Analog_blk_pwr_off_ctrl	2	R/W	0	analog block power off control , LVDSPLL only 0: normal mode 1: isolation mode	
GDI_pwr_off_blk_iso_ctrl	1	R/W	0	GDI power off block isolation control 0: normal mode 1: isolation mode	
GDI_pwr_off_blk_soft_rst	0	R/W	0	GDI power off block soft reset 0: normal 1: reset	

Register:: Power_Ctrl2	0x0B
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Name	Bit	R/W	Default	Description	Config.
Powoff_EI_sel	7	R/W	0	Top power off block power cut cell strong control enable select 0: controlled by F/W 0x09[5] 1: controlled by power cut cell weak control flag, so the flow will be weak on -> strong on	
GDIoff_EI_sel	6	R/W	0	GDI power off block power cut cell strong control enable select 0: controlled by F/W 0x0A[5] 1: controlled by power cut cell weak control flag, so the flow will be weak on -> strong on	
AUX_PHY_PS_CLK_SEL	5:4	R/W	00	aux_phy_ps_top clock select 00: from EMB_OSC 01: from Xtal 10: from M2PLL/N 11: from M2PLL/N (Divider N is set in CR22[6:3], 1~15)	
reserved	3	R/W	0	Reserved	
ldo_on	2	R	--	1: LDO controlled by Page0, 0xDF, 0xE0 0: LDO is disabled in this chip	
sync_pro_sync_sel	1	R/W	0	Select Sync processor V-sync2/H-sync2 source 0: from PAD_AVSS1(pin40) / PAD_AHS1(pin39) 1: from d-domain DVS/DHS	
OSC_27M_EN	0	R/W	0	EMB_OSC 27MHz and 14.318MHz select 0: 14.318MHz 1: 27MHz	

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Watch Dog

Address: 0C WATCH_DOG_CTRL0			Default: 00h
Bit	Mode	Function	
7	R/W	Auto Switch When Input HSYNC/VSYNC Error 0: Disable (Default) 1: Enable (See CR02[6] and CR02[5])	
6	R/W	Auto Switch When Input HSYNC/VSYNC Timeout or Overflow 0: Disable (Default) 1: Enable (See CR52[4] and CR54[5:4])	
5	R/W	Auto Switch When Display VSYNC Timeout 0: Disable (Default) 1: Enable	
4	R/W	Auto Switch When ADC-PLL Unlock 0: Disable (Default) 1: Enable	
3	R/W	Auto Switch When Overflow or Underflow (for Frame-Sync Display) 0: Disable (Default) 1: Enable	
2	R/W	Watch-Dog Action if Event Happened (for Display Timing) 0: Disable (Default) 1: Free Run	
1	R/W	Watch-Dog Action if Event Happened (for Display Data) 0: Disable (Default) 1: Background (Turn off overlay function and switch to background display simultaneously)	
0	R	Display VSYNC Timeout Flag (for CR0C[5]) 0: DVS is present 1: DVS is timeout The line number of Display HS is equal to Display Vertical Total; this bit is set to "1". (Write to clear status).	

Address: 0D WATCH_DOG_CTRL1			Default: 00h
Bit	Mode	Function	
7	R/W	Auto Switch When Input HSYNC Changed 0: Disable (Default) 1: Enable (See CR58[3])	
6	R/W	Auto Switch When Input VSYNC Changed 0: Disable (Default) 1: Enable (See CR58[2])	
5	R/W	Wstate WD enable 0:Disable(Default) 1:enable	
4	R/W	New_m_state 0:Disable(Default) 1:enable	
3	R/W	Change_mode_happen 0:Disable(Default) 1:enable	
2	R/W	HDMI_WD for D-domain 0: disable(I-domain) 1: enable(D-domain)	
1	R/W	DP WD for D-domain 0: disable(I-domain) 1: enable(D-domain)	
0	R/W	Reserved to 0	

Register::bond_control					0x0E
Name	Bit	R/W	Default	Description	Config
Reserved	7:0	R/W	0x00	Reserved to 0	

Register::ID_Reg_02					0x0F
Name	Bit	R/W	Default	Description	Config
ID	7:0	R	0x10	MSB 4 bits: 0001 product code LSB 4 bits: 0000 rev. code	

Input Video Capture

Address: 10 VGIP_CTRL (Video Graphic Input Control Register) Default: 00h

Bit	Mode	Function																
7	R/W	8 bit Random Generator 0: Disable(Default) 1: Enable																
6	R/W	Input Test Mode: 0: Disable (Default) 1: Test data input will go through RGB channel, AVS=>IVS, AHS=>IHS, VCLK=>ICLK																
5	R/W	VGIP Double Buffer Ready 0: Not Ready to Apply 1: Ready to Apply When the list table of CR10[4] is set, then enable CR10[5] . Finally, hardware will auto load these values into VGIP double buffer registers as the trigger event happens and clear CR10[5] to 0.																
4	R/W	VGIP Double Buffer Mode Enable (Each register described below has its own double buffer) 0: Disable (Original- Write instantly by MCU write cycles) 1: Enable (Double Buffer Function Write Mode) <table border="1"> <thead> <tr> <th>Register</th> <th>Trigger Event</th> </tr> </thead> <tbody> <tr> <td>PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])</td> <td>Falling edge of Ivactive</td> </tr> <tr> <td>IPH_ACT_STA (CR14[2:0],CR15)</td> <td>Falling edge of Ivactive</td> </tr> <tr> <td>IPV_ACT_STA (CR18[2:0],CR19) IV_DV_LINES (CR40)</td> <td>Falling edge of Ivactive</td> </tr> <tr> <td>IVS_DELAY (for capture) (CR1C,CR1E[1])</td> <td>Falling edge of Ivactive</td> </tr> <tr> <td>IHS_DELAY (for capture) (CR1D, CR1E[0])</td> <td>Falling edge of Ivactive</td> </tr> <tr> <td></td> <td></td> </tr> <tr> <td></td> <td></td> </tr> </tbody> </table>	Register	Trigger Event	PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])	Falling edge of Ivactive	IPH_ACT_STA (CR14[2:0],CR15)	Falling edge of Ivactive	IPV_ACT_STA (CR18[2:0],CR19) IV_DV_LINES (CR40)	Falling edge of Ivactive	IVS_DELAY (for capture) (CR1C,CR1E[1])	Falling edge of Ivactive	IHS_DELAY (for capture) (CR1D, CR1E[0])	Falling edge of Ivactive				
Register	Trigger Event																	
PLLPHASE(CRB3,CRB4) Add 1-clk Delay to IHS Delay (CR12[4]) HSYNC Synchronize Edge (CR12[3])	Falling edge of Ivactive																	
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IVS_DELAY (for capture) (CR1C,CR1E[1])	Falling edge of Ivactive																	
IHS_DELAY (for capture) (CR1D, CR1E[0])	Falling edge of Ivactive																	
3:2	R/W	Input Pixel Format 00: Embedded ADC (ADC_HS)(Default) 01: Embedded TMDS 10: Reserved 11: Reserved																
1	R/W	Input Graphic/Video Mode 0: From analog input (input captured by ‘Input Capture Window’) (Default) 1: From digital input (captured start by ‘enable signal’, but still stored in ‘capture window size’)																
0	R/W	Input Sampling Run Enable 0: No data is transferred (Default) 1: Sampling input pixels																

Address: 11 VGIP_SIGINV (Input Control Signal Inverted Register) Default: 00h

Bit	Mode	Function
7	R/W	Safe Mode 0: Normal (Default) 1: Safe Mode Enable, mask 1 frame IVS of every 2 frame IVS, slow down input frame rate.
6	R/W	IVS Sync with IHS Control (Avoid VS bouncing) 0: Enable (Default) 1: Disable
5	R/W	HS Signal Inverted for Field Detection 0: Negative Edge (Default) 1: Positive Edge
4	R/W	Input Video ODD Signal Invert Enable 0: Not inverted (ODD = positive polarity) (Default) 1: Inverted (ODD = negative polarity)
3	R/W	Input VS Signal Polarity Inverted

		0: Not inverted (VS = positive polarity) (Default) 1: Inverted (VS = negative polarity)
2	R/W	Input HS Signal Polarity Inverted 0: Not inverted (HS = positive polarity) (Default) 1: Inverted (HS = negative polarity)
1	R/W	Input ENA Signal Polarity Inverted 0: Not inverted (input high active) (Default) 1: Inverted (while input low active)
0	R/W	Video Input Clock Polarity 0: Rising edge latched (Default) 1: Falling edge latched

Address: 12 VGIP_DELAY_CTRL Default: 00h

Bit	Mode	Function
7	R	6-Iclk-delay HS Level Latched by VS Rising Edge
6	R	HS Level Latched by VS Rising Edge
5	R	HS Level Latched by 6-Iclk-delay VS Rising Edge
4	R/W/D	Add One Clock Delay to IHS Delay 0: Disable (Default) 1: Enable
3	R/W/D	HSYNC Synchronize Edge 0: HSYNC is synchronized by the positive edge of the input clock 1: HSYNC is synchronized by the negative edge of the input clock (HSYNC source is selected by CR48[0] and then synchronized)
2	R/W	VSYNC Synchronize Edge 0: Latch VS by the negative edge of input HSYNC (Default) 1: Latch VS by the positive edge of input HSYNC
1:0	R/W	Video Input Clock Delay Control: 00: Normal (Default) 01: 1ns delay 10: 2ns delay 11: 3ns delay

Address: 13 VGIP_ODD_CTRL (Video Graphic Input ODD Control Register) Default: 00h

Bit	Mode	Function
7	R/W	ODD Inversion for ODD-Controlled-IVS-Delay 0: Not Invert (Default) 1: Invert
6	R/W	ODD-Controlled-IVS-Delay One-Line Enable 0: Disable (Default) 1: Enable (Both for Auto and Capture)
5	R/W	Safe Mode ODD Inversion 0: Not inverted (Default) 1: Inverted
4	R/W	Force ODD Toggle Enable (Without ODD/EVEN Toggle Select in Safe Mode) 0: Disable (Default) 1: Enable
3	R/W	422 to 444 Conversion by duplicate style 0: Disable (Default) 1: Enable
2	R/W	Decode Video8 when ADC or TMDS Active 0: Disable (Default) 1: Enable
1	R/W	EAV Error Correction Enable in Video-8 0: Disable 1: Enable
0	R/W	Internal ODD Signal Selection 0: ODD signal from EAV or SAV or HDMI (Default) 1: Internal Field Detection ODD signal by CR1A[5] (Also support under VGA, DVI input)

Input Frame Window

(All capture window setting unit is 1)

Address: 14 IPH_ACT_STA_H (Input Horizontal Active Start) Default: 00h

Bit	Mode	Function
7:4	R/W/D	Input Video Horizontal Active Width -- High Byte [11:8]
3:0	R/W/D	Input Video Horizontal Active Start -- High Byte [11:8]

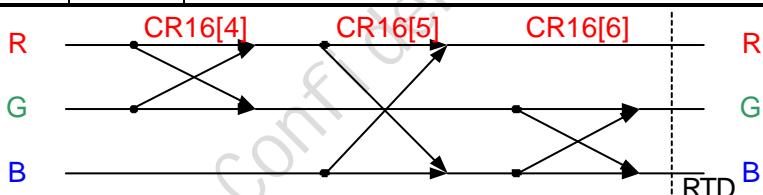
Address: 15 IPH_ACT_STA_L (Input Horizontal Active Start Low) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input Video Horizontal Active Start -- Low Byte [7:0]

- In analog mode, **IPH_ACT_STA** means the delay number of pixel clock from the leading edge of HS to the first pixel of each active line. Actual delay number of pixel clock = **IPH_ACT_STA(>=2) +2**,
- In digital mode, **IPH_ACT_STA** means the delay number of pixel clock from the leading edge of DE to the first pixel of each active line. Actual delay number of pixel clock = **IPH_ACT_STA(>=0)**

Address: 16 IPH_ACT_WID_H (Input Horizontal Active Width High) Default: 00h

Bit	Mode	Function
7	R/W	Test Data Input Latch Bus MSB to LSB Swap Control: 0: Normal (Default) 1: Swap Test Data MSB to LSB sequence into LSB to MSB
6	R/W	ADC Input G/B Swap 0: No Swap 1: Swap
5	R/W	ADC Input R/B Swap 0: No Swap 1: Swap
4	R/W	ADC Input R/G Swap 0: No Swap 1: Swap
3	R/W	Double Clock Input 0: Single Clock 1: Double Clock
2	R/W	Drop next frame when APLL double buffer is triggered 0: Disable(Default) 1: Enable You'd better wait for IVS before enable fast PLL mechanism And APLL setting if drop next frame.
1:0	R/W	Reserved



Address: 17 IPH_ACT_WID_L (Input Horizontal Active Width Low) Default: 00h

Bit	Mode	Function
7:0	R/W	Input Video Horizontal Active Width -- Low Byte [7:0]

This register defines the number of active pixel clocks to be captured.

Address: 18 IPV_ACT_STA_H (Input Vertical Active Start High) Default: 00h

Bit	Mode	Function
7:4	R/W	Input Video Vertical Active Lines – High Byte [11:8]
3:0	R/W/D	Input Video Vertical Active Start – High Byte [11:8]

Address: 19 IPV_ACT_STA_L (Input Vertical Active Start Low) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input Video Vertical Active Start – Low Byte [7:0]

The numbers of lines from the leading edge of selected input video VSYNC to the first line of the active window.
The value above should be larger than 1.

Address: 1A IPV_ACT_LEN_H (Input Vertical Active Lines) Default: 00h

Bit	Mode	Function
7	R	SAV/EAV 2-Bit Error Happened (Set if happened and write to clear)
6	R	SAV/EAV 1-Bit Error Happened (Set if happened and write to clear)
5	R	Internal Field Detection ODD Toggle Happened (Set if happened and write to clear) The function should be worked under no input clock
4:3	R	Number of Input HS between 2 Input VS (LSB bit [1:0])
2:0	R/W	Reserved

Address: 1B IPV_ACT_LEN_L (Input Vertical Active Lines) Default: 00h

Bit	Mode	Function
7:0	R/W	Input Video Vertical Active Lines – Low Byte [7:0]

This register defines the number of active lines to be captured.

Address: 1C IVS_DELAY (Internal Input-VS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input VSYNC Delay for Capture[7:0] (Counted by Input HSYNC) It's IVS delay for capture and digital filter, not for auto function

Address: 1D IHS_DELAY (Internal Input-HS Delay Control Register) Default: 00h

Bit	Mode	Function
7:0	R/W/D	Input HSYNC Delay for Capture [7:0] (Counted by Input Pixel Clock) It's IHS delay for capture and digital filter, not for auto function

Address: 1E VGIP_HV_DELAY Default: 00h

Bit	Mode	Function
7:6	R/W	Input HSYNC Delay for Auto Function (Counted by Input Pixel Clock) 00: No delay 01: 32 pixels 10: 64 pixels 11: 96 pixels
5:4	R/W	Input VSYNC Delay for Auto Function (Counted by Input HSYNC) 00: No delay 01: 3 line 10: 7 line 11: 15 line
3	R/W	Select DataEnable or HSync to adjust clock phase 0: use DataEnable to adjust clock phase (Default) 1: use HSync to adjust clock phase (while input source as ADC)
2	---	Reserved
1	R/W/D	Input VSYNC Delay for Capture[8] (Counted by Input HSYNC)
0	R/W/D	Input HSYNC Delay for Capture[8] (Counted by Input Pixel Clock)

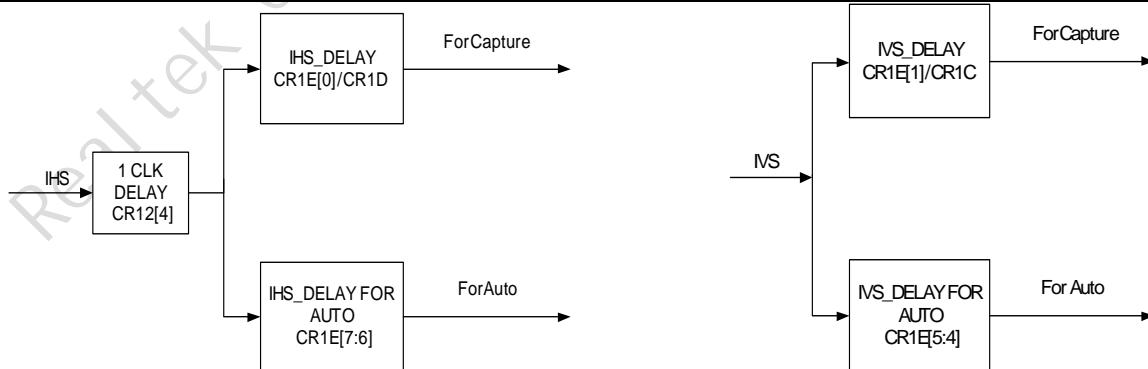


Figure 15: Input HSYNC/VSYNC Delay Path Diagram

Address: 1F V8 Source Select & YUV422 to YUV444Conversion Default: 00h

Bit	Mode	Function
7	R/W	Reorder the data flow 0: dfilter -> color_conversion -> dithering -> HSD (Default) 1: dfilter -> dithering -> color_conversion -> HSD
6	R/W	Test Data source select 0: From Pin 31~39 (excluding pin 38) 1: From Pin 41~48 Reserved
5:4	R/W	Reserved to 2'b10
3	R/W	Video 4:2:2->4:4:4 Enable before Scale-Down 0: Disable (Default) 1: Enable (This bit should be always enable when in HDMI YUV422 mode.)
2	R/W	Video 4:2:2->4:4:4 Mode Select 0: Interpolation (Default) 1: Duplicate (This bit would be work only while CR1F[3] is enable)
1	R/W	Output 444 Format (only work in Interpolation Mode) 0: $Y_0U_0V_0, Y_1\frac{(U_0+U_2)/2}{(V_0+V_2)/2}, Y_2U_2V_2, Y_3\frac{(U_2+U_4)/2}{(V_2+V_4)/2}...$ 1: $Y_0U_0V_1, Y_1\frac{(U_0+U_2)/2}{V_1}, Y_2U_2\frac{(V_1+V_3)/2}{(U_2+U_4)/2}V_3, Y_3\frac{(U_2+U_4)/2}{V_3}...$
0	R/W	UV Swap (for YUV422 to YUV444) (only work in Interpolation Mode) 0: Sequence 444 result: Y, U, V 1: Sequence 444 result: Y, V, U

Address: 20 V8CLK_SEL (v8clk selection setting) Default: 00h

Bit	Mode	Function
7	R/W	Reorder the color conversion flow 0: YUVtoRGB (default) 1: YUVtoRGB after DLTI/DCTI
6	R/W	Reserved
5:4	R/W	I-Domain clk divider: 00: div 2 (Default) 01: div 4 10: div 8 11: reserved
3	---	Reserved
2:0	R/W	I-Domain clk_phase: 000: phase 0 (Default) 001: phase 1 010: phase 2 (not work while div2) 011: phase 3 (not work while div2) 100: phase 4 (not work while div2 & div4) 101: phase 5 (not work while div2 & div4) 110: phase 6 (not work while div2 & div4) 111: phase 7 (not work while div2 & div4)

FIFO Frequency
Address: 22 FIFO Frequency Default: 50h

Bit	Mode	Function
7	R/W	Test Mode 0: Disable 1: Input data of VGIP Replaced by Background Color in CR6D
6:3	R/W	Divider of M2PLL Clock. Active when bit2 is set to 1. 0000 : Div = 2; 0001 : Div = 2; 0010 : Div = 2; 1010 : Div = 10; (Default) 1111 : Div = 15;
2	R/W	Internal Xtal Frequency 0: Fxtal 1: Fxtal * M2PLL_M / M2PLL_N / Div. (refer to bit6~3)
1:0	R/W	FIFO Frequency 00: MPLL 01: ICLK 10: DCLK 11: Test CLK

Scaling Down Control

Address: 23 SCALE_DOWN_CTRL (Scale Down Control Register)			Default:00h
Bit	Mode	Function	
7	R/W	Vertical scale down function mode selection: 0: Use line interpolation mode (Default) 1: Use drop line mode (Note: This bit is only valid while CR23[0]=1'b1.)	
6	R	Bist for Line Buffer one & two ok 0: Fail 1: Ok	
5	R/W	FIFO Line Buffer Bist Function Start (Auto clear to 0 when finish) 0: Finish 1: Start	
4	R/W	Reserved	
3	R/W	Horizontal non-linear scale down 0: Linear 1: Non-linear	
2	R/W	Vertical Scale-Down Compensation 0: Disable (Default) 1: Enable	
1	R/W	Horizontal scale down function enable: 0: Disable scale down function (Default) 1: Enable scale down function	
0	R/W	Vertical scale down function enable: 0: Disable scale down function (Default) 1: Enable scale down function (Note: There is a bit to select interpolation or dropping for vertical scale down at CR23[7].)	

Address: 24 Scale_Down_Access_Port Control			Default: 00h
Bit	Mode	Function	
7	R/W	Enable scale-down access port	
6:0	R/W	Scale-down port address	

Address: 25-00 V_SCALE_INIT		
Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Vertical Scale Down Initial Select [5:0]

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-01 V_SCALE_DH (Vertical scale down factor register)		
Bit	Mode	Function
7:3	R/W	Reserved
2:0	R/W	Vertical Scale Down Factor [18:16]

Address: 25-02 V_SCALE_DM (Vertical scale down factor register)		
Bit	Mode	Function
7:0	R/W	Vertical Scale Down Factor [15:8]

Address: 25-03 V_SCALE_DL (Vertical scale down factor register)		
Bit	Mode	Function
7:0	R/W	Vertical Scale Down Factor [7:0]

- Registers {V_SCALE_DH, V_SCALE_DM, V_SCALE_DL} = (Yi/Ym)*(2^17).
- The largest scale down ratio is 1/4 (integer part 2 bits)
- Meanwhile, Yi = vertical input length; Ym=vertical memory write length

Address: 25-04 H_SCALE_INIT		
Bit	Mode	Function
7:6	--	Reserved to 0

5:0	R/W	Horizontal Scale Down Initial Select [5:0] 1) Do Quincunx down sampling odd line 2) SBS Quincunx align part, depends on CR25-2E[4:3],[2:1] 3) SBS normal left half plane
-----	-----	--

- Scale Down Initial Point Select: for example, if the value is 43, we select the initial point is 43/64

Address: 25-05 H_SCALE_DH

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [23:16]

Address: 25-06 H_SCALE_DM

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [15:8]

Address: 25-07 H_SCALE_DL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Factor [7:0]

- For linear scale down, registers {H_SCALE_DH, HSCALE_DM, HSCALE_DL} = $(X_i/X_m) * (2^{20})$.
- Meanwhile, X_i = vertical input length; X_m =vertical memory write length

Address: 25-08 H_SCALE_ACCH

Bit	Mode	Function
7	--	Reserved
6:0	R/W	Horizontal Scale Down Accumulated Factor [14:8]

Address: 25-09 H_SCALE_ACCL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Accumulated Factor [7:0]

Address: 25-0A SD_ACC_WIDTHH

Bit	Mode	Function
7:2	--	Reserved
1:0	R/W	Horizontal Scale Down Accumulated Width [9:8]

Address: 25-0B SD_ACC_WIDTHL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Accumulated Width [7:0]

Address: 25-0C SD_FLAT_WIDTHH

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Horizontal Scale Down Flat Width [10:8]

Address: 25-0D SD_FLAT_WIDTHL

Bit	Mode	Function
7:0	R/W	Horizontal Scale Down Flat Width [7:0]

Address: 25-10 Input Pattern Generator Ctrl 0 Default: 8'h00

Bit	Mode	Function
7	R/W	Pattern reset to initial value 0 : 1 frame 1 : 16 frame
6	R/W	Random generator mode 0 : $x^9 + x^3 + 1$ 1 : $x^{29}+x^{6}+x^{4}+x+1$ (Green, Blue, Red)
5	R/W	Data update (RED) 0 : Reference data enable(pixel base) 1 : Reference horizontal data enable end(line base)

4	R/W	Data update (GREEN) 0 : Reference data enable 1 : Reference horizontal data enable end
3	R/W	Data update (BLUE) 0 : Reference data enable 1 : Reference horizontal data enable end
2	R/W	Pattern generator mode (RED) 0 : Random generator (ref. CR25-10[6] 1 : Pattern generator (reg. CR25-11[2]))
1	R/W	Pattern generator mode (GREEN) 0 : Random generator (ref. CR25-10[6]) 1 : Pattern generator (reg. CR25-11[1]))
0	R/W	Pattern generator mode (BLUE) 0 : Random generator (ref. CR25-10[6]) 1 : Pattern generator (reg. CR25-11[0]))

Address: 25-11 Input Pattern Generator Ctrl 1 Default: 8'h00

Bit	Mode	Function
7-3	R/W	Reserved to 0
2	R/W	Pattern generator (RED) 0 : Out(n) = Out(n-1) 1 : Out(n) = Out(n-1) + 1
1	R/W	Pattern generator (GREEN) 0 : Out(n) = Out(n-1) 1 : Out(n) = Out(n-1) + 1
0	R/W	Pattern generator (BLUE) 0 : Out(n) = Out(n-1) 1 : Out(n) = Out(n-1) + 1

Address: 25-12 Input Pattern Generator RED Initial Value Default: 8'h01

Bit	Mode	Function
7-0	R/W	RED Initial Value [7:0]

Address: 25-13 Input Pattern Generator GREEN Initial Value Default: 8'h01

Bit	Mode	Function
7-0	R/W	Green Initial Value [7:0]

Address: 25-14 Input Pattern Generator BLUE Initial Value Default: 8'h01

Bit	Mode	Function
7-0	R/W	BLUE Initial Value [7:0]

Address: 25-15 Input Pattern Generator RED/GREEN/BLUE Initial Value Default: 8'h00

Bit	Mode	Function
7-6	R/W	Reserved to 0
5-4	R/W	RED Initial Value [9:8]
3-2	R/W	GREEN Initial Value [9:8]
1-0	R/W	BLUE Initial Value [9:8]

Other Setting for Auto Function

Address: 25-1D HSYNC_SYNC_EDGE_CHANGED_PHASE_START Default: 00h

Bit	Mode	Function
7:6	R/W	Reserved to 0
5:0	R/W	Phase Start For The Range Of Hsync Sync Edge Changed

Address: 25-1E HSYNC_SYNC_EDGE_CHANGED_PHASE_END Default: 00h

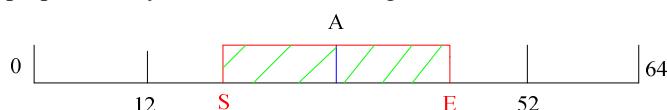
Bit	Mode	Function
7:6	R/W	Reserved to 0
5:0	R/W	Phase End For The Range Of Hsync Sync Edge Changed

Address: 25-1F HSYNC_SYNC_EDGE_CHANGED_CTRL Default: 00h



Bit	Mode	Function
7:2	R/W	Reserved to 0
1	R/W	HSYNC Synchronize Edge by input clock in Select Range 0: Negative(Default) 1: Positive When current phase is in range of start and end point, HSYNC is synchronized by selected edge, and synchronized by opposite edge for other range.
0	R/W	Auto Change Hsync Sync Edge Enable 0: Disable(Default) 1: Enable(Only effective when auto phase) Update the register HSYNC Synchronize Edge (CR12[3]) according to current phase before disable the function.

E.g. At phase A = 24 ($12 \leq A < 52$), where the leading edge of input clock and HSync superpose. It is recommend that we avoid the superposition by ± 12 (FW Define) range from A,



thus the start and end position should be assigned as blow,

$$S: CR25_1D[5:0] = A - 12 = 24 - 12 = 12$$

$$E: CR25_1E[5:0] = A + 12 = 24 + 12 = 36$$

$$CR25_1F[1] = 0$$

$$CR25_1F[0] = 1$$

E.g. At phase A = 4 ($0 \leq A < 12$),



the start and end position should be assigned as blow,

$$S: CR25_1D[5:0] = A + 12 = 4 + 12 = 16$$

$$E: CR25_1E[5:0] = 64 - 12 + A = 64 - 12 + 4 = 56$$

$$CR25_1F[1] = 1$$

$$CR25_1F[0] = 1$$

E.g. At phase A= 56 ($52 \leq A < 64$),



the start and end position should be assigned as blow,

$$S: CR25_1D[5:0] = A + 12 - 64 = 56 + 12 - 64 = 4$$

$$E: CR25_1E[5:0] = A - 12 = 56 - 12 = 44$$

$$CR25_1F[1] = 1$$

$$CR25_1F[0] = 1$$

Address: 25-32 SD_IN_WID_M

Bit	Mode	Function
7:4	--	reserved
3:0	R/W	Width before horizontal scale down[11:8]

Address: 25-33 SD_IN_WID_L

Bit	Mode	Function
7:0	R/W	Width before horizontal scale down[7:0]

Address: 25-34 SD_IN_LEN_M

Bit	Mode	Function
7:4	--	reserved
3:0	R/W	Length before vertical scale down[11:8]

Address: 25-35 SD_IN_LEN_L

Bit	Mode	Function
7:0	R/W	Length before vertical scale down[7:0]

Address: 25-36 SD_OUT_WID_M

Bit	Mode	Function
7:4	--	reserved
3:0	R/W	Width after horizontal scale down[11:8]

Address: 25-37 SD_OUT_WID_L

Bit	Mode	Function
7:0	R/W	Width after horizontal scale down[7:0]

Address: 25-38 SD_OUT_LEN_M

Bit	Mode	Function
7:4	--	reserved
3:0	R/W	Length after vertical scale down[11:8]

Address: 25-39 SD_OUT_LEN_L

Bit	Mode	Function
7:0	R/W	Length after vertical scale down[7:0]

Address: 26 V8 Source Select & YUV444 to YUV422 or YUV411 Conversion Default: 00h

Bit	Mode	Function
7	R/W	In I-domain, YUV 444 to 411 0: Disable(Default) 1: Enable
6	R/W	In I-domain, YUV 444 to 411 0: Drop Mode YoU0[7:4], Y1U0[3:0], Y2V2[7:4], Y3V2[3:0], ... 1: Average Mode Yo(Uavg0[7:4]), Y1(Uavg0[3:0]), Y2(Vavg0[7:4]), Y3(Vavg0[3:0]) Uavg0 = (U0+U1+U2+U3)/4, Uavg0 = (V0+V1+V2+V3)/4
5:4	R/W	Reserved
3	R/W	In I-domain, YUV 444 to 422 0: Disable(Default) 1: Enable
2	R/W	Reserved
1	R/W	In I-domain, YUV 444 to 422: 0: Drop C directly a. uv_mode = 0: Y ₀ U ₀ , Y ₁ V ₀ , Y ₂ U ₂ , Y ₃ V ₂ ... b. uv_mode = 1: Y ₀ U ₀ , Y ₁ V ₁ , Y ₂ U ₂ , Y ₃ V ₃ ... 1: Interpolation Mode a. uv_mode = 0: Y ₀ (U ₀ +U ₁)/2, Y ₁ (V ₀ +V ₁)/2, Y ₂ (U ₂ +U ₃)/2, Y ₃ (V ₂ +V ₃)/2... b. uv_mode = 1: Y ₀ (U ₀ +U ₁)/2, Y ₁ (V ₁ +V ₂)/2, Y ₂ (U ₂ +U ₃)/2, Y ₃ (V ₃ +V ₄)/2...
0	R/W	In I-domain, 444to422 U/V type 0: U0 V0 U2 V2 U4 V4 ... 1: U0 V1 U2 V3 U4 V5 ...

Address: 27 Reserved

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Display Format

Address: 28 VDIS_CTRL (Video Display Control Register) Default: 20h

Bit	Mode	Function
7	R/W	Force Display Timing Generator Enable: (Should be set when in Free-Run mode) 0: wait for input IVS trigger 1: force enable
6	R/W	Display Data Output Inverse Enable 0: Disable (Default) 1: Enable (only when data bus clamp to 0)
5	R/W	Display Output Force to Background Color 0: Display output operates normally 1: Display output is forced to the color as selected by background color (CR6D) (Default)
4	R/W	Display 18 bit RGB Mode Enable 0: All individual output pixels are full 24-bit RGB (Default) 1: All individual output pixels are truncated to 18-bit RGB (LSB 2 bits = 0)
3	R/W	Frame Sync Mode Enable 0: Free running mode (Default) 1: Frame sync mode
2	R/W	Display Output Double Port Enable 0: Single port output (Default) (Not effective if CR8C-A0[1]=1'b1) 1: Double port output
1	R/W	Display Output Run Enable 0: DHS, DVS, DEN & DATA bus are clamped to “0” (Default) 1: Display output normal operation.
0	R/W	Display Timing Run Enable 0: Display Timing Generator is halted, Zoom Filter halted (Default) 1: Display Timing Generator and Zoom Filter enabled to run normally

Steps to disable output: First set CR28[1]=0, set CR28[6], then set CR28[0]=0 to disable output.

Address: 29 VDISP_SIGINV (Display Control Signal Inverted) Default: 00h

Bit	Mode	Function
7	R/W	DHS Output Format Select (only available in Frame Sync) 0: The first DHS after DVS is active (Default) 1: The first DHS after DVS is inactive
6	R/W	Display Data Port Even/Odd Data Swap(Both for mLVDS/LVDS) 0: Disable (Default) 1: Enable
5	R/W	Display Data Port Red/Blue Data Swap(Both for mLVDS/LVDS) 0: Disable (Default) 1: Enable
4	R/W	Display Data Port MSB/LSB Data Swap(Both for mLVDS/LVDS) 0: Disable (Default) 1: Enable
3	R/W	Skew Display Data Output 0: Non-skew data output (Default) 1: Skew data output
2	R/W	Display Vertical Sync (DVS) Output Invert Enable: 0: Display Vertical Sync output normal active high logic (Default) 1: Display Vertical Sync output inverted logic
1	R/W	Display Horizontal Sync (DHS) Output Invert Enable: 0: Display Horizontal Sync output normal active high logic (Default) 1: Display Horizontal Sync output inverted logic
0	R/W	Display Data Enable (DEN) Output Invert Enable: 0: Display Data Enable output normal active high logic (Default) 1: Display Data Enable output inverted logic

Address: 2A DISP_ADDR (Display Format Address Port)

Bit	Mode	Function
7	R/W	Display Setting Double buffer enable

		0 : Disable 1 : Enable	
		Register	Trigger Event
		DH_TOTAL	DVS Rising
		ODD_FIXED_LAST EVEN_FIXED_LAST	DVS Rising
6	R/W	Display Double Buffer Ready 0: Not Ready to Apply 1: Ready to Apply When the list table of DISP_ADDR[7] is set, then enable DISP_ADDR[6], finally, hardware will auto load these value into RTD as the trigger event happens and clear DISP_ADDR[6] to 0.	
5:0	R/W	Display Format Address	

Address: 2B DISP_DATA (Display Format Data Port)

Bit	Mode	Function
7:0	R/W	Display Format Data

Address: 2B-00 DH_TOTAL_H (Display Horizontal Total Pixels)

Bit	Mode	Function
7	R/W	Series four line buffer
6:4	--	Reserved to 0
3:0	R/W	Display Horizontal Total Pixel Clocks: High Byte[11:8]

Address: 2B-01 DH_TOTAL_L (Display Horizontal Total Pixels)

Bit	Mode	Function
7:0	R/W	Display Horizontal Total Pixel Clocks: Low Byte[7:0]

Real DH_Total (Target value)= DH_Total (Register value)+ 4

Address: 2B-02 DH_HS_END (Display Horizontal Sync End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Sync End[7:0]: Determines the width of DHS pulse in DCLK cycles

Address: 2B-03 DH_BKGD_STA_H (Display Horizontal Background Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Background Start: High Byte [11:8]

Address: 2B-04 DH_BKGD_STA_L (Display Horizontal Background Start)

Bit	Mode	Function
7:0	R/W	Display Horizontal Background Start: Low Byte [7:0] (Minimum value of horizontal start is 0x0D)

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Background region.

Real DH_BKGD_STA (Target value)= DH_BKGD_STA (Register value)+ 10

Address: 2B-05 DH_ACT_STA_H (Display Horizontal Active Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Active Region Start: High Byte [11:8]

Address: 2B-06 DH_ACT_STA_L (Display Horizontal Active Start)

Bit	Mode	Function
7:0	R/W	Display Horizontal Active Region Start: Low Byte [7:0] (Minimum value of horizontal start is 0x0D)

Determines the number of DCLK cycles from leading edge of DHS to first pixel of Active region.

Real DH_ACT_STA (Target value)= DH_ACT_STA (Register value)+ 10

Address: 2B-07 DH_ACT_END_H (Display Horizontal Active End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Active End: High Byte [11:8]

Address: 2B-08 DH_ACT_END_L (Display Horizontal Active End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Active End: Low Byte [7:0]

Determines the number of DCLK cycles from leading edge of DHS to the pixel of background region.

Real DH_ACT_END (Target value) = DH_ACT_END (Register value) + 10

Address: 2B-09 DH_BKGD_END_H (Display Horizontal Background End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Horizontal Background end: High Byte [11:8]

Address: 2B-0A DH_BKGD_END_L (Display Horizontal Background End)

Bit	Mode	Function
7:0	R/W	Display Horizontal Background end: Low Byte [7:0]

Real DH_BKGD_END (Target value) = DH_BKGD_END (Register value) + 10

Address: 2B-0B DV_TOTAL_H (Display Vertical Total Lines)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Total: High Byte [11:8]

Address: 2B-0C DV_TOTAL_L (Display Vertical Total Lines)

Bit	Mode	Function
7:0	R/W	Display Vertical Total: Low Byte [7:0]

CR2B-0B, CR2B-0C are used as watch dog reference value in *frame sync* mode, the event should be the line number of display HS is equal to DV Total.

Address: 2B-0D DVS_END (Display Vertical Sync End)

Bit	Mode	Function
7:5	--	Reserved to 0
4:0	R/W	Display Vertical Sync End[4:0]: Determines the duration of DVS pulse in lines

Address: 2B-0E DV_BKGD_STA_H (Display Vertical Background Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Background Start: High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of background region.

Address: 2B-0F DV_BKGD_STA_L (Display Vertical Background Start)

Bit	Mode	Function
7:0	R/W	Display Vertical Background Start: Low Byte [7:0]

Address: 2B-10 DV_ACT_STA_H (Display Vertical Active Start)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Active Region Start: High Byte [11:8] Determines the number of lines from leading edge of DVS to first line of active region.

Address: 2B-11 DV_ACT_STA_L (Display Vertical Active Start)

Bit	Mode	Function
7:0	R/W	Display Vertical Active Region Start: Low Byte [7:0]

Address: 2B-12 DV_ACT_END_H (Display Vertical Active End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Active Region End: High Byte [11:8]

Address: 2B-13 DV_ACT_END_L (Display Vertical Active End)

Bit	Mode	Function
7:0	R/W	Display Vertical Active Region End: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of following background region.

Address: 2B-14 DV_BKGD_END_H (Display Vertical Background End)

Bit	Mode	Function
7:4	--	Reserved to 0
3:0	R/W	Display Vertical Background end: High Byte [11:8]

Address: 2B-15 DV_BKGD_END_L (Display Vertical Background End)

Bit	Mode	Function
7:0	R/W	Display Vertical Background End: Low Byte [7:0]

Determine the number of lines from leading edge of DVS to the line of start of vertical blanking.

Address: 2B-16~2B-1F Reserved

Display Fine Tune

Address: 2B-20 **DIS_TIMING** (Display Clock Fine Tuning Register) **Default:** 00h

Bit	Mode	Function
7	R/W	Reserved to 0
6:4	R/W	Display Output Clock Fine Tuning Control: 000: DCLK rising edge corresponds with output display data 001: 1ns delay 010: 2ns delay 011: 3ns delay 100: 4ns delay 101: 5ns delay 110: 6ns delay 111: 7ns delay
3	---	Reserved
2	---	Reserved
1	R/W	DCLK Output Enable 0: Disable 1: Enable
0	R/W	DCLK Polarity Inverted 0: Disable 1: Enable

Address: 2B-21 **OSD_REFERENCE_DEN** **Default:** 00h

Bit	Mode	Function
7:0	R/W	Position Of Reference DEN for OSD[7:0] When Page12 CRA0[7:6] = 11, this register can't be 0x00.

Address: 2B-22 **NEW_DV_CTRL** **Default:** 00h

Bit	Mode	Function
7	R/W	New Timing Enable 0: Disable 1: Enable
6	R/W	Line Compensation Enable 0: Disable 1: Enable
5	R/W	Pixel Compensation Enable 0: Disable 1: Enable
4	R/W	Reserve to 0
3:0	R/W	DCLK_Delay[11:8]

Address: 2B-23 **NEW_DV_DLY** **Default:** 00h

Bit	Mode	Function
7:0	R/W	DCLK_Delay[7:0]

When CR2B-22[7]=1, DCLK_Delay[11:0] can't be 0.

Address: 2B-24 **SSCG_NEW_Timing_Mode Setting** **Default:** 00h

Bit	Mode	Function
7	R/W	SSCG New Timing Mode Even/Odd last line setting iverse 0: no inverse 1: inverse
6	R/W	SSCG New Timing Mode Even/Odd last line setting enable 0: disable 1: enable
5:0	R/W	Reserve

Address: 2B-25 **MN_FRAME_RATE_EN** **Default:** 00h

Bit	Mode	Function
-----	------	----------

7	R/W	Enable MN rate frame sync (ivs:dvs = M:N) 0:disable 1:enable
6:0	R/W	reserved

Address: 2B-26 M_for_MN_FRAME_RATE **Default: 00h**

Bit	Mode	Function
7:0	R/W	ivs skipped , for MN frame sync[7:0] (M=register value +1)

Address: 2B-27 N_for_MN_FRAME_RATE **Default: 00h**

Bit	Mode	Function
7:0	R/W	dvs generated by free run , for MN frame sync[7:0] (N = register value +1)

Address: 2B-28 FREE_RUN_DVS_CNT **Default: 00h**

Bit	Mode	Function
7:0	R	Counter of free run DVS,for MN frame sync[7:0]

Address: 2B-28 FRAME_SYNC_DVS_FLAG **Default: 00h**

Bit	Mode	Function
7	R	Frame sync DVS IRQ flag(Write 1 clear)
6	R/W	Frame sync DVS IRQ Enable 0:disable 1:enable
5:0	---	Reserved

Address: 2B-30~2B-FF reserved

Cyclic-Redundant-Check
Address: 2C OP_CRC_CTRL (Output CRC Control Register)
Default: 00h

Bit	Mode	Function
7:6	R/W	CRC Selector 0x: CRC after scale-down (after FIFO) 10: CRC after all-processing 11: reserved When [8D,8E]0x07[5] = 1, CRC after scale-down is valid.
5:1	--	Reserved to 0
0	R/W	Output CRC Control: 0: Stop or finish (Default) 1: Start

CRC function = $X^{24} + X^7 + X^2 + X + 1$.
Address: 2D OP_CRC_CHECKSUM (Output CRC Checksum)

Bit	Mode	Function
7:0	R/W	1^{st} read=> Output CRC-24 bit 23~16 2^{nd} read=> Output CRC-24 bit 15~8 3^{rd} read=> Out put CRC-24 bit 7~0

- The read pointer should be reset when 1. OP_CRC_BYTEx is written
2. Output CRC Control starts.
- The read back CRC value address should be auto-increase, the sequence is shown above

FIFO Window

Address: 30 FIFO_WIN_ADDR (FIFO Window Address Port)

Bit	Mode	Function
7:5	--	Reserved to 0
4:0	R/W	FIFO Window Address Port

Address: 31 FIFO_WIN_DATA (FIFO Window Data Port)

Bit	Mode	Function
7:0	R/W	FIFO Window Data Port

- Port address will increase automatically after read/write.

Address: 31-00 DRL_H_BSU (Display Read High Byte Before Scaling-Up)

Default: 00h

Bit	Mode	Function
7:4	R/W	Display window read width before scaling up: High Byte [11:8]
3:0	R/W	Display window read length before scaling up: High Byte [11:8]

Address: 31-01 DRW_L_BSU (Display Read Width Low Byte Before Scaling-Up)

Default: 00h

Bit	Mode	Function
7:0	R/W	Display window read width before scaling up: Low Byte [7:0] the value must be even

Address: 31-02 DRL_L_BSU (Display Read Length Low Byte Before Scaling-Up)

Default: 00h

Bit	Mode	Function
7:0	R/W	Display window read length before scaling up: Low Byte [7:0]

- The setting above should be use 2 as unit
- The setting above should be use 2 as unit

Address: 31-03~31-FF reserved

Scaling Up Function

Address: 32 **SCALE_CTRL (Scale Control Register)**

Default: 00h

Bit	Mode	Function
7	R/W	Video mode compensation: 0: Disable (Default) 1: Enable
6	R/W	Internal ODD-signal inverse for video-compensation 0: No invert (Default) 1: invert
5	R	Display Line Buffer Ready 0: Busy 1: Ready
4	R/W	Enable Full Line buffer: 0: Disable (Default) 1: Enable
3	R/W	Vertical Line Duplication 0: Disable 1: Enable
2	R/W	Horizontal pixel Duplication 0: Disable 1: Enable
1	R/W	Enable the Vertical Filter Function: 0: By pass the vertical filter function block (Default) 1: Enable the vertical filter function block
0	R/W	Enable the Horizontal Filter Function: 0: By pass the horizontal filter function block (Default) 1: Enable the horizontal filter function block

- When using H/V duplication mode, FIFO window width set original width, but FIFO window height should be 2X the original height.

Address: 33 **SF_ACCESS_Port**

Default: 00h

Bit	Mode	Function
7	R/W	Enable scaling-factor access port
6	R/W	Merge two line buffer to 1 line buffer when scale up (for resolution over line buffer size)
5	R/W	I domain Share display line buffer when vertical scale down
4:0	R/W	Scaling factor port address (Active when bit7 = 1)

- When disable scaling factor access port, the access port pointer will reset to 0

Address: 34-00 **HOR_SCA_H (Horizontal Scale Factor High)**

Bit	Mode	Function
7	R/W	Display line buffer number shared with i_domain (active when 0x33[5]=1) 0 : 1 line (default) 1 : 2 line
6	R/W	Use 3 line buffer for 2D scale up
5:4	--	Reserved to 0
3:0	R/W	Bit [19:16] of horizontal scale factor

Address: 34-01 **HOR_SCA_M (Horizontal Scale Factor Medium)**

Bit	Mode	Function

7:0	R/W	Bit [15:8] of horizontal scale factor
-----	-----	--

Address: 34-02 HOR_SCA_L (Horizontal Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [7:0] of horizontal scale factor

Address: 34-03 VER_SCA_H (Vertical Scale Factor High)

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Bit [19:16] of vertical scale factor

Address: 34-04 VER_SCA_M (Vertical Scale Factor Medium)

Bit	Mode	Function
7:0	R/W	Bit [15:8] of vertical scale factor

Address: 34-05 VER_SCA_L (Vertical Scale Factor Low)

Bit	Mode	Function
7:0	R/W	Bit [7:0] of vertical scale factor

This scale-up factor includes a 20-bit fraction part to present a vertical scaled up size over the stream input. For example, for 600-line original picture scaled up to 768-line, the factor should be as follows:
 $(600/768) \times 2^{20} = 0.78125 \times 2^{20} = 819200 = C8000h = 0Ch, 80h, 00h.$

Address: 34-06 Horizontal Scale Factor Segment 1 Pixel **Default: 00h**

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Bit [10:8] of Scaling Factor Segment 1 pixel

Address: 34-07 Horizontal Scale Factor Segment 1 Pixel **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 1 pixel

Address: 34-08 Horizontal Scale Factor Segment 2 Pixel **Default: 00h**

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Bit [10:8] of Scaling Factor Segment 2 pixel

Address: 34-09 Horizontal Scale Factor Segment 2 Pixel **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 2 pixel

Address: 34-0A Horizontal Scale Factor Segment 3 Pixel **Default: 00h**

Bit	Mode	Function
7:3	--	Reserved
2:0	R/W	Bit [10:8] of Scaling Factor Segment 3 pixel

Address: 34-0B Horizontal Scale Factor Segment 3 Pixel **Default: 00h**

Bit	Mode	Function
7:0	R/W	Bit [7:0] of Scaling Factor Segment 3 pixel

Address: 34-0C Horizontal Scale Factor Delta 1		Default: 00h
Bit	Mode	Function
7:5	--	Reserved

4:0 R/W Bit [12:8] of Horizontal Scale Factor delta 1

Address: 34-0D Horizontal Scale Factor Delta 1		Default: 00h
Bit	Mode	Function
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 1

Address: 34-0E Horizontal Scale Factor Delta 2		Default: 00h
Bit	Mode	Function
7:5	--	Reserved

4:0 R/W Bit [12:8] of Horizontal Scale Factor delta 2

Address: 34-0F Horizontal Scale Factor Delta 2		Default: 00h
Bit	Mode	Function
7:0	R/W	Bit [7:0] of Horizontal Scale Factor delta 2

Address: 34-10 Horizontal Filter Coefficient Initial Value		Default: C4h
Bit	Mode	Function
7:0	R/W	Accumulate Horizontal filter coefficient initial value Applied to all lines when by_line_scale_up is disabled (0x35[3]=0) Only for even-line when by_line_scale_up is disabled (0x35[3]=1)

*even-line: flag in switch type is 0.

Address: 34-11 Vertical Filter Coefficient Initial Value		Default: C4h
Bit	Mode	Function
7:0	R/W	Accumulate Vertical filter coefficient initial value

Address: 34-12 Horizontal Filter Coefficient Initial Value for odd line		Default: C4h
Bit	Mode	Function
7:0	R/W	Accumulate Horizontal filter coefficient initial value Only for odd-line when by_line_scale_up is enabled (0x35[3]=1)

*odd-line: flag in switch type is 1.

Address: 34-13 Horizontal Filter Coefficient Initial Value control		Default: 00h
Bit	Mode	Function
7	R/W	Internal odd-signal for by_line_scale_up inverse by frame 0: No invert(default) 1: invert (If Switch type of L frame is 010101, then R frame turn to 101010)
6:0	R/W	Reserved to 0

Address: 35 FILTER_CTRL (Filter Control Register)		Default: 00h
Bit	Mode	Function
7	R/W	Enable Filter Coefficient Access 0: Disable (Default) 1: Enable

6	R/W	Select H/V User Defined Filter Coefficient Table for Access Channel 0: 1 st coefficient table (Default) 1: 2 nd coefficient table 2D Scale Up: 1st coefficient table: H/V 128-taps filter coefficient 3 line Scale Up: 1st coefficient table: 128-taps filter coefficient 2nd coefficient table: 96-taps filter coefficient
5	R/W	Select Horizontal user defined filter coefficient table 0: 1 st Horizontal Coefficient Table (Default) 1: 2 nd Horizontal Coefficient Table 2D Scale Up: Select 1st Coefficient Table 3 line Scale Up: Select 1st Coefficient Table
4	R/W	Select Vertical user defined filter coefficient table 0: 1st Vertical Coefficient Table (Default) 1: 2 nd Vertical Coefficient Table 2D Scale Up: Select 1st Coefficient Table 3 line Scale Up: Select 2nd Coefficient Table
3:0	R/W	Reserved

- The User Defined Filter Coefficient Table can't be modified on-line. Only the non-active coefficient-table can be modified, and then switch it to active.

Address: 36 FILTER_PORT (User Defined Filter Access Port) Default: 00h

Bit	Mode	Function
7:0	W	Access port for user defined filter coefficient table

- When enable filter coefficient accessing, the first write byte is stored into the LSB(bit[7:0]) of coefficient #1 and the second byte is into MSB (bit[8:11]). Therefore, the valid write sequence for this table is c0-LSB, c0-MSB, c1-LSB, c1-MSB, c2-LSB, c2-MSB ... c63-LSB & c63-MSB, totally 64 * 2 cycles. Since the 128 taps is symmetric, we need to fill the 64-coefficient sequence into table only.

Address: 37 SCALE_UP_FOR_LINE_INTERLEAVE Default: 00h

Bit	Mode	Function
7:3	R/W	Reserved
2	R/W	Vertical Scale up for line interleave 0: Disable 1: Enable Normal: wait for DVS trigger If this bit is enabled, then VPK, VCTI should be disabled.
1	R/W	Vertical Scale up for line interleave 0: 3 line scale up (default) 1: 2 line scale up 3line scale up: 96-taps filter coefficient, for 4 th line (0x36) should be zero 2line scale up: 128-taps filter coefficient Normal: wait for DVS trigger
0	R/W	Enable Line switch when line interleave 0: Disable 1: Enable wait for DVS trigger

Address: 38~3C Reserved

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Frame Sync Fine Tune

Address: 3D IV_DV_DELAY_CLK_FINE

Default: 00h

Bit	Mode	Function
7:4	R/W	IV_DV_DELAY_CLK_ODD_addition[3:0], step is one pixel Applied to all fields when Interlaced_FS_Delay_Fine_Tuning is disabled (CR43[1] = 0) Only for odd-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1) Should be double buffer by CR10[5:4]
3:0	R/W	IV_DV_DELAY_CLK_EVEN_addition[3:0], step is one pixel Only for even-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1) Should be double buffer by CR10[5:4]

Address: 3E IVS2DVS_DEALY_LINES_H (IVS to DVS Lines)

Default: 00h

Bit	Mode	Function
7:4	R/W	reserved
3:0	R/W	IVS to DVS Lines, high byte [11:8]: (Only for FrameSync Mode) The number of input HS from IVS to DVS. Should be double buffer by CR10[5:4]

Address: 40 IVS2DVS_DEALY_LINES (IVS to DVS Lines)

Default: 00h

Bit	Mode	Function

7:0	R/W	IVS to DVS Lines: (Only for FrameSync Mode) The number of input HS from IVS to DVS. Should be double buffer by CR10[5:4]
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Address: 41 IV_DV_DELAY_CLK_ODD (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function
7:0	R/W	Frame Sync Mode Delay Fine Tune [7:0] Applied to all fields when Interlaced_FS_Delay_Fine_Tuning is disabled (CR43[1] = 0) Only for odd-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1) Should be double buffer by CR10[5:4]

In Frame Sync Mode , CR41[7:0] represents output VS delay fine-tuning. It delays the number of (CR41 [7:0] *16 + 16) input clocks if CR41[7:0] is not equal to 0. (No delay fine-tune if CR41[7:0] = 0)

Address: 42 IV_DV_DELAY_CLK_EVEN (Frame Sync Delay Fine Tuning) Default: 00h

Bit	Mode	Function
7:0	R/W	Frame Sync Mode Delay Fine Tune [7:0] “00” to disable Only for even-field when Interlaced_FS_Delay_Fine_Tuning is enabled (CR43[1] = 1) Should be double buffer by CR10[5:4]

Address: 43 FS_DELAY_FINE_TUNING Default: 00h

Bit	Mode	Function
7	R/W	Enable measure last line by field 0 : disable 1: enable
6	R/W	Reference field in last line measure 0 : Odd 1 : Even
5:2	R/W	Reserved to 0
1	R/W	Interlaced_FS_Delay_Fine_Tuning 0: Disable (Default) 1: Enable
0	R/W	Internal ODD-signal inverse for Interlaced_FS_Delay_Fine_Tuning 0: No invert (Default) 1: Invert

Address: 44 LAST_LINE_H Default: 00h

Bit	Mode	Function
7	R/W	Last-line-width / DV-Total Selector : 0: CR44 [3:0] and CR45 indicate last-line width counted by display clock (Default) 1: CR44 [3:0] and CR45 indicate DHS total number between 2 DVS.
6	R/W	DV sync with 4X clock 0: Disable 1: Enable
5	R/W	BIST Test Enable 0: Disable 1: Enable (Auto clear when finish)
4	R/W	BIST Test Result 0: Fail 1: Ok
3:0	R	DV Total or Last Line Width[11:8] Before Sync in Frame Sync Mode

Address: 45 LAST_LINE_L

Bit	Mode	Function
7:0	R	DV Total or Last Line Width[7:0] Before Sync in Frame Sync Mode

Address: 46 Reserved as page selector for new sync-processor feature

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Sync Processor

Address: 47 SYNC_SELECT Default: 00h

Bit	Mode	Function
7	R/W	On line Sync Processor Power Down (Stop Crystal Clock In) 0: Normal Run (Default) 1: Power Down
6	R/W	Hsync Type Detection Auto Run 0: manual (Default) 1: automatic
5	R/W	De-composite circuit enable 0: Disable (Default) 1: Enable
4	R/W	Input Sync. Source selection 0: HS_RAW(SS/CS) (Default) 1: SOG/SOY
3	R/W	SOG Source Selection 0: SOG0/SOY0 (Default) 1: SOG1/SOY1 (Useless)
2	R/W	VGA-ADC HS/VS Source 0: 1 ST HS/VS (Default) (Original HS/VS of ADC source) 1: 2 ND HS/VS (HS/VS from D domain)
1	R/W	Measured by Crystal Clock (Result shown in CR59) (in Digital Mode) 0: Input Active Region (Vertical IDEN start to IDEN stop) (Result pop up at IDEN STOP) (Default) 1: Display Active Region(Vertical DEN start to DEN stop) (Result pop up at DEN STOP) The function should work correctly when IVS or DVS occurs and enable by CR50[4].
0	R/W	Hsync & Vsync Measured Mode 0: HS period counted by crystal clock & VS period counted by HS (Analog mode) (Default) 1: H resolution counted by input clock & V resolution counted by ENA (Digital mode) (Get the correct resolution which is triggered by enable signal, ENA)

Address: 48 SYNC_INVERT Default: 00h

Bit	Mode	Function
7	R/W	COAST Signal Invert Enable: 0: Not inverted (Default) 1: Inverted
6	R/W	COAST Signal Output Enable: 0: Disable (Default) 1: Enable
5	R/W	HS_OUT Signal Invert Enable: 0: Not inverted (Default) 1: Inverted
4	R/W	HS_OUT Signal Output Enable: 0: Disable (Default) 1: Enable
3	R/W	CS_RAW Inverted Enable 0: Normal (Default) 1: Invert
2	R/W	CLAMP Signal Output Enable 0: Disable (Default) 1: Enable
1	R/W	HS Recovery in Coast 0: Disable (Default) (SS/SOY) 1: Enable (CS or SOG)
0	R/W	Hsync Synchronize source 0: AHS (Default) 1: Feedback HS

Address: 49 SYNC_CTRL (SYNC Control Register) Default: 00h

Bit	Mode	Function
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7	R/W	CLK Inversion to latch Feedback HS for Coast Recovery (Coast Recovery means HS feedback to replace input HS) 0: Non Inversion (Default) 1: Inversion
6	R/W	Select HS_OUT Source Signal 0: Bypass (SeHs)(Use in Separate Mode) 1: Select De-Composite HS out(DeHs) (In Composite mode)
5	R/W	Select ADC_VS Source Signal (Auto switch in Auto Run Mode) 0: VS_RAW 1: DeVs
4	R/W	CLK Inversion to latch ADC HS for Clamp 0: Non Inversion (Default) 1: Inversion
3	R/W	Inversion of HSYNC to measure VSYNC 0: Non Inversion (Default) 1: Inversion
2	R/W	HSYNC Measure Source(ADC_HS1) 0: Select ADC_HS(Default) 1: Select SeHS or DeHS by CR49[6]
1:0	R/W	Measure HSYNC/VSYNC Source Select: 00: TMDS (Default) 01: VIDEO8 10: ADC_HS1/ADC_VS 11: CS_RAW/VS_RAW

Address: 4A STABLE_HIGH_PERIOD_H Default: 00h

Bit	Mode	Function
7	R	Even/Odd Field of Measure Input Source (Reference CR49[1:0])(By Line-Count Mode) 0: Even 1: Odd
6	R	The Toggling of Polarity of Measure Input Source (Reference CR49[1:0]) Field Happened (By Line-Count Mode) 0: No toggle 1: Toggle
5	R	Even/Odd Field of Measure Input Source (Reference CR49[1:0]) (By VS-Position Mode) 0: Even 1: Odd
4	R	The Toggling of Polarity of Measure Input Source (Reference CR49[1:0]) Field Happened (By VS-Position Mode) 0: No toggle 1: Toggle
3	R/W	Odd Detection Mode 0: Line-Count Mode (Default) 1: VS-Position Mode
2:0	R	Stable High Period[10:8] Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4B STABLE_HIGH_PERIOD_L

Bit	Mode	Function
7:0	R	Stable High Period[7:0] Compare each line's high pulse period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 4C VSYNC_COUNTER_LEVEL_MSB Default: 03h

Bit	Mode	Function
7	R	HSYNC Type Detection Auto Run Result ready
6:4	R	HSYNC Type Detection Auto Run Result 000: No Signal 001: Not Support

		010: YPbPr 011: Serration Composite SYNC 100: XOR/OR-Type Composite SYNC with Equalizer 101: XOR/OR-Type Composite SYNC without Equalizer 110: HSYNC with VS_RAW (Separate HSYNC) 111: HSYNC without VS_RAW (HSYNC only) Reference when Hsync type detection auto run result ready (CR4C[7])
3	R/W	Syncprocess Clock Select 0: Fxtal (Default) 1: Fxtal * M2PLL_M / M2PLL_N / Div. (refer to CR5D-0A[7:4])
2:0	R/W	VSYNC counter level count [10:8] MSB VSYNC detection counter start value.

Address: 4D VSYNC_COUNTER_LEVEL_LSB Default: 00h		
Bit	Mode	Function
7:0	R/W	VSYNC counter level count [7:0] LSB

Address: 4E HSYNC_TYPE_DETECTION_FLAG		
Bit	Mode	Function
7	R	HSYNC Overflow (16-bits)
6	R	Stable Period Change (write clear when CR4E[6]=1 or CR4F[0]=1)
5	R	Stable Polarity Change (write clear when CR4E[5]=1 or CR4F[0]=1)
4	R	VS_RAW Edge Occurs (write clear when CR4E[4]=1 or CR4F[0]=1) If VS_RAW edge occurs, this bit is set to "1".
3	R	Detect Capture Window Unlock Repeated 32 Times (write clear when CR4E[3]=1 or CR4F[0]=1)
2	R	HSYNC with Equalization (write clear when CR4E[2]=1 or CR4F[0]=1)
1	R	HSYNC Polarity Change (write clear when CR4E[1]=1 or CR4F[0]=1)
0	R	Detect Capture Window Unlock (write clear when CR4E[0]=1 or CR4F[0]=1)

Address: 4F STABLE_MEASURE Default: 00h		
Bit	Mode	Function
7	R	Stable Flag 0: Period or polarity can't get continuous stable status. 1: Both polarity and period are stable.
6	R	Stable Polarity 0: Negative 1: Positive Compare each line's polarity; if we get continuous > 64 lines with the same one, the polarity is updated as the stable polarity.
5:4	R/W	Feedback HSYNC High Period Select by ADC Clock: 00: 32 (Default) 01: 64 10: 96 11: 128
3	R/W	Stable Period Tolerance 0: ±2 crystal clks (Default) 1: ±4 crystal clks
2	R/W	VSYNC measure invert Enable 0: Disable (Default) 1: Enable
1	R/W	Pop Up Stable Value 0: No Pop Up (Default) 1: Pop Up Result, (CR4A[2:0], CR4B[7:0], CR4F[6], CR50[2:0], CR51[7:0])
0	R/W	Stable Measure Start 0 : Stop (Default) 1 : Start

Address: 50 Stable_Period_H Default: 00h		
Bit	Mode	Function

7	R	Measure One Frame Status 0: Auto clear to 0 after measure finished in one frame (Both H/V measure and active region measure finished in one frame whenever on-line measure (CR52[7]) opened or not. 1: Measuring Now
6	R	CS_RAW Inverted by Auto Run Mode 0: Not inverted 1: Inverted
5	R/W	HS_OUT Bypass PLL into VGIP 0: Disable (Default) 1: Enable
4	R/W	Active Region Measure Enable 0: Disable (Default) 1: Enable
3	R/W	ADC_VS Source Select in Test Mode 0: Select ADC_VS Source in Normal Mode or Auto Mode by CR47[6] (Default) 1: Select ADC_VS Source in Test Mode (Select VS_RAW or DeVS by CR49[5])
2:0	R	Stable Period[10:8] Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 51 Stable_Period_L

Bit	Mode	Function
7:0	R	Stable Period[7:0] Compare each line's period, if we get continuous 64 lines with the same one, the period is updated as the stable period.

Address: 52 MEAS_HS_PER_H (HSYNC Period Measured Result) Default: 8'b000xxxxx

Bit	Mode	Function
7	R/W	Auto Measure Enable 0: Disable (Default) 1: Enable
6	R/W	Pop Up Period Measurement Result 0: No Pop Up (Default) 1: Pop Up Result
5	R/W	Start a HS & VS period / H & V resolution & polarity measurement (on line monitor) 0: Finished/Disable (Default) 1: Enable to start a measurement, auto cleared after finished
4	R	Over-flow bit of Input HSYNC Period Measurement 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	Input HSYNC Period Measurement Result: High Byte[11:8]

Address: 53 MEAS_HS_PER_L (HSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	Input HSYNC Period Measurement Result: Low Byte[7:0]

- The result is expressed as the average number of crystal clocks (CR47[0]=0), or input clocks (CR47[0]=1) between 2 HSYNC.
- The result is the total number of crystal/input clocks inside 16-HSYNC periods divided by 16.
- Fractional part of measure result is stored in CR56[3:0].

Address: 54 MEAS_VS_PER_H (VSYNC Period Measured Result)

Bit	Mode	Function
7	R	Input VSYNC Polarity Indicator 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
6	R	Input HSYNC Polarity Indicator 0: negative polarity (high period is longer than low one) 1: positive polarity (low period is longer than high one)
5	R	Time-Out bit of Input VSYNC Period Measurement (No VSYNC occurred) 0: No Time Out

		1: Time Out occurred (512 time_clk ref CR5D-18[7:6])
4	R	Over-flow bit of Input VSYNC Period Measurement 0: No Over-flow occurred 1: Over-flow occurred
3:0	R	Input VSYNC Period Measurement Result: High Byte[11:8]

Address: 55 MEAS_VS_PER_L (VSYNC Period Measured Result)

Bit	Mode	Function
7:0	R	Input VSYNC Period Measurement Result: Low Byte[7:0]

- This result is expressed in terms of input HS pulses.
- When measured digitally, the result is expressed as the number of input ENA signal within a frame.

Address: 56 MEAS_HS&VS_HI_H (HSYNC&VSYNC High Period Measured Result)

Bit	Mode	Function
7:4	R	Input HSYNC High Period Measurement Result: High Byte[11:8] (CR58[0] = 0) Input VSYNC High Period Measurement Result: High Byte[11:8] (CR58[0] = 1)
3:0	R	Input HSYNC Period Measurement Fractional Result (See CR52,53)

Address: 57 MEAS_HS&VS_HI_L (HSYNC&VSYNC High Period Measured Result)

Bit	Mode	Function
7:0	R	Input HSYNC High Period Measurement Result: Low Byte[7:0] (CR58[0] = 0) Input VSYNC High Period Measurement Result: Low Byte[7:0] (CR58[0] = 1)

- This result of HSYNC high-period is expressed in terms of crystal clocks. When measured digitally, the result of HSYNC high-period is expressed as the number of input clocks inside the input enable signal.
- This result of VSYNC high-period is expressed in terms of input HS pulses

Address: 58 MEAS_HS&VS_HI_SEL (VSYNC High Period Measured Result) Default:00h

Bit	Mode	Function
7:6	R/W	HSYNC_MAX_DELTA 00: Don't care (CR58[3] will never go high) 01: 4-clock 10: 8-clock 11: 16-clock
5:4	R/W	VSYNC_MAX_DELTA 00: Don't care (CR58[2] will never go high) 01: 2-HSYNC 10: 4-HSYNC 11: 8-HSYNC
3	R	HSYNC_OVER_RANGE Set to 1 if variation of HSYNC larger than HSYNC_MAX_DELTA is detected by on-line measurement (CR52[7]=1). Write to clear this flag.
2	R	VSYNC_OVER_RANGE Set to 1 if variation of VSYNC larger than VSYNC_MAX_DELTA is detected by on-line measurement (CR52[7]=1). Write to clear this flag.
1	R/W	Start Measurement after Mode Detection Auto-mode 0: Disable (Default) 1: Enable
0	R/W	HSYNC/VSYNC High Period Measurement Result Select 0: HSYNC 1: VSYNC (See CR56~CR57)

Address: 59 MEAS_ACTIVE_REGION_H (Active Region Measured by CRSTL_CLK Result)

Bit	Mode	Function
7:0	R/W	Active Region Measured By Crystal Clock 1st read: Measurement Result: High Byte[23:16] 2nd read: Measurement Result: High Byte[15:8] 3rd read: Measurement Result: High Byte[8:0] Read pointer is auto increase, if write, the pointer is also reset to 1 st result.

Address: 5A SYNC_TEST_MISC Default: 00h

Bit	Mode	Function
7	R/W	Clamp Reference Source Selection 0: Clamp source from normal HS 1: Clamp source from CS_RAW
6	R/W	HS/ENA source swap for measurement 0: HS for analog mode, ENA for digital mode 1: HS for digital mode, ENA for analog mode
5:4	R/W	Active Region Measurement Option 00: Active Data Region (first ENA rising to last ENA falling,) 01: Whole Frame (VS rising to VS rising) 10: Back Porch (VS rising to first EAN rising) 11: Front Porch (last ENA falling to VS Rising)
3	R/W	vs/vs_org select option 0: vs/vs_org 1: vs_raw/vs_raw
2:0	R	The Number of Input HS between 2 Input VSYNC. LSB bit [2:0] for YPbPr

Address: 5B HS_DETECT Default: 00h

Bit	Mode	Function
7	R/W	HS detected flag, write clear. 0: no detect result 1: HS detected. (enable by CR5D-19[7])
6	R/W	SOG detected flag, write clear. 0: no detect result 1: SOG detected. (enable by CR5D-19[6])
5	R/W	VS detected flag, write clear. 0: no detect result 1: VS detected. (enable by CR5D-19[4])
4	R/W	Coast Signal Generate Reference Source 0: capture window 1: Normal (DeHs) (Default) 0: Normal (DeHs) (Default) 1: capture window
3	R/W	Miss DeHs In DeVs Region If Unlock Occurred Enable 0: Disable.(Default) 1: Enable
2	R/W	Miss DeHs In Coast Region Enable 0: Disable.(Default) 1: Enable
1:0	R/W	DeVs Counter Level Select 00: Stable Period x 1/2 (Default) 01: Stable high period x 2 10: Stable high period x 4 11: Normal (Reference CR4C[2:0]~CR4D)

Address: 5C SYNC_PROC_PORT_ADDR Default: 00h

Bit	Mode	Function
7:5	R/W	Reserved
4:0	R/W	Sync Processor Access Port Address

Address: 5D SYNC_PROC_PORT_DATA Default: 00h

Bit	Mode	Function
7:0	R/W	Sync Processor Access Port Data

- Port address will increase automatically after read/write.

Address: 5D-00 G_CLAMP_START (Clamp Signal Output Start) Default: 04h

Bit	Mode	Function
7:0	R/W	Start of Output Clamp_L Signal Pulse for Y/G Channel[7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal. (High Byte [11:8] at 5D-0x0D[7:4])

Address: 5D-01 G_CLAMP_END (Clamp Signal Output End) Default: 10h

Bit	Mode	Function
7:0	R/W	End of Output Clamp_L Signal Pulse for Y/G Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal. (High Byte [11:8] at 5D-0x0D[3:0])

Address: 5D-02 BR_CLAMP_START (Clamp Signal Output Start) Default: 04h

Bit	Mode	Function
7:0	R/W	Start of Output Clamp_L Signal Pulse for B/Pb and R/Pr Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal. (High Byte [11:8] at 5D-0x0E[7:4])

Address: 5D-03 BR_CLAMP_END (Clamp Signal Output End) Default: 10h

Bit	Mode	Function
7:0	R/W	End of Output Clamp_L Signal Pulse for B/Pb and R/Pr Channel [7:0]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal. (High Byte [11:8] at 5D-0x0E[3:0])

Address: 5D-04 CLAMP_CTRL0 Default:00h

Bit	Mode	Function
7	R/W	Clamp Trigger Edge Inverse for Y/G Channel 0: Trailing edge (Default) 1: Leading edge
6	R/W	Clamp Trigger Edge Inverse for B/Pb and R/Pr Channel 0: Trailing edge (Default) 1: Leading edge
5:0	R/W	Mask Line Number before DeVS [5:0]

Address: 5D-05 CLAMP_CTRL1 Default: 00h

Bit	Mode	Function
7	R/W	Clamp Mask Enable 0: Disable (Default) 1: Enable
6	R/W	Select Clamp Mask as De VS 0: Disable 1: Enable
5:0	R/W	Mask Line Number after DeVS [5:0]

CR5D-04[5:0] and CR5D-05[5:0] will set number of Mask Line before/after DeVS for Clamp Mask.

Address: 5D-06 CLAMP_CTRL2 Default: 00h

Bit	Mode	Function
7	R/W	Clamp Clock Source 0: ADC_Clock (Default) 1: Crystal Clock
6	R/W	Clamp Counter Unit (0x5D-00 – 0x5D-03) 0: Double Pixels (Default) 1: Single Pixel
5	R/W	ADC1_clamp_enable 0: Disable (Default) 1: Enable (useless, because there is no ADC1)

4	R/W	ADC0_clamp_enable 0: Disable (Default) 1: Enable
3	R/W	ADC-3 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
2	R/W	ADC-2 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
1	R/W	ADC-1 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR
0	R/W	ADC-0 Clamp Source 0: Clamp-G (Default) 1: Clamp-BR

Address: 5D-07 COAST_CTRL Default: 21h

Bit	Mode	Function
7:4	R/W	Start of COAST before DeVs Leading Edge [3:0]
3:0	R/W	End of COAST after DeVs Trailing Edge [3:0]

Address: 5D-08 CAPTURE_WINDOW_SETTING Default: 04h

Bit	Mode	Function
7	R/W	Coast_sel 0: de_coast (Default) 1: coast_org
6	R/W	Capture Miss Limit during Hsync Extraction 0: 32 (Default) 1: 16
5	R/W	Capture Window add step as Miss Lock 0: ±1 crystal clks (Default) 1: ±2 crystal clks
4:0	R/W	Capture Window Tolerance 5'h00: ±6 crystal clks for capture window 5'h01 ~ 5'b1F : ±1 ~ ±31 crystal clks for capture window

Address: 5D-09 DETECTION_TOLERANCE_SETTING Default: 04h

Bit	Mode	Function
7	R/W	Clamp Signal Inverted Enable 0: Not inverted (Default) 1: Invert
6:5	R/W	Stable Period Tolerance Extension 00: Use 0x4F[3] Setting (Default) 01: ±4 crystal clks 10: ±8 crystal clks 11: ±16 crystal clks
4:0	R/W	H-sync for De-composite De-bounce Length 5'h00: Disable De-bounce Function 5'h01 ~ 5'h1F : De-bounce 1 ~ 31 crystal clks for de-composite

Address: 5D-0A DEVS_CAP_NUM_H Default: 90h

Bit	Mode	Function
7:4	R/W	Divider of Fxtal * M2PLL_M / M2PLL_N Clock. Enable when CR4C[3] is set to 1. 0000 : Div = 1(Reserved) 0001 ~ 0111 : Div 1~Div7(Reserved) 1000 : Div = 8 1001 : Div = 9 (Default) 1111 : Div = 15
3:0	R	The munber of Capture window between DeVs high period: High Byte[11:8]

Address: 5D-0B DEVS_CAP_NUM_L
Default: 00h

Bit	Mode	Function
7:0	R	The number of Capture window between DeVs high period: High Byte[7:0]

Address: 5D-0C HSYNC_GLITCH_COUNTER_CTRL
Default: 00h

Bit	Mode	Function
7	R/W	Enable Hsync Glitch Counter 0: Disable 1: Enable.(Counter results pop up to bit3~0)
6:4	R/W	Reserved to 0
3:0	R/W	Glitch Counter Number,Write Clear By Write Bit7 To 0. (Active when bit7 enabled) 0~15: The glitch counter number between two hs, max glitch number is 15 if glitch number greater than 15.

Address: 5D-0D G_CLAMP_START_H (Clamp Signal Output Start/End)
Default: 00h

Bit	Mode	Function
7:4	R/W	Start of Output Clamp Signal Pulse for Y/G Channel[11:8]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.
3:0	R/W	End of Output Clamp Signal Pulse for Y/G Channel[11:8]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.

Address: 5D-0E BR_CLAMP_START_H (Clamp Signal Output Start/End)
Default: 00h

Bit	Mode	Function
7:4	R/W	Start of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [11:8]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the start of the output CLAMP signal.
3:0	R/W	End of Output Clamp Signal Pulse for B/Pb and R/Pr Channel [11:8]: Determine the number of input double-pixel between the trailing edge of input HSYNC and the end of the output CLAMP signal.

Address: 5D-0F HV_DELAY_CTRL
Default: 05h

Bit	Mode	Function
7	R	Original VS level be latched by HS rising edge which N Xtal delayed.(N reference bit2:0)
6	R	VS level be latched by original HS rising edge.
5	R	VS level which N Xtal delayed be latched by original HS rising edge.(N reference bit2:0)
4	R/W	Delay HS Or Original HS Out Select For Measurement 0: Original.(Default) 1: Delay HS
3	R/W	Delay VS Or Original VS Out Select For Measurement 0: Original.(Default) 1: Delay VS
2:0	R/W	HS Or VS Delay Crystal (or IOSC) Clock Counter 101: (Default 6 XTAL) 000 ~ 111: 1~8 crystal clk for HS or VS delay counter.

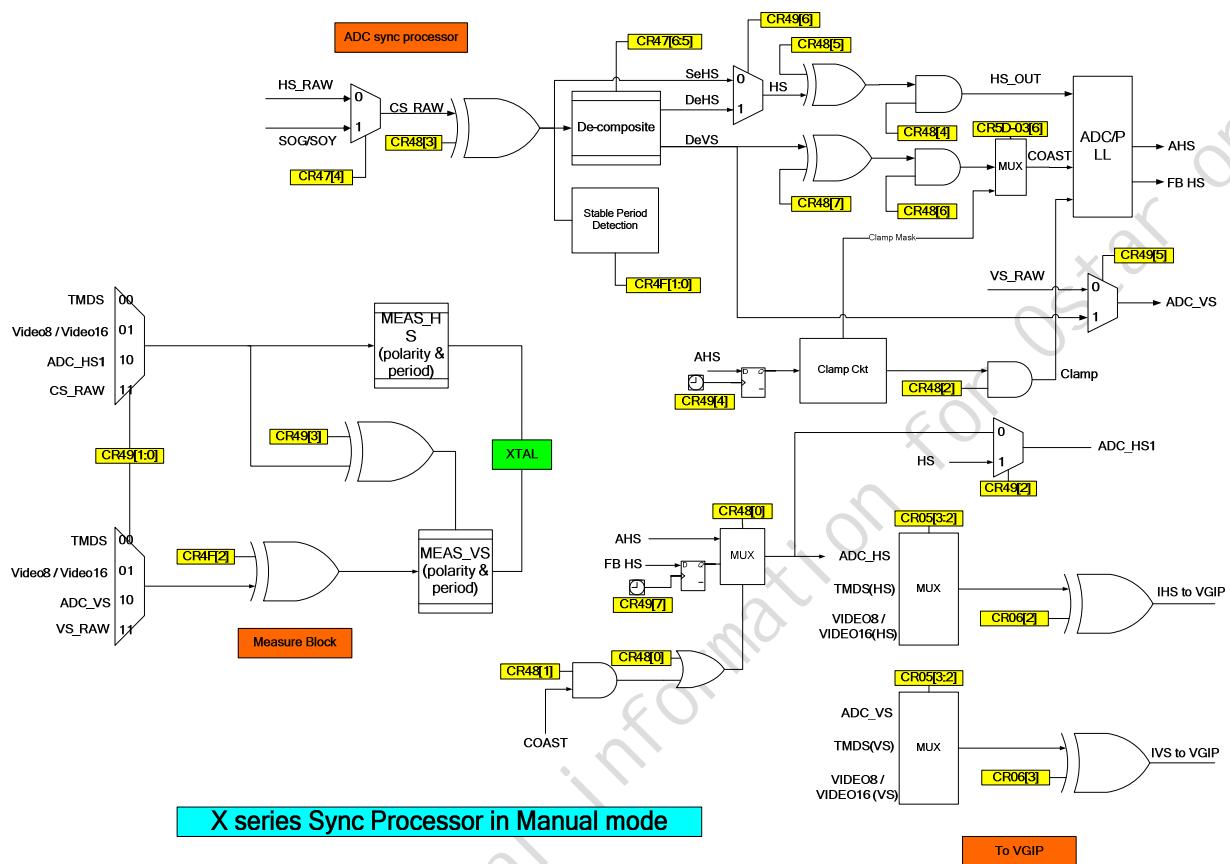
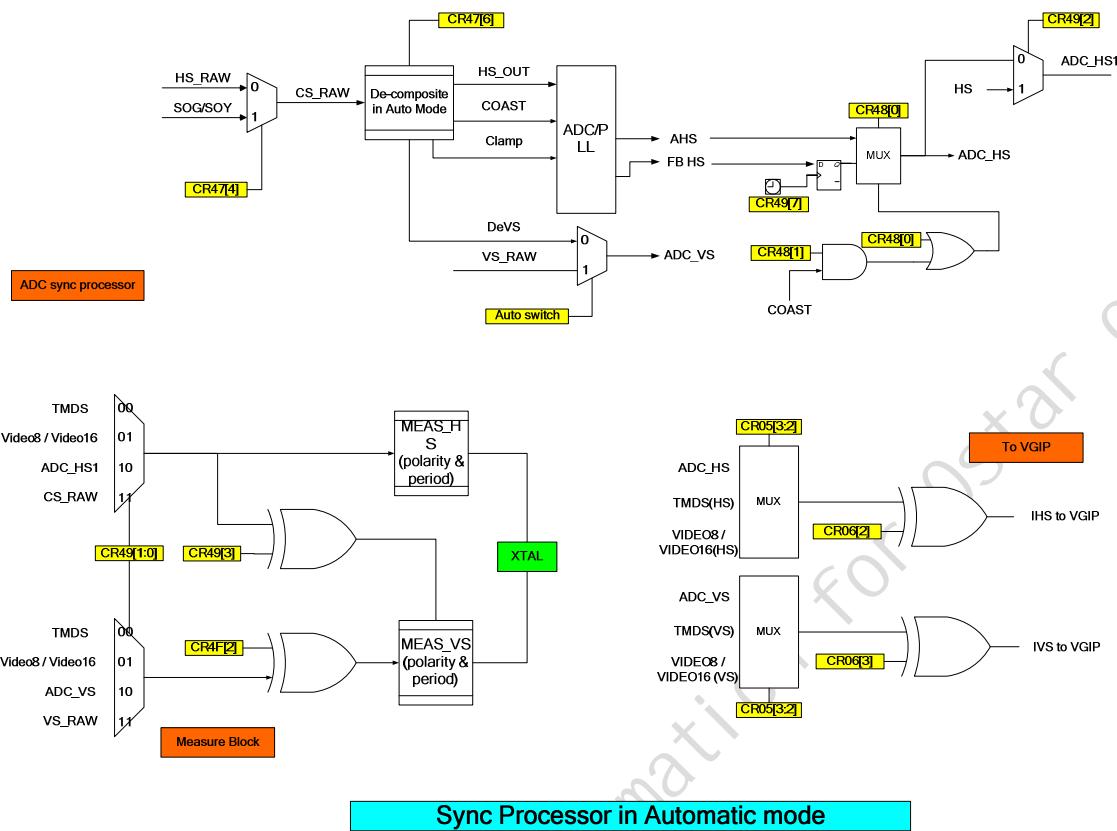


Figure 16: Sync processor



Sync processor in Automatic mode

Address 0x5E is reserved

Highlight window

Address: 60 **Highlight Window Access Port control**

Default: 00h

Bit	Mode	Function
7	R/W	Enable highlight window access port
6	R/W	Enable highlight window
5:4	--	Reserved
3:0	R/W	Highlight-window port address (Active when bit7 = 1)

Address: 61-00 **Highlight Window Horizontal Start**

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window horizontal start[11:8]

Address: 61-01 **Highlight Window Horizontal Start**

Bit	Mode	Function
7:0	R/W	Highlight window horizontal start[7:0]

Address: 61-02 **Highlight Window Horizontal End**

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window horizontal end[11:8]

Address: 61-03 **Highlight Window Horizontal End**

Bit	Mode	Function
7:0	R/W	Highlight window horizontal end[7:0]

Address: 61-04 **Highlight Window Vertical Start**

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window vertical start[11:8]

Address: 61-05 **Highlight Window Vertical Start**

Bit	Mode	Function
7:0	R/W	Highlight window vertical start[7:0]

Address: 61-06 **Highlight Window Vertical End**

Bit	Mode	Function
7:4	--	Reserved
3:0	R/W	Highlight window vertical end[11:8]

Address: 61-07 **Highlight Window Vertical End**

Bit	Mode	Function
7:0	R/W	Highlight window vertical end[7:0]

Highlight window horizontal/vertical reference point is DEN (display background start).

Address: 61-08 **Highlight Window Border**

Bit	Mode	Function
7	R/W	Highlight window border select: Left 0: border active (default) 1: non-active
6	R/W	Highlight window border select: Right 0: border active (default) 1: non-active
5	R/W	Highlight window border select: Top 0: border active (default) 1: non-active
4	R/W	Highlight window border select: Bottom

		0: border active (default) 1: non-active
3:0	R/W	Highlight window border width

Note : 1. Corner is intersection of two adjacent borders. Any one of these two borders is active, the corner is active.
 2. When border is non-active, the border will be viewed as a part of inside window.

Address: 61-09 Highlight Window Border Color

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border red color MSB 6bit (red color 2-bit LSB = 00)

Address: 61-0A Highlight Window Border Color

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border green color MSB 6bit (green color 2-bit LSB = 00)

Address: 61-0B Highlight Window Border Color

Bit	Mode	Function
7:6	--	Reserved
5:0	R/W	Highlight window border blue color MSB 6bit (blue color 2-bit LSB = 00)

Set up of highlight
 window:
 border width=15
 border start = 79
 border end = 143


Address: 61-0C Highlight Window Control 0

Default : 00h

Bit	Mode	Function

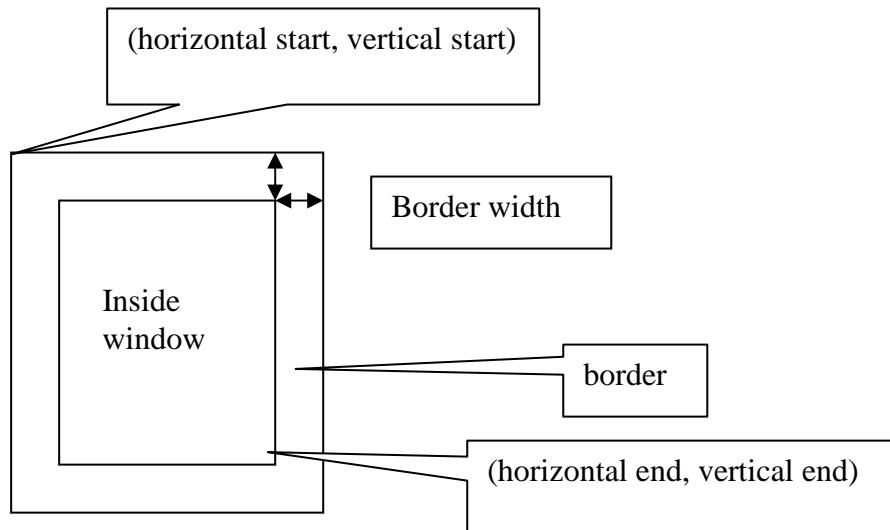
7:6	R/W	Contrast / brightness application control																																														
		00: Set A used on full region 01: Set B used inside highlight window 10: Set A used outside highlight window 11: Set A used outside highlight window, and Set B used inside highlight window																																														
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Address: 61-0D Highlight Window Control 1
Default : 00h

Bit	Mode	Function																				
7:6	R/W	<p>sRGB application control</p> <p>00: sRGB used on full region 01: sRGB used inside highlight window 10: sRGB used outside highlight window 11: Reserved</p> <table border="1"> <thead> <tr> <th>sRGB (CR62[2])</th> <th>Application control</th> <th>Inside window</th> <th>Outside window</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>X</td> <td>bypass</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0D[7:6]=00 CR60[6]=0</td> <td>sRGB</td> <td>sRGB</td> </tr> <tr> <td>1</td> <td>CR61-0D[7:6]=01 && CR60[6]=1</td> <td>sRGB</td> <td>bypass</td> </tr> <tr> <td>1</td> <td>CR61-0D[7:6]=10 && CR60[6]=1</td> <td>bypass</td> <td>sRGB</td> </tr> </tbody> </table>	sRGB (CR62[2])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0D[7:6]=00 CR60[6]=0	sRGB	sRGB	1	CR61-0D[7:6]=01 && CR60[6]=1	sRGB	bypass	1	CR61-0D[7:6]=10 && CR60[6]=1	bypass	sRGB
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5:4	R/W	<p>DCR/CABC application control</p> <p>00: DCR/CABC used on full region. 01: DCR/CABC used inside highlight window. 10: DCR/CABC used outside highlight window. 11: Reserved.</p> <table border="1"> <thead> <tr> <th>DCR(Page 7 CRD8[0]) /CABC(Page7 CRDB[2])</th><th>Application control</th><th>Inside window</th><th>Outside window</th></tr> </thead> <tbody> <tr> <td>0</td><td>X</td><td>bypass</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[5:4]=00 CR60[6]=0</td><td>DCR/CABC</td><td>DCR/CABC</td></tr> <tr> <td>1</td><td>CR61-0D[5:4]=01 && CR60[6]=1</td><td>DCR/CABC</td><td>bypass</td></tr> <tr> <td>1</td><td>CR161-0D[5:4]=10 && CR60[6]=1</td><td>bypass</td><td>DCR/CABC</td></tr> </tbody> </table>	DCR(Page 7 CRD8[0]) /CABC(Page7 CRDB[2])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0D[5:4]=00 CR60[6]=0	DCR/CABC	DCR/CABC	1	CR61-0D[5:4]=01 && CR60[6]=1	DCR/CABC	bypass	1	CR161-0D[5:4]=10 && CR60[6]=1	bypass	DCR/CABC
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3:2	R/W	<p>D domain DLCTI_CTRL</p> <p>00: DLCTI used on full region. 01: DLCTI used inside highlight window. 10: DLCTI used outside highlight window. 11: Reserved.</p> <table border="1"> <thead> <tr> <th>DLCTI(Page11 CRF0[5]/CRF4[0])</th><th>Application control</th><th>Inside window</th><th>Outside window</th></tr> </thead> <tbody> <tr> <td>0</td><td>X</td><td>bypass</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[3:2]=00 CR60[6]=0</td><td>DLCTI</td><td>DLCTI</td></tr> <tr> <td>1</td><td>CR61-0D[3:2]=01 && CR60[6]=1</td><td>DLCTI</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[3:2]=10 && CR60[6]=1</td><td>bypass</td><td>DLCTI</td></tr> </tbody> </table>	DLCTI(Page11 CRF0[5]/CRF4[0])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0D[3:2]=00 CR60[6]=0	DLCTI	DLCTI	1	CR61-0D[3:2]=01 && CR60[6]=1	DLCTI	bypass	1	CR61-0D[3:2]=10 && CR60[6]=1	bypass	DLCTI
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1:0	R/W	<p>Sharpness_CTRL</p> <p>00: SHP used on full region. 01: SHP used inside highlight window. 10: SHP used outside highlight window. 11: Reserved.</p> <table border="1"> <thead> <tr> <th>DCR(Page 12 CRA0[06])</th><th>Application control</th><th>Inside window</th><th>Outside window</th></tr> </thead> <tbody> <tr> <td>0</td><td>X</td><td>bypass</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[1:0]=00 CR60[6]=0</td><td>SHP</td><td>SHP</td></tr> <tr> <td>1</td><td>CR61-0D[1:0]=01 && CR60[6]=1</td><td>SHP</td><td>bypass</td></tr> <tr> <td>1</td><td>CR61-0D[1:0]=10 && CR60[6]=1</td><td>bypass</td><td>SHP</td></tr> </tbody> </table>	DCR(Page 12 CRA0[06])	Application control	Inside window	Outside window	0	X	bypass	bypass	1	CR61-0D[1:0]=00 CR60[6]=0	SHP	SHP	1	CR61-0D[1:0]=01 && CR60[6]=1	SHP	bypass	1	CR61-0D[1:0]=10 && CR60[6]=1	bypass	SHP
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0	X	bypass	bypass																			
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1	CR61-0D[1:0]=01 && CR60[6]=1	SHP	bypass																			
1	CR61-0D[1:0]=10 && CR60[6]=1	bypass	SHP																			



Inside window left-top point = (horizontal start + border width, vertical start + border width)

Inside window right-bottom point = (horizontal end, vertical end)

Border window left-top point = (horizontal start, vertical start)

Border window right-bottom point = (horizontal end+ border width, vertical end + border width)

Border = border window – inside window

Outside window = screen – border window

Color Processor Control

Address: 62 COLOR_CTRL (Color Control Register) Default: 00h

Bit	Mode	Function
7	R/W	sRGB Coefficient Write Ready 0: Not ready or cleared after finished 1: Ready to write (wait for DVS to apply)
6	R/W	sRGB Precision 0: Normal (Default) 1: Multiplier Coefficient Bit Left Shift
5:3	R/W	sRGB Coefficient Write Enable 000: Disable 001: Write R Channel (RRH,RRL,RGH,RGL,RBH,RBL) (address reset to 0 when written) 010: Write G Channel (GRH,GBL,GGH,GGL,GBH,GBL) (address reset to 0 when written) 011: Write B Channel (BRH,BRL,BGH,BGL,BBH,BBL) (address reset to 0 when written) 100: R Offset (RoffsetH, RoffsetL) (address reset to 0 when written) 101: G Offset (GoffsetH, GoffsetL) (address reset to 0 when written) 110: B Offset (BoffsetH, BoffsetL) (address reset to 0 when written)
2	R/W	Enable sRGB Function 0: Disable (Default) 1: Enable
1	R/W	Enable Contrast Function: 0: disable the coefficient (Default) 1: enable the coefficient
0	R/W	Enable Brightness Function: 0: disable the coefficient (Default) 1: enable the coefficient

Address: 63 SRGB_ACCESS_PORT

Bit	Mode	Function
7:0	W	sRGB_COEF[7:0]

- For Multiplier coefficient: 9 bit: 1 bit sign, 8 bit fractional part
- For filling multiplier coefficient, the sequence should be SIGN bit (High Byte), 8 bit fractional (Low Byte)
- For Offset Coefficient: 1 sign, 8 integer, 4 bit fractional part

- R G : 8 bit integer, 2bit fractional
- sRGB output saturation to 1023 and Clamp to 0
- sRGB Output is 10 bit

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} 1+RR & RG & RB \\ GR & 1+GG & GB \\ BR & BG & 1+BB \end{bmatrix} \begin{bmatrix} R \\ G \\ B \end{bmatrix} + \begin{bmatrix} Roffset \\ Goffset \\ Boffset \end{bmatrix}$$

New SRGB(RL6093/RTD2382)	
{62[6], 68[6:5]}	Bit Definition
100	1-bit shift-left
101	2-bit shift-left (S1.7)
110	3-bit shift-left (S2.6)
111	6-bit shift-left (S0.08)
0xx	0-bit shift-left (S0.08)

Old SRGB (RTD2472D, RTD2472RD)	
{62[6], 68[6]}	Bit Definition
10	1-bit shift-left (S0.8)
11	2-bit shift-left (S1.7)
0x	0-bit shift-left (S0.08)

Contrast/Brightness Coefficient

Address: 64 Contrast /Brightness Access Port Control

Default: 00h

Bit	Mode	Function
7	R/W	Enable Contrast /Brightness access port
6	R/W	Contrast/Brightness and sRGB swap 0: sRGB before Contrast/Brightness(Default) 1: Contrast/Brightness before sRGB (for PCM)
5:0	R/W	Contrast /Brightness port address

Access data port continuously will get address auto increase.

Address: 65-00 BRI_RED_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Red Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-01 BRI_GRN_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Green Coefficient: Valid range: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-02 BRI_BLU_COE (Set A)

Bit	Mode	Function
7:0	R/W	Brightness Blue Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-03 CTS_RED_COE (Set A)

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-04 CTS_GRN_COE (Set A)

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-05 CTS_BLU_COE (Set A)

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-06 BRI_RED_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Red Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-07 BRI_GRN_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Green Coefficient: Valid range: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-08 BRI_BLU_COE (Set B)

Bit	Mode	Function
7:0	R/W	Brightness Blue Coefficient: Valid range: -128(00h) ~ 0(80h) ~ +127(FFh)

Address: 65-09 CTS_RED_COE (Set B)

Bit	Mode	Function
-----	------	----------

7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)
-----	-----	---

Address: 65-0A CTS_GRN_COE (Set B)

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0B CTS_BLU_COE (Set B)

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

When highlight window is disable, coefficient set A is used.

Address: 65-0C CTS_RED2_COE (Set A)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0D CTS_GRN2_COE (Set A)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0E CTS_BLU2_COE (Set A)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-0F CTS_RED2_COE (Set B)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Red Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-10 CTS_GRN2_COE (Set B)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Green Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-11 CTS_BLU2_COE (Set B)

Default: 80h

Bit	Mode	Function
7:0	R/W	Contrast Blue Coefficient: Valid range: 0(00h) ~ 1(80h) ~ 2(FFh)

Address: 65-12

Register:: CTS_Threshold (Set A)

Name	Bit	R/W	Default	Description	Config
CTS_Threshold	7:0	R/W	0xFF	Threshold of GAIN1 and GAIN2 of Set A	

Address: 65-13

Register:: CTS_Threshold (Set B)

Name	Bit	R/W	Default	Description	Config
CTS_Threshold	7:0	R/W	0xFF	Threshold of GAIN1 and GAIN2 of Set B	

If input value > threshold, the CTS_ADDING_VALUE will be applied.

Address: 65-14

Register:: CTS_R_GAIN_ADDING_VALUE_H (Set A)

Name	Bit	R/W	Default	Description	Config
CTS_R_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The adding value High byte [11:8] of GAIN2 region	

Address: 65-15

Register:: CTS_R_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_R_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The adding value Low byte [7:0] of GAIN2 region	

Address: 65-16

Register:: CTS_G_GAIN_ADDING_VALUE_H (Set A) 0x5B -0C					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The green channel adding value High byte [11:8] of GAIN2 region	

Address: 65-17

Register:: CTS_G_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The green channel adding value Low byte [7:0] of GAIN2 region	

Address: 65-18

Register:: CTS_B_GAIN_ADDING_VALUE_H (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The blue channel adding value High byte [11:8] of GAIN2 region	

Address: 65-19

Register:: CTS_B_GAIN_ADDING_VALUE_L (Set A)					
Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The blue channel adding value Low byte [7:0] of GAIN2 region	

Address: 65-1A

Register:: CTS_GAIN_ADDING_VALUE_H (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_R_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The adding value High byte [11:8] of GAIN2 region	

Address: 65-1B

Register:: CTS_GAIN_ADDING_VALUE_L (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_R_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The adding value Low byte [7:0] of GAIN2 region	

Address: 65-1C

Register:: CTS_G_GAIN_ADDING_VALUE_H (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The green channel adding value High byte [11:8] of GAIN2 region	

Address: 65-1D

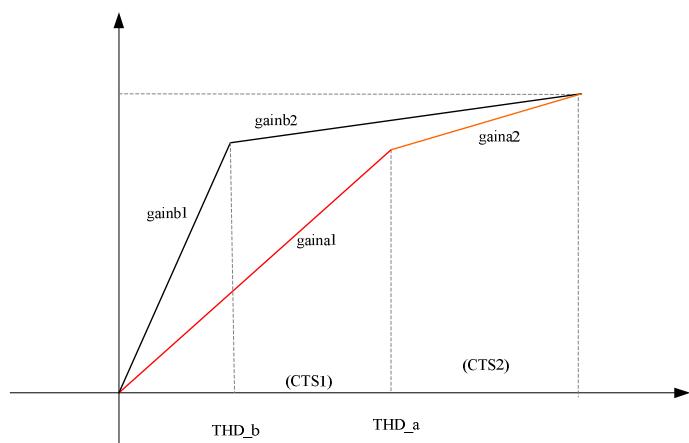
Register:: CTS_G_GAIN_ADDING_VALUE_L (Set B)					
Name	Bit	R/W	Default	Description	Config
CTS_G_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The green channel adding value Low byte [7:0] of GAIN2 region	

Address: 65-IE
Register:: CTS_B_GAIN_ADDING_VALUE_H (Set B)

Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_VALUE_H	7:0	R/W	0x00	The blue channel adding value High byte [11:8] of GAIN2 region	

Address: 65-IF
Register:: CTS_B_GAIN_ADDING_VALUE_L (Set B)

Name	Bit	R/W	Default	Description	Config
CTS_B_GAIN_ADDING_VALUE_L	7:0	R/W	0x00	The blue channel adding value Low byte [7:0] of GAIN2 region	


InWin:

$$Yout = Yin \cdot CT1 + BR$$

$$Yout = (Yin - THD_a) \cdot CT2 + THD_a \cdot CT1 \\ = Yin \cdot CT2 + BR + (CT1 - CT2) \cdot THD_a$$

$$\text{gain_adding_value } a = (\text{gainb1} - \text{gaina2}) \cdot THD_a \\ \text{u1.7} * \text{u8} = \text{u9.7}$$

-> truncate lsb 4bit => u9.3

$$\text{gain_adding_value } b = (\text{gainb1} - \text{gainb2}) \cdot THD_b$$

Address:65-20~65-FF reserved

Gamma Control

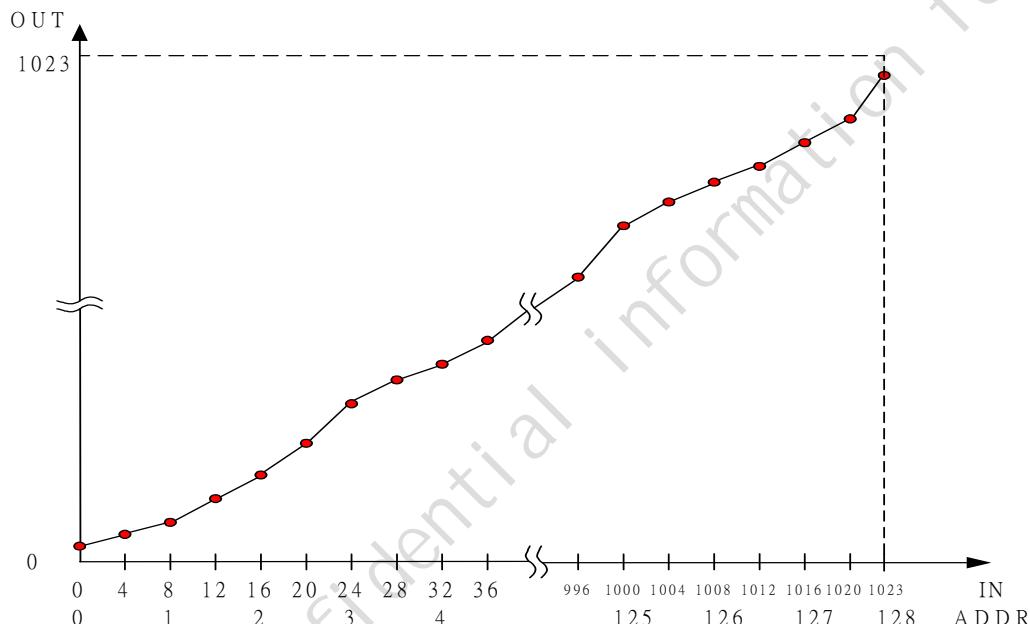
Address: 66 GAMMA_PORT

Bit	Mode	Function
7:0	R/W	Access port for gamma correction table

- The Gamma Table written to this port should follow the sequences as expressed below:

{2'b0, g0[9:4]}, {g0[3:0]}, 2'b0, g4[9:8]}, {g4[7:0]}	<- addr = 0
{2'b0, g8[9:4]}, {g8[3:0]}, 2'b0, g12[9:8]}, {g12[7:0]}	<- addr = 1
...	
{2'b0, g1016[9:4]}, {g1016[3:0]}, 2'b0, g1020[9:8]}, {g1020[7:0]}	<- addr = 127
{2'b0, g1023[9:4]}, {g1023[3:0]}, 4'b0}, {8'b0}	<- addr = 128
- When CR67[3] is set to 1, we can directly specify the initial address of Gamma Table in this port.
- When CR67[3] is set to 1, the value of this port is the address of Gamma Table that you are going to R/W.
- When CR67[3] is set to 0, we can read the value of Gamma Table in the following order.

{2'b0, g_4*2n [9:4]}, {g_4*2n [3:0]}, 2'b0, g4*(2n+1)[9:8]}, {g4*(2n+1)[7:0]}	
{2'b0, g_4*(2n+2)[9:4]}, {g_4*(2n+2) [3:0]}, 2'b0, g4*(2n+3) [9:8]}, {g4*(2n+3)[7:0]}	
...	
{2'b0, g_1023[9:4]}, {g_1023*(2n+2) [3:0]}, 4'b0}, {8'b0}	



When support PCM, the table setting will be as below :

To Latch

- {2'b00, gamma_data0[9:4]}, {gamma_data0[3:0]}, 2'b00, gamma_data1[9:8]}, { gamma_data1[7:0]}.
- {2'b00, gamma_data2[9:4]}, {gamma_data2[3:0]}, 2'b00, gamma_data3[9:8]}, { gamma_data3[7:0]}.
- {2'b00, gamma_data4[9:4]}, {gamma_data4[3:0]}, 4'h00}, {8'h00}.
- {2'b00, gamma_data6[9:4]}, {gamma_data6[3:0]}, 2'b00, gamma_data5[9:8]}, { gamma_data5[7:0]}.
- {8'h00}, {6'h00, gamma_data7[9:8] }, { gamma_data7[7:0]}.
- {2'b00, gamma_data8[9:4]}, {gamma_data8[3:0]}, 2'b00, gamma_data9[9:8]}, { gamma_data9[7:0]}
- {2'b00, gamma_data10[9:4]}, {gamma_data10[3:0]}, 2'b00, gamma_data11[9:8]}, { gamma_data11[7:0]}
- {2'b00, gamma_data12[9:4]}, {gamma_data12[3:0]}, 2'b00, gamma_data13[9:8]}, { gamma_data13[7:0]}

To SDRAM

- {8'h00}, {8'h00}, {8'h00}
 - {2'b00, gamma_data14[9:4]}, {gamma_data14[3:0]}, 2'b00, gamma_data15[9:8]}, { gamma_data15[7:0]}.
 - {2'b00, gamma_data16[9:4]}, {gamma_data16[3:0]}, 2'b00, gamma_data17[9:8]}, { gamma_data17[7:0]}.
-

Address: 67 GAMMA_CTRL
Default: 00h

Bit	Mode	Function
7	R/W	Enable Access Channels for Gamma Correction Coefficient: 0: Disable these channels (Default) 1: Enable these channels
6	R/W	Gamma table enable 0: By pass (Default) 1: Enable
5:4	R/W	Color Channel of Gamma Table 00: Red Channel (Default) 01: Green Channel 10: Blue Channel 11: Red/Green/Blue Channel (R/G/B Gamma are the same)
3	R/W	Gamma Port Address Access Enable 0: Normal function. (Default) 1: Gamma Port is used as specifying initial address.
2	R/W	Write Table to SRAM or Latch Select 0: To SRAM (Default) 1: To Latch
1	R/W	Reg_dither_keep4frame_seq: 0: every frame change sequence table set 1: every 4 frames change sequence table set Suggestion : Enable this bit to avoid some 4 bit (ex: 10b to 6 b) dither side effect, when Dither_temp (CR6A[4]) & Reg_multi_seq_en (CR6B[1]) are enabled
0	R/W	Reg_dither_pr_type: line interleave dither for PR type select 0: Normal dither 1: Interleave dither When Reg_dither_pr_type (CR67[0])=1, select line interleave dither, the offset between L and R dither table is defined by Reg_dither_lr_table_offset (CR68[4:3])

Address: 68 GAMMA_BIST (Color Control Register)
Default: 60h

Bit	Mode	Function
7	R/W	Test_mode 0: Disable, dither_out = dither_result[9:2] // truncate to integer number (Default) 1: Enable, dither_out = dither_result[7:0] // propagate decimal part for test
6:5	R/W	sRGB multiplier coefficient precision 00: 1-bit Shift-left 10: 3-bit Shift-left 01: 2-bit Shift-left 11: 0-bit shift-left (Default)
4:3	R/W	Reg_dither_lr_table_offset: Select the offset of dither table between L and R in PR type, if L select table n and R will select table n+offset 00: No offset. 01: Offset 1 10: Offset 2 11: Offset 3
2	R/W	Gamma BIST_En 0: BIST disable (Default) 1: BIST enable
1	R	Gamma BIST_Period Progress 0: BIST is done (Default) 1: BIST is running
0	R	Gamma BIST Test Result (It will go low first during BIST period) 0: SRAM Fail 1: SRAM OK

Dithering Control(For Display Domain)

Register:: DITHERING_DATA_ACCESS				0x69	
Name	Bits	Read/Write	Reset State	Comments	Config
DITHERING_DATA_ACCESS	7:0	W	0	Refer to following description	

A. When CR6A[7:6] is 2'b01, dithering sequence table access is enabled:

- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, ..., s31.
- Each element has 2 bit to index one of 4 dithering table.
- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, ..., {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, ..., {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, ..., {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.
- There are 4 sequence table for r, g, b channel each. The writing sequence table order is r0, g0, b0, r1, g1, b1, r2, g2, b2, r3, g3, b3
- If reg_multi_seq_en (CR6B[1]) = 1:
 - When reg_dither_seq_share_mode (CR6B[3]) = 0, one channel can use 4 set of sequence table.
 - When reg_dither_seq_share_mode (CR6B[3]) = 1, one channel can use r,g,b total 12 set of sequence table.
 - Else only one sequence is used for each channel.
- When reg_seq_inverse (CR6C[7]) = 1, the sequence can be inverted and used as a new table.
- DITHER_SEQ_SET (CR6B[2]) can be used only when Reg_multi_seq_en (CR6B[1]) = 0.
- The relationship between register setting, sequence arrangement and frame number is listed as the table below: (rn represents r sequence n, gn represents g sequence n, bn represents b sequence n, ~rn represents inverted r sequence n, gn represents inverted g sequence n, bn represents inverted b sequence n)

num	register setting			
	multi_seq_en	dither_seq_share_mode	dither_seq_inv	dither_seq_inv_mode
1	1			
2		1		
3			1	
4	1	1		
5		1	1	
6	1		1	
7	1	1	1	
8	1	1		1
9	1		1	1
10		1	1	1

R channel:

frame num	sequence arrangement																								
	CR67[1] = 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
	CR67[1] = 1	1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32	33-36	37-40	41-44	45-48	49-52	53-56	57-60	61-64	65-68	69-72	73-76	77-80	81-84	85-88	89-92	93-96
1	r0	r1	r2	r3	r0	r1	r2	r3	r0	r1	r2	r3	r0	r1	r2	r3	r0	r1	r2	r3	r0	r1	r2	r3	
2	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	
3	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	r0	~r0	
4	r0	r1	r2	r3	g0	g1	g2	g3	b0	b1	b2	b3	r0	r1	r2	r3	g0	g1	g2	g3	b0	b1	b2	b3	
5	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	
6	r0	r1	r2	r3	~r0	~r1	~r2	~r3	r0	r1	r2	r3	~r0	~r1	~r2	~r3	r0	r1	r2	r3	~r0	~r1	~r2	~r3	
7	r0	r1	r2	r3	~r0	~r1	~r2	~r3	g0	g1	g2	g3	~g0	~g1	~g2	~g3	b0	b1	b2	b3	~b0	~b1	~b2	~b3	
8	r0	r1	r2	r3	g0	g1	g2	g3	b0	b1	b2	b3	~r0	~r1	~r2	~r3	~g0	~g1	~g2	~g3	~b0	~b1	~b2	~b3	
9	r0	r1	r2	r3	~r0	~r1	~r2	~r3	r0	r1	r2	r3	~r0	~r1	~r2	~r3	~r0	~r1	~r2	~r3	~r0	~r1	~r2	~r3	
10	r0	g0	b0	~r0	~g0	~b0	r0	g0	b0	~r0	~g0	~b0	r0	g0	b0	~r0	~g0	~b0	r0	g0	b0	~r0	~g0	~b0	

G channel:



frame \ num	CR67[1]	sequence arrangement																							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	= 0	g0	g1	g2	g3	g0	g1	g2	g3	g0	g1	g2	g3	g0	g1	g2	g3	g0	g1	g2	g3	g0	g1	g2	g3
2	= 1	1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32	33-36	37-40	41-44	45-48	49-52	53-56	57-60	61-64	65-68	69-72	73-76	77-80	81-84	85-88	89-92	93-96
3		g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0	g0	b0	r0
4		g0	g1	g2	g3	b0	b1	b2	b3	r0	r1	r2	r3	g0	g1	g2	g3	b0	b1	b2	b3	r0	r1	r2	r3
5		g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0
6		g0	g1	g2	g3	~g0	~g1	~g2	~g3	g0	g1	g2	g3	~g0	~g1	~g2	~g3	g0	g1	g2	g3	~g0	~g1	~g2	~g3
7		g0	g1	g2	g3	~g0	~g1	~g2	~g3	b0	b1	b2	b3	~b0	~b1	~b2	~b3	r0	r1	r2	r3	~r0	~r1	~r2	~r3
8		g0	g1	g2	g3	b0	b1	b2	b3	r0	r1	r2	r3	~g0	~g1	~g2	~g3	b0	b1	b2	b3	~r0	~r1	~r2	~r3
9		g0	g1	g2	g3	~g0	~g1	~g2	~g3	g0	g1	g2	g3	~g0	~g1	~g2	~g3	~g0	~g1	~g2	~g3	~g0	~g1	~g2	~g3
10		g0	b0	r0	~g0	~b0	~r0	g0	b0	r0	~g0	~b0	~r0	g0	b0	r0	~g0	~b0	~r0	g0	b0	r0	~g0	~b0	~r0

B channel:

frame \ num	CR67[1]	sequence arrangement																							
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	= 0	1-4	5-8	9-12	13-16	17-20	21-24	25-28	29-32	33-36	37-40	41-44	45-48	49-52	53-56	57-60	61-64	65-68	69-72	73-76	77-80	81-84	85-88	89-92	93-96
2	= 1	b0	b1	b2	b3	b0	b1	b2	b3	b0	b1	b2	b3	b0	b1	b2	b3	b0	b1	b2	b3	b0	b1	b2	b3
3		b0	~b0	g0	b0	r0	~g0	b0	r0	g0	b0	r0	~g0												
4		b0	b1	b2	b3	r0	r1	r2	r3	g0	~g1	~g2	~g3	b0	b1	b2	b3	r0	r1	r2	r3	g0	~g1	~g2	~g3
5		b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0	b0	~b0	r0	~r0	g0	~g0
6		b0	b1	b2	b3	~b0	~b1	~b2	~b3	b0	b1	b2	b3	b0	b1	b2	b3	~b0	~b1	~b2	~b3	b0	~b1	~b2	~b3
7		b0	b1	b2	b3	~b0	~b1	~b2	~b3	r0	r1	r2	r3	~r0	~r1	~r2	~r3	r0	~r1	~r2	~r3	~r0	~r1	~r2	~r3
8		b0	b1	b2	b3	r0	r1	r2	r3	g0	~g1	~g2	~g3	~b0	~b1	~b2	~b3	~r0	~r1	~r2	~r3	~g0	~g1	~g2	~g3
9		b0	b1	b2	b3	~b0	~b1	~b2	~b3	b0	b1	b2	b3	~b0	~b1	~b2	~b3	b0	~b1	~b2	~b3	~b0	~b1	~b2	~b3
10		b0	r0	~g0	~b0	~r0	~g0	b0	r0	~g0	~b0	~r0	~g0	b0	r0	~g0	~b0	~r0	~g0	~b0	~r0	~g0	~b0	~r0	~g0

B. When CR6A[7:6] is 2'b10, dithering table access is enabled:

- For dithering table access, the red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.
- Input data sequence is [Dr00 Dr01], [Dr02,Dr03], ..., [Dr30,Dr31], [Dr32,Dr33], [Dg00,Dg01], [Dg02,Dg03], ..., [Dg30,Dg31], [Dg32,Dg33], [Db00,Db01], [Db02,Db03], ..., [Db30,Db31], [Db32,Db33].

D00	D01	D10	D11	D20	D21	D30	D31
D02	D03	D12	D13	D22	D23	D32	D33

C. When CR6A[7:6] is 2'b11, temporal offset access is enabled:

- There are 16 element for temporal offset table, t0, t1, ..., t15. Each element has 2 bit to index one of 4 temporal offset.
- Input data sequence is {t3,t2,t1,t0}, {t7,t6,t5,t4}, {t11,t10,t9,t8}, {t15,t14,t13,t12}.

Register:: DITHERING_CTRL1								0x6A
Name	Bits	Read/Write	Reset State	Comments				Config
Dither_Access	7:6	R/W	0	Enable Access Control 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset				
Dither_en	5	R/W	0	Enable Dithering Function 0: disable (Default) 1: enable				
Dither_temp	4	R/W	0	Temporal Dithering 0: Disable (Default) 1: Enable				
Dither_table	3	R/W	0	Dithering Table Value Sign 0: unsigned 1: signed (2's complement)				
Dither_mode	2	R/W	0	Dithering Mode 0: New (Default) 1: Old				
Dither_V_Fram_M	1	R/W	0	Vertical Frame Modulation 0: Disable (Default) 1: Enable				
Dither_VH_Fram_M	0	R/W	0	Horizontal Frame Modulation				

				0: Disable (Default) 1: Enable	
--	--	--	--	-----------------------------------	--

Dithering Control (Display Domain)

Register::: DITHERING_CTRL2					0x6B
Name	Bits	Read/ Write	Reset State	Comments	Config
DITHER_THD_SEL_EN	7	R/W	0x0	Dither RGB level threshold select enable 0: Disable 1: Enable	
DITHER_THD_SEL	6:4	R/W	0x00	Dither RGB level threshold select (0x69) 000: {6'h0, R_THD[9:8]} 001: R_THD[7:0] 010: {6'h0, G_THD[9:8]} 011: G_THD[7:0] 100: {6'h0, B_THD[9:8]} 101: B_THD[7:0] 110: {6'h0, ALL R/G/B[9:8]} 111: ALL R/G/B[7:0]	
Reg_dither_seq_share_mode	3	R/W	0	R, G, B sequence sharing select 0: R, G, B can only use its own dither sequences (4 each channel) 1: R, G, B can share dither sequences, each channel can use 12 dither sequences.	
DITHER_SEQ_SET	2	R/W	0	Sequence table select 0: All select setting0 1: Select setting1 only if R/G/B < THD This bit is valid only when 0x6B[1] = 0.	
Reg_multi_seq_en	1	R/W	0	Dither sequence number select 0: 1 set of sequence for each channel 1: 4 set of sequence for each channel	
Dither_Table_Ref	0	R/W	1	Table reference 0: By VS/HS 1: By DEN (Default)	

Overlay/Color Palette/Background Color Control

Address: 6C **OVERLAY_CTRL (Overlay Display Control Register)** **Default: 00h**

Bit	Mode	Function
7	R/W	Reg_dither_seq_inv: 0: Normal 1: Each dither sequence can be used inverted as another new sequence.
6	R/W	Reg_dither_seq_inv_mode: Valid only when Reg_dither_seq_inv (CR6C[7]) = 1 0: Sequence r, ~r, g, ~g, b, ~b 1: Sequence r, g, b ~r, ~g, ~b
5	R/W	Background color access enable 0: Disable(Reset CR6D Write Pointer to R) 1: Enable
4:2	R/W	Alpha blending level (Also enable OSD frame control register 0x003 byte 1[3:2]) 000: Disable (Default) 001 ~111: 1/8~ 7/8
1	R/W	Overlay Sampling Mode Select: 0: Single pixel per clock (Default) 1: Dual pixels per clock (The OSD will be zoomed 2X in horizontal scan line)
0	R/W	Overlay Port Enable: 0: Disable (Default) 1: Enable Turn off overlay enable and switch to background simultaneously when auto switch to background.

Address: 6D **BGND_COLOR_CTRL** **Default: 00h**

Bit	Mode	Function
7:0	R/W	Background color RGB 8-bit value[7:0]

- There are 3 bytes color select of background R, G, B, once we enable Background color access channel(CR6C[5]) and the continuous writing sequence is R/G/B

Address: 6E **OVERLAY_LUT_ADDR (Overlay LUT Address)** **Default: 00h**

Bit	Mode	Function
7	R/W	Enable Overlay Color Plate Access: 0: Disable (Default) 1: Enable
6	R/W	Double buffer write enable (auto clear) 0: disable 1: enable
5:0	R/W	Overlay-64*24 Look-Up-Table Write Address [5:0]

- Auto-increment while every accessing “Overlay LUT Access Port”.
- While OSDON, enable double buffer write is optional for modifying color palette LUT.
If double buffer write is enable, the flow below must be followed:
 - Write [6] to be 1 and set LUT write address first
 - Write 3 data R[7:0], G[7:0], B[7:0] to 6F
 - Wait for [6] auto clear to be 0, then repeat the flow until the procedure is done

Address: 6F **COLOR_LUT_PORT (LUT Access Port)**

Bit	Mode	Function
7:0	W	Color Palette 64*24 Look-Up-Table access port [7:0]

- Using this port to access overlay color plate which addressing by the above registers.
- The writing sequence into LUT is [R0, G0, B0, R1, G1, B1, ...R63, G63, and B63] and the address counter will be automatic increment and circular from 0 to 63.

Image Auto Function

Address: 70 H_BOUNDARY_H

Bit	Mode	Function
7:4	R/W	Horizontal Boundary Start: High Byte [11:8]
3:0	R/W	Horizontal Boundary End: High Byte [11:8]

Address: 71 H_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	Horizontal Boundary Start: Low Byte [7:0]

Address: 72 H_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	Horizontal Boundary End: Low Byte [7:0]

Address: 73 V_BOUNDARY_H

Bit	Mode	Function
7:4	R/W	Vertical Boundary Start: High Byte [11:8]
3:0	R/W	Vertical Boundary End: High Byte [11:8]

Vertical boundary search should be limited by Vertical boundary start.

Address: 74 V_BOUNDARY_STA_L

Bit	Mode	Function
7:0	R/W	Vertical Boundary Start: Low Byte [7:0]

Address: 75 V_BOUNDARY_END_L

Bit	Mode	Function
7:0	R/W	Vertical Boundary End: Low Byte [7:0]

Address: 76 RED_NOISE_MARGIN (Red Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Red pixel noise margin setting register
1:0	--	Reserved to 0

Address: 77 GRN_NOISE_MARGIN (Green Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Green pixel noise margin setting register
1:0	--	Reserved to 0

Address: 78 BLU_NOISE_MARGIN (Blue Noise Margin Register)

Bit	Mode	Function
7:2	R/W	Blue pixel noise margin setting register
1	R/W	Auto phase result address write 0: CR-86 read only 1: CR-86 for result index
0	R/W	Auto phase result mode 0: old mode (default) 1: new mode

Address: 79 DIFF_THRESHOLD

Bit	Mode	Function
7:0	R/W	Difference Threshold (Threshold for DIFF no matter CR7D[2] = 0 or 1)

Address: 7A AUTO_ADJ_CTRL0 Default: 00h

Bit	Mode	Function
7	R/W	Field_Select_Enable: Auto-Function only active when Even or Odd field. 0: Disable (Default)

		1: Enable
6	R/W	Field_Select: Select Even or Odd field. Active when Field_Select_Enable . 0: Active when ODD signal is "0" (Default) 1: Active when ODD signal is "1"
5	R/W	Low Pass Filter (121-LPF) 0: Disable (Default) 1: Enable
4	R/W	Auto Function Acceleration : 0: Disable (Default) 1: Enable For auto-balance (CR7D[1]=0), this function must be disabled.
3:2	R/W	Vertical boundary search: 00: 1 pixel over threshold (Default) 01: 2 pixel over threshold 10: 4 pixel over threshold 11: 8 pixel over threshold
1:0	R/W	Color Source Select for Detection: 00: B color (Default) 01: G color 10: R color 11: ALL (the result will be divided by 2)

Address: 7B HW_AUTO_PHASE_CTRL0
Default: 00h

Bit	Mode	Function
7:3	R/W	Number of Auto-Phase Step (Valut+1) (How many times (steps reference CR7B[2:0]) jumps when using Hardware Auto)
2:0	R/W	Hardware Auto Phase Step 000: Step =1 (Default) 001 Step =2 010: Step =4 011: Step =8 1xx: Step =16

Address: 7C HW_AUTO_PHASE_CTRL1
Default: 00h

Bit	Mode	Function
7	R/W	Hardware Auto Phase Select Trigger 0: IVS 1: Vertical Boundary End
6:0	R/W	Initial phase of Auto-Phase (0~127)

Address: 7D AUTO_ADJ_CTRL1
Default: 00h

Bit	Mode	Function
7	R/W	Measure Digital Enable Info when boundary search active 0: Normal Boundary Search (Default) 1: Digital Enable Info Boundary Search.(Digital mode)
6	R/W	Hardware / Software Auto Phase Switch 0: Software (Default) 1: Hardware
5	R/W	Color Max or Min Measured Select: 0: MIN color measured (Only when Balance-Mode, result must be complemented) (Default) 1: MAX color measured
4	R/W	Accumulation or Compare Mode 0: Compare Mode (Default) 1: Accumulation Mode
3	R/W	Mode Selection For SOD 0: SOD Edge Mode (Default) 1: SOD Edge + Pulse Mode
2	R/W	Type Selection For DIFF 0: DIFF 1: (DIFF/4) * (DIFF/4)

		Total result for each color is divided by 8 if this bit is 1.
1	R/W	Function (Phase/Balance) Selection 0: Auto-Balance (Default) 1: Auto-Phase
0	R/W	Start Auto-Function Tracking Function: 0: stop or finished (Default) 1: start

Control Table/ Function	Sub-Function	CR7D.6	CR7D.5	CR7D.4	CR7D.3	CR7D.1	CR7C
Auto-Balance	Max pixel	X	1	0	0	0	X
	Min pixel	X	0	0	0	0	X
Auto-Phase Type	Mode1	1	1	1	0	1	Th
	Mode2	1	1	1	1	1	Th
Accumulation	All pixel	1	1	1	0	0	0

Table 1 Auto-Tracking Control Table

Address: 7E VER_START_END_H (Active region vertical start Register)

Bit	Mode	Function
7:4	R	Active region vertical START measurement result: bit[11:8]
3:0	R	Active region vertical END measurement result: bit[11:8]

Address: 7F VER_START_L (Active region vertical start Register)

Bit	Mode	Function
7:0	R	Active region vertical start measurement result: bit[7:0]

Address: 80 VER_END_L (Active region vertical end Register)

Bit	Mode	Function
7:0	R	Active region vertical end measurement result: bit[7:0]

Address: 81 H_START_END_H (Active region horizontal start Register)

Bit	Mode	Function
7:4	R	Active region horizontal START measurement result: bit [11:8]
3:0	R	Active region horizontal END measurement result: bit[11:8]

Address: 82 H_START_L (Active region horizontal start Register)

Bit	Mode	Function
7:0	R	Active region horizontal start measurement result: bit[7:0]

Address: 83 H_END_L (Active region horizontal end Register)

Bit	Mode	Function
7:0	R	Active region horizontal end measurement result: bit[7:0]

Address: 84 AUTO_PHASE_3 (Auto phase result byte3 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[31:24]

Address: 85 AUTO_PHASE_2 (Auto phase result byte2 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[23:16]

Address: 86 AUTO_PHASE_1 (Auto phase result byte1 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[15:8] When CR-78[1] set to 1, auto phase result read index 0~255 indicates for maximum 64 auto phase results (4 Bytes every result)

Address: 87 AUTO_PHASE_0 (Auto phase result byte0 register)

Bit	Mode	Function
7:0	R	Auto phase measurement result: bit[7:0] The measured value of R or G or B color max or min. (Auto-Balance) When CR-78[0] set to 1, read CR-87 continuously for auto phase results

- CR-87 can be read continuously for totally 256 Bytes (64 results).
 The multiple results, Address: 84~87, are stored in mcu's xdata space.

SOD Xdata space Range is set by SOD_DATA_LOCATION(0xFFEF[6:5]).
 Enable SOD Access Xram by SOD_ACCESS_DISABLE(0xFFE4[7]) .
 Xdata access method is suggested method.

- Set CR-78[1] and CR-86 for read index before read CR-87.
- Once CR-87 has been read 4 times, read index in CR-86 will increase automatically.

When input is 2560x1600, there will be three case for Register 0x84~0x87:

a. Only SOD + Pulse for RGB

$2560 \times 1600 \times 255 \times 2 \times 3 = 6266880000$ need 33 bits to indicate.

CR 84~87 will give bit [32:1].

b. $(SOD/4)^2 / 8 +$ Pulse for RGB

$2560 \times 1600 \times (255/4)^2 / 8 \times 2 \times 3 = 12484800000$ need 34 bits to indicate.

CR 84~87 will give bit [33:2]

c. $(SOD/4)^2 / 8 +$ Pulse only for one color

$2560 \times 1600 \times (255/4)^2 / 8 \times 2 = 4161600000$ need 32 bits to indicate.

CR 84~87 will give bit [31:0]

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Dithering Control (For Input Domain)

Register:: I_DITHERING_DATA_ACCESS					0x88
Name	Bits	Read/Write	Reset State	Comments	Config
DITHERING_DATA_ACCESS	7:0	W	0	Refer to following description	

A. When CR88[7:6] is 2'b01, dithering sequence table access is enabled:

- There are three set of dithering sequence table, each table contains 32 elements, s0, s1, ..., s31.
- Each element has 2 bit to index one of 4 dithering table.
- Input data sequence is {sr3,sr2,sr1,sr0}, {sr7,sr6,sr5,sr4}, ..., {sr31,sr30,sr29,sr28}, {sg3,sg2,sg1,sg0}, ..., {sg31,sg30,sg29,sg28}, {sb3,sb2,sb1,sb0}, ..., {sb31,sb30,sb29,sb28} for red, green and blue channel.
- R + (2R+1) * C choose sequence element, where R is Row Number / 2, and C is Column Number / 2.

B. When CR88[7:6] is 2'b10, dithering table access is enabled:

- For dithering table access, the red, green, blue each channel has 4 dithering table, each table is 2x2 elements, and one element has 4 bit for 10B/8B, the elements should fill 0 to 3, for 10B/6B, the elements should fill 0 to 15.
- Input data sequence is [Dr00 Dr01],[Dr02,Dr03], ..., [Dr30,Dr31],[Dr32,Dr33], [Dg00,Dg01],[Dg02,Dg03], ..., [Dg30,Dg31],[Dg32,Dg33], [Db00,Db01],[Db02,Db03], ..., [Db30,Db31],[Db32,Db33].

D00	D01	D10	D11	D20	D21	D30	D31
D02	D03	D12	D13	D22	D23	D32	D33

C. When CR88[7:6] is 2'b11, temporal offset access is enabled:

- There are 16 element for temporal offset table, t0, t1, ..., t15.
- Each element has 2 bit to index one of 4 temporal offset.
- Input data sequence is {t3,t2,t1,t0}, {t7,t6,t5,t4}, {t11,t10,t9,t8}, {t15,t14,t13,t12}.

Register:: I_DITHERING_CTRL1					0x89
Name	Bits	Read/Write	Reset State	Comments	Config
Dither_Access	7:6	W	0	Enable Access Control 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset	
Dither_en	5	R/W	0	Enable Dithering Function 0: disable (Default) 1: enable	
Dither_temp	4	R/W	0	Temporal Dithering 0: Disable (Default) 1: Enable	
Dither_table	3	R/W	0	Dithering Table Value Sign 0: unsigned 1: signed (2's complement)	
Dither_mode	2	R/W	0	Dithering Mode 0: New (Default) 1: Old	
Dither_V_Fram_M	1	R/W	0	Vertical Frame Modulation 0: Disable (Default) 1: Enable	
Dither_VH_Fram_M	0	R/W	0	Horizontal Frame Modulation 0: Disable (Default) 1: Enable	

Register:: I_DITHERING_CTRL2					0x8A
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	R/W	0	Reserved	
Reg_Dither_Test_en	1	R/W	0	Test_mode	

				0: Disable, dither_out = dither_result[9:2]; // truncate to integer number (Default) 1: Enable, dither_out = dither_result[7:0]; // propagate decimal part for test	
Dither_Table_Ref	0	R/W	1	Table reference 0: By VS/HS 1: By DEN (Default)	

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Global Control for LVDS

Register::: LVDS_ADDR_PORT					0x8B
Name	Bits	R/W	Default	Name	Config
LVDS_ADDR_PORT	7:0	R/W	0x0	Address port for embedded LVDS access	

Register::: LVDS_DATA_PORT					0x8C
Name	Bits	R/W	Default	Name	Config
LVDS_DATA_PORT	7:0	R/W	0x0	Data port for embedded LVDS access	

Register::: LVDS_CTRL15					0x 8C-00
Name	Bits	R/W	Default	Comments	Config
Reserved	7:2	--	--	Reserved	
DISP_TYPE	1:0	R/W	0x1	DISP_TYPE 00: TTL 01: LVDS (Default) 10: Hi-Z 11: mini-LVDS	

Register::: LVDS_CTRL16					0x 8C-01
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register::: LVDS_CTRL17					0x 8C-02
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register::: LVDS_CTRL18					0x 8C-03
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register::: LVDS_CTRL19					0x 8C-04
Name	Bits	R/W	Default	Comments	Config
LVDS_SLVDSIL	7:6	R/W	0x2	8 bit LVDS driver current option $I = ([1]*20\mu A + [0]*10\mu A + 50\mu A) * SL[2:0]$. See Table 1. 10 bit LVDS CR8C-04[7:6]、CR8C-04[5:4]、CR8C-04[3:2] must set the same	
LVDS_SLVDSECKIL	5:4	R/W	0x2	8 bit LVDS driver current option for Even port CLK $I = ([1]*20\mu A + [0]*10\mu A + 50\mu A) * SECKL[2:0]$. See Table 1. 10 bit LVDS CR8C-04[7:6]、CR8C-04[5:4]、CR8C-04[3:2] must set the same	
LVDS_SLVDSOCKIL	3:2	R/W	0x2	8 bit LVDS driver current option for Odd port CLK $I = ([1]*20\mu A + [0]*10\mu A + 50\mu A) * SOCKL[2:0]$. See Table 2 10 bit LVDS CR8C-04[7:6]、CR8C-04[5:4]、CR8C-04[3:2] must set the same	
LVDS_TYPE_SELL	1	R/W	0x1	0: Type A → ECK driver current for TXEC (Pin92、Pin93), OCK driver current for TXOC(Pin80、Pin81) ,Data driver current for (pin74~79、pin82、pin83、pin86~91、pin94、 pin95) 1: Type B → ECK driver current for TXEC (Pin88、 Pin89) , OCK driver current for TXOC (Pin76、 Pin77) ,Data driver current for (pin74、pin75、pin78~83、 pin86、pin87、pin90~95))	Type B 需修正

Reserved	0	--	--	Reserved	
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Register:: LVDS_CTRL20					0x 8C-05
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	R/W	--	Reserved	
LVDS_CK1X_DELAYL	5:4	R/W	0x00	Even/Odd port CK1X delay cell 00: ck1x 0 delay, 01: ck1x delay 3stages 10: ck1x delay 6stages 11: ck1x delay 9stage	
Reserved	3	R/W	0x0	Reserved	
LVDS_CKPHS	2	R/W	0x0	CK1X sample Data in the Analog interface 0: ck1x rising edge sample 1: ck1x falling edge sample	
LVDS_CK7X_DELAYL	1:0	R/W	0x0	Even/Odd port CK7X delay cell 00: ck7x 0 delay, 01: ck7x delay 3stages 10: ck7x delay 6stages 11: ck7x delay 9stage,	

Register:: LVDS_CTRL21					0x 8C-06
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved.	
LVDS_SL	5:3	R/W	0x6	8 bit LVDS driver current multiplier (See Table 1) 000 : x14 001 : x20 010 : x22 011 : x30 100 : x33 101 : x37 110 : x50 111 : x75 10 bit LVDS CR8C-06[5:3]、CR8C-06[2:0]、CR8C-07[5:3] must set the same	
LVDS_SECKL	2:0	R/W	0x6	8 bit LVDS driver current multiplier/ Even port CLK (See Table 1) 000 : x14 001 : x20 010 : x22 011 : x30 100 : x33 101 : x37 110 : x50 111 : x75 10 bit LVDS CR8C-06[5:3]、CR8C-06[2:0]、CR8C-07[5:3] must set the same	

Register:: LVDS_CTRL22					0x 8C-07
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved.	
LVDS_SOCKL	5:3	R/W	0x6	8 bit LVDS/LVDS driver current multiplier Odd port CLK (See Table 1) 000 : x14 001 : x20 010 : x22 011 : x30 100 : x33	

				101 : x37 110 : x50 111 : x75 10 bit LVDS CR8C-06[5:3]、CR8C-06[2:0]、CR8C-07[5:3] must set the same	
Reserved	2:0	--	--	Reserved.	

Register:: LVDS_CTRL23					0x 8C-08
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL24					0x 8C-09
Name	Bits	R/W	Default	Comments	Config
LVDS_ODALAGL	7:3	R/W	0x0	Select CK/Data align or lead T/N for even port (N= 12 for miniLVDSx6, 14 for LVDS, 16 for miniLVDSx8) 0: align 1: lead T/N 10000: (Pin74、Pin75) 01000: (Pin76、Pin77) 00100: (Pin78、Pin79) 00010: (Pin80、Pin81) 00001: (Pin82、Pin83)	
Reserved	2:0	--	--	Reserved to 0	

Register:: LVDS_CTRL25					0x 8C-0A
Name	Bits	R/W	Default	Comments	Config
LVDS_EDALAGL	7:1	R/W	0x0	Select CK/Data align or lead T/N for odd port (N= 12 for miniLVDSx6, 14 for LVDS, 16 for miniLVDSx8) 0: align 1: lead T/N 1000000: (Pin86、Pin87) 0100000: (Pin88、Pin89) 0010000: (Pin90、Pin91) 0001000: (Pin92、Pin93) 0000100: (Pin94、Pin95) 0000010: (Pin96、Pin97) 0000001: (Pin98、Pin99)	
Reserved	0	--	--	Reserved to 0	

Register:: LVDS_CTRL26					0x 8C-0B
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved to 0	
LVDS_PRE_SR_ENL	5	R/W	0x0	Enable /Disable pre-emphasis or slew rate control function 0: Disable 1: Enable	
LVDS_PRE_SR_SELL	4	R/W	0x0	Pre-emphasis/ Slew rate control selection 0: pre-emphasis 1: slew rate control	
LVDS_PRE_SR_SL	3:0	R/W	0	8bit LVDS pre-emphasis driving current multiplier for data port/ LVDS slew rate control for Even/Odd data port 0000: X4 0001: X8 0011: X12 0111: X16	

			1111: X20 Ref Table 2 10 bit LVDS CR8C-0B[3:0]、CR8C-0C[7:4]、CR8C-0C[3:0] must set the same	
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Register:: LVDS_CTRL27 0x 8C-0C					
Name	Bits	R/W	Default	Comments	Config
LVDS_PRE_SECKL	7:4	R/W	0x0	8bit LVDS pre-emphasis driving current multiplier for Even clock port /LVDS slew rate control 0000: X4 0001: X8 0011: X12 0111: X16 1111: X20 Ref Table 2 10 bit LVDS CR8C-0B[3:0]、CR8C-0C[7:4]、CR8C-0C[3:0] must set the same	
LVDS_PRE_SOCKL	3:0	R/W	0x0	8bit LVDS pre-emphasis driving current multiplier for Odd clock port/LVDS slew rate control 0000: X4 0001: X8 0011: X12 0111: X16 1111: X20 Ref Table 2 10 bit LVDS CR8C-0B[3:0]、CR8C-0C[7:4]、CR8C-0C[3:0] must set the same	

Register:: LVDS_CTRL28 0x 8C-0D					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	R/W	0x0	LVDS even port reserve pin	
LVDS_outcapEDAL	3:2	R/W	0x0	8 bit LVDS Even port data outcap : 00: Even port data output 0pF 01: Even port data output 1.62pF 10: Even port data output 3pF 11: Even port data output 4.62pF 10 bit LVDS CR8C-0D[3:2]、CR8C-0D[1:0]、CR8C-0E[3:2]、CR8C-0E[1:0] must set the same	
LVDS_outcapECKL	1:0	R/W	0x0	8 bit LVDS Even port clk outcap : 00: Even port clk output 0pF 01: Even port clk output 1.62pF 10: Even port clk output 3pF 11: Even port clk output 4.62pF 10 bit LVDS CR8C-0D[3:2]、CR8C-0D[1:0]、CR8C-0E[3:2]、CR8C-0E[1:0] must set the same	

Register:: LVDS_CTRL29 0x 8C-0E					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	R/W	0x0	LVDS odd port reserve pin	
LVDS_outcapODAL	3:2	R/W	0x0	8 bit LVDS Odd port data outcap : 00:Odd port data output 0pF 01:Odd port data output 1.62pF 10:Odd port data output 3pF 11:Odd port data output 4.62pF	

				10 bit LVDS CR8C-0D[3:2]、CR8C-0D[1:0]、CR8C-0E[3:2]、CR8C-0E[1:0] must set the same	
LVDS_outcapOCKL	1:0	R/W	0x0	8 bit LVDS Odd port clk outcap : 00: Odd port clk output 0pF 01: Odd port clk output 1.62pF 10: Odd port clk output 3pF 11: Odd port clk output 4.62pF 10 bit LVDS CR8C-0D[3:2]、CR8C-0D[1:0]、CR8C-0E[3:2]、CR8C-0E[1:0] must set the same	

Register::: LVDS_CTRL30 0x 8C-0F					
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_LVNL	7:6	R/W	0x2	Select LVDS P2S ratio 0X: 6X for miniLVDS 10: 7X for LVDS 11: 8X for miniLVDS	
LVDS_PLL_DIVOL	5	R/W	0x0	PLL Output divider 0:Div1 1:Div2	
LVDS_PLL_EPI_ENL	4	R/W	0x0	Enable/disable even port clk pair phase interpolation 0: Disable 1: Enable	
LVDS_PLL_OPI_ENL	3	R/W	0x0	Enable/disable odd port clk pair phase interpolation 0: Disable 1: Enable	
LVDS_PLL_DIVNL	2:1	R/W	0x2	Feedback Divider Ratio 0x: 6 10: 7 11: 8	
Reserved	0	--	--	Reserved	

Register::: LVDS_CTRL31 0x 8C-10					
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_RSL	7:5	R/W	0x3	PLL Loop Filter Resister Control 000:1.5K 001:2.3K 010:3.1K 011:3.8K 100:4.4K 101:6.0K 110:6.7K 111:7.4K	
LVDS_PLL_CSL	4:3	R/W	0x2	PLL Loop Filter Capacitor Control CS= 00:24p, 01:48p, 10:72p, 11:96p	
LVDS_PLL_CPL	2	R/W	0x0	CP Control 0:CP=1pF 1:CP=2pF	
LVDS_PLL_VSET_SEL	1:0	R/W	0x01	set VCO vc voltage 00:0.24V 01:0.48V 10:0.72V 11:0.96V	

Register::: LVDS_CTRL32 0x 8C-11					
Name	Bits	R/W	Default	Comments	Config

LVDS_PLL_IPL	7:5	R/W	0x02	PLL Charge Pump Current Control Icp=(2.5uA+2.5uA* [0]+5uA* [1]+10uA* [2])	
LVDS_PLL_SEL_FBKL	4:3	R/W	0x01	sel PFD input frequency 00: fref 01: fbk 10: 1.2V(Reserved) 11:1.2V(Reserved)	
Reserved	2	--	--	Reserved	
Reserved	1	--	--	Reserved	
LVDS_PLL_VCORSTBL	0	R/W	0x1	RESET VCO (active Low)	

Register:: LVDS_CTRL33					0x 8C-12
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_VCOMDL	7:6	R/W	0x3	PLL VCO Default band mode 00: VCO slowest, 11: VCO fastest	
LVDS_PLL_CALBPL	5	R/W	0x0	PLL bypass calibration(active high) 0: calibration 1: no calibration	
LVDS_PLL_CALSWL	4	R/W	0x0	calibration validated (go high after power on 1200us)	
LVDS_PLL_CALLCHL	3	R/W	0x0	latch calibration (go high after power on 1100us)	
LVDS_PLL_CMPENL	2	R/W	0x0	cmp enable (go high after power on 1000us)	
LVDS_PLL_VO2	1	R	0x0	DPLL CAL OUT2	
LVDS_PLL_VO1	0	R	0x0	DPLL CAL OUT1	

Register:: LVDS_CTRL34					0x 8C-13
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_CAL	7:6	R	0x0	DPLL calibrated VCO code	
Reserved	5	--	--	Reserved	
LVDS_PLL_RESERVED1L	4	R/W	0x0	LVDS PLL RESERVED	
LVDS_PLL_RESERVED	3:0	R/W	0x0	LVDS PLL RESERVED	

Register:: LVDS_CTRL35					0x 8C-14
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_SEL_PSCTRLVBPL	7:6	R/W	0x0	Select Phase interpolation bias option 00: Max, PI bias 11: Min, PI bias	
Reserved	5:4	--	--	Reserved	
LVDS_PLL_PSCTRREL[11:8]	3:0	R/W	0x0	LVDS even port clock phase selection. Ref.table 3	

Register:: LVDS_CTRL36					0x 8C-15
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_PSCTRREL[7:0]	7:0	R/W	30	LVDS even port clock phase selection. Ref. table 3	

Register:: LVDS_CTRL37					0x 8C-16
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	--	--	Reserved	
LVDS_PLL_PSCTRLOL[11:8]	3:0	R/W	0x0	LVDS odd port clock phase selection. Ref. table 3	

Register:: LVDS_CTRL38					0x 8C-17
Name	Bits	R/W	Default	Comments	Config
LVDS_PLL_PSCTRLOL[7:0]	7:0	R/W	30	LVDS odd port clock phase selection. Ref. table 3	

Register:: LVDS_CTRL39					0x 8C-18
Name	Bits	R/W	Default	Comments	Config

Reserved	7:0	--	--	Reserved.	
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Register:: LVDS_CTRL40					0x 8C-19
Name	Bits	R/W	Default	Comments	Config
LVDS_OSCKPHSL	7:3	R/W	0x08	Enable odd port phase selection 0: disable, use phase 0 1: enable, use LVDS_PLL_PSCTRREL 10000: (Pin74、Pin75) 01000: (Pin76、Pin77) 00100: (Pin78、Pin79) 00010: (Pin80、Pin81) 00001: (Pin82、Pin83)	
Reserved	2:0	--	--	Reserved to 0	

Register:: LVDS_CTRL41					0x 8C-1A
Name	Bits	R/W	Default	Comments	Config
LVDS_ESCKPHSL	7:1	R/W	0x20	Enable even port phase selection 0: disable, use phase 0 1: enable, use LVDS_PLL_PSCTRREL 1000000: (Pin86、Pin87) 0100000: (Pin88、Pin89) 0010000: (Pin90、Pin91) 0001000: (Pin92、Pin93) 0000100: (Pin94、Pin95) 0000010: (Pin96、Pin97) 0000001: (Pin98、Pin99)	
Reserved	0	-	-	Reserved to 0	

Table1

SLVDSIL[1:0]				
SL[2:0]	00	01	10	11
000(x14)	0.7mA	0.84mA	0.98mA	1.12mA
001(x20)	1.00mA	1.20mA	1.40mA	1.60mA
010(x22)	1.10mA	1.32mA	1.54mA	1.76mA
011(x30)	1.50mA	1.80mA	2.10mA	2.40mA
100(x33)	1.65mA	1.98mA	2.31mA	2.64mA
101(x37)	1.85mA	2.22mA	2.59mA	2.96mA
110(x50)	2.50mA	3.00mA	3.50mA	4.00mA
111(x75)	3.75mA	4.50mA	5.25mA	6.00mA

Table 2

SR control				
SLVDSIL[1:0]				
PRE_SR_SL[3:0]	00	01	10	11
0000(x 4)	-/+0.2mA	-/+0.24mA	-/+0.28mA	-/+0.32mA
0001(x 8)	-/+0.4mA	-/+0.48mA	-/+0.56mA	-/+0.64mA
0011(x12)	-/+0.6mA	-/+0.72mA	-/+0.84mA	-/+0.96mA
0111(x16)	-/+0.8mA	-/+0.96mA	-/+1.12mA	-/+1.28mA
1111(x20)	-/+1mA	-/+1.2mA	-/+1.4mA	-/+1.6mA
Pre-emphasis				
0000(x 4)	+/-0.2mA	+/-0.24mA	+/-0.28mA	+/-0.32mA

0001(x 8)	+/-0.4mA	+/-0.48mA	+/-0.56mA	+/-0.64mA
0011(x12)	+/-0.6mA	+/-0.72mA	+/-0.84mA	+/-0.96mA
0111(x16)	+/-0.8mA	+/-0.96mA	+/-1.12mA	+/-1.28mA
1111(x20)	+/-1mA	+/-1.2mA	+/-1.4mA	+/-1.6mA

Table 3

Phase	MSB[7:0]	LSB[3:0]
0	0000 0011	0000
	0000 0011	0001
	0000 0011	0011
	0000 0011	0111
4	0000 0110	1111
	0000 0110	1110
	0000 0110	1100
	0000 0110	1000
8	0000 1100	0000
	0000 1100	0001
	0000 1100	0011
	0000 1100	0111
12	0001 1000	1111
	0001 1000	1110
	0001 1000	1100
	0001 1000	1000
16	0011 0000	0000
	0011 0000	0001
	0011 0000	0011
	0011 0000	0111
20	0110 0000	1111
	0110 0000	1110
	0110 0000	1100
	0110 0000	1000
24	1100 0000	0000
	1100 0000	0001
	1100 0000	0011
	1100 0000	0111
28	1000 0001	1111
	1000 0001	1110
	1000 0001	1100
	1000 0001	1000

Register:: LVDS_CTRL42					0x 8C-1B
Name	Bits	R/W	Default	Comments	Config
LVDS_RoutEDAL	7:6	R/W	0x0	8 bit LVDS Even port data output resistor termination : 00: no termination(infinity ohm) 01: 168ohm 10: 250ohm 11: 492ohm 10 bit LVDS CR8C-1B[7:6]、CR8C-1B[5:4]、CR8C-1B[3:2]、CR8C-1B[1:0] must set the same	
LVDS_RoutODAL	5:4	R/W	0x0	8 bit LVDS Odd port data output resistor termination :	

				00: no termination(infinity ohm) 01: 168ohm 10: 250ohm 11: 492ohm 10 bit LVDS CR8C-1B[7:6]、CR8C-1B[5:4]、CR8C-1B[3:2]、CR8C-1B[1:0] must set the same	
LVDS_RoutECKL	3:2	R/W	0x0	8 bit LVDS Even port clk output resistor termination : 00: no termination(infinity ohm) 01: 168ohm 10: 250ohm 11: 492ohm 10 bit LVDS CR8C-1B[7:6]、CR8C-1B[5:4]、CR8C-1B[3:2]、CR8C-1B[1:0] must set the same	
LVDS_RoutOCKL	1:0	R/W	0x0	8 bit LVDS Odd port clk output resistor termination : 00: no termination(infinity ohm) 01: 168ohm 10: 250ohm 11: 492ohm 10 bit LVDS CR8C-1B[7:6]、CR8C-1B[5:4]、CR8C-1B[3:2]、CR8C-1B[1:0] must set the same	

Register:: LVDS_CTRL43					0x 8C-1C
Name	Bits	R/W	Default	Comments	Config
LVDS_pre_rEDAL	7:6	R/W	0x3	8bit LVDS Even port DATA pair First internal resistor. (Second resistor set is controlled by CR8C-24[4:3]): 00: 6.5 KΩ 01: 6 KΩ 10: 300 Ω 11: 290 Ω 10 bit LVDS CR8C-1C[7:6]、CR8C-1C[5:4]、CR8C-1C[3:2]、CR8C-1C[1:0] must set the same	
LVDS_pre_rODAL	5:4	R/W	0x3	8bit LVDS Odd port DATA pair First internal resistor. (Second resistor set is controlled by CR8C-25[4:3]): 00: 6.5 KΩ 01: 6 KΩ 10: 300 Ω 11: 290 Ω 10 bit LVDS CR8C-1C[7:6]、CR8C-1C[5:4]、CR8C-1C[3:2]、CR8C-1C[1:0] must set the same	
LVDS_pre_rECKL	3:2	R/W	0x3	8bit LVDS Even port CLK pair First internal resistor. (Second resistor set is controlled by CR8C-24[2:1]): 00: 6.5 KΩ 01: 6 KΩ 10: 300 Ω 11: 290 Ω 10 bit LVDS CR8C-1C[7:6]、CR8C-1C[5:4]、CR8C-1C[3:2]、CR8C-1C[1:0] must set the same	
LVDS_pre_rOCKL	1:0	R/W	0x3	8bit LVDS Odd port CLK pair First internal resistor. (Second resistor set is controlled by CR8C-25[2:1]): 00: 6.5 KΩ 01: 6 KΩ 10: 300 Ω 11: 290 Ω	

				10 bit LVDS CR8C-1C[7:6]、CR8C-1C[5:4]、CR8C-1C[3:2]、CR8C-1C[1:0] must set the same	
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Register:: MLVDS_CTRL2 0x 8C-1D				
Name	Bits	R/W	Default	Comments
Reserved	7:0	--	--	Reserved

Register:: LVDS_CTRL44 0x 8C-1E				
Name	Bits	R/W	Default	Comments
LVDS_CLK	7:0	R/W	0xE3	LVDS CLK timing (default : 11100011)

Register:: LVDS_CTRL45 0x 8C-1F				
Name	Bits	R/W	Default	Comments
LVDS_pswEL	7:6	R/W	0x1	Adjust Even Port output driver PMOS ratio 00: can't be used. 01: X12 10: X4 11: X16
LVDS_nswEL	5:4	R/W	0x1	Adjust Even Port output driver NMOS ratio 00: can't be used. 01: X4 10: X2 11: X6
LVDS_pswOL	3:2	R/W	0x1	Adjust Odd Port output driver PMOS ratio 00: can't be used. 01: X12 10: X4 11: X16
LVDS_nswOL	1:0	R/W	0x1	Adjust Odd Port output driver NMOS ratio 00: can't be used. 01: X4 10: X2 11: X6

TCLK+

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
TXE1	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
TXE2	EB3	EB2	DEN	VS	HS	EB5	EB4	EB3	EB2	DEN*6	VS*5
TXE3	ER7	ER6	RSV	EB7	EB6	EG7	EG6	ER7	ER6	RSV*7	EB7
TXO0	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5
TXO1	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
TXO2	OB3	OB2	DEN	VS	HS	OB5	OB4	OB3	OB2	DEN*2	VS*1
TXO3	OR7	OR6	RSV	OB7	OB6	OG7	OG6	OR7	OR6	RSV*3	OB7

TABLE 1 Bit-Mapping 6bit(5~0)+2bit(7~6)

TCLK+

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER3	ER2	EG2	ER7	ER6	ER5	ER4	ER3	ER2	EG2	ER7
TXE1	EG4	EG3	EB3	EB2	EG7	EG6	EG5	EG4	EG3	EB3	EB2

TXE2	EB5	EB4	DEN	VS	HS	EB7	EB6	EB5	EB4	DEN*6	VS*5
TXE3	ER1	ER0	RSV	EB1	EB0	EG1	EG0	ER1	ER0	RSV*7	EB1
TXO0	OR3	OR2	OG2	OR7	OR6	OR5	OR4	OR3	OR2	OG2	OR7
TXO1	OG4	OG3	OB3	OB2	OG7	OG6	OG5	OG4	OG3	OB3	OB2
TXO2	OB5	OB4	DEN	VS	HS	OB7	OB6	OB5	OB4	DEN*2	VS*1
TXO3	OR1	OR0	RSV	OB1	OB0	OG1	OG0	OR1	OR0	RSV*3	OB1

TABLE 2 Bit-Mapping 6bit(7~2)+2bit(1~0)

TCLK+

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER5	ER4	EG4	ER9	ER8	ER7	ER6	ER5	ER4	EG4	ER9
TXE1	EG6	EG5	EB5	EB4	EG9	EG8	EG7	EG6	EG5	EB5	EB4
TXE2	EB7	EB6	DEN	VS	HS	EB9	EB8	EB7	EB6	DEN	VS
TXE3	ER3	ER2	RSV	EB3	EB2	EG3	EG2	ER3	ER2	RSV	EB3
TXE4	ER1	ER0	RSV	EB1	EB0	EG1	EG0	ER1	ER0	RSV	EB1
TXO0	OR5	OR4	OG4	OR9	OR8	OR7	OR6	OR5	OR4	OG4	OR9
TXO1	OG6	OG5	OB5	OB4	OG9	OG8	OG7	OG6	OG5	OB5	OB4
TXO2	OB7	OB6	DEN	VS	HS	OB9	OB8	OB7	OB6	DEN	VS
TXO3	OR3	OR2	OSV	OB3	OB2	OG3	OG2	OR3	OR2	OSV	OB3
TXO4	OR1	OR0	OSV	OB1	OB0	OG1	OG0	OR1	OR0	OSV	OB1

TABLE 3 Bit-Mapping 6bit(9~4)+2bit(3~2) +2bit(1~0)

TCLK+

LVDS	Bit 1	Bit 0	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 6	Bit 5
TXE0	ER1	ER0	EG0	ER5	ER4	ER3	ER2	ER1	ER0	EG0	ER5
TXE1	EG2	EG1	EB1	EB0	EG5	EG4	EG3	EG2	EG1	EB1	EB0
TXE2	EB3	EB2	DEN	VS	HS	EB5	EB4	EB3	EB2	DEN	VS
TXE3	ER7	ER6	RSV	EB7	EB6	EG7	EG6	ER7	ER6	RSV	EB7
TXE4	ER9	ER8	RSV	EB9	EB8	EG9	EG8	ER9	ER8	RSV	EB9
TXO0	OR1	OR0	OG0	OR5	OR4	OR3	OR2	OR1	OR0	OG0	OR5
TXO1	OG2	OG1	OB1	OB0	OG5	OG4	OG3	OG2	OG1	OB1	OB0
TXO2	OB3	OB2	DEN	VS	HS	OB5	OB4	OB3	OB2	DEN	VS
TXO3	OR7	OR6	RSV	OB7	OB6	OG7	OG6	OR7	OR6	RSV	OB7
TXO4	OR9	OR8	RSV	OB9	OB8	OB9	OG8	OR9	OR8	RSV	OB9

TABLE 4 Bit-Mapping 6bit(5~0)+2bit(7~6) +2bit(9~8)

Register::: DIS_FORMAT1				0x 8C-20								
Name	Bits	R/W	Default	Comments								Config
Reserved	7:5	--	--	Reserved								
ADC_mLVDS_RAM	4	R/W	0x00	SRAM for 0:ADC Noise Reduction 1:mLVDS								
D_SRAM_BIST_EN	3	R/W	0x0	Dual3 SRAM BIST enable 0:Disable 1:Enable								
D_SRAM_BIST_DONE	2	R	0x0	Dual3 SRAM BIST Test Finished 0:Running 1:Done								
D_SRAM_BIST_FAIL	1	R	0x0	Dual3 SRAM BIST Test fail flag 0:Ok 1:Failed								
DISP_CONV_TEST_SEL	0	R/W	0x0									

Register::: LVDS_CTRL46				0x 8C-21							

Name	Bits	R/W	Default	Comments	Config
reg_ft_mode	7	R/W	0	1: FT test mode, force EE, OE pair output data to verify LVDS analog 0: normal function	
LVDS_Reserved01	6:2	R/W	0x00	Reserved	
Disp_conv_test_sel2	1	R/W	0x0	Switch test pins of disp_conv 0: [29:0] data_flip: R_cnt[7:0], W_cnt[7:0], Even_line Mem_csb, Mem_web, Disp_ena_stuff_r, R_equal_half, R_region, Flip_ena_pre_nostuff, Stuff, Stuff_en, Flip_en, Flip_half_inv, Equal_half, R_select_front, Latch_mem_data 1: [29:17] adjacent_pixel Polen_d, Polen, Polen_int_ro, Polen_int Accu_cnt[3:0], Sum, Result1, Result2, Result3. [16:0]: mlvds_remapping W_end, W_RST, W_count_up, Bypass_cnt[2:0], Bypass_region, Bypass_region_end, R_b_RST, R_region_b, R_cnt_b[5:0], Remmapping_ena_pre	
Disp_conv_test_sel3	0	R/W	0x0	0: select 0x8C-20[0] test output 1: select 0x8C-21[1] test output	

Register:: LVDS_CTRL47 0x 8C-22					
Name	Bits	R/W	Default	Comments	Config
LVDS_Reserved02	7:0	R/W	0x00	Reserved	

Register:: LVDS_CTRL48 0x 8C-23					
Name	Bits	R/W	Default	Comments	Config
LVDS_RESL	7:0	R/W	0xFF	Analog Reserved LVDS_RESL[7:0]= reserved pins	

Register:: LVDS_CTRL49 0x 8C-24					
Name	Bits	R/W	Default	Comments	Config
LVDS_RESVREL	7:5	R/W	0x00	Analog Reserved	

				Even port reserved pin	
LVDS_RESVREL[4:3]	4:3	R/W	0x00	8bit LVDS Even port DATA pair Second internal resistor. (First resistor set is controlled by CR8C-1C[7:6]): 00: 290 Ω 01: 300 Ω 10: 6 KΩ 11: 6.5 KΩ 10 bit LVDS CR8C-24[4:3]、CR8C-24[2:1]、CR8C-25[4:3]、CR8C-25[2:1] must set the same	
LVDS_RESVREL[2:1]	2:1	R/W	0x00	8bit LVDS Even port CLK pair Second internal resistor. (First resistor set is controlled by CR8C-1C[3:2]): 00: 290 Ω 01: 300 Ω 10: 6 KΩ 11: 6.5 KΩ 10 bit LVDS CR8C-24[4:3]、CR8C-24[2:1]、CR8C-25[4:3]、CR8C-25[2:1] must set the same	
LVDS_RESVREL[0]	0	R/W	0	ck7xsel: Even port P2S's ck7x polarity selection 0: ck7x inverted 1: ck7x non-inverted	

Register:: LVDS_CTRL50					0x 8C-25
Name	Bits	R/W	Default	Comments	Config
LVDS_RESVROL	7:5	-- R/W	-- 0x00	Analog Reserved Odd port reserved pin	
LVDS_RESVROL[4:3]	4:3	R/W	0x00	8bit LVDS Odd port DATA pair Second internal resistor. (First resistor set is controlled by CR8C-1C[5:4]): 00: 290 Ω 01: 300 Ω 10: 6 KΩ 11: 6.5 KΩ 10 bit LVDS CR8C-24[4:3]、CR8C-24[2:1]、CR8C-25[4:3]、CR8C-25[2:1] must set the same	
LVDS_RESVROL[2:1]	2:1	R/W	0x00	8bit LVDS Odd port CLK pair Second internal resistor. (First resistor set is controlled by CR8C-1C[1:0]): 00: 290 Ω 01: 300 Ω 10: 6 KΩ 11: 6.5 KΩ 10 bit LVDS CR8C-24[4:3]、CR8C-24[2:1]、CR8C-25[4:3]、CR8C-25[2:1] must set the same	
LVDS_RESVROL[0]	0	R/W	0	ck7xsel: Odd port P2S's ck7x polarity selection 0: ck7x inverted 1: ck7x non-inverted	

Control for LVDS

Register:: LVDS_CTRL0					0x 8C-A0
Name	Bits	R/W	Default	Comments	Config
LVDS_IBPOWL	7	R/W	0x0	Power Up LVDS IBGEN 0: Power down (Default)	

				1: Normal	
LVDS_E2LVDSPOWL	6	R/W	0x0	Power Up mLVDS/LVDS pin96~99 0: Power down (Default) 1: Normal	
LVDS_ELVDSPOWL	5	R/W	0x0	Power Up mLVDS/LVDS pin86~95 0: Power down (Default) 1: Normal	
LVDS_OLVDSPOWL	4	R/W	0x0	Power Up mLVDS/LVDS pin74~83 0: Power down (Default) 1: Normal	
LVDS_PLL_WDRSTL	3	R/W	0x0	DPLL WD Reset 0: Normal 1: Reset	
LVDS_PLL_WDSETL	2	R/W	0x0	DPLL WD Set 0: Normal 1: Set	
LVDS_bit_Type	1	R/W	0x0	LVDS bit type 0: 8 bits 1: 10 bits	
LVDS_PLL_WDO	0	R	0x0	mLVDS Watch Dog 0: Normal 1: Abnormal	

Register:: LVDS_CTRL1					0x 8C-A1
Name	Bits	R/W	Default	Comments	Config
Reserved	7	--	--	Reserved	
LVDS_SVOXML[3]	6	R/W	0x0	VOCM option[3]	
LVDS_STSTIL	5:3	R/W	0x2	TSTPAD output control 000 : PLL_WDO 001 : VOCM 010 : IB40U 011 : IBVOCM 100 : PLLTST-fin 101 : PLLTST-fbak 110 : LVTST-LVDSIN[6] 111 : LVTST-CKDIN	
LVDS_SVOXML[2:0]	2:0	R/W	0x4	VOCM option[2:0] VCM option set by (8C-A1[6]+8C-A1[2:0]) 0000 : 1.07v 0001 : 1.12v 0010 : 1.17v 0011 : 1.22v 0100 : 1.29v 0101 : 1.33v 0110 : 1.38v 0111 : 1.43v 1000 : 0.5v 1001 : 0.55v 1010 : 0.6v 1011 : 0.65v 1100 : 0.7v 1101 : 0.75v 1110 : 0.8v 1111 : 0.85v	

Register:: LVDS_CTRL2					0x 8C-A2
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	--	Reserved	
LVDS_ENIB40UX2L	5	R/W	0x0	ENIB40UX2L: Double the mLVDS/LVDS output swing 0: 1X	

				1: 2X	
LVDS_SIBXL	4	R/W	0x1	SIBXL: Select the LVDS/mini LVDS driving/vocom biasing current source 0: From ADC internal bandgap 1: From GDI refer to external resistor	
LVDS_PLL_POLAR	3	R/W	0x0	The phase of clock when PLL latch data 0: Postive 1: Negative	
LVDS_SIBGENL	2:0	R/W	0x3	SIBGENL (mLVDS/LVDS Current Source correction) 40u: mLVDS driving current, 100u: mLVDS VOCM(default) 000 : 25uA/62.5uA 001 : 30uA/75uA 010 : 35uA/87.5uA 011 : 40uA/100uA (Default) 100 : 45uA/112.5uA 101 : 50uA/125uA 110 : 55uA/137.5uA 111 : 60uA/150uA	

Register::: LVDS_CTRL3 0x 8C-A3					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	--	--	Reserved	
LVDS_MIRROR	6	R/W	0x0	LVDS Mirror For 8 bit : 0: Normal (TXE3+, TXE3-, TXEC+, TXEC-, TXE2+, TXE2-, TXE1+, TXE1-, TXE0+, TXE0-, TXO3+, TXO3-, TXOC+, TXOC-, TXO2+, TXO2-, TXO1+, TXO1-, TXO0+, TXO0-) 1: Mirror (TXE0-, TXE0+, TXE1-, TXE1+, TXE2-, TXE2+, TXEC-, TXEC+, TXE3-, TXE3+, TXO0-, TXO0+, TXO1-, TXO1+, TXO2-, TXO2+, TXOC-, TXOC+, TXO3-, TXO3+) For 10 bit : 0: Normal (TXE4+, TXE4-, TXE3+, TXE3-, TXEC+, TXEC-, TXE2+, TXE2-, TXE1+, TXE1-, TXE0+, TXE0-, TXO4+, TXO4-, TXO3+, TXO3-, TXOC+, TXOC-, TXO2+, TXO2-, TXO1+, TXO1-, TXO0+, TXO0-) 1: Mirror (TXE0-, TXE0+, TXE1-, TXE1+, TXE2-, TXE2+, TXEC-, TXEC+, TXE3-, TXE3+, TXO4+, TXO4-, TXO0-, TXO0+, TXO1-, TXO1+, TXO2-, TXO2+, TXOC-, TXOC+, TXO3-, TXO3+, TXO4-, TXO4+)	
Reserved	5:1	--	--	Reserved	
LVDS_BMTS	0	R/W	0x0	BMTS: Bit-Mapping Table Select 0: Table 1 for 8bit LVDS / Table 3 for 10bit LVDS (Default) 1: Table 2 for 8bit LVDS / Table 4 for 10bit LVDS	

Register::: LVDS_CTRL4 0x 8C-A4					
Name	Bits	R/W	Default	Comments	Config
LVDS_RSV0_E	7:6	R/W	0x2	E_RSV0: even port reserve signal select 11: Always '1' 10: Always '0' 01: TCON [11] 00: PWM_0	
LVDS_DEN_E	5:4	R/W	0x0	E_DEN: even port data enable signal select 11: Always '1' 10: Always '0' 01: TCON [9] 00: DENA	
LVDS_VS_E	3:2	R/W	0x0	E_VS: even port VS signal select 11: Always '1' 10: DENA 01: TCON [7]	

				00: DVS	
LVDS_HS_E	1:0	R/W	0x0	E_HS: even port HS signal select 11: Always '1' 10: DENA 01: TCON [5] 00: DHS	

Register:: LVDS_CTRL5 0x 8C-A5					
Name	Bits	R/W	Default	Comments	Config
LVDS_RSV0_O	7:6	R/W	0x2	O_RSV0: odd port reserve signal select 11: Always '1' 10: Always '0' 01: TCON [13] 00: PWM_1	
LVDS_DEN_O	5:4	R/W	0x0	O_DEN: odd port data enable signal select 11: Always '1' 10: Always '0' 01: TCON [9] 00: DENA	
LVDS_VS_O	3:2	R/W	0x0	O_VS: odd port VS signal select 11: Always '1' 10: DENA 01: TCON [7] 00: DVS	
LVDS_HS_O	1:0	R/W	0x0	O_HS: odd port HS signal select 11: Always '1' 10:DENA 01: TCON [5] 00: DHS	

Register:: LVDS_CTRL6 0x 8C-A6					
Name	Bits	R/W	Default	Comments	Config
PN_SWAP	7	R/W	0x0	mLVDS/LVDS Differential pair PN swap (data) (Also refer to CR50[2:0]) 0: No Swap (Default) 1: Swap	
Reserved	6	R/W	--	Reserved	
LVDS_RSV0_E_CTRL	5:4	R/W	0x0	E_rsv0_ctrl: even port reserve signal select reference to 0x8C-A6[1]: 11: field 10: L/R signal, 1=L 01: L/R signal, 0=L 00: Normal (8C-A4[7:6])	
LVDS_RSV0_O_CTRL	3:2	R/W	0x0	O_rsv0_ctrl: odd port reserve signal select reference to 0x8C-A6[1]: 11: field 10: L/R signal, 1=L 01: L/R signal, 0=L 00: Normal (8C-A5[7:6])	
LR_signal_ref	1	R/W	0	L/R signal reference 0:DVS(bypass) 1:TCON[2]	
LVDS_PLL_POWL	0	R/W	0x0	Power Up mLVDS/LVDS PLL 0: Power down (Default) 1: Normal	

Register:: LVDS_CTRL7 0x 8C-A7					
Name	Bits	R/W	Default	Comments	Config
LVDS_RSV1_E	7:6	R/W	0x2	E_RSV1: even port reserve signal select	

				11: Always '1' 10: Always '0' (Default) 01: TCON [3] 00: PWM_2 Effectively only if CR8C-A0[1]=1'b1 (10 bit LVDS)	
LVDS_RSV1_O	5:4	R/W	0x2	O_RSV1: odd port reserve signal select 11: Always '1' 10: Always '0' (Default) 01: TCON [1] 00: PWM_3 Effectively only if CR8C-A0[1]=1'b1 (10 bit LVDS)	
Reserved	3:0	R/W	--	Reserved	

Register:: LVDS_CTRL8 0x 8C-A8					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL9 0x 8C-A9					Config
Name	Bits	R/W	Default	Comments	Config
LVDS_pulldown_2L	7	— R/W	— 0x1	LVDS pin96~pin99 weak pull Down 0: disable 1: enable (Auto Pull Down When POR Occur) Effective when 10 bit LVDS	
LVDS_pulldown_EL	6	R/W	0x1	LVDS pin86~pin95 weak pull Down 0: disable 1: enable (Auto Pull Down When POR Occur) Effective when 8/10 bit LVDS dual port output and single port output	
LVDS_pulldown_DL	5	R/W	0x1	LVDS pin74~pin83 weak pull Down 0: disable 1: enable (Auto Pull Down When POR Occur) Effective when 8/10 bit LVDS dual port output	
Reserved	4:0	--	--	Reserved	

Register:: LVDS_CTRL10 0x 8C-AA					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL11 0x 8C-AB					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL12 0x 8C-AC					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL13 0x 8C-AD					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Register:: LVDS_CTRL14 0x 8C-AE					Config
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	--	--	Reserved	

Reserved	7:0	--	--	Reserved		
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Address:8C-AF~8C-FF reserved

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Test function

Register::Pin_config_Addr_Port						0x8D
Name	Bit	R/W	Default	Description		Config
Pin_config_Addr_Port	7:0	R/W	00	Address port for pin configuration control access		

Register::Pin_config_Data_Port						0x8E
Name	Bit	R/W	Default	Description		Config
Pin_config_Data_Port	7:0	R/W	00	Data port for pin configuration control access		

Pin 55	TCON[0]	TCON[5]	
Pin 56	TCON[1]	TCON[4]	
Pin 57	TCON[9]	TCON[11]	
Pin 58	TCON[7]	TCON[10]	
Pin 59	TCON[3]	TCON[5]	
Pin 63	TCON[1]	TCON[8]	
Pin 64	TCON[0]	TCON[7]	
Pin 65	TCON[1]	TCON[7]	
Pin 66	TCON[2]	TCON[4]	
Pin 67	TCON[5]	TCON[9]	
Pin 68	TCON[3]	TCON[13]	
Pin 69	TCON[3]	TCON[7]	
Pin 70	TCON[9]	TCON[11]	
Pin 71	TCON[8]	TCON[10]	
Pin 72	TCON[6]	TCON[12]	
Pin 99	TCON[6]	TCON[11]	
Pin 100	TCON[3]	TCON[12]	
Pin 101	TCON[0]		
Pin 102	TCON[10]		
Pin 103	TCON[8]		
Pin 104	TCON[5]		
Pin 105	TCON[9]		
Pin 108	TCON[7]		
Pin 109	TCON[3]		
Pin 110	TCON[2]	TCON[6]	TCON[7]
Pin 111	TCON[4]	TCON[7]	
Pin 112	TCON[5]	TCON[9]	
Pin 113	TCON[1]	TCON[11]	
Pin 114	TCON[0]	TCON[13]	

Name	8D-00[7] = 1'b0	8D-00[7] = 1'b1	PLL clock	scan	72pin	128pin
PAD_GPIO119				scan_mode	62	119
PAD_TXO3P			audio_pll	si[0]	37	74
PAD_TXO3N				si[1]	38	75
PAD_TXO2P	tst[0]	tst[0]	ck108_pll27x	si[2]	39	78
PAD_TXO2N	tst[1]	tst[1]		si[3]	40	79
PAD_TXO1P	tst[2]	tst[16]		fav4	si[4]	41
PAD_TXO1N	tst[3]	tst[17]			si[5]	42
PAD_TXOOP	tst[4]	tst[18]			si[6]	43
						81
						82

			xclk			
PAD_TXO0N	tst[5]	tst[19]		si[7]	44	83
PAD_TXE3P	tst[6]	tst[20]	dpll	so[0]	45	86
PAD_TXE3N	tst[7]	tst[21]		so[1]	46	87
PAD_TXECP	tst[8]	tst[22]	test2out	so[2]	47	88
PAD_TXECN	tst[9]	tst[23]		so[3]	48	89
PAD_TXE2P	tst[10]	tst[24]	dpll_status	so[4]	49	90
PAD_TXE2N	tst[11]	tst[25]		so[5]	50	91
PAD_TXE1P	tst[12]	tst[26]	test1out	so[6]	51	92
PAD_TXE1N	tst[13]	tst[27]		so[7]	52	93
PAD_TXE0P	tst[14]	tst[28]	m2pll		53	94
PAD_TXE0N	tst[15]	tst[29]			54	95
PAD_TCON0				scan_en		64
PAD_GPIO63				scan_clk		63

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RTD2486VTD

72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
71	1	TMDS_VDD				
72	2	PAD_RXEXT				
1	3	PAD_RX2P0				
2	4	PAD_RX2N0				
3	5	PAD_RX1P0				
4	6	PAD_RX1N0				
5	7	PAD_RX0P0				
6	8	PAD_RX0N0				
7	9	PAD_RXCP0				
8	10	PAD_RXCN0				
	11	TMDS_GND				
	12	PAD_RX2P1				
	13	PAD_RX2N1				
	14	PAD_RX1P1				
	15	PAD_RX1N1				
	16	PAD_RX0P1				
	17	PAD_RX0N1				
	18	PAD_RXCP1				
	19	PAD_RXCN1				
	20	TMDS_VDD				
9	21	PAD_AVSO			AVS_I	
10	22	PAD_AHS0			AHS_I	
11	23	ADC_VDD12_GDI				
11	23	ADC_VDD12				
12	24	PAD_BIN0N				
13	25	PAD_BIN0P				
14	26	PAD_GIN0N				
15	27	PAD_GIN0P				
	28	PAD_SOGIN0				
16	29	PAD_RIN0N				
17	30	PAD_RIN0P				
	31	PAD_BIN1N	PD.7		V8[7]_I	
	32	PAD_32	PD.6		V8[6]_I	
	33	PAD_33	PD.5		V8[5]_I	
	34	PAD_34	PD.4		V8[4]_I	
	35	PAD_35	PD.3		V8[3]_I	
	36	PAD_36	PD.2		V8[2]_I	
	37	PAD_37	PD.1	si[0]	V8[1]_I	
18	38	ADC_GND12		si[1]		
18	38	ADC_GNDOFF				
18	38	ADC_AUD_GNDOFF				
18	38	Audio_ADC_GND				
19	39	PAD_39	PD.0	si[2]	V8[0]_I	
20	40	PAD_40	PC.4	si[3]		
	41	PAD_VIN0P	PB.7	si[4]		
	42	PAD_VIN0N	PB.6	si[5]		
	43	PAD_VIN1P	PB.5	si[6]		
	44	PAD_VIN1N	PB.4	si[7]		
	45	PAD_VIN2P	PB.3	so[0]		
	46	PAD_VIN2N	PB.2	so[1]		
	47	PAD_VIN3P	PB.1	so[2]		
	48	PAD_VIN3N	PB.0	so[3]		
	49	AVDD_SARADC_APAD		so[4]		
	49	AVDD_BB0_APAD				
	49	AVDD_BB1_DACVREF_APAD				
21	50	PAD_ADCA0	P6.0	so[5]		
22	51	PAD_ADCA1	P6.1	so[6]		
23	52	PAD_ADCA2	P6.2	so[7]		
24	53	PAD_ADCA3	P6.3			
	54	PAD_ADCA4	P6.4			
25	55	PAD_ADCB0	P6.5	DCLK_I		
26	56	PAD_ADCB1	P6.6	ADC_CLK_I		
27	57	PAD_ADCB2	P6.7	M2PLL_CLK_I		
28	58	PAD_DDCSCL1	P3.0/RXD(I/O)	HDMI_CP_ACLK_I		
72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
29	59	PAD_DDCSDA1	P3.1/TXD(O)	10C	HDMI_CP_CLK_I	
30	60	PAD_VCK				
	61	PAD_GND				
31	62	PAD_PVCC		scan_mode		



72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
29	59	PAD_DDCSDA1	P3.1/TXD(O)		HDMI_CP_CLK_I	
30	60	PAD_VCCK				
	61	PAD_GND				
31	62	PAD_PVCC		scan_mode		
32	63	PAD_GPIO63	PC.3 /INT0(I)	scan_clk		
33	64	PAD_TCON0	P1.0/T2(I) /INT1(I)	scan_en		clk_pll27x
34	65	PAD_TCON1	P1.1/T2EX(I)			
35	66	PAD_TCON2	P1.2/CLKO2(O)			
36	67	PAD_TCON5	P1.3			
	68	PAD_TCON13	P1.4			
	69	PAD_TCON3	P1.5			
	70	PAD_TCON9	P1.6			
	71	PAD_TCON8	P1.7			
	72	PAD_TCON6	PC.2			
	73	PAD_VCCK				
37	74	PAD_TXO3P	P9.0			audio_pll
38	75	PAD_TXO3N	P9.1			
	76	PAD_TXOCP	P9.2			
	77	PAD_TXOCN	P9.3			
39	78	PAD_TXO2P	P9.4		Test_IO[0]	ck108_pll27x
40	79	PAD_TXO2N	PA.0		Test_IO[1]	
41	80	PAD_TXO1P	PA.1		Test_IO[2]	fav4
42	81	PAD_TXO1N	PA.2		Test_IO[3]	
43	82	PAD_TXO0P	PA.3		Test_IO[4]	xclk
44	83	PAD_TXO0N	PA.4		Test_IO[5]	
	84	PAD_PVCC				
	85	PAD_PGND				
45	86	PAD_TXE3P			Test_IO[6]	dpll
46	87	PAD_TXE3N			Test_IO[7]	
47	88	PAD_TXECP			Test_IO[8]	test2out
48	89	PAD_TXEYN			Test_IO[9]	
49	90	PAD_TXE2P			Test_IO[10]	dpll_status
50	91	PAD_TXE2N			Test_IO[11]	
51	92	PAD_TXE1P			Test_IO[12]	test1out
52	93	PAD_TXE1N			Test_IO[13]	
53	94	PAD_TXE0P			Test_IO[14]	m2pll
54	95	PAD_TXE0N			Test_IO[15]	
	96	PAD_PWM0	P5.2		Test_IO[16]	
	97	PAD_PWM1	P5.3		Test_IO[17]	
	98	PAD_PWM2	P5.4		Test_IO[18]	
	99	PAD_PWM3	P5.5		Test_IO[19]	
	100	PAD_PWM4	P5.6		Test_IO[20]	
	101	PAD_PWM5	P5.7		Test_IO[21]	
	102	PAD_SPDIF3	P7.6		Test_IO[22]	
55	103	PAD_SPDIF2	P7.5		Test_IO[23]	
56	104	PAD_SPDIF1	P7.4		Test_IO[24]	
	105	PAD_SPDIF0	P8.0		Test_IO[25]	
57	106	PAD_PVCC				
	107	PAD_PGND				
	108	PAD_MCK	P8.1/CLKO1(O)		Test_IO[26]	
	109	PAD_SCK	P3.2/INT0(I)		Test_IO[27]	
	110	PAD_WS	P3.3/INT1(I)		Test_IO[28]	
	111	PAD_SD0	P3.4/T0		Test_IO[29]	
	112	PAD_SD1	P3.5(BS)/T1			
	113	PAD_SD2	P3.6			
	114	PAD_SD3	P3.7			
58	115	PAD_SPI_SCLK				
59	116	PAD_SI				
60	117	PAD_SO				
61	118	PAD_CS				
62	119	PAD_GPIO119	PC.1			
63	120	PAD_VCCK				

72 pin	128 pin		GPIO	Scan	Test Mode	Clock Out
63	120	PAD_VCCK				
64	121	PAD_DDCSCL3	P7.3			
65	122	PAD_DDCSDA3	P7.2			
66	123	PAD_DDCSDA2	P7.1		ISP_DDCSCL	
67	124	PAD_DDCSCL2	P7.0		ISP_DDCSDA	
68	125	PAD_RESETB				
	126	PAD_126	PC.0			
69	127	PAD_XO				
70	128	PAD_XI				

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Register::TEST_MODE						0x00
Name	Bit	R/W	Default	Description	Config	
Select_data_test_mode	7	R/W	0	<p>Select Data Test mode LSB</p> <p>A. for 72 pin, pin54~45, 44~39</p> <p>0 : select Data test mode [15:0] 1: select Data test mode [29:16],[1:0]</p> <p>B. for 128 pin, pin95~86, 83~78</p> <p>0 : select Data test mode [15:0] 1 : select Data test mode [29:16],[1:0]</p> <p>pin 111~108, 105~96 is Data test mode [29:16]</p>		
Test mode select	6:5	R/W	00	00:Normal 01:test_output mode Others are Reserved		
Test_output_Mode	4	R/W	0	<p>0:Select Data test mode Select Data test output to 128pin 95~86, 83~78 or 64pin 49~40, 38~33 depend on bit7, bit3~bit0</p> <p>1:PLL test mode {dpll, m2pll,audio_pll, tie to GND , IOSC, mppll, dpllstatus,test1out, test2out, fav4, xclk, dpll(digital pad)} will be outputted to 128 pin {86, 94, 74, X, 64, 78, 90, 92, 88, 80, 82, 126} or 64 pin {40, 48, 31, X, 30, 33, 44, 46, 42, 35, 37} when set to 1, clock frequency of some test pin could be divided by assigning its corresponding TST_CLK_CTRL</p>		
Data_Test_mode	3:0	R/W	0	<p>0000: 1'b0, Z0TST[3:0], pclk_tst, Red[7:0], Green[7:0], Blue[7:0] through VGIP</p> <p>0001: 1'b0, Z0TST[3:0], adc_clk, Red[7:0], Green[7:0], Blue[7:0] After Scale Down</p> <p>0010: Z0TST[3:0], adc_clk, IVS_DLY, IHS_DLY, IFD_ODD, IENA, VSD_DEN, VSD_ACT,Auto_hs, Auto_vs, auto_field, 1'b0, COAST, test_s1, test_s2, CLAMP_G, CLAMP_BR, SOG_IN0, SOG_IN1, FAV4,final_pe_com, t_s[1:0], pe_extrab, high_88, recur_delay_chain_en, high_127</p> <p>0011: adc_clk, MCUWR, MCURD, MCU_ADR_INC, MIN[7:0], MCUWR, MCURD, MADR[7:0], MPLL_SDMOUT_TST[3:0], SDMOUT_TST[3:0]</p> <p>0100: 1'b0, adc_clk, RAW_VS, RAW_HS, RAW_ODD, RAW_DEN, SDMOUT_TST[3:0], Green[9:0], Red[9:0] through VGIP</p> <p>0101: 1'b0, adc_clk, Red[9:0], Green[9:0], raw_vs, raw_hs, en_flag, meas_ihs, HSOUT_sync_proc, coast, CLAMP_G, CLAMP_BR</p> <p>0110: 1'b0, adc_clk, raw_vs, raw_hs, test_s1, test_s2, raw_filed, Blue[9:0], Green[9:0], hs0_schmitt, hs1_schmitt, ~appl_por</p> <p>0111: 3'b0, adc_clk, Green[9:0], iclk_tst,</p>		

				raw_vs, raw_hs, raw_filed, fifo_clk, internal_crystal, test_s1, test_s2, sync_pro_tst[7:0] 1000: AUDIO_DAC enable signal test pin: dac_2ch_otpin[29:0] 1001: VSDMAIN test mode: pclk_tst,, vsd_pr[7:0], vsd_y[7:0],vsd_pb[7:0],den,dvs,dhs,ch 1_ivs, vsd_den, 1010: Auto_soy test mode 1010: misc, ref CR-8E-0D[3:0] 1011: avc_eq_test[29:0] 1100: Embedded MCU test out mode 1101: HDMI test in mode HDMI_TST_IN [0:29] will be assigned to {124~121, 114~108, 105~100, 72~64, 54~51} 1110: HDMI test out mode HDMI_TST_OUT [0:29] will be assigned to {124~121, 114~108, 105~100, 72~64, 54~51} 1111: 4'b0,decmp_hs,clamp_g, new_fifo_odata_g, new_fifo_odata_b, new_fifo_odata_r When set to 0010/0110/0111,test_s1 & test_s2 can be assigned by “Select_Tst_s1s2”	
Others are reserved					

Register:::TST_CLK_CTRL0					0x01
Name	Bits	Read/ Write	Reset State	Comments	Config
DPLL_OEN	7	R/W	0	DPLL frequency output enable 0: output disabled 1: output enabled	
M2pll_OEN	6	R/W	0	M2PLL frequency output enable 0: output disabled 1: output enabled	
Audio_pll_OEN	5	R/W	0	Audio_PLL frequency output enable 0: output disabled 1: output enabled	
Reserved	4	R/W	0	Reserved to 0	
CLK108_PLL27X_OEN	3	R/W	0	CLK108_PLL27X frequency output enable (M_domain clk, refer to CR_22[1:0]) 0: output disabled 1: output enabled	
Test1out_OEN	2	R/W	0	Test1out frequency output enable 0: output disabled 1: output enabled	
Test2out_OEN	1	R/W	0	Test2out frequency output enable 0: output disabled 1: output enabled	
Fav4_OEN	0	R/W	0	Fav4 frequency output enable 0: output disabled 1: output enabled	

Register:::TST_CLK_CTRL1					0x02
Name	Bits	Read/ Write	Reset State	Comments	Config
XCLK_OEN	7	R/W	0	XCLK frequency output enable 0: output disabled 1: output enabled	

CKT_PLL27X_OEN	6	R/W	0	CKT_PLL27X frequency output enable 0: output disabled 1: output enabled	
Rev	5:0	---	---	Reserved	

Register::TST_CLK_CTRL2					
Name	Bit	R/W	Default	Description	Config
Rev	7:6	---	---	Reserved	
DPLL_DIV_CTRL	5:4	R/W	00	DPLL frequency is divided by 00:1 01:2 10:4 11:8	
M2pll_DIV_CTRL	3:2	R/W	11	M2PLL frequency is divided by 00:1 01:2 10:4 11:8	
Audio_pll_DIV_CTRL	1:0	R/W	00	Audio PLL frequency is divided by 00:1 01:2 10:4 11:8	

Register:: TST_CLK_CTRL3					
Name	Bit	R/W	Default	Description	Config
Fav4_DIV_CTRL	7:6	R/W	00	Fav frequency is divided by 00:1 01:2 10:4 11:8	
Test1out_DIV_CTRL	5:4	R/W	00	Test1out frequency is divided by 00:1 01:2 10:4 11:8	
Test2out_DIV_CTRL	3:2	R/W	00	Test2out frequency is divided by 00:1 01:2 10:4 11:8	
CLK108_pll27xDIV_CTRL	1	R/W	0	(M_domain clk DIV) 0:Divided by 1 1:Divided by 4	
Ckt_pll27x DIV_CTRL	0	R/W	0	0:divided by 1 1:divided by4	

Register:: Select_Tst_s1s2					
Name	Bit	R/W	Default	Description	Config
Reserved	7	R/W	0	Reserved	
Select_Tst_s1	6:4	R/W	001	Select test function of test_s1 3'b000: DPLL clock (TIE LOW NOW) 3'b001: PLLS fbk clock 3'b010: CKOAD2(High Speed) 3'b011: PLL status 3'b100: HSOUT 3'b101: ADC clock(from PLLS)(High Speed) 3'b110: Empty Flag	

				3'b111: BVS(Video8)	
Reserved	3	R/W	0	Reserved	
Select_Tst_s2	2:0	R/W	010	Select test function of test_s1 3'b000: PLLS phase swallow clock (High speed) 3'b001: DPLL status(TIE LOW NOW) 3'b010: PLLS phase0 clock(High speed) 3'b011: M2PLL clock(Not in APLL) 3'b100: HSFB 3'b101: TP2_MX5 3'b110: Full Flag 3'b111: BHS(Video8)	

Register:: Select_Tstinclock 0x06					
Name	Bit	R/W	Default	Description	Config
DPLL_TST_IN	7	R/W	0	0:Normal 1:DCLK enter from pin 55_50	
ADCPLL_TST_IN	6	R/W	0	0:Normal 1:ADC CLK enter from pin 56_51	
M2PLL_TST_IN	5	R/W	0	0:Normal 1:M2PLL CLK enter from pin 57_52	
HDMI_CP_ACLK_TST_IN	4	R/W	0	0:Normal 1:HDMI_CP_ACLK enter from pin 58	
HDMI_CP_CLK_TST_IN	3	R/W	0	0:Normal 1:HDMI_CP_CLK enter from pin 59	
SCAN_CLK_TST_IN	2	R/W	1	0:Normal 1:SCAN CLK enter from pin 9863	
DPLL_NDIV2_EN	1	R/W	0	DPLL Test Mode Divider Enable 0:use pin 50 div2 as dclk 1:use pin 50 as dclk	
MPLL_TST_IN	0	R/W	0	0:Normal 1:MPLL CLK enter from pin 51(128pin) or pin?? (68pin)	

TEST MODE in FIFO

Register:: ADC TEST MODE 0x07					
Name	Bit	R/W	Default	Description	Config
ADC_TEST_MODE	7	R/W	0	0:Disable 1:Enable	
ADC_TEST_MODE_2	6	R/W	0	Useless	
FIFO_TEST_MODE	5	R/W	0	0:Disable 1:Enable test the CRC from FIFO · and open the Pattern Gen to d domain. Pattern Gen Seed (R = 01,G=00,B=00)	
ADC_TEST_START	4	R	0	Under ADC_TEST_MODE = 1, ADC_TEST_START will high when the new fifo is full , then read out data from FIFO by sending DCLK from outside test pin.	
Rev	3:0	---	---	Reserved	

Register:: ADC TEST MODE ADDR MSB 0x08					
Name	Bit	R/W	Default	Description	Config
ADC_TEST_ADDR[1:0]	7:6	R/W	0X00	Read the FIFO initial Addr.	

Rev	5:0	---	---	Reserved	
-----	-----	-----	-----	----------	--

Register:: ADC TEST MODE ADDR LSB 0x09					
Name	Bit	R/W	Default	Description	Config
ADC_TEST_ADDR[7:0]	7:0	R/W	0X04	Read the FIFO initial Addr.	

Register:: ADC FIFO CRC 0x0A					
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[23:16]	7:0	R	0	NEW FIFO CRC	

Register:: ADC FIFO CRC 0x0B					
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[15:8]	7:0	R	0	NEW FIFO CRC	

Register:: ADC FIFO CRC 0x0C					
Name	Bit	R/W	Default	Description	Config
NEW_FIFO_CRC[7:0]	7:0	R	0	NEW FIFO CRC	

Register:: Auto_soy_test 0x0D					
Name	Bit	R/W	Default	Description	Config
Auto_soy_test_mode	7	R/W	0	0: Normal 1: Test mode clk will be from pin51 & 6 bits data will be from {pin 32~pin37}	
Auto_soy_test_sel	6:4	R/W	0	Test function sel 0000: adcnr_test_out(tie 0) 0001: color processing test out 0010: disp conv test out 0011: idclti test out, refer to page 0x11, CR-A1[4] 0100: vivid color test out, refer to page 0x11, CR-F0p7:6] 0101: autosoy test 1000: CEC test out 1001: Display_test_out :{15' bo, wradr_cnt[1:0], rdadr_cnt[1:0], fsync_dvs_flag, ivs_mn_fsync, ivs, dvs, ihs, , dhs, i_lr, d_lr, i_den, d_den} Others are reserved.	

Register:: Testout_sel0 0x0E					
Name	Bit	R/W	Default	Description	Config
reg_force_testout	7	R/W	0	0: Normal 1: Force output selected testout	

				signal Default mapping is reference to Data_Test_mode[3:0]	
reg_test0_map	6:2	R/W	0	Test0 signal bit selection 5' h00: Bit0 5' h01: Bit1 ...	
reg_trig_edge_sel0	1	R/W	0	Trigger Edge Selection 0: Choose positive edge 1: Choose negative edge.	
reg_bypass_sel0	0	R/W	0	Final Output Signal Selection 0: Bypass original test signal 1: Choose one-hot latched signal.	

Register::Testout_sel1					
Name	Bit	R/W	Default	Description	Config
reg_test1_map	7:3	R/W	0	Test1 signal bit selection 5' h00: Bit0 5' h01: Bit1 ...	
reg_trig_edge_sel1	2	R/W	0	Trigger Edge Selection 0: Choose positive edge 1: Choose negative edge.	
reg_bypass_sel1	1	R/W	0	Final Output Signal Selection 0: Bypass original test signal 1: Choose one-hot latched signal.	
Reserved	0	R/W	0	Reserved	

Register::Testout_sel2					
Name	Bit	R/W	Default	Description	Config
reg_test2_map	7:3	R/W	0	Test2 signal bit selection 5' h00: Bit0 5' h01: Bit1 ...	
reg_trig_edge_sel2	2	R/W	0	Trigger Edge Selection 0: Choose positive edge 1: Choose negative edge.	
reg_bypass_sel2	1	R/W	0	Final Output Signal Selection 0: Bypass original test signal 1: Choose one-hot latched signal.	
Reserved	0	R/W	0	Reserved	

Register::Testout_sel3					
Name	Bit	R/W	Default	Description	Config
reg_test3_map	7:3	R/W	0	Test3 signal bit selection 5' h00: Bit0 5' h01: Bit1 ...	
reg_trig_edge_sel3	2	R/W	0	Trigger Edge Selection 0: Choose positive edge 1: Choose negative edge.	
reg_bypass_sel3	1	R/W	0	Final Output Signal Selection	

				0: Bypass original test signal 1: Choose one-hot latched signal.	
Reserved	0	R/W	0	Reserved	

Embedded OSD

Address: 90 OSD_ADDR_MSB (OSD Address MSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD MSB 8-bit address

Address: 91 OSD_ADDR_LSB (OSD Address LSB 8-bit)

Bit	Mode	Function
7:0	R/W	OSD LSB 8-bit address

Address: 92 OSD_DATA_PORT (OSD Data Port)

Bit	Mode	Function
7:0	W	Data port for embedded OSD access

Refer to the embedded OSD application note for the detailed.

Address: 93 OSD_SCRAMBLE Default: 05h

Bit	Mode	Function
7	R/W	BIST Start 0: stop (Default) 1: start (auto clear)
6	R	BIST Result 0: fail (Default) 1: success
5	--	Reserved (Default 0)
4	R	Double_Buffer_Write_Status 0: double buffer write out is finish, or data write to double buffer is not ready, or no double buffer function. 1: after data write to dbuf and before dbuf write out, such that double buffer is busy.
3	R/W	OSDADRHSB 0: If initial address lower than or equal to 12K 1: If initial address higher than 12K The bit will be designed to control 20K bytes SRAM. However it will have no effect for WINDOW setting. Also please remember to set {OSDADRHSB, OSDADRMBS(CR90), OSDADRLSB(CR91) } again while you like to R/W a new address.
2:0	R/W	Double buffer depth (Default=6) 000~101=>1~6

Address: 94 OSD_TEST

Bit	Mode	Function
7:0	R/W	Testing Pattern

Dithering Control(For Memory Domain)

Register:: M_DITHERING_DATA_ACCESS						0x95
Name	Bits	Read/ Write	Reset State	Comments	Config	
Dithering_DATA_ACCESS	7:0	W	0	Refer to following description		

Register:: M_DITHERING_CTRL1						0x96
Name	Bits	Read/ Write	Reset State	Comments	Config	
Dither_Access	7:6	W	0	Enable Access Control 00: disable (Default) 01: enable access dithering sequence table 10: enable access dithering table 11: enable access temporal offset		
Dither_en	5	R/W	0	Enable Dithering Function 0: disable (Default) 1: enable		
Dither_temp	4	R/W	0	Temporal Dithering 0: Disable (Default) 1: Enable		
Dither_table	3	R/W	0	Dithering Table Value Sign 0: unsigned 1: signed (2's complement)		
Dither_mode	2	R/W	0	Dithering Mode 0: New (Default) 1: Old		
Dither_V_Fram_M	1	R/W	0	Vertical Frame Modulation 0: Disable (Default) 1: Enable		
Dither_VH_Fram_M	0	R/W	0	Horizontal Frame Modulation 0: Disable (Default) 1: ENABLE		

Register:: M_DITHERING_CTRL2						0x97
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:1	R/W	0	Reserved		
Dither_Table_Ref	0	R/W	1	Table reference 0: By VS/HS 1: By DEN (Default)		

Digital Filter

Address: 98		DIGITAL_FILTER_CTRL	Default: 00h
Bit	Mode	Function	
7:4	R/W	Access Port Write Enable 0000: disable 0001: phase access port 0010: negative smear access port 0011: positive smear access port 0100: negative ringing access port 0101: positive ringing access port 0110: mismatch access port 0111: Y(B)/Pb(G)/Pr(R) channel digital filter enable 1xxx: noise reduction access port	
3:2	R/W	Two condition occur continuous (ringing to smear) 00: disable(hardware is off , depend on firmware) 01: only reduce ringing condition 10: only reduce smear condition 11: no adjust (hardware is on, but do nothing)	
1	R/W	When noise reduction and mismatch occur, select 0: mismatch 1: noise reduction	
0	--	Reserved to 0	

Address: 99		DIGITAL_FILTER_PORT	Default: 00h
DIGITAL_FILTER_CTRL[7:4] = 0111		Function	
Bit	Mode	Function	
7	R/W	Y EN (G) : function enable 0: function disable 1: function enable	
6	R/W	Pb EN (B) : function enable 0: function disable 1: function enable	
5	R/W	Pr EN (R) : function enable 0: function disable 1: function enable	
4	R/W	Initial value: 0: raw data 1: extension	
3:0	--	Reserved to 0	

DIGITAL_FILTER_CTRL[7:4] = 0000 ~0110 or 1xxx		Function
Bit	Mode	Function
7	R/W	EN : function enable 0: function disable 1: function enable
6:4	R/W	THD_OFFSET Threshold value of phase and mismatch and noise reduction or offset value of smear and ringing
3:2	R/W	DIV : divider value of phase, smear and ringing 00: 0 01: 1 10: 2 11: 3
1:0	--	Reserved to 0

THD_OFFSET define:

The THD value definition of phase enhance function

Bit6~4	000	001	010	011	100	101	110	111
Value	112	128	144	160	176	192	208	224

The offset value definition of smear and ringing reduce function

Bit6~4	000	001	010	011	100	101	110	111
Value	no use	16	32	48	64	80	96	112

The THD value definition of mismatch enhance function

Bit6~4	000	XX1
Value	1	2

The THD value definition of noise reduction function

Bit6~4	000	001	010	011	100	101	110	111
Value	0	1	2	3	4	5	6	7

Video Color Space Conversion(Input Domain) YUV2RGB

Address: 9C YUV_RGB_CTRL (YUV <-> RGB Control Register) Default: 10h

Bit	Mode	Function
7	R/W	Y_OUT Shift 0: Bypass 1: Y_Out+64
6	R/W	CbCr_Out_Shift: 0 : Bypass 1: Cb_Out+512, Cr_Out+512
5	---	Reserved
4	R/W	Color Conversion Type 0: YUV->RGB 1: RGB->YUV (U,V are translated to unsigned 10-bit number)
3	R/W	Enable YUV/RGB coefficient Access: 0: Disable 1: Enable If this bit is set to 0, the address of the data port will reset to 0, and continuously writes 18 bytes
2	R/W	Cb Cr Clamp 0: Bypass 1: Cb-512, Cr-512 (MSB Inversion)
1	R/W	Y Gain/Offset: 0 : Bypass 1: (Y-64)*1.164
0	R/W	Enable YUV <-> RGB Conversion: 0: Disable YUV<->RGB conversion (Default) 1: Enable YUV<->RGB conversion

Address: 9D YUV_RGB_COEF_DATA

Bit	Mode	Function
7:0	W	COEF_DATA[7:0]

YUV->RGB matrix : (CR9C[4] = 0)

- CR9C[1] = 0, CR9C[2] = 1,

$$\begin{aligned} R &= h00*Y + h01*(Cb-512) + h02*(Cr-512) \\ G &= h10*Y + h11*(Cb-512) + h12*(Cr-512) \\ B &= h20*Y + h21*(Cb-512) + h22*(Cr-512) \end{aligned}$$

- CR9C[1] = 1, CR9C[2] = 1,

$$\begin{aligned} R &= h00*(1.164*(Y-64)) + h01*(Cb-512) + h02*(Cr-512) \\ G &= h10*(1.164*(Y-64)) + h11*(Cb-512) + h12*(Cr-512) \\ B &= h20*(1.164*(Y-64)) + h21*(Cb-512) + h22*(Cr-512) \end{aligned}$$

The output, Rout / Gout / Bout, should be calculated by offset / gain operation

$$Rout = (R' + Roffset) * Rgain$$

$$Gout = (G' + Goffset) * Ggain$$

$$Bout = (B' + Boffset) * Bgain$$

RGB->YUV matrix : (CR9C[4] = 1, CR9C[2:1] = 00)

$$Y = h00*R + h01*G + h02*B$$

$$Cb = h10*R + h11*G + h12*B$$

$$Cr = h20*R + h21*G + h22*B$$

All 'h' coefficients are expressed as 2's complement with 4-bit signed-extension, 2-bit integer and 10-bit fractional number. (0x0400 means 1.0)

When color conversion setting is YUV->RGB (CR9C[4]=0), h00, h10 and h20 is not effective(force to 1.0 internally).

Integer part is only effective for h02, h21. For other coefficients, integer part must be the same as signed- extension.

Offsets are S(14,4) 14bits, 10-bits signed integer and 4-bit fractional bits

Gains are U(10,9) 10bits, 1-bit integer and 9-bit fractional bits.

Coefficient Sequence (30-byte) : h00 (High-byte), h00 (Low-byte), h01 (High-byte), h01 (Low-byte), h02 (High-byte), h02 (Low-byte), h10 (High-byte), h10 (Low-byte), h11 (High-byte), h11 (Low-byte), h12 (High-byte), h12 (Low-byte), h20 (High-byte), h20 (Low-byte), h21 (High-byte), h21 (Low-byte), h22 (High-byte), h22 (Low-byte).Roffset (Hight-byte), Roffset(Low-byte), Goffset (Hight-byte), Goffset(Low-byte), Boffset (Hight-byte), Boffset(Low-byte)Rgain (Hight-byte), Rgain (Low-byte), Ggain (Hight-byte), Ggain (Low-byte), Bgain (Hight-byte), Bgain (Low-byte)

Default value:

h00=0105h,h01=0202,h02=0063h,h10=ff69h,h11=fed8h,h12=01c0h,h20=01c0h,h21=fe89h,h22=ffb8h,offset=0x000h,gain=0x0200h

Address:0x9E reserved

Paged Control Register

Address: 9F		PAGE_SEL	Default: 00h
Bit	Mode	Function	
7:5	R/W	Reserved to 0	
4:0	R/W	<u>Page Selector (CRA0~CRFF)</u> <u>Page 0: Embedded ADC/ABL/LVR/Schmitt trigger</u> <u>Page 1: PLL</u> <u>Page 2: HDMI</u> <u>Page 3: LiveShow</u> <u>Page 4: SDRAM control</u> <u>Page 5: FRC</u> <u>Page 6: IOSC AudioDAC</u> <u>Page 7: Vivid color/DCC/ICM</u> <u>Page 8: Audio volume control</u> <u>Page 9: Input Gamma</u> <u>Page A: Reserved</u> <u>Page B: GDI PHY</u> <u>Page C: GDI MAC</u> <u>Page D: MCU</u> <u>Page E: MCU</u> <u>Page F: MCU</u> <u>Page 10: Pin Share Control</u> <u>Page 11: Ultra Vivid</u> <u>Page 12: Ultra Vivid</u> <u>Page 13: Ultra Vivid</u> <u>Page 14: ADC Noise Reduction</u> <u>Page 15: Timing Control</u> Others: reserved	

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Embedded ADC (Page 0)

Register::ADC_POWER_SOG_SOY_CONTROL[7:0]						0XBA
Name	Bit	R/W	Default	Description	Config	
Reserved	7:6	R/W	0b0	Reserved		
ADC_SOG1_DAC[5:0]	5:0	R/W	0b100000	Reserved		

Register:: ADC_2X_SAMPLE[7:0]						0XBB
Name	Bit	R/W	Default	Description	Config	
ADC_2X_SAMPLE[7]	7	R/W	0b0	ADC 2x over sample (0:1x 1:2x)		
ADC_2X_SAMPLE[6]	6	R/W	0b0	2x Clock Polarity (0:Negative 1:Positive)		
ADC_2X_SAMPLE[5]	5	R/W	0b0	1x Clock Polarity (0:Negative 1:Positive)		
ADC_2X_SAMPLE[4]	4	R/W	0	VCM Source Selection (from resistor or bandgap) 0: from Vdd33 Resistor ladder; 1:Bandgap		
ADC_2X_SAMPLE[4:3]	4:3	R/W	0b00	Reserved		
ADC_2X_SAMPLE[3]	3	R/W	0			
ADC_2X_SAMPLE[2]	2	R/W	0b0	Clock input select (0:from CKOAD_V33, 1:from CKOAD_V12)		
ADC_2X_SAMPLE[1:0]	1:0	R/W	0b00	Reserved refgen' ckt P-side gate resistor short enable 0: disable (default), 1: enable		
ADC_2X_SAMPLE[1]	1	R/W	0b0			
ADC_2X_SAMPLE[0]	0	R/W	0b0	refgen' ckt N-side gate resistor short enable 0: disable (default), 1: enable		

Register:: ADC_CLOCK[7:0]						0XBC
Name	Bit	R/W	Default	Description	Config	
ADC_CLOCK[7]	7	R/W	0b0	Input Clock Polarity (0:Negative 1:Positive)		
ADC_CLOCK[6]	6	R/W	0b0	Output Divider Clock Polarity (0:Normal 1:Inverted)		
ADC_CLOCK[5:4]	5:4	R/W	0b0	ADC_OUT_PIXEL Delay (00:1.05n 01:1.39n 10:1.69n 11:1.97n)		
ADC_CLOCK[3]	3	R/W	0b0	1X or 2X from APLL (0:1X 1:2X)		
ADC_CLOCK[2]	2	R/W	0b0	Single Ended or Diff. Clock from APLL (0:Diff. 1:Single Ended)		
ADC_CLOCK[1:0]	1:0	R/W	0b1	Duty Stablizer(00: 48% 01:50% 10: 51% 11:52%)		

Register:: ADC_TEST[7:0]						0XBD
Name	Bit	R/W	Default	Description	Config	
ADC_TEST[7]	7	R/W	0b0	Reserved		
ADC_TEST[6:4]	6:4	R/W	0b000	Test Ouput Selection SOGINO (000:X 001:gnd 010:vrefn 011:vcm 100:vrefp 101:vdd (for vref) 110:vdd vboot 111:vdd (for adc core))		
ADC_TEST[3]	3	R/W	0b0	Test Ouput Selection VTTEST_GDI for Testing, valid only when ADC_TEST[6:4]=000 & ADC_POWER2[6]=0; SOGINO(0:X 1:VTTEST_GDI)		
ADC_TEST[2]	2	R/W	0b0	Reserved		
ADC_TEST[1:0]	1:0	R/W	0b00	Clock Output Divider (00: 1/1 01: 1/2 10: 1/3 11: 1/4)		

Register::RGB gain_LSB						0XBE
Name	Bit	R/W	Default	Description	Config	
Reserved	7:6	R/W	0b0	Reserved		
ADC_GAI_RED[1:0]	5:4	R/W	0x0	Red Channel Gain Adjust[1:0]		
ADC_GAI_GRN[1:0]	3:2	R/W	0x0	Green Channel Gain Adjust[1:0]		
ADC_GAI_BLU[1:0]	1:0	R/W	0x0	Blue Channel Gain Adjust[1:0]		

0xBF is reserved

Register::RGB offset_LSB						0XBF
Name	Bit	R/W	Default	Description	Config	
Reserved	7:6	R/W	0b0	Reserved		
ADC_OFF_RED[1:0]	5:4	R/W	0x0	Red Channel Offset Adjust[1:0] Red Channel Offset Adjust[2:1]		
ADC_OFF_RED[2:1]						
ADC_OFF_GRN[1:0]	3:2	R/W	0x0	Green Channel Offset Adjust[1:0] Green Channel Offset Adjust[2:1]		
ADC_OFF_GRN[2:1]						
ADC_OFF_BLU[1:0]	1:0	R/W	0x0	Blue Channel Offset Adjust[1:0] Blue Channel Offset Adjust[2:1]		
ADC_OFF_BLU[2:1]						

Register::red gain_MSB						0XC0
Name	Bit	R/W	Default	Description	Config	
ADC_GAI_RED[9:2]	7:0	R/W	0x80	Red Channel Gain Adjust[9:2]		

Register::green gain_MSB						0XC1
Name	Bit	R/W	Default	Description	Config	
ADC_GAI_GRN[9:2]	7:0	R/W	0x80	Green Channel Gain Adjust[9:2]		

Register::blue gain_MSB						0XC2
Name	Bit	R/W	Default	Description	Config	
ADC_GAI_BLU[9:2]	7:0	R/W	0x80	Blue Channel Gain Adjust[9:2]		

Register::RED OFFSET_MSB						0XC3
Name	Bit	R/W	Default	Description	Config	
ADC_OFF_RED[9:2]	7:0	R/W	0x80	Red Channel Offset Adjust[9:2] Red Channel Offset Adjust[10:3]		
ADC_OFF_RED[10:3]						

Register::GREEN OFFSET_MSB						0XC4
Name	Bit	R/W	Default	Description	Config	
ADC_OFF_GRN[9:2]	7:0	R/W	0x80	Green Channel Offset Adjust[9:2] Green Channel Offset Adjust[10:3]		
ADC_OFF_GRN[10:3]						

Register::BLUE OFFSET_MSB						0XC5
Name	Bit	R/W	Default	Description	Config	
ADC_OFF_BLU[9:2]	7:0	R/W	0x80	Blue Channel Offset Adjust[9:2] Blue Channel Offset Adjust[10:3]		
ADC_OFF_BLU[10:3]						

Register:: ADC_POWER[7:0]						0XC6
Name	Bit	R/W	Default	Description	Config	

ADC_POWER[7]	7	R/W	1	ADC Regulator Power On (0: Power Down 1: Power On) Reserved to ADC Regulator Power On	
ADC_POWER[6]	6	R/W	0	ADC clock Power On (0: Power Down 1: Power On)	
ADC_POWER[5]	5	R/W	0b0	SOG_ADC0 Power On (0: Power Down 1: Power On)	
ADC_POWER[4]	4	R/W	0b0	ADC_V15GEN /IBIAS[4:0] Power On (0: Power Down 1: Power On)	
ADC_POWER[3]	3	R/W	0b0	Bandgap Power On (0: Power Down 1: Power On) If ADC_POWER2[0] = 0 ADC VCM & ADC Regulator & Band-gap Power On control by ADC_POWER[3] (0: Power Down 1: Power On) If ADC_POWER2[0] = 1 Band-gap Power On control by ADC_POWER[3] (0: Power Down 1: Power On) ADC VCM Power on control by ADC_POWER2[1] ADC Regulator Power On control by ADC_POWER2[2] LDO_ADC: Regulator Power on control by ADC_POWER2[3]	
ADC_POWER[2]	2	R/W	0b0	Red Channel ADC Power On (0: Power Down 1: Power On)	
ADC_POWER[1]	1	R/W	0b0	Green Channel ADC Power On (0: Power Down 1: Power On)	
ADC_POWER[0]	0	R/W	0b0	Blue Channel ADC Power On (0: Power Down 1: Power On)	

Register:: ADC_IBIAS0[7:0]					0XC7
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS0[7:6]	7:6	R/W	0b01	PGA Input GM Current, High 2 bits Low 2 bits=ADC_IBIAS1<7:6> (0000: 0u, 0001: 50u, 0010: 100u, 0011: 150u 0100: 200u, 0101: 250u, 0110: 300u, 0111: 350u 1000: 400u, 1001: 450u, 1010: 500u, 1011: 550u 1100: 600u, 1101: 650u, 1110: 700u, 1111: 750u) Reserved for PGA Input GM Current	
ADC_IBIAS0[5:4]	5:4	R/W	0b01	Bias Current of RSDS20U (00:16u-01:20u 10:24u 11:28u) Reserved for Bias Current of RSDS20U	
ADC_IBIAS0[3:2]	3:2	R/W	0b10	Bias Current of LVDS20U (00:16u-01:20u 10:24u 11:28u) Bias Current of LVDS (00:15u 01:25u 10:20u 11:30u)	

ADC_IBIAS0[1:0]	1:0	R/W	0b01	Bias Current of RSDS_TTL20U (00:16u 01:20u 10:24u 11:28u) Reserved for Bias Current of RSDS_TTL20U	
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Register:: ADC_IBIAS1[7:0] 0XC8					
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS1[7:6]	7:6	R/W	0b01	PGA Input GM Current, Low 2 bits High 2 bits=ADC_IBIAS0<7:6> Reserved for PGA Input GM Current	
ADC_IBIAS1[5:4]	5:4	R/W	0b01 0b01	Reserved VCM Voltage Control (Valid only when ADC_2X_SAMPLE[4]=1) 00: 660mV 01: 700mV 10: 740mV 11: 780mV	
ADC_IBIAS1[3:2]	3:2	R/W	0b01	Reserved	
ADC_IBIAS1[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_IBIAS2[7:0] 0XC9					
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS2[7:5]	7:5	R/W	0b000	Select output voltage of ADC Regulator (000 : 1.203V 001 : 1.143V 010 : 1.085V 011 : 1.246V) (100 : 1.298V 101 : 1.355V 110 : 1.424V 111 : 1.508V) Select output voltage of ADC Regulator 000:1.3V 001:1.4V 010:1.5V 011:1.2V 100:1.35V 101:1.45V 110:1.55V 111:1.25V	
ADC_IBIAS2[4:2]	4:2	R/W	0b001	Bias Current of DAC(000:22.5u 001:25u 010: 27.5u 011:30u 100:32.5u 101:35.0u 110:17.5u 111:20u) Reserved for ADC_IBIAS2[4:2] Bias Current of DAC	
ADC_IBIAS2[1:0]	1:0	R/W	0b01	Bias Current of Audio_DAC (00:16u 01:20u 10:24u 11:28u) (reserved circuit, not used) Reserved for ADC_IBIAS2[1:0] Bias Current of Audio_DAC	

Register:: ADC_IBIAS3[7:0] 0XA0					
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS3[7:6]	7:6	R/W	0b01	Bias Current of ADC_SF (00:15u 01:20u 10:25u 11:30) Bias Current of ADC_SF: ADC_IBIAS3[7:6] works together with ADC_POWER2[5] If ADC_POWER2[5]=0 ADC_IBIAS3[7:6]= 00:15u,01:20u (Default),10:25u,11:30u, If ADC_POWER2[5]=1	

				ADC_IBIAS3[7:6]= 00:5u,01:10u,10:35u,11:40u	
ADC_IBIAS3[5:3]	5:3	R/W	0b011	Bias Current of 1.2v mbias (000:17.5u 001:20u 010:22.5u 011:25u 100:27.5u 101:30u 110:32.5u 111:35u) Reserved for Bias Current of 1.2v mbias	
ADC_IBIAS3[2:0]	2:0	R/W	0b001	Bias Current of SH,MDAC (000:12u 001:18u 010:24u 011:27u 100:30u 101:33u 110:39u 111:45u) Bias Current of SUBADC (000:10u 001:10u 010:10u 011:10u 100:20u 101:20u 110:20u 111:20u)	

低頻, 13.5M-50M, 將 ADC_IBIAS3=76-5A(50.7uA), 為解決低頻共模震盪問題

中高頻, 50M-200M, 將 ADC_IBIAS3=5C(30uA)

超高頻, >200M 將, ADC_IBIAS3=5E(39uA)

Register:: ADC_IBIAS4[7:0]					0XCB
Name	Bit	R/W	Default	Description	Config
ADC_IBIAS4[7:6]	7:6	R/W	0b01	Bias Current of DPLL20U (00:16u- 01:20u 10:24u 11:28u) Reserved for Bias Current of DPLL20U	
ADC_IBIAS4[5:4]	5:4	R/W	0b01	Bias Current of APLL_IB60U (00:48u- 01:60u 10:72u 11:84u) Reserved for Bias Current of APLL_IB60U	
ADC_IBIAS4[3:2] [3]	3:2 3	R/W	0b01 0	Reserved SF LPF enable 0: disable (default), 1: enable If ADC_IBIAS4[3]=0, SF LPF is disabled. If ADC_IBIAS4[3]=1, SF LPF is enabled, the setting is as follows: ADC_CLAMP_CTRL2[5]=0: ADC_DCR_CTRL[2:1]= 00:73 MHz, 01:158 MHz, 10:250 MHz, 11:340 MHz ADC_CLAMP_CTRL2[5]=1: ADC_DCR_CTRL[2:1]= 00:38 MHz, 01:63 MHz, 10:96 MHz, 11:131 MHz	
ADC_IBIAS4[2]	2	R/W	0b1	Reserved	
ADC_IBIAS4[1:0]	1:0	R/W	0b01	Reserved	

Register:: ADC_VBIAS0[7:0]					0XCC
Name	Bit	R/W	Default	Description	Config
ADC_VBIAS0[7:6]	7:6	R/W	0b00	PGA Input Ioffset Current, High 2 bits Voffset=Ioffset*2.4K Low 2 bits at CRCC[3:2] 0000: 0u, 0001: 40u, 0010: 80u, 0011: 120u 0100: 160u, 0101: 200u, 0110: 240u, 0111: 280u, 1000: 320u, 1001: 360u, 1010: 400u,	

				1011: 440u, 1100: 480u, 1101: 520u, 1110: 560u, 1111: 600u Reserved for PGA Input Ioffset Current, High 2 bits Voffset=Ioffset*2.4K	
ADC_VBIAS0[5:4]	5:4	R/W	0b01	1.5v regulator adjust (00:1.4 01:1.5 10:1.6 11:1.7) Reserved	
ADC_VBIAS0[3:2]	3:2	R/W	0b00	PGA Input Ioffset Current, Low 2 bits High 2 bits = ADC_VBIAS0[7:6] Reserved for PGA Input Ioffset Current	
ADC_VBIAS0[1:0]	1:0	R/W	0b01	Bandgap Voltage (00:1.15 01:1.25 10:1.34 11:1.42)	

Register::: ADC_VBIAS1[7:0]					0XCD
Name	Bit	R/W	Default	Description	Config
ADC_VBIAS1[7]	7	R/W	0b0	ADC Gain Calibration (0: Normal 1: Calibration)	
ADC_VBIAS1[6]	6	R/W	0b0	R Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[5]	5	R/W	0b0	G Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[4]	4	R/W	0b0	B Channel Clamp to -300mV (0: 0mV 1:-300mV)	
ADC_VBIAS1[3]	3	R/W	0b1	SH boost enable (0: no boost, 1: boost)	
ADC_VBIAS1[2]	2	R/W	0b0	SH boost adjust (0:0.8V, 1:0.85V)	
ADC_VBIAS1[1]	1	R/W	0b0	Select reference voltage to ADC_REG_OP =(PORB_33V*ADC_VBIAS1[1]) 0 : from bandgap 1 : from Vdd of power supply*resistance ratio Ref. to D2[7] Reserved for Select reference voltage to ADC_REG_OP =(PORB_33V*ADC_VBIAS1[1])	
ADC_VBIAS1[0]	0	R/W	0b1	PGA Input GM Power On (0: Power Down, 1: Power On), Reserved for PGA Input GM Power On	

Register::: ADC_CTL_RGB[7:0]					0XCE
Name	Bit	R/W	Default	Description	Config
ADC_CTL_RGB[7:4]	7:4	R/W	0b1000	SH gain(0000:0.95, 0001:1, 0010:1.05, 0011:1.1, 0100:1.15, 0101:1.2, 0110:1.25, 0111:1.3, 1000:1.35, 1001:1.4, 1010:1.45) SH gain (0000:0.792, 0001:0.833, 0010:0.875, 0011:0.916 0100:0.958, 0101:1.0, 0110:1.042, 0111:1.083 1000:1.125, 1001:1.166, 1010:1.208,	

				1011:1.35, 1100: 1.5, others:1.35)	
ADC_CTL_RGB[3]	3	R/W	0b0	Dual (0: Input0 1: force to ground)	
ADC_CTL_RGB[2]	2	R/W	0b1	Single Ended or Diff. Input (0: Single Ended 1: Diff)	
ADC_CTL_RGB[1:0]	1:0	R/W	0b10	Bandwidth (00: 75M 01: 150M 10: 300M 11: 500M) LPF Embedded in SH Block Bandwidth(00:75M, 01:150M, 10: 250M, 11:350M)	

Register:: ADC_CTL_RED[7:0] 0XCF					
Name	Bit	R/W	Default	Description	Config
ADC_CTL_RED[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB) //ADC_VBIAS1[6]==0	
ADC_CTL_RED[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_RED[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No Yes 1:RGB No, YPrPb No)	
ADC_CTL_RED[2:0]	2:0	R/W	0b000	Red Channel ADC Fine Tune Delay, Step=90ps	

Register:: ADC_CTL_GRN[7:0] 0XD0					
Name	Bit	R/W	Default	Description	Config
ADC_CTL_GRN[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB)	
ADC_CTL_GRN[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_GRN[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No Yes 1:RGB No, YPrPb No)	
ADC_CTL_GRN[2:0]	2:0	R/W	0b0	Green Channel ADC Fine Tune Delay, Step=90ps	

Register:: ADC_CTL_BLU[7:0] 0XD1					
Name	Bit	R/W	Default	Description	Config
ADC_CTL_BLU[7]	7	R/W	0b0	RGB/YPrPb Clamp (0: RGB 1:YPrPB)	
ADC_CTL_BLU[6:4]	6:4	R/W	0b100	Clamp Voltage (0V~700mV, Step=100mV)	
ADC_CTL_BLU[3]	3	R/W	0b0	Offset Depends on Gain (0: RGB Yes, YPrPb No Yes 1:RGB No, YPrPb No)	
ADC_CTL_BLU[2:0]	2:0	R/W	0b0	Blue Channel ADC Fine Tune Delay, Step=90ps	

Register:: ADC_SO_G_CMP[7:0] 0XD2					
Name	Bit	R/W	Default	Description	Config
ADC_Bandgap_SEL	7	R/W	0	Embedded regulator bandgap select 0: from POR bandgap 1: from ADC bandgap Reserved for Embedded regulator bandgap select	
ADC_SO_G_CMP[6]	6	R/W	0	Select Absolute VDD (0: from 3.3V, 1: from 1.2V)	
ADC_SO_G_CMP[5]	5	R/W	0	ADC Gain Calibration, Always Enable Clamp Signal 0: ADC_CLAMP[7:0]	

				ADC_CLAMPP[7:0] & ADC_CLAMPN[7:0]= from sync processor 1: ADC_CLAMP[7:0] ADC_CLAMPP[7:0] & ADC_CLAMPN[7:0]= H High)	
ADC_SOG_CMP[4]	4	R/W	0	<p>ADC Gain Calibration Voltage Source 0: from RGB + Bandgap, 1: from Gain_Cal_DAC3B, Refer to ADC_SOG_CMP[2:0]</p> <p>ADC Gain Calibration Voltage Source REV_REG0[2](CR[D8]-bit2)=0 (old mode): ADC_SOG_CMP[4]=0: Vmidi from RGB Bandgap , Voffset from RGB Bandgap ADC_SOG_CMP[4]=1: Vmidi from Gain_Cal_DAC3B , Voffset from Gain_Cal_DAC3B</p> <p>REV_REG0[2](CR[D8]-bit2)=1 (new mode): ADC_SOG_CMP[4]=0: Vmidi from RGB Bandgap , Voffset from RGB Bandgap ADC_SOG_CMP[4]=1: Vmidi from Gain_Cal_DAC3B , Voffset from RGB Bandgap Refer to ADC_SOG_CMP[2:0] default:0b'0</p>	
ADC_SOG_CMP[3]	3	R/W	0	ADC Gain Calibration Voltage Source of Gain_Cal_DAC3B (0: from Absolute VDD, 1:from Bandgap)	
ADC_SOG_CMP[2:0]	2:0	R/W	0	<p>ADC Gain Calibration Gain_Cal_DAC3B Voltage, 要可以量測 可以直接量測 R/G/B,P/N 電壓差即可 (同量測 VMID, VOFFSET 方法)</p> <p>正端 (000:0.40V 001:0.50V 010:0.60V 011:0.70V) (100:0.80V 101:0.90V 110:1.00V 111:1.10V)</p> <p>負端 0.7V</p>	

Register::: ADC_DCRESTORE_CTRL[7:0] 0XD3					
Name	Bit	R/W	Default	Description	Config
ADC_DCR_CTRL[7]	7	R/W	0	Reserved	
ADC_DCR_CTRL[6]	6	R/W	0	Reserved	
ADC_DCR_CTRL[5]	5	R/W	0	Reserved	
ADC_DCR_CTRL[4]	4	R/W	0	SOG0 DC Restore Enable(0:Disable 1:Enable)	
ADC_DCR_CTRL[3]	3	R/W	0	Reserved	
ADC_DCR_CTRL[2] ADC_DCR_CTRL[2:1]	2 2:1	R/W	0	Reserved SF LPF BW control (ADC_CLAMP_CTRL2[5] works together with ADC_DCR_CTRL[2:1]) If ADC_IBIAS4[3]=0, SF LPF is	

				disabled. If ADC_IBIAS4[3]=1, SF LPF is enabled, the setting is as follows: ADC_CLAMP_CTRL2[5]=0: ADC_DCRESTORE_CTRL[2:1]= 00:73 MHz, 01:158 MHz, 10:250 MHz, 11:340 MHz ADC_CLAMP_CTRL2[5]=1: ADC_DCRESTORE_CTRL[2:1]= 00:38 MHz, 01:63 MHz, 10:96 MHz, 11:131 MHz	
ADC_DCR_CTRL[1]	1	R/W	0	Reserved	
ADC_DCR_CTRL[0]	0	R/W	0	Reserved	

Register:: ADC_CLAMP_CTRL0[7:0] 0XD4					
Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTR_L0[7:6]	7:6	R/W	0	Reserved for R channel Common-mode control ckt selection for PGA input	
ADC_CLAMP_CTR_L0[6]	6	R/W	0	Reserved	
ADC_CLAMP_CTR_L0[5]	5	R/W	0	Reserved	
ADC_CLAMP_CTR_L0[4]	4	R/W	0	SOG0 Clamp Enable(0:Disable 1:Enable)	
ADC_CLAMP_CTR_L0[3:2]	3:2	R/W	0	Reserved for G channel Common-mode control ckt selection for PGA input	
ADC_CLAMP_CTR_L0[2]	2	R/W	0	Reserved	
ADC_CLAMP_CTR_L0[1]	1	R/W	0	Reserved	
ADC_CLAMP_CTR_L0[0]	0	R/W	0	Reserved	

Register:: ADC_CLAMP_CTRL1[7:0] 0XD5					
Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTR_L1[7:6]	7:6	R/W	0	Reserved for B channel Common-mode control ckt selection for PGA input	
ADC_CLAMP_CTR_L1[6]	6	R/W	0	Reserved	
ADC_CLAMP_CTR_L1[5]	5	R/W	0	Reserved	
ADC_CLAMP_CTR_L1[4]	4	R/W	0	Reserved Reserved	
ADC_CLAMP_CTR_L1[3]	3	R/W	0	Bias Current of ADC_REG_OP =(PORB_33V*ADC_CLAMP1[3]) (0: Normal Mode(1mA), 1: Low Standby Mode(0.25mA)) Reserved	
ADC_CLAMP_CTR_L1[2]	2	R/W	0	SOG0 Bias Current Source (0: from POR, 1: from ADC)	
ADC_CLAMP_CTR_L1[1]	1	R/W	0	SOG0 clamp -300mV (0: normal clamp 1:clamp -300m) //IR	
ADC_CLAMP_CTR_L1[0]	0	R/W	0	Bias Current of SOG0 0: Normal mode 1: Low Standby mode	

Register:: ADC_CLAMP_CTRL2[7:0]	0XD6
---------------------------------	------

Name	Bit	R/W	Default	Description	Config
ADC_CLAMP_CTR_L2[7:6]	7:6	R/W	0b01	SOG0 DC restore resister (00:open 01:500k 10:1M 11:5M) , 500K/1M are Poly R	
ADC_CLAMP_CTR_L1[5:4] ADC_CLAMP_CTR_L1[5]	5:4	R/W	0b01 0b0	Reserved SF LPF BW control (ADC_CLAMP_CTRL2[5] works together with DC_DCR_CTRL[2:1]) If ADC_IBIAS4[3]=0, SF LPF is disabled. If ADC_IBIAS4[3]=1, SF LPF is enabled, the setting is as follows: ADC_CLAMP_CTRL2[5]=0: ADC_DCR_CTRL[2:1]= 00:73 MHz, 01:158 MHz, 10:250 MHz, 11:340 MHz ADC_CLAMP_CTRL2[5]=1: ADC_DCR_CTRL[2:1]= 00:38 MHz, 01:63 MHz, 10:96 MHz, 11:131 MHz	
ADC_CLAMP_CTR_L1[4]	4	R/W	0b1	Reserved	
ADC_CLAMP_CTR_L1[3]	3	R/W	0 0b1	RGB input range adjust (0: 0.5V-1.0V, 1:0.25V-1.25V)	
ADC_CLAMP_CTR_L1[2]	2	R/W	0	Red channel clamp to top (0: normal 1: top)	
ADC_CLAMP_CTR_L1[1]	1	R/W	0	Green channel clamp to top (0: normal 1: top)	
ADC_CLAMP_CTR_L1[0]	0	R/W	0	Blue channel clamp to top (0: normal 1: top)	

Register::ADC_SOG_DAC_SOY_CONTROL[7:0] 0XD7					
Name	Bit	R/W	Default	Description	Config
Reserved	7:6	---	0b00	Reserved	
ADC_SOG0_DAC[5:0]	5:0	R/W	0b100000	SOG0 DAC input	

Address:D8 PTNPOS_H			Default: 00h
Bit	Mode	Function	
7:4	R/W	Test Pattern V Position Register [11:8] —Assign the test pattern digitized position in line after V_Start.	
3:0	R/W	Test Pattern H Position Register [11:8] —Assign the test pattern digitized position in pixel after H_Start.	

Address:D9 PTNPOS_V_L		
Bit	Mode	Function
7:0	R/W	Test Pattern V Position Register [7:0] —Assign the test pattern digitized position in line after V_Start..

Address:D4 PTNPOS_H_L		
Bit	Mode	Function
7:0	R/W	Test Pattern H Position Register [7:0] —Assign the test pattern digitized position in line after H_Start..

Use PTNPOS to assign the pixel position after HSYNC leading edge that input signal digitized. Each time the PTNPOS is written, the digitized results will be loaded into PTNRD, PTNGD and PTNBD. For test issue, make the input signal a fixed pattern before PTNPOS is written. Then the same digitized output will be got.

Address:D8 PTNRD		
Bit	Mode	Function
7:0	R	Test Pattern Red Channel Digitized Result.

Address:D8 PTNGD		
Bit	Mode	Function

7:0	R	Test Pattern Green Channel Digitized Result.
-----	---	---

Address: DD PTNBD

Bit	Mode	Function
7:0	R	Test Pattern Blue Channel Digitized Result.

Address: DE TEST_PATTERN_CTRL Default: 00h

Bit	Mode	Function
7	R/W	Enable Test 0: Finish (and result sequence is R-G-B) (Default) 1: Start
6:0	--	Reserved to 0

Register:: REV_REG0[7:0]					0xD8
Name	Bit	R/W	Default	Description	Config
REV_REG0[7]	7	R/W	0b1	refgep' ckt P-side cascode on/off selection 0: off, 1:on(default)	
REV_REG0[6]	6	R/W	0b1	refgep' ckt N-side cascode on/off selection 0: off, 1:on(default)	
REV_REG0[5]	5	R/W	0b0	DAC for refgen & vmidi,voffset 's internal current multiply by 2(improve DAC's PSRR@10M) 0: not multiply (default), 1:multiplied by 2	
REV_REG0[4]	4	R/W	0b0	DAC for refgen & vmidi,voffset 's internal current mirror'bias passing a large R(improve DAC's PSRR @ 10M) 0: without R(default), 1:with R	
REV_REG0[3]	3	R/W	0b1	DCGEN's output voltage passing a LPF(improve vmidi,voffset's PSRR @ 10M) 0: without LPF, 1:with LPF(default)	
REV_REG0[2]	2	R/W	0	REV_REG0[2]=0 (old mode): ADC_SOG_CMP[4]=0: Vmidi from RGB Bandgap , Voffset from RGB Bandgap ADC_SOG_CMP[4]=1: Vmidi from Gain_Cal_DAC3B , Voffset from Gain_Cal_DAC3B REV_REG0[2]=1 (new mode): ADC_SOG_CMP[4]=0: Vmidi from RGB Bandgap , Voffset from RGB Bandgap ADC_SOG_CMP[4]=1: Vmidi from Gain_Cal_DAC3B , Voffset from Gain_Cal_DAC3B	
REV_REG0[1:0]	2:0	R/W	0b000	Reserved	

Register:: REV_REG1[7:0]					0xD9
Name	Bit	R/W	Default	Description	Config
REV_REG1[7]	7	R/W	0b0	reserved for choose ADC with or without PGA(improve noise performance)	
REV_REG1[6:0]	6:0	R/W	0b1110000	Reserved	

Register:: ADC_POWER2[7:0]	0xDA
-----------------------------------	-------------

Name	Bit	R/W	Default	Description	Config
ADC_POWER2[7]	7	R/W	0b0	ADC 1.2V Generated by Resistor, PS/PD mode (0: Disable, 1: Enable)	
ADC_POWER2[6]	6	R/W	0b0	Test Output Selection Vbg for Testing, valid only when ADC_TEST[6:4]=000; SOGIN0(0: X, 1:Vbg)	
ADC_POWER2[5]	5	R/W	0b0	Bias Current of ADC_SF: ADC_POWER2[5] works together with ADC_IBIAS3[7:6] If ADC_POWER2[5]=0 ADC_IBIAS3[7:6]= 00:15u,01:20u (Default),10:25u,11:30u, If ADC_POWER2[5]=1 ADC_IBIAS3[7:6]= 00:5u,01:10u,10:35u,11:40u	
ADC_POWER2[4]	4	R/W	0b0	ADC Regulator Output Voltage Switch (0: 1.3V not short to ground 1: 1.3V short to ground) If use internal ADC Regulator, PS/PD mode set ADC_POWER2 [4]=1	
ADC_POWER2[3]	3	R/W	0b0	This bit is valid only when ADC_POWER2[0]=1 LDO_ADC: Regulator for Pipeline ADC & Bias Power On (0:disable, 1:enable)	
ADC_POWER2[2]	2	R/W	0b0	This bit is valid only when ADC_POWER2[0]=1 LDO_REF: Regulator for VREF Power On (0:disable, 1:enable)	
ADC_POWER2[1]	1	R/W	0b0	This bit is valid only when ADC_POWER2[0]=1 ADC VCM Power on (0:disable, 1:enable)	
ADC_POWER2[0]	0	R/W	0b0	If ADC_POWER2[0] = 0 ADC VCM & ADC Regulator & Band-gap Power On control by ADC_POWER[3] (0: Power Down 1: Power On) If ADC_POWER2[0] = 1 Band-gap Power On control by ADC_POWER[3] (0: Power Down 1: Power On) And ADC VCM Power on control by ADC_POWER2[1] LDO_REF: Regulator Power On control by ADC_POWER2[2] LDO_ADC: Regulator Power on control by ADC_POWER2[3]	

Register::: ADC_CTL [7:0]					0xDB
Name	Bit	R/W	Default	Description	Config
ADC_CTRL[7]	7	R/W	0	en_pd_delay for so-called CM Oscillation Issue. 0: bypass pd_delay; 1: enable pd delay	
ADC_CTRL[6:5]	6:5	R/W	2b'01	REG_VCM_SHI for SH Input CM Clamp to avoid so-called cm oscillation issue:	

				00: Vcm_shi=0.9V; 01: 1.3V; 10: 1.6V; 11:2.0V	
ADC_CTRL[4]	4	R/W	0	Voffset adjustment depends on SH gain. 0: SH=1.1, voffset step 1: SH=1.35, voffset step*1.1/1.35	
ADC_CTL[3]	3	R/W	0	ib_vb adjustment (for bootstrap switch, vb adjustment) 0: ib_vb=30uA; 1: ib_vb=40uA	
ADC_CTL[2]	2	R/W	1	SH/MDAC1 Opamp input CM Vcmi Biasing Current Control for driving capability 0: driving capability x1; 1: driving capability x2	
ADC_CTL[1:0]	1:0	R/W	0b00	SH Opamp Compensation Capacitor (Cc) Selection (for Noise Reduction & Phase Margin) 00: normal (Cc~1.3pF); 01: +0.2pF, (suggest condition: ADC_CTL_RGB[7:4] =“0100”时, ADC_CTL[1:0]=01, for PM Issue); 10: Cc +0.6pF; 11: Cc +0.8pF,(ADC work at low frequency [less than 50MHz], ADC_CTL[1:0]=11);	

Register::RGB offset_LSB 0xDC					
Name	Bit	R/W	Default	Description	Config
Reserved	7:3	R/W	0x0	Reserved	
ADC_OFF_RED[0]	2	R/W	0b0	Red Channel Offset Adjust[0]	
ADC_OFF_GRN[0]	1	R/W	0b0	Green Channel Offset Adjust[0]	
ADC_OFF_BLU[0]	0	R/W	0b0	Blue Channel Offset Adjust[0]	

Register:: REV_REG2[7:0] 0xDD					
Name	Bit	R/W	Default	Description	Config
REV_REG2[7:6]	7:6	R/W	0b11	LPF Embedded in SH block, Changing Rsw of Sampling switches Bandwidth(00:75M, 01:150M, 10: 250M, 11:350M)	
REV_REG2[5:2]	5:2	R/W	0b110000	Reserved	
REV_REG2[1]	1		0b0	ADC 1.2V from Digital 1.2V, PS/PD Mode (0: Disable, 1: Enable)	
REV_REG2[0]	0	R/W	0b0	ADC Range Fine Tuning, 0: (vrefp-vrefn), 1: 0.95*(vrefp-vrefn)	

Register:: REV_REG3[7:0] 0xDE					
Name	Bit	R/W	Default	Description	Config
REV_REG3[7:5]	7:5	R/W	0b11110000	Reserved	
REV_REG3[4:3]	4:3		0b10	Clamp voltage setting for DC Restore Ckt 2 (REG_VDCR[1:0]) 00:200mV, 01:150mV, 10:100mV, 11:50mV	
REV_REG3[2]	2		0b0	DC Restore Ckt 2 Enable(REG_DCR2CTRL) 0:disabled, 1:enabled	
REV_REG3[1]	1		0b0	DC Restore Ckt 2 Pull Down Current Control (REG_IDCR2CTRL)	

				0:4uA, 1:12uA	
REV_REG3[0]	0		0b0	DC Restore Ckt 2 Input to ground(REG_DCR2PULLDN) 0:disabled, 1:enabled	

Address:DF~E1 reserved

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ABL(Page 0)

Address: E2 AUTO_BLACK_LEVEL_CTRL1 Default: 10h		
Bit	Mode	Function
7	R/W	ABL Mode 0: RGB (Default) 1: YPbPr
6	R/W	On-line/Off-line ABL Mode 0: Off-line (Default) 1: On-line
5:4	R/W	Width of ABL region in each line 00: 16 pixels 01: 32 pixels (Default) 10: 64 pixels 11: 4 pixels
3	R	R/Pr Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <= LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
2	R	G/Y Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <= LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
1	R	B/Pb Channel ABL Result (write clear) 0: not equal 1: equal (Black Level = Target Value) On-line mode: Black Level - Target Value <= LOCK_MGN Off-line mode: Black Level - Target Value <= EQ_MGN
0	R/W	Auto Black Level Enable (write 0 force stop) 0: Finished/Disable (Default) 1: Enable to start ABL, auto cleared after finished Cleared to 0 when off-line mode completes.

- Parameters can only be changed when EN_ABL is 0
- The on-line mode never stops unless EN_ABL is 0.
- Off-line mode completes when MAX_FRAME is measured or the result is equal.
- ABL must be disabled before switching On-line/Off-line mode and then enable again.

Address: E3 AUTO_BLACK_LEVEL_CTRL2 Default: 08h		
Bit	Mode	Function
7:5	R/W	Line averaged for each ABL adjustment 000 : 2 (Default) 001 : 4 010 : 8 011 : 16 100 : 32 101 : 64 110: Reserved 111: Reserved
4:0	R/W	Start Vertical Position of ABL in each line Determine the start line of auto-black-level after the leading edge of Vsync

Address: E4 AUTO_BLACK_LEVEL_CTRL3 Default: 10h		
Bit	Mode	Function
7:4	R/W	Y/R/G/B Target value 0000: 1 0001: 2 (Default)

		0010: 3 0011: 4 1111:16 (Pb/Pr Target level is fixed 128)
3:2	R/W	Lock Margin 00: 1 (Default) 01: 2 10: 4 11: 6
1:0	R/W	End Vertical Position of ABL measurement region [9:8] Determine the last line of auto-black-level measurement for every frame/field countd by double line

- Off-line mode rule:
Measures once for each field / frame, and the offset is the delta.
- On-line mode rule:
If (delta <= EQ_MGN) offset = 0
Else if (delta < L_MGN) offset = +/-1
Else offset = +/-L_MGN
- ADC offset is updated immediately.

Address: E5 AUTO_BLACK_LEVEL_CTRL4			Default: 0Ah
Bit	Mode	Function	
7:0	R/W	End Vertical Position of ABL measurement region [7:0] Determine the last line of auto-black-level measurement for every frame/field counted by double line.	

- Note: ABL will fail if End Vertical Position < Start Vertical Position + Average Line(CRC1[7:6])

Address: E6 AUTO_BLACK_LEVEL_CTRL5			Default: 80h
Bit	Mode	Function	
7:0	R/W	Start Position of ABL in Each Line Determine the start position of auto-black-level after the trailing edge of reference signal. (When ABL mode in YPbPr, the reference signal is input Hsync. In RGB mode, the reference signal is clamp signal.) High Byte at P0_CREF[3:0]	

- In each region, hardware compare the average value in the target region (fixed 16 input pixels after start position of ABL) with target value and add +1/-1 or +L_MGN / -L_MGN to ADC offset. (+ for greater than target value, - for smaller than target value).

Address: E7 AUTO_BLACK_LEVEL_CTRL6			Default: F8h
Bit	Mode	Function	
7:6	R/W	Large Error Margin (L_MGN) (For on-line Mode) 00: 2 01: 4 10: 6 11: 8 (Default)	
5:4	R/W	Max. Frame/Field Count (For off-line mode) 00: 4 01: 5 10: 6 11: 7 (Default)	
3	R/W	Setting Width of ABL region in each line be multiplied (P0_CRE2[5:4]) 0 : x1 1 : x4 (Default)	
2:0	R/W	Lines delayed between each measurement region (For on-line Mode) 000: 16 (Default) 001: 32 010: 64 011: 128 100: 192 101: 256 110: 384 111: 640	

Address: E8 AUTO_BLACK_LEVEL_CTRL7			Default: 60h
Bit	Mode	Function	
7	--	Reserved	
6	R/W	Equal Condition (Off-line mode) 0: To trigger status until measurement achieve Max Frame/Field Count. Reference by P0_CRE7[5:4]. 1: To trigger status once if Black Level - Target Value <= EQ_MGN. When Equal Condition is met, ABL will stop and auto clear P0_CRE2[0]. (Default)	
5	R/W	Measure Pixels Method 1: Minimum value (Default) 0: Average value	
4	R/W	Measure Error Flag Reset 0: Normal 1: Reset	
3	R	Measure Error Flag 0: Normal 1: Error (This flag is occurred when Hsync trailing edge is met during measurement.)	
2	R/W	Hsync Start Reference Select 0: HS leading edge (Default) 1: HS trailing edge	
1:0	R/W	Equal margin (EQ_MGN) 00: 0 (Default) 01: 1 10: 2 11: 3	

Address: E9 AUTO_BLACK_LEVEL_RED_VALUE		
Bit	Mode	Function
7:0	R	Minimum/Average Value of Red Channel in Test Mode (only show MSB 8bit.)

Address: EA AUTO_BLACK_LEVEL_GREEN_VALUE		
Bit	Mode	Function
7:0	R	Minimum/Average Value of Green Channel in Test Mode (only show MSB 8bit.)

Address: EB AUTO_BLACK_LEVEL_BLUE_VALUE		
Bit	Mode	Function
7:0	R	Minimum/Average Value of Blue Channel in Test Mode (only show MSB 8bit.)

Address: EC AUTO_BLACK_LEVEL_NOISE_VALUE_OF_RED_CHANNEL		
Bit	Mode	Function
7:0	R	Noise Value of Red Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

Address: ED AUTO_BLACK_LEVEL_NOISE_VALUE_OF_GREEN_CHANNEL		
Bit	Mode	Function
7:0	R	Noise Value of Green Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

Address: EE AUTO_BLACK_LEVEL_NOISE_VALUE_OF_BLUE_CHANNEL		
Bit	Mode	Function
7:0	R	Noise Value of Blue Channel in Test Mode after Equal status is triggered. (only show MSB 8bit.)

Address: EF AUTO_BLACK_LEVEL_CTRL8			Default: 01h
Bit	Mode	Function	
7:4	--	Reserved	
3:0	R/W	Start Position of ABL in Each Line [11:8] Determine the start position of auto-black-level after the trailing edge of reference signal. (When ABL mode in YPbPr, the reference signal is input Hsync. In RGB mode, the reference signal is clamp signal.) Low Byte at P0_CRE6[7:0]	

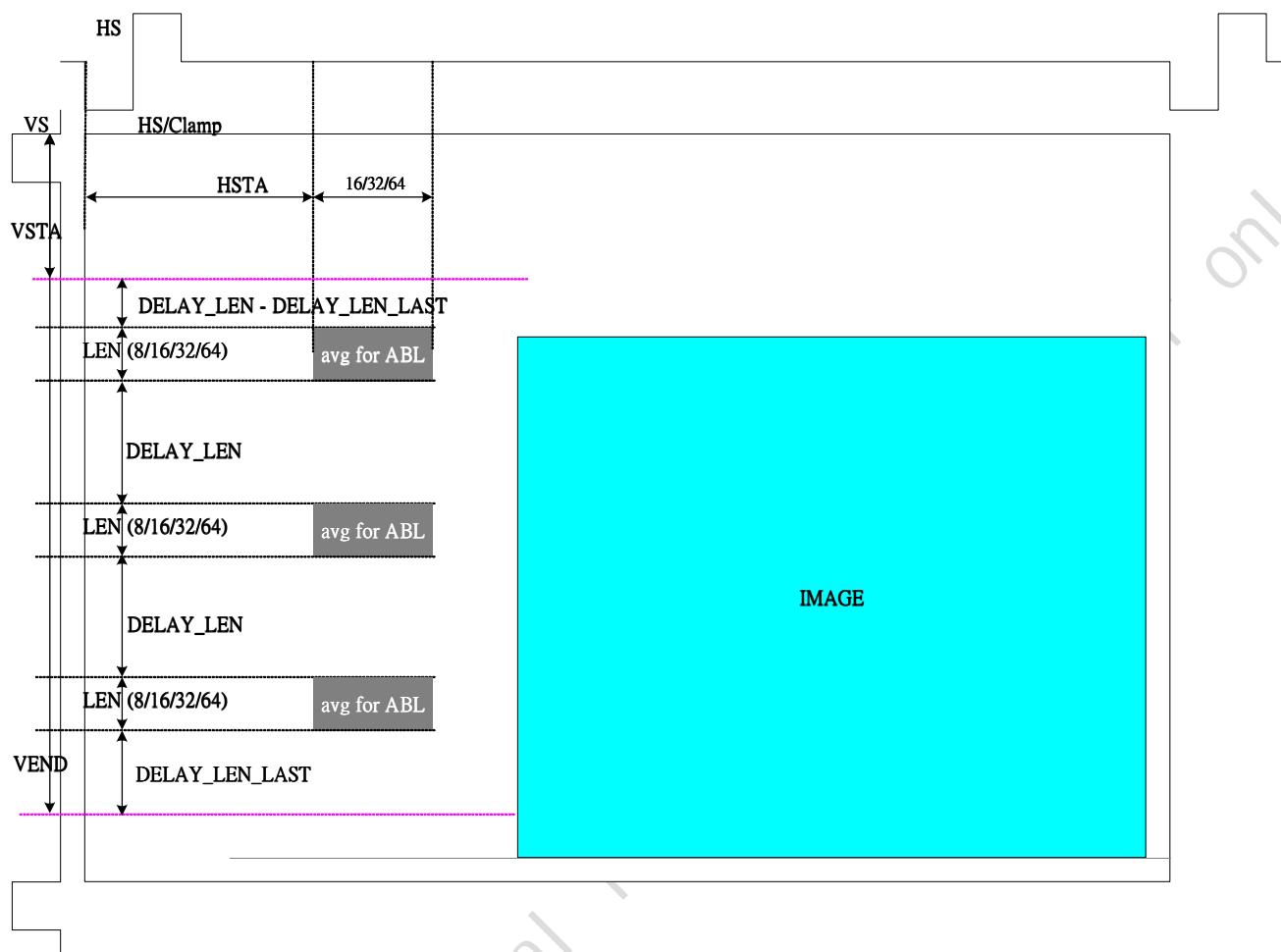


Figure-1: Auto Black Level active region – case 1

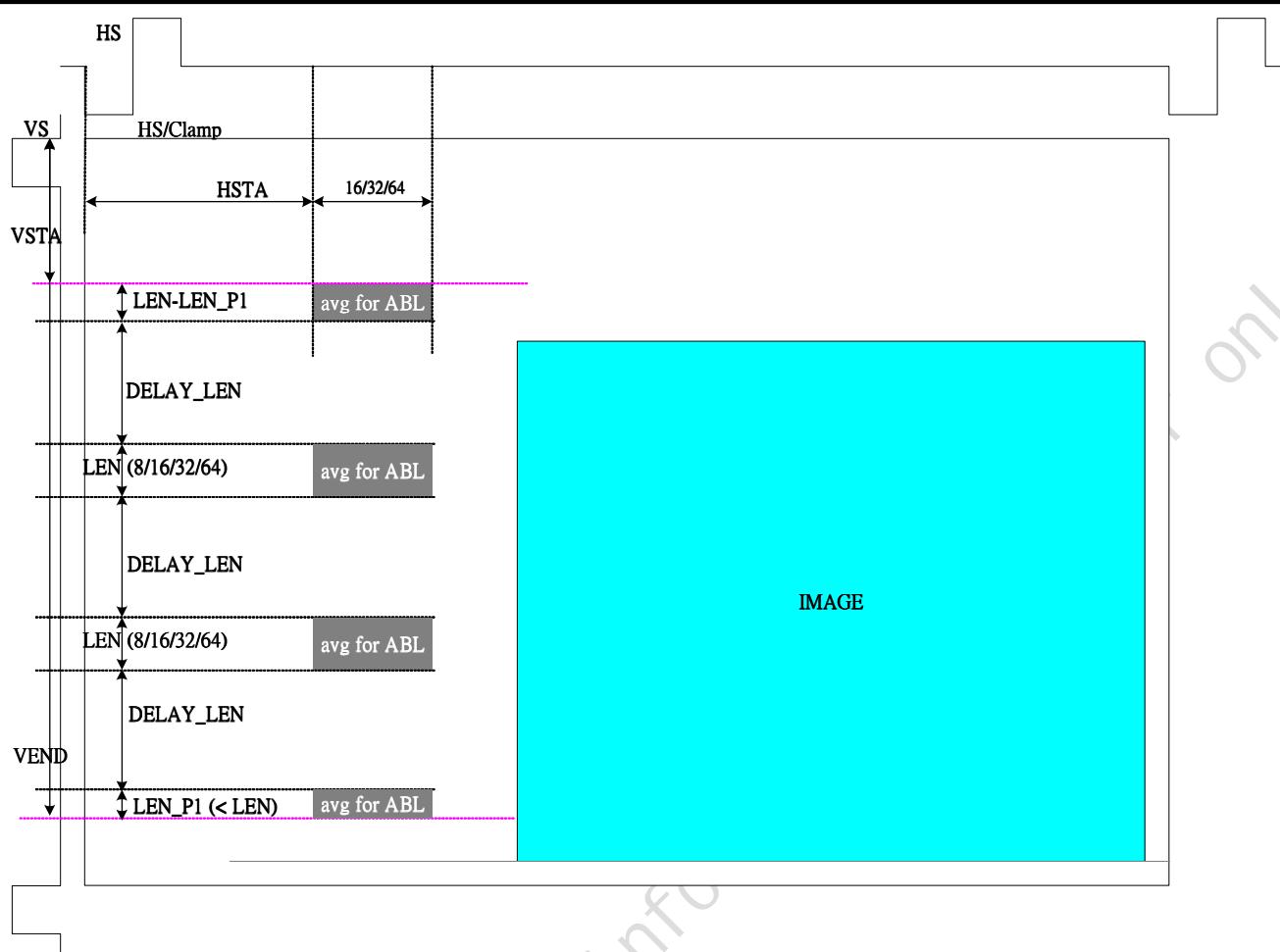


Figure-2: Auto Black Level active region – case 2

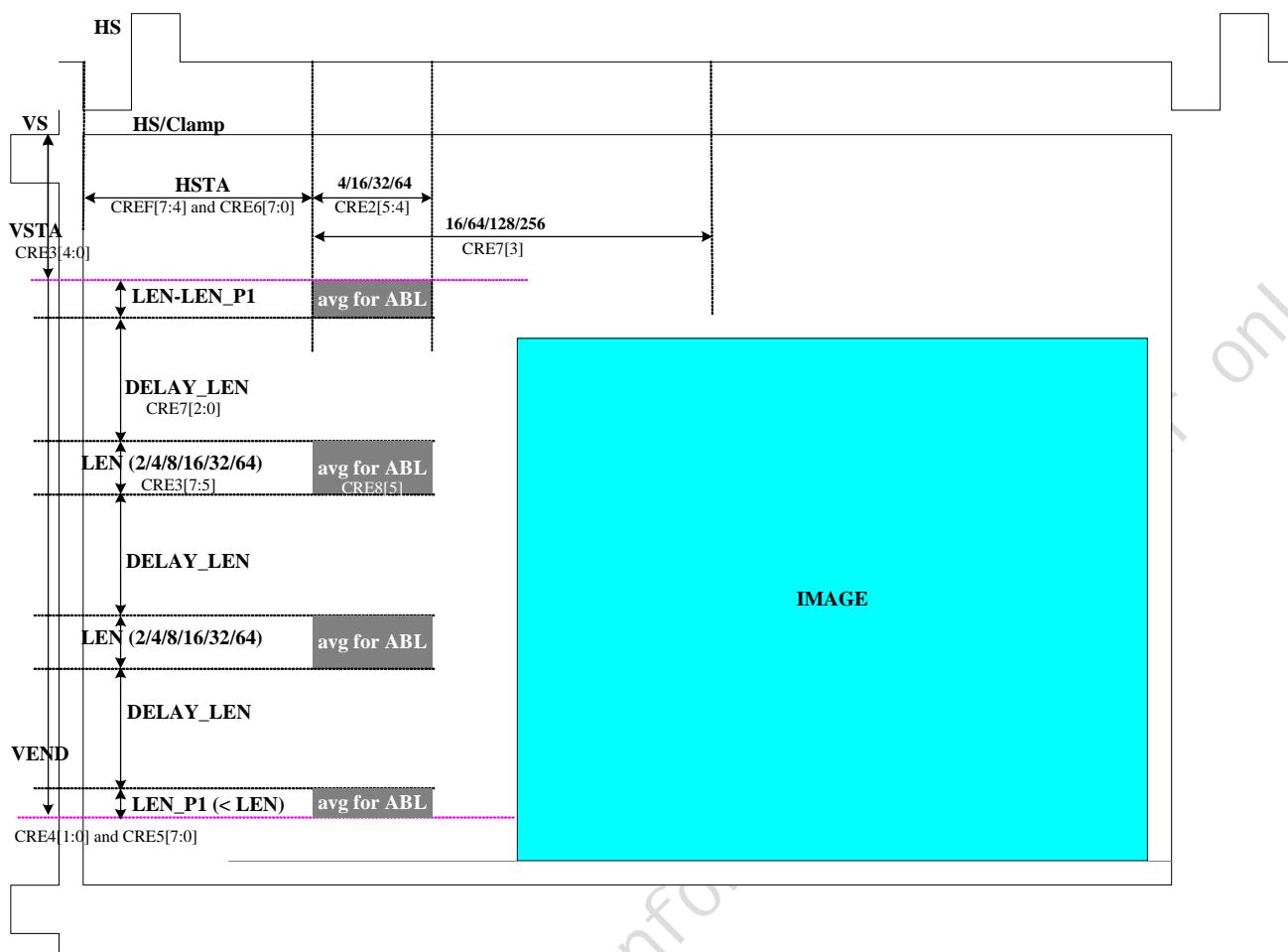
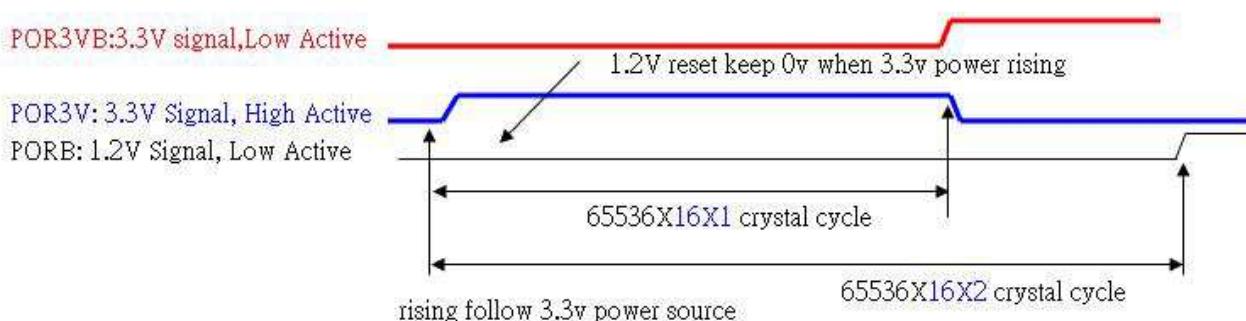
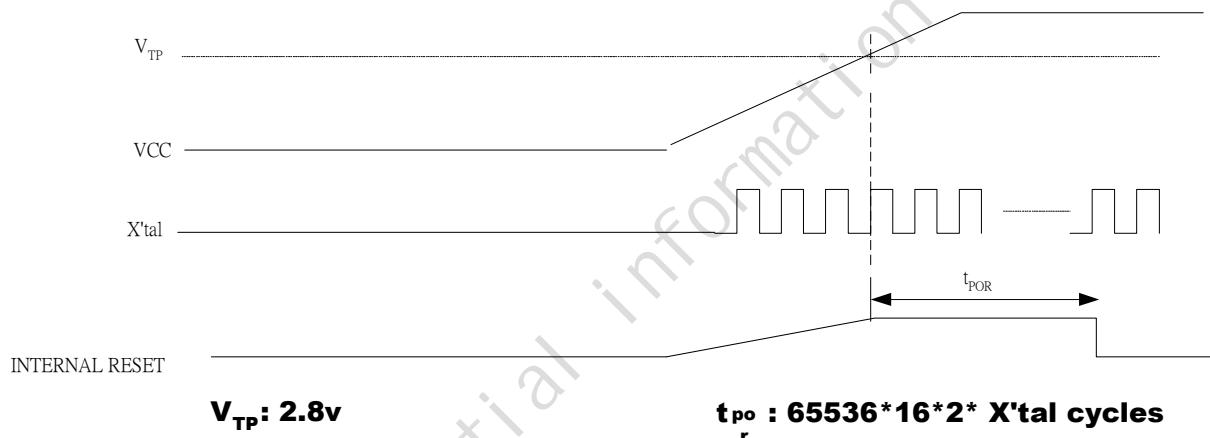


Figure-3: Auto Black Level active region – case 3

LVR(Page 0)

Register::: POWER_ON_RESET					0xF3
Name	Bits	R/W	Default	Comments	Config
Porvset	7:6	R/W	0x3	Negative Threshold Value For Power on Reset (POR reset time=160ms) (VTP=2.8V) 00: 2.4V 01: 2.6V 10: 2.5V 11: 2.7V(Default)	
Pormcuvsset	5:4	R/W	0x0	PORMCUVSET (LVR Threshold Voltage) (VTN=0.66, VTP=0.88) (Core LVR voltage: tied to 2'b00 by hardware)	
Reserved	3	R/W	0x0	Reserved	
Reserved	2	R/W	0x0	Reserved	
Adc_rglt_vol	1:0	R/W	0x0	XI/XO Pad Driving 00: Strong (default) 01: Medium 10: Medium 11: Weak	



Schmitt trigger(Page 0)

Address :F2 HS_SCHMITT_TRIGGER_CTRL2

Default:00h

Bit	Mode	Function
7	R/W	HSYNC Schmitt new 2 mode 0: Disable (Default) 1: Enable Enable this mode, Schmitt trigger threshold should be reference to table2 as follow
6:0	--	Reserved

New2 mode:(bit[7] = 1)

There is a mode of the HSYNC Schmitt trigger.

F4-bit[6]=1 (Positive HSYNC)				F4-bit[6] = 0 (Negative HSYNC)				Tolerance
F4-bit[3:2]	V _t ⁺	F4-bit[1:0]	V _t ⁻	F4-bit[3:2]	V _t ⁺	F4-bit[1:0]	V _t ⁻	
00	1.49	00	Vt+ - 1.23	00	1.91	00	Vt+ - 1.25	+ - 5%
01	1.72	01	Vt+ - 1.06	01	2.12	01	Vt+ - 1.05	+ - 5%
10	1.91	10	Vt+ - 0.84	10	2.31	10	Vt+ - 0.85	+ - 5%
11	2.12	11	Vt+ - 0.64	11	2.52	11	Vt+ - 0.64	+ - 5%

Address :F 4 HS_SCHMITT_TRIGGER_CTRL

Default:41h

Bit	Mode	Function
7	R/W	HSYNC Schmitt Power Down (Only for Schmitt trigger new mode) 0: Power down (Default) 1: Normal
6	R/W	Polarity Select 0: Negative HSYNC (high level) 1: Positive HSYNC (low level) (Default)
5	R/W	Schmitt Trigger Mode 0: Old mode (Default) 1: New mode
4	R/W	Threshold Voltage Fine Tune (only for Schmitt trigger new mode) 0: 0V (Default) 1: -0.1V
3:2	R/W	Positive Threshold Voltage
1:0	R/W	Negative Threshold Voltage

New mode:(bit[5] = 1)

- There is a mode of the HSYNC Schmitt trigger.
- New mode: Fully programmable Schmitt trigger.

The following table will determine the Schmitt Trigger positive and negative voltage:

bit[6]=1 (Positive HSYNC)				bit[6] = 0 (Negative HSYNC)			
bit[3:2]	V _t ⁺	bit[1:0]	V _t ⁻	bit[3:2]	V _t ⁺	bit[1:0]	V _t ⁻
00	1.4V	00	V _t ⁺ - 1.2V	00	1.8V	00	V _t ⁺ - 1.2V
01	1.6V	01	V _t ⁺ - 1.0V	01	2.0V	01	V _t ⁺ - 1.0V
10	1.8V	10	V _t ⁺ - 0.8V	10	2.2V	10	V _t ⁺ - 0.8V
11	2.0V	11	V _t ⁺ - 0.6V	11	2.4V	11	V _t ⁺ - 0.6V

bit[6]=1 (Positive HSYNC)				bit[6] = 0 (Negative HSYNC)				Tolerance
bit[3:2]	V _t ⁺	bit[1:0]	V _t ⁻	bit[3:2]	V _t ⁺	bit[1:0]	V _t ⁻	
00	1.49	00	Vt+ - 1.23	00	1.91	00	Vt+ - 1.25	+ - 5%
01	1.72	01	Vt+ - 1.06	01	2.12	01	Vt+ - 1.05	+ - 5%
10	1.91	10	Vt+ - 0.84	10	2.31	10	Vt+ - 0.85	+ - 5%

++	2.12	++	V _{t+} - 0.64	++	2.52	++	V _{t-} - 0.64	+ - 5%
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Notice: 2b'11 is an unsafe step under low voltage environment, not suggest using this step.

- After we get the threshold voltage by the table, we still can fine tune it:

$$\text{Final Positive Threshold Voltage} = V_t^+ - 0.1 * \text{bit}[4]$$

$$\text{Final Negative Threshold Voltage} = V_t^- - 0.1 * \text{bit}[4]$$

- The following table is measured average data of 3pes

Page0- CR[F4]	bit[6]=1 (Positive HSYNC)	bit[6]=0 (Negative HSYNC)

OLD mode:(bit[5] = 0)

bit[6]=1 (Positive HSYNC)				bit[6] = 0 (Negative HSYNC)				Tolerance
bit[1:0]	V _{t⁺}	bit[1:0]	V _{t⁻}	bit[1:0]	V _{t⁺}	bit[1:0]	V _{t⁻}	
00	no toggle	00	no toggle	00	1.91	00	1.08	+ - 5%
01	2.39	01	1.71	01		01		+ - 5%
10	2.03	10	1.30	10		10		+ - 5%
11	1.75	11	1.19	11		11		+ - 5%

MEMORY PLL (Page 0)

Register:::MPLL_M					0xF5
Name	Bits	R/W	Default	Comments	Config

MPLL_M[7:0]	7:0	R/W	4E	MPLL DPM value - 2	
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Register::MPLL_N 0xF6					
Name	Bits	R/W	Default	Comments	Config
MPLL_RESERVED1	7	R/W	0	Reserved	
MPLL_BPN	6	R/W	0	MPLLBN 0: N divider enable. 1: N divider disable, OUT=ckxtal.	
MPLL_O[1:0]	5:4	R/W	1	MPLL Output Divider 00: Div1 01: Div2 (Default) 10: Div4 11: Div8	
MPLL_N[3:0]	3:0	R/W	3	MPLL DPN value - 2	

- Assume MPLL_M=0x7D, DPM=0x7D+2=127; MPLL_N=0x0A, DPN=0x0A+2=12; Divider=1/4, F_IN = 24.576MHz.
 $F_{MPLL} = F_{IN} \times DPM / DPN \times \text{Divider} = 24.576 \times 127 / 12 / 4 = 65.024\text{MHz}$.

CRF5~CRF6 are double buffer.

Register::MPLL_CRNT 0xF7					
Name	Bits	R/W	Default	Comments	Config
MPLL_RS[2:0]	7:5	R/W	3	MPLL Loop Filter Resister Control 000: 16K 001: 18K 010: 20K 011: 22K (Default) 100: 24K 101: 26K 110: 28K 111: 30K	
MPLL_CS[1:0]	4:3	R/W	2	MPLL Loop Filter Capacitor Control 00: 18p 01: 20p 10: 24p (Default) 11: 28p	
MPLL_IP[2:0]	2:0	R/W	2	MPLL Charger Pump Current Control $I_{CP} = (2.5\mu A + 2.5\mu A * \text{bit}[0] + 5\mu A * \text{bit}[1] + 10\mu A * \text{bit}[2])$ Keep DPM/Icp constant=10.67	

Register::MPLL_WD 0xF8					
Name	Bits	R/W	Default	Comments	Config
MPLL_WDO	7	R	0	MPLL WD Status 0: Normal 1: Abnormal	
MPLL_WDRST	6	R/W	0	MPLL WD Reset 0: Normal (Default) 1: Reset	
MPLL_WDSET	5	R/W	0	MPLL WD Set 0: Normal (Default) 1: Set	
MPLL_FUPDN	4	R/W	1	MPLL Frequency Tuning 0: Freq Up 1: Freq Dn(Default)	

MPLL_STOP	3	R/W	1	MPLL Frequency Tuning 0: Disable 1: Enable (Default)	
MPLL_FREEZE	2	R/W	0	MPLL Output Freeze 0: Normal (Default) 1: Freeze Active high.	
MPLL_VCORSTB	1	R/W	0	Reset VCO 0: Normal (Default) 1: Reset Active high.	
MPLL_PWDN	0	R/W	1	Power Down MPLL 0: Power on 1: Power down(Default) Active high.	

Register::MPLL_CAL 0xF9					
Name	Bits	R/W	Default	Comments	Config
MPLL_VCOMD[1:0]	7:6	R/W	3	MPLL VCO Default Mode 00: VCO slowest 11: VCO fastest (Default)	
MPLL_CALBP	5	R/W	0	MPLL Bypass Calibration 0: Reference by Calibration Result(Default) 1: Reference by CRF9[7:6] Active high.	
MPLL_CALSW	4	R/W	0	Calibration Validated Go high after power on 1200us. 0: Reference by CR F9 [7:6] 1: Refernect by Calibration Result	
MPLL_CALLCH	3	R/W	0	Latch Calibration Go high after power on 1100us. 0: Disable Latch 1: Enable Latch	
MPLL_CMPEN	2	R/W	0	CMP Enable Go high after power on 1000us. 0: Diable CMPEN 1: Enable CMPEN	
MPLL_CP	1	R/W	0	CP Control 0: 1.77pF 1: 2.1pF	
MPLL_RESERVE	0	R/W	1	Reserved for MPLL Phase Swallow Circuit 0: Path0 1: Path1	

MCLK Spread Spectrum (Page 0)

Register:: MCLK_FINE_TUNE_OFFSET_MSB 0xFA					
Name	Bits	R/W	Default	Comments	Config

RSV_FA_74	7:4	---	0	Reserved	
MCLK_OFFSET[11:8]	3:0	R/W	0	MCLK Offset [11:8]	

Register::: MCLK_FINE_TUNE_OFFSET_LSB 0xFB					
Name	Bits	R/W	Default	Comments	Config
MCLK_OFFSET[7:0]	7:0	R/W	0	MCLK Offset [7:0]	

Register::: MCLK_SPREAD_SPECTRUM 0xFC					
Name	Bits	R/W	Default	Comments	Config
MCLK_SPREAD_RANGE	7:4	R/W	0	MCLK Spreading range (0.0~7.5%) The bigger setting, the spreading range will be bigger, but not uniform	
MCLK_FMDIV	3	R/W	0	Spread Spectrum FMDIV (SSP_FMDIV)//(0) 0: 33K 1: 66K	
MCLK_READY	2	R/W	0	Spread Spectrum Setting Ready for Writing (Auto Clear) 0: Not ready 1: Ready to write	
MCLK_DDS	1	R/W	0	DDS Spread Spectrum Test Enable 0: Disable (Default) 1: Enable	
MCLK_DDS_EN	0	R/W	0	Enable DDS Spread Spectrum Output Function 0: Disable (Default) 1: Enable	

- The “Spread Spectrum Setting Ready for Writing” means 3 kinds of registers will be set after this bit is set:
 1. MCLK spreading range
 2. Spread spectrum FMDIV
 3. MCLK offset setting

Register:::MPLL_RESULT 0xFD					
Name	Bits	R/W	Default	Comments	Config
RSV_FD_74	7:4	---	0	Reserved	
MPLL_VO2	3	R	0	MPLL CAL OUT2	
MPLL_VO1	2	R	0	MPLL CAL OUT1	
MPLL_CAL[1:0]	1:0	R	0	MPLL calibrated VCO code	

ADC PLL (Page 1)

Address: A0 PLL_DIV_CTRL			Default: 08h
Bit	Mode	Function	
7	R/W	DDS Tracking Edge 0: HS positive edge (Default) 1: HS negative edge	
6	R/W	Tracking direction inversion 0: if HS leads HSFB => phase lead => m, k ↑ (Default) 1: if HS lags HSFB => phase lag => m, k ↓	
5:4	R/W	Waiting HS lines to start counting divider for Fast Lock function 00: 4 (default) 01: 3 10: 2 11: 1	
3:2	R/W	Delay Compensation Mode 00: Mode 0 No delay from PLL phase0 to DDS pfd input 01: Mode 1 Delay the path from PLL phase0 to DDS pfd input to be around 5.8 ns 10: Mode 2 (default) Delay the path from PLL phase0 to DDS pfd input to be around 6.05 ns 11: Mode 3 Delay the path from PLL phase0 to DDS pfd input to be around 6.3 ns	
1	R/W	Reserved to 0	
0	R/W	Reserved to 0	

Address: A1 I_CODE_M			Default: 01h
Bit	Mode	Function	
7	R/W	Reserved to 0	
6:0	R/W	I_CODE[14:8]	

Address: A2 I_CODE_L			Default: 04h
Bit	Mode	Function	
7:0	R/W	I_CODE[7:0]	

Address: A3 P_CODE			Default: 20h
Bit	Mode	Function	
7:0	R/W	P_CODE[7:0]	

Address: A4 PFD_CALIBRATED_RESULTS			Default: 8'bxxxxxxxx
Bit	Mode	Function	
7	R/W	PFD Calibration Enable (auto clear when finished) Overwrite 0 to 1 return a new PFD calibrated value.	
6:4	R/W	Reserved to 0	
3:0	R	PFD Calibrated Results [11:8]	

Address: A5 PFD_CALIBRATED_RESULTS			Default: 8'bxxxxxxxx
Bit	Mode	Function	
7:0	R	PFD Calibrated Results [7:0]	

Address: A6 PE_MEASURE			Default: 8'bxxxxxxxx
Bit	Mode	Function	
7	R/W	PE Measure Enable (auto clear when finished) 0: Disable (Default) 1: Start PE Measurement, clear after finish.	
6:4	R/W	Reserved to 0	
3:0	R	PE Value Result [11:8]	

Address: A7 PE_MEARSURE			Default: 8'bxxxxxxxxx
Bit	Mode		Function
7:0	R	PE Value Result [7:0]	

Address: A8 PE_MAX_MEASURE			Default: 8'b0xxxxxxxx
Bit	Mode		Function
7	R/W	PE Max. Measure Enable 0: Disable (Default) 1: Start PE Max. Measurement	
6:4	R/W	Reserved to 0	
3:0	R	PE Max Value [11:8]	

Address: A9 PE_MAX_MEASURE			Default: 8'bxxxxxxxxx
Bit	Mode		Function
7:0	R	PE Max Value [7:0]	

Address: AA FAST_PLL_CTRL			Default: 00h
Bit	Mode		Function
7	R/W	PE Max. Measure Clear 0: clear (Default) 1: write '1' to clear PE Max. Value	
6	R/W	Enable APLL Setting 0: Disable (Default) 1: Enable (Auto clear when finished) When CRAA[5] enabled, enable this bit will write P_CODE, I_CODE, PLL M/N, PLL K, PLLDIV and DDS SUM_I at the end of input vertical data enable	
5	R/W	Enable Fast PLL Mechanism 0: Disable (Default) 1: Enable (Auto clear when finished)	
4	R/W	Force APLL Setting Enable Force to write PLL M/N, K, PLLDIV and SUM_I while got no V_ACTIVE signal 0: Disable (Default) 1: Enable (Auto clear when finished)	
3	R/W	DDS SUM_I Setting Updated Enable 0: Disable (Default) 1: Enable (Auto clear when finished)	
2	R/W	Measure SUM_I 0: Disable 1: Enable (Auto clear after finish)	
1	R/W	Enable Port AB 0: Disable Port AB Access 1: Enable Port AB Access When this bit is 0, port address will be reset to 00, and will auto increase when read or write	
0	R/W	Select SUM_I for Read 1: Select SUM_I_NOW [26:0] for read 0: Select SUM_I_PRE [26:0] for read	

Address: AB FAST_PLL_SUM_I		
Bit	Mode	Function
7:0	R/W	SUM_I_PRE (Auto Increase) 1st [00000, SUM_I [26:24]] 2nd SUM_I [23:16] 3rd SUM_I [15:8] 4th SUM_I [7:0]

SUM_I [26] is the signed bit

The operation steps are as following:
SUM_I Access Port Indexing=0,

**SUM_I Access Port Indexing=1,
SUM_I selection =1, Fast Lock Function=1**

Latch SUM_I_NOW=1

Read SUM_I_NOW from SUM_I_ACCESS_PORT for 4 times:

SUM_I_NOW [26:24]

SUM_I_NOW [23:16]

SUM_I_NOW [15:8]

SUM_I_NOW [7:0]

Calculate new freq. SUM_I_PRE and write to SUM_I_ACCESS_PORT for 4 times:

SUM_I_PRE [26:24]

SUM_I_PRE [23:16]

SUM_I_PRE [15:8]

SUM_I_PRE [7:0]

SUM_I_PRE_SET =1

Write PLL2 M/N code and DDS feed back divider

Write New P/I code

Setting Auto Load =1

Wait for next frame start or polling Reg [2E].6

Address: AC PLL_M (M Parameter Register)			Default: 19h
Bit	Mode	Function	
7:0	R/W	PLLM[7:0] (PLL DPM value – 3)	

Address: AD PLL_N (N Parameter Register)			Default: 20h
Bit	Mode	Function	
7:4	R/W	PLLSPHNEXT[3:0] (K) (default is 0000)	
3	R/W	PLLSNBP 0: N is followed by the value of REGAD [3:1] 1: N is always 1	
2:0	R/W	PLLN[2:0] (PLL DPN value – 2) (default is 000) It is supposed to be always bigger than 2	

- PLL1_N modify to only 4-bit.
- Assume PLL1_M=0x0B, P1M=0x0B+3=14; PLL1_N=0x03, P1N=0x03+2=5; K=7; F_IN = 24.576MHz. F_PLL = F_IN x ((P1M+7/16) / P1N) = 24.576 x 14.4375 / 5 = 70.9632MHz
- If the target frequency is F_ADC, the constraint of F_PLL is $(M+7/16)/N * XTCLK < F_PLL < (M+8/16)/N * XTCLK$
- Although the new dds provides +15/-16 phase margin for tracking. However it is better not to set M, N and K to be some freq. that PLL has to swallow +15/-16 phases. Because under that condition, SDM will get saturation problem.
- For NO shrink IC => PLLN setting will have no limitation
- For shrink IC and timing factor predicted as 0.8 => crystal clock 27 MHZ => PLLN can't be 0 while APLL VCO is lower than 167MHZ
crystal clock 24.576 MHZ => PLLN can't be 0 while APLL VCO is lower than 84 MHZ
- For shrink IC and timing factor predicted as 0.9 => crystal clock 27 MHZ => PLLN can't be 0 while APLL VCO is lower than 74 MHZ
crystal clock 24.576 MHZ => PLLN can't be 0 while APLL VCO is lower than 52 MHZ

Address: AE PLL_CRNT (PLL Current/Resistor Register)			Default: 6Fh
Bit	Mode	Function	
7:5	R/W	PLLVR [2:0] (PLL Loop Filter Resister Control) 000: 7K 001: 9.5K 010: 12K 011: 14.5K(Default) 100: 17K 101: 19.5K 110: 22K 111: 24.5K	
4:0	R/W	PLLSI [4:0] (PLL Charger Pump Current IchDpll) (Default: 00011b) Icp = 2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]+20uA*bit[3]+30uA*bit[4]	

- Keep Icp/DPM constant

Address: AF PLL_WD (PLL Watch Dog Register) Default: 09h

Bit	Mode	Function
7	R	PLLSTATUS (PLL WD Status) 0: Normal (Default) 1: Abnormal
6	R/W	PLLWDRST (PLL WD Reset) 0: Normal (Default) 1: Reset
5	R/W	PLLWDSET (PLL WD Set) 0: Normal (Default) 1: Set
4:3	R/W	PLLWDVSET[1:0] (PLL WD Voltage Set) 00: 2.46V 01: 1.92V(Default) 10: 1.36V 11: 1.00V
2	R/W	HS_dds2synp latch edge 0: falling edge (Default) 1: rising
1	R/W	Reset DDS 0: normal (Default) 1: reset whole DDS
0	R/W	PLLPWDN (PLL Power Down) 0: Normal Run 1: Power Down (Default)

- HSFB_dds2synp & HS_dds2synp will be both sampled by AF [2]

Address: B0 PLL_MIX Default: 8'b0000_000x

Bit	Mode	Function
7	R/W	PLLSVR3
6	---	Reserved to 0
5	R/W	PLLSVC3
4	---	Reserved to 0
3	---	Reserved to 0
2:1	R/W	ADCKMODE [1:0] (ADC Input Clock Select Mode) 00: Single Clock Mode (Default) 01: Single Inverse-Clock Mode 10: External Clock Mode 11: Dual Clock Mode (1x and 2x Clock)
0	R	Swallow phase enable (K mask disabled) The pll can't enable swallow phase function while pll just be power up. Waiting for 64 clock cycles then start to enable phase swallow function. While power down, the counter will be reset. While power up, the counter start to work

Address: B1 PLLDIV_H Default: 45h

Bit	Mode	Function
7	---	Reserved to 0
6	R/W	Phase_Select_Method 0: Manual 1: Look-Up-Table (default)
5	R/W	PLLPH0PATH 0: Short Path (Default) 1: Long Path (Compensate PLL_ADC path delay)
4	R/W	PLLD2 0: ADC CLK=1/2 VCO CLK (Default) 1: ADC CLK=1/4 VCO CLK
3:0	R/W	PLL Divider Ratio Control. High-Byte [11:8]. (Default: 5h)

Address: B2 PLLDIV_L
Default: 2Eh

Bit	Mode	Function
7:0	R/W	PLL Divider Ratio Control, Low-Byte [7:0]. PLLDIV should be double buffered when PLLDIV_LO changes and IDEN_STOP occurs.

- This register determines the number of output pixel per horizontal line. PLL derives the sampling clock and data output clock (DCLK) from input HSYNC. *The real operation Divider Ratio = PLLDIV+1*
- The power up default value of PLLDIV is 053Fh(=1343, VESA timing standard, 1024x768 60Hz, Horizontal time).
- The setting of PLLDIV must include sync, back-porch, left border, active, right border, and front-porch times.
- Control-Register B1 & B2 will filled in when Control-Register B2 is written.

Address: B3 PLLPHASE_CTRL0 (Select Phase to A/D)
Default: 30h

Bit	Mode	Function
7	R/W	PLLD2X control (Default=0)
6	R/W	PLLD2Y control (Default=0)
5	R/W	PLLX (PLL X Phase control) (Default=1)
4	R/W	PLLY (PLL X Phase control) (Default=1)
3:0	R/W	PLLSCK [4:1] (PLL 32 Phase Pre-Select Control) (Default=0h)

Address: B4 PLLPHASE_CTRL1 (Select Phase to A/D)
Default: 00h

Bit	Mode	Function
7	R/W	PLLSCK [0] (PLL 32 Phase Pre-Select Control) (Default=0)
6	R/W	MSB of 128 phase (Only for ADC CLK=1/4 VCO CLK) (Default=0)
5:0	R/W	Phase Select the index of Look-Up-Table[5:0] (Default=0)

- When Phase_Select_Method=1, Phase is selected by CRB4[6:0].
- When Phase_Select_Method=0, PLLD2X, PLLD2Y, PLLX, PLLY, PLLSCLK[4:0] Should be double buffered when PLLSCK[0] is updated

Address: B5 PLL_PHASE_INTERPOLATION
Default: 50h

Bit	Mode	Function
7:6	R/W	PLL Phase Interpolation Control Load (Default: 01)
5:3	R/W	PLL Phase Interpolation Control Source (Default: 010)
2:1	R/W	PLL Add Phase Delay 00: Original phase selected by X,Y and 16-phase pre-select 01-11: Add 1-3 delay to Original phase selected by X,Y and 32-phase pre-select
0	R/W	Reserved to 0

Phase	[XY ^ ^ ^ ^ ^]	Phase	[XY ^ ^ ^ ^ ^]	Phase	[XY ^ ^ ^ ^ ^]	Phase	[XY ^ ^ ^ ^ ^]
0	[11 00000]	16	[01 10000]	32	[10 00000]	48	[00 10000]
1	[11 00001]	17	[01 10001]	33	[10 00001]	49	[00 10001]
2	[11 00010]	18	[01 10010]	34	[10 00010]	50	[00 10010]
3	[11 00011]	19	[01 10011]	35	[10 00011]	51	[00 10011]
4	[11 00100]	20	[01 10100]	36	[10 00100]	52	[00 10100]
5	[11 00101]	21	[00 10101]	37	[10 00101]	53	[00 10101]
6	[11 00110]	22	[00 10110]	38	[10 00110]	54	[00 10110]
7	[11 00111]	23	[01 10111]	39	[10 00111]	55	[00 10111]
8	[11 01000]	24	[01 11000]	40	[10 01000]	56	[00 11000]
9	[11 01001]	25	[01 11001]	41	[10 01001]	57	[00 11001]
10	[01 01010]	26	[10 11010]	42	[10 01010]	58	[11 11010]
11	[01 01011]	27	[10 11011]	43	[10 01011]	59	[11 11011]
12	[01 01100]	28	[10 11100]	44	[00 01100]	60	[11 11100]
13	[01 01101]	29	[10 11101]	45	[00 01101]	61	[11 11101]
14	[01 01110]	30	[10 11110]	46	[00 01110]	62	[11 11110]
15	[01 01111]	31	[10 11111]	47	[00 01111]	63	[11 11111]

Address: B6 P_CODE mapping methods
Default: 18h

Bit	Mode	Function
7:6	R/W	Mapping method: 00: normal mapping P_CODE x G value (default)

		01: nonlinear mapping I 10: nonlinear mapping II 11: nonlinear mapping III	smaller than Q(PE) P_CODE x	2 1	4 2	8 4	16 8	32 32	64 128	128 128
			P_CODE x	1	2	2	8	32	256	256
			P_CODE x	1	2	8	16	32	128	512
5:2	R/W	G value 0000: 0 0001: 1 0010: 4 0011: 16 0100: 64 0101: 128 0110: 256 (default) 0111: 512 1000: 1/4 1001: 1/16 1010: 1/64 1011: reserved to 0 1100: reserved to 0 1101: reserved to 0 1110: reserved to 0 1111: reserved to 0								
1	R/W	<i>Adaptive tracking enable for I_CODE</i> 0: disable to use adaptive I_CODE (default) 1: enable to use adaptive I_CODE								
0	R/W	<i>Adaptive tracking enable for P_CODE</i> 0: disable to use adaptive P_CODE (default) 1: enable to use adaptive P_CODE								

Address: B7 PE tracking method Default: 02h

Bit	Mode	Function
7:6	R/W	Threshold value of Q (PE) to decide if starting adaptive tracking 00: 2 (default) 01: 4 10: 8 11: 15
5:4	R/W	Threshold times to decide if starting adaptive tracking while Q(PE) < Threshold value successively 00: 3 (default) 01: 7 10: 11 11: 15
3	R/W	Mask high speed testing pins (test1out, test2out, fav4) 0: normal 1: mask
2	R/W	Adaptive tracking enable => refer to B6 [1:0] to decide if I_CODE or P_CODE enables adaptive tracking or not 0: disable (default) 1: enable
1:0	R/W	Decrease ratio for adaptive tracking Adaptive tracking will be enabled while getting Q (PE) <=2 for over 8 times, and it will be triggered only under delay-chain mode 00: 1/2 01: 1/4 10: 1/8 (default) 11: 1/16

Address: B8 DDS_MIX_1 Default: 06h

Bit	Mode	Function
7:6	R	DDS tracking state [1:0] 00: not lock

		01: lock 10: unlock but not using new tracking mode yet 11: unlock & using new tracking mode
5	R/W	Reserved to 0
4	R/W	Delay 1 cycle for PE delay chain reset (To avoid PE delay chain reset while lock statuses transfers condition) 0: Disable 1: Enable
3:1	R/W	Judge threshold lock already => while Q (PE) keep smaller than threshold for 32 HS 000: 3 001: 6 010: 9 011: 11 (default) 100: 23 101: 46 110: 91 111: 171
0	R	PLL lock already 0: not lock already 1: lock already

Address: B9 DDS_MIX_2 Default: 00h

Bit	Mode	Function
7:0	R/W	P_code_max[16:9] Set p_code_max value to clamp the GAIN of APLL

Address: BA DDS_MIX_3 Default: 00h

Bit	Mode	Function
7:0	R/W	P_code_max[8:1] Set p_code_max value to clamp the GAIN of APLL

Address: BB DDS_MIX_4 Default: 1Bh

Bit	Mode	Function
7	R/W	P_code_max[0] Set p_code_max value to clamp the GAIN of APLL
6	R/W	New mode enable 0: disable new mode tracking (default) 1: enable new mode tracking
5:3	R/W	New mode enable threshold 000: 8 001: 20 010: 60 011: 120 (default) 100: 200 101: 450 110: 800 111: 1200
2:0	R/W	New mode lock threshold=> while Q (PE) keep smaller than threshold for 32 HS 000: 3 001: 6 010: 9 011: 11 (default) 100: 23 101: 46 110: 91 111: 171

- New mode enable threshold should be larger than new mode lock threshold, otherwise, the track state will always be at lock state and new mode function will not be enabled while new mode enable threshold < Q (PE) < new mode lock threshold

Address: BC
DDS_MIX_5
Default: A0h

Bit	Mode	Function
7:6	R/W	Delay chain length select (only valid while new mode enable and track state is 01 10 11) 00: cnt=7 => 59.6ns 01: cnt=15 => 117ns 10: cnt=23 => 184.4ns (default) 11: cnt=31 => 246.8ns
5:4	R/W	Phase error sample period choose (only valid while new mode enable and track state is 01 10 11) 00: every 1 cycle sample 01: every 2 cycle sample 10: every 3 cycle sample (default) 11: every 4 cycle sample
3	R/W	Delay chain reset period select 0: short reset (2ns) (default) 1: long reset (1 fbck)
2	R/W	Reset delay chain saturation flag 0: normal (default) 1: reset flag
1	R	Delay chain saturation flag 0: not saturate 1: saturate => it need to enlarge the sample period or set bigger N code
0	R/W	APLL_free_run enable 0: normal state (default) 1: force APLL to free run state

- While we got delay chain saturation flag 1'b1, that means that the big jitter is bigger than what we image and we have to reset the delay chain length setting BC [7:6]. Also we have to enlarge the sampling period & delay chain length
- The choice for sampling period will be set by the rule as following:
(Delay chain length * 78 +50) * each tap delay + 10(ns) must be < N * TxCLK * sample period
if delay chain saturation flag goes high, then we must enlarge the delay chain length & set bigger sampling period
- While we enable free run mode, DDS will keep reset status until disable free run

Address: BD
DDS_MIX_6

Bit	Mode	Function
7:0	R	Final M code to APLL

- While we like to read final M code & K code, we have to enable measure PE 9E[7] first. Otherwise we will get glitch value

Address: BE
DDS_MIX_7
Default: 00h

Bit	Mode	Function
7:4	R	Final K code to APLL
3:1	R/W	Change mode threshold => triggered by any Q (PE) > threshold 000: 600 (default) 001: 850 010: 1100 011: 1350 100: 1600 101: 1850 110: 2100 111: 2350
0	R/W	new_mode_i_code_en 0: while new mode enable, I code will have no effect on SUM_I. All phase error will be compensated by P code (default) 1: while new mode enable, I code will be operated as normal state

- For APLL interrupt status that include 4 different types:

No lock: initial is 1 => over lock threshold B8 [3:1] => 1

Wait state: initial is 1 => valid only while u enable new mode => over new mode enable threshold BB [5:3] => 1

New mode state: initial is 1 => valid only while u enable new mode => over new mode lock threshold BB [2:0] => 1

Change mode happen state: initial is 1 => over change mode threshold BE [3:1] => 1

DISPLAY PLL (Page 1)

Register:::DPLL_M 0xBF					
Name	Bits	R/W	Default	Comments	Config
DPLL_M[7:0]	7:0	R/W	4E	DPLL DPM value - 2	

Register:::DPLL_N 0xC0					
Name	Bits	R/W	Default	Comments	Config
DPLL_RESERVED1	7	R/W	0	Reserved	
DPLL_BPN	6	R/W	0	DPLL BPN 0: N divider enable. 1: N divider disable, OUT=ckxtal.	
DPLL_O[1:0]	5:4	R/W	1	DPLL Output Divider 00: Div1 01: Div2 (Default) 10: Div4 11: Div8	
DPLL_N[3:0]	3:0	R/W	3	DPLL DPN value - 2	

- Assume DPLL_M=0x7D, DPM=0x7D+2=127; DPLL_N=0x0A, DPN=0x0A+2=12; Divider=1/4, F_IN = 24.576MHz.
 $F_{DPLL} = F_{IN} \times DPM / DPN \times \text{Divider} = 24.576 \times 127 / 12 / 4 = 65.024\text{MHz}$.

CRBF~CRC0 are double buffer.

Register:::DPLL_CRNT 0xC1					
Name	Bits	R/W	Default	Comments	Config
DPLL_RS[2:0]	7:5	R/W	3	DPLL Loop Filter Resister Control 000: 16K 001: 18K 010: 20K 011: 22K (Default) 100: 24K 101: 26K 110: 28K 111: 30K	
DPLL_CS[1:0]	4:3	R/W	2	DPLL Loop Filter Capacitor Control 00: 18p 01: 20p 10: 24p (Default) 11: 28p	
DPLL_IP[2:0]	2:0	R/W	2	DPLL Charger Pump Current Control $I_{CP} = (2.5\mu A + 2.5\mu A * \text{bit}[0] + 5\mu A * \text{bit}[1] + 10\mu A * \text{bit}[2])$ $I_{CP} = 0.5 * M/N * 14.318/27$	

DCLK Spread Spectrum (Page 1)

Register:::DPLL_WD 0xC2					
Name	Bits	R/W	Default	Comments	Config
DPLL_WDO	7	R	0	DPLL WD Status 0: Normal 1: Abnormal Write 1 to clear.(WD enable when DPLL power on)	wclr_out
DPLL_WDRST	6	R/W	0	DPLL WD Reset 0: Normal (Default) 1: Reset	
DPLL_WDSET	5	R/W	0	DPLL WD Set 0: Normal (Default) 1: Set	
Revered	4	R/W	0	Reserved	
DPLL_STOP	3	R/W	1	DPLL Frequency Tuning 0: Disable 1: Enable (Default)	
DPLL_FREEZE	2	R/W	0	DPLL Output Freeze 0: Normal (Default) 1: Freeze Active high.	
DPLL_VCORSTB	1	R/W	0	Reset VCO 0: Normal (Default) 1: Reset Active high.	
DPLL_PWDN	0	R/W	1	Power Down DPLL 0: Power on 1: Power down(Default) Active high.	

Register:::DPLL_CAL 0xC3					
Name	Bits	R/W	Default	Comments	Config
DPLL_VCOMD[1:0]	7:6	R/W	3	DPLL VCO Default Mode 00: VCO slowest 11: VCO fastest (Default)	
DPLL_CALBP	5	R/W	0	DPLL Bypass Calibration 0: Reference by Calibration result(Default) 1: Reference by CRC3[7:6] Active high.	
DPLL_CALSW	4	R/W	0	Calibration Validated Go high after power on 1200us. 0: Reference by CRC3[7:6] 1: Refernect by cal result	
DPLL_CALLCH	3	R/W	0	Latch Calibration Go high after power on 1100us. 0: Disable Latch 1: Enable Latch	
DPLL_CMPEN	2	R/W	0	CMP Enable Go high after power on 1000us. 0: Diable CMPEN 1: Enable CMPEN	
DPLL_CP	1	R/W	0	CP Control 0: 1.77pF 1: 2.1pF	
DPLL_RESERVE	0	R/W	1	Reserved for DPLL Phase Swallow Circuit 0: Path0	

			1: Path1	
--	--	--	----------	--

Register:: Initial DCLK_FINE_TUNE_OFFSET_MSB 0xC4				
Name	Bits	R/W	Default	Comments
DPLL_LINEAR_CHANGE	7	R/W	0	Linear change offset value function 0 : disable 1: enable (auto clear when finish) It should work on DDS Spread Spectrum Output function enable. When function is done, the initial offset and DPLLUPDN value would be the target offset and DPLLUPDN value.
DPLL_EVEN_OLD_EN	6	R/W	0	Only Even / Odd Field Mode Enable 0: Disable (Default) 1: Enable
DPLL_EVEN_OD_SEL	5	R/W	0	Even / Odd Field Select 0: Even (Default) 1: Odd
DPLL_FUPDN	4	R/W	1	DPLLFUPDN (DPLL Frequency Tuning) 0: Freq Up 1: Freq Down (Default)
DCLK_OFFSET[11:8]	3:0	R/W	0	Initial DCLK Offset [11:8] in Fixed Last Line DVTOTAL & DHTOTAL

Register:: Initial DCLK_FINE_TUNE_OFFSET_LSB 0xC5				
Name	Bits	R/W	Default	Comments
DCLK_OFFSET[7:0]	7:0	R/W	0	Initial DCLK Offset [7:0] in Fixed Last Line DVTOTAL & DHTOTAL

Register:: DCLK_SPREAD_SPECTRUM 0xC6				
Name	Bits	R/W	Default	Comments
DCLK_SPREAD_RANGE	7:4	R/W	0	DCLK Spreading range (0.0~7.5%) The bigger setting, the spreading range will bigger, but not uniform
DCLK_FMDIV	3	R/W	0	Spread Spectrum FMDIV (SSP_FMDIV)//(0) 0: 33K 1: 66K
DCLK_READY	2	R/W	0	Spread Spectrum Setting Ready for Writing (Auto Clear) 0: Not ready 1: Ready to write
FREQ_SYNTHESIS_SEL	1:0	R/W	0	Frequency Synthesis Select (F & F-N*dF) 00~11: N=1~4

- The “Spread Spectrum Setting Ready for Writing” means 4 kinds of registers will be set after this bit is set:
 (When 0xCA [0] = “b1 , the apply would be effective)

 1. DCLK spreading range
 2. Spread spectrum FMDIV
 3. DCLK offset setting
 4. Frequency synthesis select

Register:: EVEN_FIXED_LAST_LINE_MSB 0xC7				
Name	Bits	R/W	Default	Comments
EVEN_FIXED_LAST_LINE[11:8]	6:4	R/W	3	Even Fixed Last Line Length [11:8]
EVEN_FIXED_DVTOTAL[11:8]	3:0	R/W	0	Even Fixed DVTOTAL [11:8]

Register:: EVEN_FIXED_LAST_LINE_LSB					0xC8
Name	Bits	R/W	Default	Comments	Config
EVEN_FIXED_DVTOTAL[7:0]	7:0	R/W	0	Even Fixed DVTOTAL [7:0]	

Register:: EVEN_FIXED_LAST_LINE_LENGTH_LSB					0xC9
Name	Bits	R/W	Default	Comments	Config
EVEN_FIXED_DVTOTAL[7:0]	7:0	R/W	0	Even Fixed Last Line Length [7:0]	

- If Even / Odd mode disable, we use EVEN_FIXED_LAST only.
- If Even/Odd mode enable, the even / odd field would be reference different setting.
- Fixed last line value can't be zero, and can't smaller than DH_Sync width.

Register:: FIXED_LAST_LINE_CTRL					0xCA
Name	Bits	R/W	Default	Comments	Config
DEGLITCH	7	R/W	0	Deglitch sscg asynchronous interface data function 0: disable 1: enable	
RSV_CA_6	6	--	0	Reserved to 0	
MEASURE_PHASE	5	R/W	0	Measure the Phase about Fixed DVTOTAL & Last Line DHTOTAL Function 0 : Disable 1 : Enable (Auto clear when finish)	
MARK_PHASE_TRACKING	4	R/W	0	Mark Phase tracking about Fixed DVTOTAL & Last Line DHTOTAL Function 0 : Disable 1 : Enable	
NED_FIXED_LAST_LINE_MODE	3	R/W	0	Enable New Design Function in Fixed Last Line Mode 0: Disable (Default) 1: Enable	
DCLK_DDS	2	R/W	0	DDS Spread Spectrum Test Enable 0: Disable (Default) 1: Enable	
DCLK_FIXED_LAST_LINE_EN	1	R/W	0	Enable the Fixed DVTOTAL & Last Line DHTOTAL Function 0: Disable (Default) 1: Enable	
DCLK_DDS_EN	0	R/W	0	Enable DDS Spread Spectrum Output Function 0: Disable (Default) 1: Enable	

Procedure:

- First, we have set M/N code and then we need to tune DCLK OFFSET to achieve frame-sync, every step of offset frequency is $DCLK/2^{15}$.
- When we finished the frame-sync, we turn on CRCA[1] to let the system running in to free-run mode, at this time, the CRC7,CRC8,CRC9 are the reference DV and DH total and Fixed last Line Length.
- But the free-run mode DVS' should be close to frame-sync mode DVS to achieve pseudo-frame-sync(actually, it is free run mode now)
- Then we use CRC6[1:0] (F-N*dF) to keep DVS' and DVS very closely to achieve pseudo-frame-sync.

Notice:

- In RTD2485XD, when all the setting above is ready, then we open spread spectrum function, the DCLK OFFSET will shift, please keep the DCLK OFFSET keeps steady when we open spread spectrum function.
- In Real free-run mode, the DV_TOTAL refers to CR2B-0B/CR2B-0C, and in Fixed-Last-Line mode, and disable “Even/Odd mode” then the free-run timing DV_TOTAL refers to CRC7/CRC8, at this time CR2B-0B/CR2B-0C serve for Vsync-timeout watch dog reference.

Register:: ODD_FIXED_LAST_LINE_MSB 0xCB					
Name	Bits	R/W	Default	Comments	Config
ODD_FIXED_LAST_LINE LENG[11:8]	6:4	R/W	0	ODD Fixed Last Line Length [11:8]	
ODD_FIXED_DVTOTAL[11:8]	3:0	R/W	0	ODD Fixed DVTOTAL [11:8]	

Register:: ODD_FIXED_LAST_LINE_DVTOTAL_LSB 0xCC					
Name	Bits	R/W	Default	Comments	Config
ODD_FIXED_DVTOTAL[7:0]	7:0	R/W	0	ODD Fixed DVTOTAL [7:0]	

Register:: ODD_FIXED_LAST_LINE_LENGTH_LSB 0xCD					
Name	Bits	R/W	Default	Comments	Config
ODD_FIXED_LAST_LINE LENG[7:0]	7:0	R/W	0	ODD Fixed Last Line Length [7:0]	

Register:: DCLK_SPREAD_SPECTRUM 0xCE					
Name	Bits	R/W	Default	Comments	Config
RSV_CE_72	7:2	---	0	Reserved	
FIXED_LAST_LINE_HIT	1	R	0	Fixed Last Line Tracking time hit Field one 0:hit field zero (If field zero is odd → hit odd field) 1:hit field one (If field one is even → hit even field)	
IVS_LEAD_LAG_TO_DVS	0	R	0	IVS Lead/Lag to DVS 0 : Lag 1 : Lead	

Register:: PHASE_RESULT_MSB 0xCF					
Name	Bits	R/W	Default	Comments	Config
RSV_CF_7	7	---	0	Reserved	
PHASE_LINE[11:8]	6:4	R	0	Phase Line [11:8]	
PHASE_PIXEL[11:8]	3:0	R	0	Phase Pixel [11:8]	

Register:: PHASE_LINE_LSB 0xD0					
Name	Bits	R/W	Default	Comments	Config
PHASE_LINE[7:0]	7:0	R	0	Phase Line [7:0]	

Register:: PHASE_PIXEL_PIXEL 0xD1					
Name	Bits	R/W	Default	Comments	Config
PHASE_PIXEL[7:0]	7:0	R	0	Lead Phase Pixel [7:0]	

Register:: TARGET_DCLK_FINE_TUNE_OFFSET_MSB 0xD2					
Name	Bits	R/W	Default	Comments	Config
RSV_D2_76	7:6	--	0	Reserved	
No_dbrdy_RST_profile	5	R/W	0	0: reset profile when CRC6[2] set to 1 1: no reset profile when CRC6[2] set to 1	

TARGET_DPLLUPDB	4	R/W	0	Target DPLLUPDN (DPLL Frequency Tuning Up/Down) 0: Freq Up(Default) 1: Freq Down	
TARGET_DCLK_OFFSET[11:8]	3:0	R/W	0	Target DCLK Offset [11:8] in Fixed Last Line DVTOTAL & DHTOTAL	

Register:: TARGET_DCLK_FINE_TUNE_OFFSET_LSB 0xD3				
Name	Bits	R/W	Default	Comments
TARGET_DCLK_OFFSET[7:0]	3:0	R/W	0	Target DCLK Offset [7:0] in Fixed Last Line DVTOTAL & DHTOTAL

Register::DPLL_RESULT 0xD4					
Name	Bits	R/W	Default	Comments	Config
DPLL_REF_CLK_SEL	7	R/W	0	DPLL reference clk select: 0: xtal_clk 1: m2pll_clk/Div, Div is reference to CR_22[6:3]	
RSV_D4_74	6:4	---	0	Reserved	
DPLL_VO2	3	R	0	DPLL CAL OUT2	
DPLL_VO1	2	R	0	DPLL CAL OUT1	
DPLL_CAL[1:0]	1:0	R	0	DPLL calibrated VCO code	

Register::SSC_REF_SEL 0xD5					
Name	Bits	R/W	Default	Comments	Config
DCLK_FMDIV_MD	7	R/W	0	Spread Spectrum FMDIV Default Mode 0: Normal mode 1: Fast mode (Active by DCLK_READY 0xC6[2] = 1)	
DCLK_FMDIV_FM_SEL	6:4	R/W	010	Spread Spectrum FMDIV Fast Mode Select 3' b 000: 77K 3' b 001: 88K 3' b 010: 99K (Default value) 3' b 011: 110K 3' b 100: 121K 3' b 101: 132K Other: Not used. (Above DCLK_SSC would be reference to 24.576MHz, active by 0xD5[7] = 1 and set DCLK_READY 0xC6[2] = 1) The actual DCLK_SSC = DCLK_SSC * (DPLL_SSC ref_clk / 24.576) DCLK_SSC: 0xD5[6:4] DPLL_SSC ref clk: 0xD5[0]	
Reserved	3:1	--	0	Reserved	
DPLL_SSC_REF_SEL	0	R/W	1	DPLL_SSC Reference clock select: 0: xtal_clk, 1: m2pll_clk/Div, Div is reference to CR_22[6:3]	

Register::DCLK_SSC_COUNT						0xD6
Name	Bits	R/W	Default	Comments	Config	
DCLK_FMDIV_CNT_EN	7	R/W	0	Spread Spectrum FMDIV Count Manual Mode 0: Disable 1: Enable (SSC FMDIV Default Mode 0xD5[7] would be invalid, active by DCLK_READY 0xC6[2] = 1)		
DCLK_FMDIV_CNT	6:1	R/W	11	The Numbers of Count for Spread Spectrum FMDIV: 6' b001011: 33K (Default value) 6' b010110: 66K 6' b111111: 189K (Above DCLK_SSC would be reference to 24.576MHz, active by 0xD6[7] = 1 and set DCLK_READY 0xC6[2] = 1) $\text{DCLK_FMDIV_CNT} = \text{DCLK_SSC} * 11 / (33K * (\text{DPLL_SSC ref_clk} / 24.576))$		
Reserved	0	--	0	Reserved		

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Multiply PLL for Input Cyrstal (Page 1)

Register:::M2PLL_M 0xE0					
Name	Bits	R/W	Default	Comments	Config
M2PLL_M[7:0]	7:0	R/W	0x42	M2PLL DPM value – 2 (M) * PLL output=input*(M/P)	

Register:::M2PLL_N 0xE1					
Name	Bits	R/W	Default	Comments	Config
M2PLL_CP	7	R/W	0	CP Control 0:CP=1.77pF 1:CP=2.1pF	
M2PLL_BPN	6	R/W	0	M2PLLBPN=0 , N divder enable M2PLLBPN=1, N divder disable , OUT=ckxtal	
M2PLL_O[1:0]	5:4	R/W	1	M2PLL Output divider 00:Div1, 01:Div2, 10:Div4, 11:Div8	
M2PLL_N[3:0]	3:0	R/W	0	M2PLL DPN value - 2	

Note: CRE0~E1 are double buffer

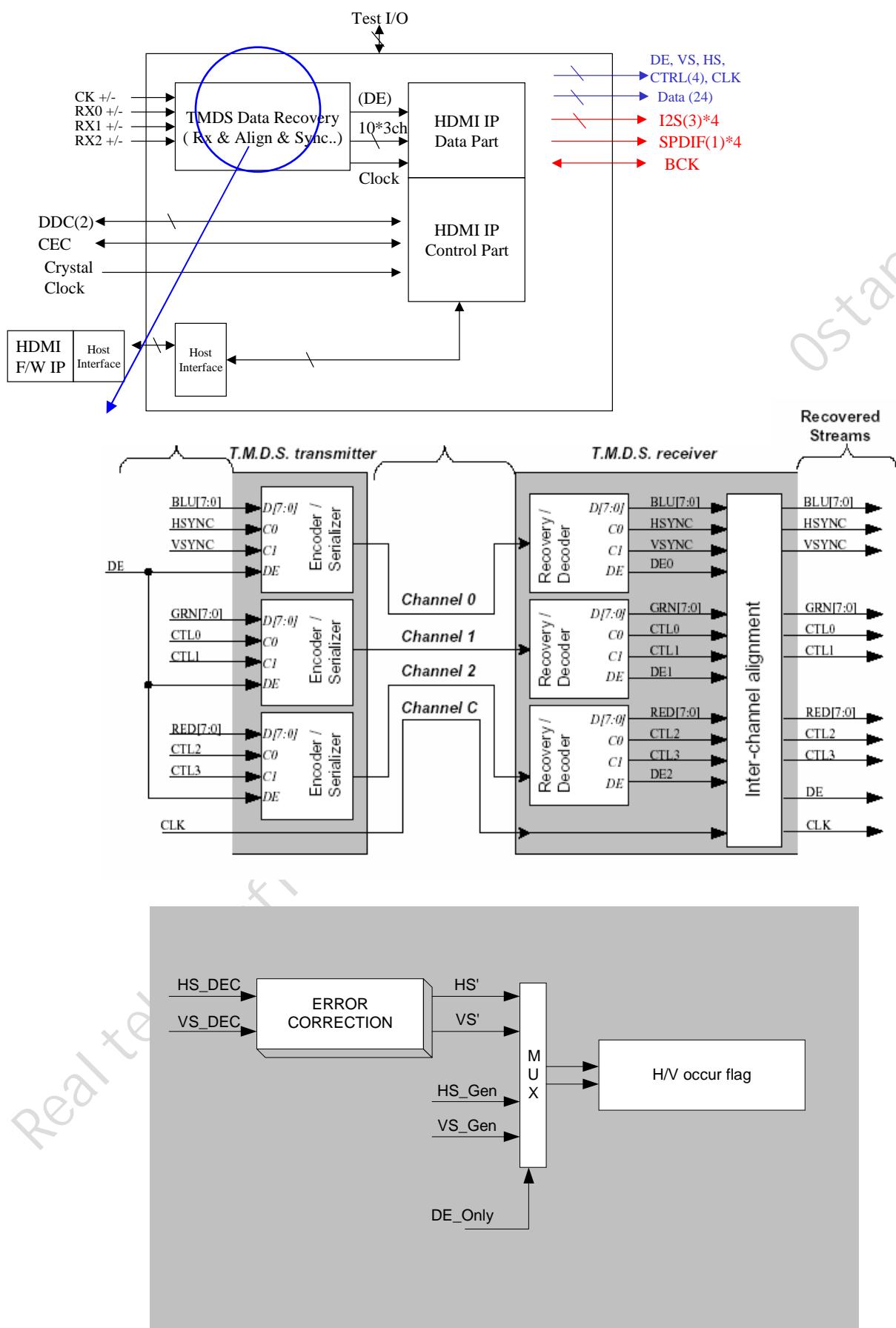
CRE2~E3 are not controlled by software reset.

Register:::M2PLL_CRNT 0xE4					
Name	Bits	R/W	Default	Comments	Config
M2PLL_RS[2:0]	7:5	R/W	3	M2PLL Loop Filter Resister Control(Rs) 000:16K, 001:18K, 010:20K, 011:22K 100: 24K, 101: 26K, 110:28K, 111:30K	
M2PLL_CS[1:0]	4:3	R/W	2	M2PLL Loop Filter Capacitor Control(Cs) 00:18p, 01:20p, 10:24p, 11:28p	
M2PLL_IP[1:0]	2:0	R/W	6	M2PLL Charge Pump Current Control $I_{cp}=(2.5\mu A+2.5\mu A*bit[0]+5\mu A*bit[1]+10\mu A*bit[2])$ $I_{cp}=0.5*M/N*14.318/27$	

Register:::M2PLL_WD 0xE5					
Name	Bits	R/W	Default	Comments	Config
M2PLL_WDO	7	R	0	M2PLL WD Status register 0:Normal 1:Abnormal Write 1 to clear.(WD enable when M2PLL power on)	wclr_out
M2PLL_WDRST	6	R/W	0	M2PLL WD Reset 0:Normal 1:Reset	
M2PLL_WDSET	5	R/W	0	M2PLL WD Set 0:Normal 1:Set	
M2PLL_VCOMD[1:0]	4:3	R/W	3	M2PLL VCO Default mode 00: VCO slowest 11: VCO fastest	
M2PLL_FREEZE	2	R/W	0	M2PLL Output Freeze 0:Normal 1:Freeze (active high)	
M2PLL_VCIRSTB	1	R/W	0	RESET VCO (active high)	
M2PLL_PWDN	0	R/W	0	Power Down M2PLL (active high)	

Address:E6~FF reserved

Overall HDMI System Function Block (Page 2)



Register: TMDS_MSR 0XA1				
Name	Bits	R/W	Reset State	Comments
TMM	7	R/W	0	Transition measurement method of hsync or data enable 0: old method: Measure the number of transition for N-clock duration (TMDS_NCP[3:0]: [3:0]*(1/12) ms) 1: new method: Measure the number of transition smaller than 16 or 64 clock period (TMDS_CTC: 0xA2[0]) for 1-frame duration (vsync)
MT	6:4	R/W	0	Measure times(exponential of 2) 000: 1 001: 2 010: 4 011: 8 100: 16 101: Not available 110: Not available 111: Not available This function will do bit [6:4] times, each time lasts for bit [3:0]/12 ms.
NCP	3:0	R/W	0	Numbers of Clock Period, measurement duration (where clock frequency is 12Khz) 0000: 16 0001: 1 0010: 2 0011: 3 1111: 15 This function will do bit [6:4] times, each time lasts for bit [3:0]/12 ms.

Register: TMDS_MRR0 0XA2				
Name	Bits	R/W	Reset State	Comments
TMS	7	R/W	0	Transition Measurement 0: Stop measure, Cleared after finish (Default) 1: Start measure
MRS	6:5	R/W	0	Measure Result Select 00: AVE Value (Default) 01: Max Value 10: Min Value
MS	4:3	R/W	0	The Selection of transition measurement of Hsync and Data_enable (select Hsync or Data enable) 00: Measure Hsync transition times before error correction 01: Measure Hsync transition times after error correction 10: Measure Data Enable transition times before error correction 11: Measure Data Enable transition times after error correction
DE_INV_DISABLE	2	R/W	0	Disable The Inversion of RGB channel Data Enable from data align (RGB channel together change polarity) 0: Invert Data Enable 1: Keep the original polarity of Data Enable
CRC_NON_STABLE	1	R	0	Check CRC is stable or not (write 1 clear) 0: means CRC is stable. 1: means CRC is not stable.
CTC	0	R/W	0	Criterion of Transition Count(de-bounce times) , duration smaller than 0: 16 clock 1: 64 clock

Register: TMDS_MRR1 0XA3				
Name	Bits	R/W	Reset State	Comments
CRC_DONE	7	R	0	CRC Calculation Finished (Calculation starts when 0xA4 bit 0 setting to 1) 0: not finished. 1: finished.
VMR	6:0	R	0	Transition measure result [6:0] of hsync or data_enable (Item refer to 0xA2[4:3])

Register:: TMDS_CTRL 0XA4				
Name	Bits	R/W	Reset State	Comments
BCD	7	R	x	Blue-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
GCD	6	R	x	Green-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
RCD	5	R	x	Red-Channel Detect whether data_enable is low 128 clk (DE low 128 clock)(write 1 clear) 0: no 1: yes
HO	4	R	x	The source of Hsync is from HDCP. Detect whether Hsync Occurs (write 1 clear) 0: no 1: yes
YO	3	R	x	The source of Vsync is from HDCP. Detect whether Vsync Occurs (write 1 clear) 0: no 1: yes
CRCTS	2:1	R/W	0	The selection of CRC calculation type 00: do CRC calculation only with DE 01: do CRC calculation only with DIEN (Data Island Enable) 10: do CRC calculation with both DE and DIEN 11: reserved
CRCC	0	R/W	0	CRC calculation enable 0: disable CRC calculation 1: enable CRC calculation

Register:: TMDS_CRCOB2 0XA5				
Name	Bits	R/W	Reset State	Comments
CRCOB2	7:0	R	--	1 st read=> Output CRC-48 bit 47~40 2 nd read=> Output CRC-48 bit 39~32 3 rd read=> Out put CRC-48 bit 31~24 4 th read=> Out put CRC-48 bit 23~16 5 th read=> Out put CRC-48 bit 15~8 6 th read=> Out put CRC-48 bit 7~0

- The read back CRC value address should be auto-increase, the sequence is shown above

Register:: TMDS_OUTCTL 0xA6				
Name	Bits	R/W	Reset State	Comments
AOE	7	R/W	0	Auto Output Enable (video output fsm mode) 0: Disable (Default), manual mode, determined by 0xA6 [6:3] 1: Enable, auto mode, determined by de_low128 from channel status
TRCOE	6	R/W	0	TMDS R Channel Output Enable 0: Disable (Default) 1: Enable
TGCOE	5:	R/W	0	TMDS G Channel Output Enable 0: Disable (Default) 1: Enable
TBCOE	4	R/W	0	TMDS B Channel Output Enable 0: Disable (Default) 1: Enable
OCKE	3	R/W	0	OCLK Enable 0: Disable (Default) 1: Enable
OCKIE	2	R/W	0	OCLK Invert Enable 0: Normal (Default) 1: Enable
de_err_puls_e_en	1	R/W	0	Enable reset de_low128 according to data_enable error pulse, data_enable error pulse comes from data_align function 0: disable 1: enable
CLK25XI_NV	0	R/W	0	Input 1x Clock Invert 0: No Invert (Default) 1: Invert

Register: TMDS_PWDCTL 0xA7				
Name	Bits	R/W	Reset State	Comments
DEO	7	R/W	0	DE-only: Generate VS/HS from DE signal 0: Disable (Default) 1: Enable
BRCW	6	R/W	0	B/R channel swap 0: No swap (Default) 1: Swap
PNSW	5	R/W	0	P/N Swap 0:No swap(Default) 1:swap
ICCAF	4	R/W	0	Input Channel control by auto function 0: Manual 1: Auto (Default)
ECC	3	R/W	0	Enable Clock channel: turn on clock channel PLL (For manual use) 0: Disable (Default) 1: Enable
ERIP	2	R/W	0	Enable Red input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable
EGIP	1	R/W	0	Enable Green input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable

EBIP	0	R/W	0	Enable Blue input port (For manual use, cut off 50ohm internal resistor) 0: Disable (Default) 1: Enable
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Register:: TMDS_ACC0 0XA8				
Name	Bits	R/W	Reset State	Comments
TUNE_UP_DOWN	7	R/W	0	AVMUTE Window Range Tune Up or Tune Down 0: Tune Down 1: Tune Up
TUNE_RANGE	6:0	R/W	0	AVMUTE Window Range If tune up, valid window = 384 cycle + 2*AVMUTE window range. If tune down, valid window = 384 cycle - 2*AVMUTE window range.

Register:: TMDS_ABC 0XA9				
Name	Bits	R/W	Reset State	Comments
WR_AKS_V_FLAG	7	R	0	Write AKSV Flag (Write 1 Clear)(in power on region) When TX writing AKSV done, this flag will be asserted.
RD_RI_FLAG	6	R	0	Read Ri Flag (Write 1 Clear) (in power on region) When TX reading HDCP's Ri, this flag will be asserted.
RD_BKSV_FLAG	5	R	0	Read BKSV Flag (Write 1 Clear) (in power on region) When TX reading HDCP's BKSV, this flag will be asserted.
HDCP_KEY_ACCE_SS_MODE	4	R/W	0	HDCP Key SRAM Access Right Control Mode 0: old mode 1: new mode (Auto switch SRAM Access Right when Aksv is received)
HDCP_KEY_ACCE_SS_RIGHT	3	R	0	HDCP Key SRAM Access Right (available when bit 4 = 1) 0: Access Right assigned to DP 1: Access Right assigned to HDMI On receiving Aksv from HDMI DDC, switch access right to HDMI. Switch back to DP after Km is calculated. HDMI has higher priority to access SRAM if both DP and HDMI write Aksv.
HIT_I2C_SLAVE_ADDRESS	2	R	0	Hit I2C slave address(Write 1 Clear)(in power on region) When TX hit I2C slave address this flag will be asserted
HIT_I2C_SLAVE_ENABLE	1	R/W	0	Hit I2C slave address IRQ enable (in power on region) 0: Disable (Default) 1: Enable
Reserved	0	--	0	Reserved

Register:: TMDS_ABC 0xAA				
Name	Bits	R/W	Reset State	Comments
Reserved	7	--	--	Reserved
HDCP_ENC_DIS	6	R/W	0	HDCP ENC DIS: 0: Original VS 1: Vertical Blanking Start
HDCP_ENC_EN	5	R	--	HDCP ENC EN flag
IRQ_AKSV_EN	4	R/W	0	IRQ Control For AKSV (Flag refer to 0xA9) 0: Disable 1: Enable

IRQ_RI_EN	3	R/W	0	IRQ Control For Ri (Flag refer to 0xA9) 0: Disable 1: Enable
IRQ_BKSV_E_N	2	R/W	0	IRQ Control For BKSV (Flag refer to 0xA9) 0: Disable 1: Enable
Reserved	1:0	--	--	Reserved to 0

Register:: TMDS_ACC2 0XAB				
Name	Bits	R/W	Reset State	Comments
REG_HS_WI_DTH_SEL	7	R/W	0	Hsnc Pulse Width Selection 0: 72 clock cycle width 1: 8 clock cycle width
HDCP_VS_SEL	6	R/W	0	HDCP Vsnc Selection 0: Choose original Vsnc. 1: Choose Virtual Vsnc.
DP_BLANK_KEEP_EN	5	R/W	1	Activated READ process of DP Audio doesn't pause even when Audio Packet assertion until the end of READ process. 0: Disable 1: Enable
DP_BLANK_EN	4	R/W	1	Block any READ request when Audio Packet assertion. 0: Disable 1: Enable
DP_BLANK_PRE_EN	3	R/W	1	Pre_block any READ request when Audio Packet assertion. 0: Disable 1: Enable
Reserved	2:0	--	0	Reserved.

Register:: TMDS_Z0CC2 0xAC				
Name	Bits	R/W	Reset State	Comments
DDCDBNC	7	R/W	1	HDCP DDC DEBOUNCE 0: Disable 1: Enable
HDE	6	R/W	0	HDMI/DVI function enable (HDCP enable is moved to HDCP) 0: Disable, gated clock and cut off TMDS pull up resistor for saving power. 1: Enable,
DBNC_LEVEL	5	R/W	1	HDCP Debounce Level Selection 0: Crystal period * 4 1: Crystal period * 8 When using 14.318 Mhz crystal clock, debounce level should be set to 0.
KM_CLK_SEL	4	R/W	0	Clock Selection for KM Calculation 0: Choose EMCU non-stop clock 1: Choose crystal clock
Reserved	3:0	R/W	--	Reserved to 0

Register:: TMDS_CPS 0xAD				
Name	Bits	R/W	Reset State	Comments
PLL_DIV2_EN	7	R/W	0	HDMI output clock div 2 (enable this register if 2x clock is needed) 0: disable 1: enable
CLKV_MEAS_SEL	6:5	R/W	01	Input Clock Source Selection. 00: Red clock (Lane 0 clock)

				01: Blue clock (Lane 2 clock) 10: Green clock (Lane 1 clock) 11: TMDS clock (Lane 3 clock)
CLKC_ME_AS_SEL	4	R/W	1	Detection Clock Source Selection. 0: Use TMDS clock as reference clock to detect input clock frequency. 1: Use crystal clock as reference clock to detect input clock frequency.
CLR_INFO_FRAME_DVI	3	R/W	0	Clear info-frame data when DVI mode 0: Disabled. 1: Enabled.
AUTO_DVI_2HDMI	2	R/W	0	In HDMI/DVI auto detection mode, auto switch to DVI mode when no signal(clk) being detected. 0: Disabled. 1: Enabled.
Reserved	1	--		Reserved.
CLKV_SEL	0	R/W	0	The video clock selection of frequency detection circuit in power-off region: 0: determined by 0xAD[6:5] 1: hdmi_cp_clk

Register::: TMDS_RPS 0xAE				
Name	Bits	R/W	Reset State	Comments
AVMUTE_FLAG	7	R/W	0	Ignore AVMUTE Flag 0: Disable 1: Enable (CLR_AVMUTE)
sram_arbiter_mode_sel	6	R/W	0	HDMI / DP use key sram arbiter mode select 0: old mode 1: arbiter mode
Reserved	5:2	--	0	Reserved.
HDCP_KEY_RDY	1	R/W	0	HDCP KEY Ready Flag This flag is for F/W to indicate HW that HDCP key is READY! 0: HDCP key not ready. 1: HDCP key ready.
AUTHST_MODE_SEL	0	R/W	0	Selection of AUTHST mode. 0: Original mode. 1: New mode, H/W will keep authst signal until HDCP key is ready. (refer to bit 1)

Register::: TMDS_WDC 0xAF				
Name	Bits	R/W	Reset State	Comments
Reserved	7	R/W	0	Reserved to 0
ARBITER_STATE	6:5	R	0	Arbiter State: 00: initial value or finish value. 01: HDMI has right to use HDCP key SRAM 10: DP has right to use HDCP key SRAM 11: useless information.
ARBITER_PRIORITY_SEL	4	R/W	0	New SRAM Arbiter Mode Priority Select: 0: HDMI High Priority 1: Display Port High Priority (When HDMI/DP request use HDCP key SRAM at same time, FW can decide the priority. Not valid when abnormal case occur: HDMI or DP occupy HDCP key SRAM for a long time, HW auto switch HDMI/DP priority.)

Reserved	3:0	R/W	0	Reserved to 0
DVI_ENC_MODE	0	R/W	0	Selection of DVI OESS mode. 0: Original mode. 1: New mode, H/W will keep running HDCP process even if ctrl3 is lost.

0xB0~0xB3 Reserved

Register:: TMDS_DPC0 0XB4				
Name	Bits	R/W	Reset State	Comments
dpc_pp	7:4	R	0	PP value of HDMI 1.3 Deep color mode. (If dpc_auto(0xB8[2]) ==0, this bit is R/W; otherwise, it is read-only)
dpc_cd	3:0	R	0	CD value of HDMI 1.3 Deep color mode. (If dpc_auto(0xB8[2]) ==0, this bit is R/W; otherwise, it is read-only)

Register:: TMDS_UDC0 0XB5				
Name	Bits	R/W	Reset State	Comments
dpc_bypass_dis	7	R/W	0	Disable Deep Color Test Mode 0: disable 1: enable
reserved	6:4	--	0	Reserved.
CP_DPLLF DDS	3	R/W	0	CP Test mode: 0: dpllfdst_gate = reg_cptest ? bckin : dpllfdds 1: dpllfdst_gate can switch to dpllfdds when reg_cptest = 1
CPTEST	2	R	0	CPTEST 0: normal mode, in which clock and data from analog are used. 1: select TSTCKIN/TSTDIN as input 2X5 clock and data respectively, for TESTING.
HMTM	1:0	R/W	0	HDCP MP TESTING MODE Force CTL[3:0] always equal to 00:Original 01:CTRL=1001 10:CTRL=1000 11:CTRL=0000

Register:: TMDS_UDC1 0XB6				
Name	Bits	R/W	Reset State	Comments
no_clk_in	7	R	0	No clock input. 0: normal, 1: no clock
cdr_rdy_red	6	R	0	CDR ready of red channel
cdr_rdy_grn	5	R	0	CDR ready of green channel
cdr_rdy_blu	4	R	0	CDR ready of blue channel
reserved	3:0	--	0	Reserved.

Register:: TMDS_UDC2 0XB7				
Name	Bits	R/W	Reset State	Comments
NL	7:5	R/W	3	The selection of error correction, ERRC_SEL<2:0> 000: original signal 001: 1 cycle debouncing 010: 1+8 cycle debouncing 011: 1+8 cycle debouncing + de masking transition of vs/hs 100: 1+8 cycle debouncing + de masking transition of vs/hs + masking first 8-line de

NLFW	4:0	R/W	0	The selection of debug signal, total has 32 kinds of debug signals. 00000: dbg_out_0 00001: dbg_out_1 11111: dbg_out_31
------	-----	-----	---	--

Register:: TMDS_DPC1 0XB8				
Name	Bits	R/W	Reset State	Comments
reserved	7:4	--	0	Reserved.
dpc_clk_source	3	R/W	0	Select the reference clock of deep color pll 0: recovered tmds clock 1: original tmds clock
dpc_auto	2	R/W	1	0: manual mode (CD/PP/default_phase fields are specified by FW) 1: auto mode (CD/PP/default_phase are directly decoded by HW)
dpc_default_ph	1	R/W	0	Default Phase of HDMI 1.3 Deep color mode. (If dpc_auto(0xB8[2]) ==0, this bit is R/W; otherwise, it is read-only)
dpc_pp_valid	0	R/W	0	Phase valid of HDMI 1.3 Deep color mode. (If dpc_auto(0xB8[2]) ==0, this bit is R/W; otherwise, it is read-only)

Register:: TMDS_OUT_CTRL 0xB9				
Name	Bits	R/W	Reset State	Comments
TMDS_BY_PASS	7	R/W	1	TMDS Bypass Control 0: RGB values will be assigned by register's setting when it is out of data enable region 1: RGB values will be set to 16'b0 when it is out of the data enable region
Rev	6:0	---		Reserved

Register:: TMDS_ROUT_HIGH_BYTE 0xBA				
Name	Bits	R/W	Reset State	Comments
TMDS_RO_UT_H	7:0	R/W	0	TMDS Rout High Byte Register Value High Byte [15:8]

Register:: TMDS_ROUT_LOW_BYTE 0xBB				
Name	Bits	R/W	Reset State	Comments
TMDS_RO_UT_L	7:0	R/W	0	TMDS Rout Low Byte Register Value Low Byte [7:0]

Register:: TMDS_GOUT_HIGH_BYTE 0xBC				
Name	Bits	R/W	Reset State	Comments
TMDS_GO_UT_H	7:0	R/W	0	TMDS Gout High Byte Register Value High Byte [15:8]

Register:: TMDS_GOUT_LOW_BYTE 0xBD				
Name	Bits	R/W	Reset	Comments

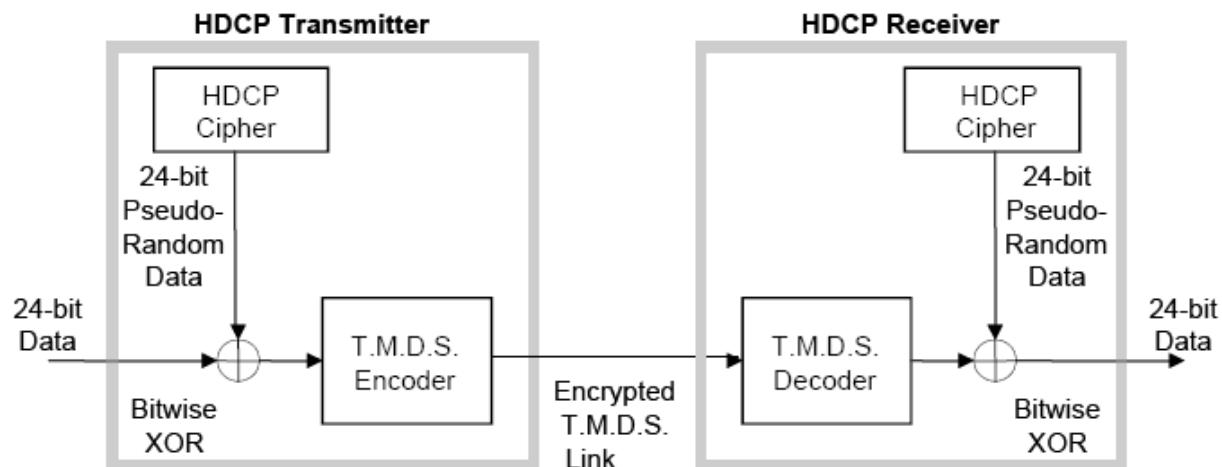
			State	
TMDS_GO UT_L	7:0	R/W	0	TMDS Gout Low Byte Register Value Low Byte [7:0]

Register:: TMDS_BOUT_HIGH_BYTE					0xBE
Name	Bits	R/W	Reset State	Comments	
TMDS_BO UT_H	7:0	R/W	0	TMDS Bout High Byte Register Value High Byte [15:8]	

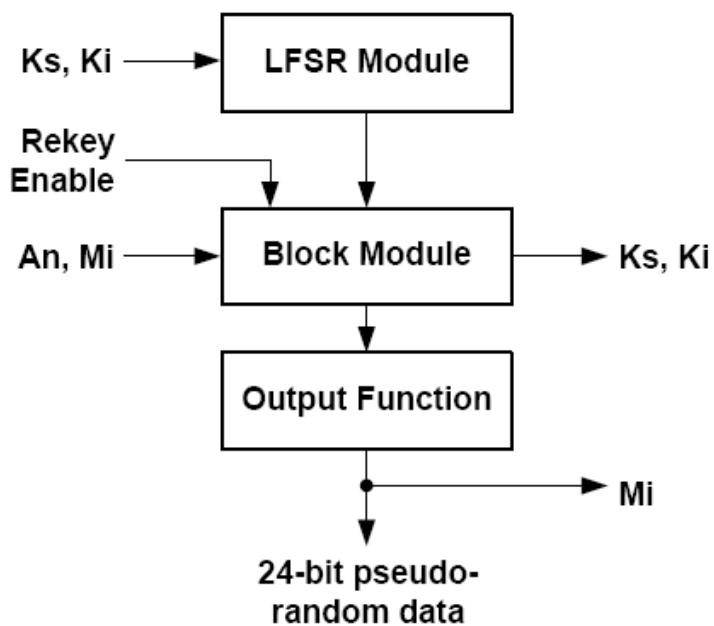
Register:: TMDS_BOUT_LOW_BYTE					0xBF
Name	Bits	R/W	Reset State	Comments	
TMDS_BO UT_L	7:0	R/W	0	TMDS Bout Low Byte Register Value Low Byte [7:0]	

HDCP 1.4 (Page 2)

HDCP Encryption and Decryption:



HDCP Cipher:



Register::: HDCP_CR 0XC0				
Name	Bits	R/W	Reset State	Comments
AC_MOD	7	R/W	1	Advance Cipher Mode 0: Old mode (AC = HDMI or (DVI & Ainfo[1])) 1: New mode (AC = Ainfo[1])
Reserve	6	R	0	Reserved.
IVSP	5	R	0	Indicate VSYNC Polarity 0: Positive, which means VS pulse is high. 1: Negative
INVVS	4	R/W	0	Invert VSYNC for HDCP when vs_manual mode (bit[3] = 1) 1: Inverted 0: Not Inverted
IVSPM	3	R/W	0	Indicate VSYNC Polarity Mode:

				1: manual mode, decided by INVVS (vs_ctrl) 0: auto mode, indicate by IVSP
MADDF	2	R/W	0	MCU Access DDC data first (when download key from MCU, force only MCU could work) 0: enable DDC channel and MCU access only when DDC is not busy 1: disable DDC channel and MCU access only
DKAPDE	1	R/W	0	Device Key Access Port download enable (download key from MCU) 1: enable 0: disable, this would reset the address of Device Key Access Port to 0.
Enable	0	R/W	0	HDCP Enable 1: Auto Enable HDCP function, when Tx I2C write Aksv, 0: Disable HDCP, except for output.

Register::: HDCP_DKAP 0XC1				
Name	Bits	R/W	Reset State	Comments
DKAP	7:0	R/W	0	When enable device key accessing 40x56 table, the 56-bit key table will be transferred to 64-bit pseudo data with 7 th , 15 th , 23rd, 31st, 39 th , 47 th , 55 th bits inserted. The inserted data are ‘0’. And the write sequence is: {D0-Byte0, D0-Byte1, D0-Byte2, D0-Byte3, D0-Byte4, D0-Byte5, D0-Byte6, D0-Byte7}, {D1-Byte0, D1-Byte1, 1-Byte2, D1-Byte3, D1-Byte4, D1-Byte5, D1-Byte6, D1-Byte7}, Accessing this port must be coded/decoded by REALTEK protection code. Note: Only available when Page C 0xA1[5] is selected to HDMI

Register::: HDCP_PCR 0xC2				
Name	Bits	R/W	Reset State	Comments
Rev	7:5	---		Reserved
ENC_TOG	4	R	0	ENC toggled. (Asserted when ENC start is received)(Write 1 clear)
AVMUTE_DIS	3	R/W	1	Auto enc_dis when AVMUTE 0: non active 1: active
DDCSEL	2:1	R/W	0	DDC Channel SEL for Key Access 00: DDCSCL2/DDCSDA2(pin 123~124) 01: DDCSCL3/DDCSDA3(pin 121~122) 10: non-useful 11: non-useful
APAI	0	R/W	0	HDCP Accessing Port Auto Increase (For Host Side) 0: auto increase 1: keep in the same address.

Register::: HDCP_AP 0XC3				
Name	Bits	R/W	Reset State	Comments
AP	7:0	R/W	0	Address port for embedded HDCP access , auto increase after DATA_PORT being accessed. (For Host Side controlled by APAI)

Register::: HDCP_DP 0XC4				
Name	Bits	R/W	Reset State	Comments

DP	7:0	R/W	0	Data port for embedded HDCP access
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I2C Control Register Map (DVI DDC side) device address: 0x74/0x75

Following register is assigned by “HDCP-address port”, “HDCP-data port” (From HDCP 1.1)

Hex Address	Write/Read	Size in Bytes	Register Name	Function
0x C4-00	R	5	BKSV	HDCP Receiver KSV. This value may be used to determine that the receiver is HDCP capable. Valid KSVs contain 20 ones and 20 zeros, a characteristic that must be verified by HDCP Transmitters before encryption is enabled. This value must be available any time the HDCP Receiver's HDCP hardware is ready to operate.
0x C4-05	R	3	Reserved	All bytes read as 0x00
0x C4-08	R	2	Ri'	Link verification response. Upon completion of the authentication computations, this register contains the R0' value. Following that, it is updated upon completion of HDCPBlockCipher if $(i \bmod 128) == 0$. It is recommended that HDCP Transmitters protect against errors in the I2C transmission by re-reading this value when unexpected values are received, though care must be taken to avoid missing legitimate mis-match conditions. This value must be available at all times between updates. R0' must be available less than 100 ms after Aksv is received. Subsequent Ri' values must be available a maximum of 128 pixel clocks following the Encryption Enable detection (ENC_EN).
0x C4-0A	R	1	Pj'	Enhanced Link Verification Response. Updated upon receipt of first video pixel received when frame counter value $(j \bmod 16) == 0$. The value is the XOR of the decrypted byte on channel zero of the first video pixel with the least significant byte of Rj. Rj is derived from the output function in the same manner as Ri, but is captured every 16 th counted frame (rather than every 128 th counted frame).
0x C4-0B	R	5	Reserved	All bytes read as 0x00
0x C4-10	R/W	5	AKSV	HDCP transmitter KSV. Writes to this multi-byte value are written least significant byte first. The final write to 0x14 triggers the authentication sequence in the HDCP Receiver, and the current Ainfo value is copied from the port, takes effect, and the port is reset to the default value of zero.
0x C4-15	R/W	1	Ainfo	Bits 7-2: Reserved zeros. Bit 1: ENABLE_1.1_FEATURES. This bit enables the Advance Cipher option. If in DVI mode, it also enables the Enhanced Encryption Status Signaling (EESS) (in HDMI mode, EESS is enabled regardless of this bit setting). This bit resets to default zero when the HDCP Receiver becomes attached or active, or is reset, or the last byte of Aksv is written. A write to the last byte of Aksv copies the port value and causes it to take effect, and then resets the port value to the default value of zero. Thus the options must be explicitly enabled prior to each authentication. Bit 0: Reserved (must be zero).
0x C4-16	R	2	Reserved	All bytes read as 0x00
0x C4-18	R/W	8	An	Session random number. This multi-byte value must be written by the HDCP Transmitter before the KSV is written.
0x C4-20	R	20	Reserved	All bytes read as 0x00
0x C4-34	R	12	Reserved	All bytes read as 0x00
0x C4-40	R	1	Bcaps	Bit 7: HDMI_RESERVED Use of this bit is reserved. HDCP Receivers not capable of supporting HDMI must clear this bit to 0.(R/W)

				<p>Bit 6: REPEATER, HDCP Repeater capability. When set to one, this HDCP Receiver supports downstream connections as permitted by the Digital Content Protection LLC license. This bit does not change while the HDCP Receiver is active.</p> <p>Bit 5: READY, KSV FIFO ready. When set to one, this HDCP Repeater has built the list of attached KSVs and computed the verification value V. This value is always zero during the computation of V.</p> <p>Bit 4: FAST. When set to one, this device supports 400 KHz transfers. When zero, 100 KHz is the maximum transfer rate supported. Note that 400KHz transfers are not permitted to any device unless all devices on the I²C bus are capable of 400KHz transfer. The transmitter may not be able to determine if the EDID ROM, present on the HDCP Receiver, is capable of 400KHz operation. This bit does not change while the HDCP Receiver is active.(R/W)</p> <p>Bits 3-2: Reserved (must be zero).</p> <p>Bit 1: 1.1_FEATURES. When set to one, this HDCP Receiver supports Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options. For the HDMI protocol, Enhanced Encryption Status Signaling (EESS) capability is assumed regardless of this bit setting. This bit does not change while the HDCP Receiver is active.</p> <p>Bit 0: FAST _REAUTHENTICATION. When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP Receiver is active.</p>
0x C4-41	R	2	Bstatus	Refer to Table 1
0x C4-43	R	1	KSV FIFO	Key selection vector FIFO. This device is not a repeater. All byte read as 0x00 for HDCP Receivers that are not HDCP Repeaters(REPEATER==0).
0x C4-44	R	124	Reserved	All bytes read as 0x00

<i>Name</i>	<i>Bit Field</i>	<i>Read/Write</i>	<i>Description</i>
Reserved	15:14	R	Read as zero.
HDMI_RESERVED_2	13	R	Reserved for future possible HDMI use.
HDMI_MODE	12	R	HDMI Mode. When set to one, the HDCP Receiver has transitioned from DVI Mode to HDMI Mode. This has occurred because the HDCP Receiver has detected HDMI bus conditions on the link. This bit must not be cleared when the HDCP Transmitter and HDCP Receiver are connected and both are operating in an active HDMI mode. This bit must be cleared upon power-up, reset, unplug or plug of an HDCP Transmitter or anytime that the HDCP Receiver has not seen at least one Data Island within 30 video frames.
	11:0	R	Read as zero.

Table 1 (Address 0x41)

Note :

When accessing this DDC register map by DDC, the address should increase automatically, except for the first accessing address is KSV FIFO, 0x43.

Register:: HDCP_BCAPS					0xC4-40
Name	Bits	R/W	Reset	Comments	

			State	
HDMI_RESERVED	7	R/W	0	HDMI_RESERVED Use of this bit is reserved. HDCP Receivers not capable of supporting HDMI must clear this bit to 0.
REPEATER	6	R	0	REPEATER HDCP Repeater capability. When set to one, this HDCP Receiver supports downstream connections as permitted by the Digital Content Protection LLC license. This bit does not change while the HDCP Receiver is active.
READY	5	R	0	READY KSV FIFO ready. When set to one, this HDCP Repeater has built the list of attached KSVs and computed the verification value V'. This value is always zero during the computation of V'. See states C0 and C2.
FAST	4	R/W	1	FAST When set to one, this device supports 400 KHz transfers. When zero, 100 KHz is the maximum transfer rate supported. Note that 400KHz transfers are not permitted to any device unless all devices on the I2C bus are capable of 400KHz transfer. The transmitter may not be able to determine if the EDID ROM, present on the HDCP Receiver, is capable of 400KHz operation. This bit does not change while the HDCP Receiver is active.
Reserved	3:2	R	0	Reserved to 0
1.1_FEATURES	1	R	0	1.1_FEATURES When set to one, this HDCP Receiver supports Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options. For the HDMI protocol, Enhanced Encryption Status Signaling (EESS) capability is assumed regardless of this bit setting. This bit does not change while the HDCP Receiver is active.
FAST_REALERTIFICATION	0	R	0	FAST_REALERTIFICATION When set to 1, the receiver is capable of receiving (unencrypted) video signal during the session re-authentication. All HDMI-capable receivers shall be capable of performing the fast re-authentication even if this bit is not set. This bit does not change while the HDCP Receiver is active.

Register::: HDCP_FCR 0xC4-C0				
Name	Bits	R/W	Reset State	Comments
Reserved	7	R	-	Reserved
FC	6:0	R	0	HDCP_frame counter[6:0]

Register::: HDCP_SIR 0xC4-C1				
Name	Bits	R/W	Reset State	Comments
AST	7	R	0	Authst (Means bksv of RTD pass Tx authorization, Tx is ready to do HDCP transaction)
AKM	6	R	0	Authkm (Means RTD finish computing KM, ri) //Hidden
ADNE	5	R	0	Authdone (means TX admitted ri value, start to do HDCP transmission)
REA	4	R/W	0	RE_AUTH
ENCM	3	R/W	0	ENC_Method
ENCE	2	R	0	ENC_ERROR (Receive ENC enable and disable at the same time)
NC	1	R	0	NO CTRL(HDCP1.0: no ctrl[3], HDCP1.1: ctrl is not 1001 nor 0001)
IB	0	R	0	Internal buffer for Ainfo[1]. Since Ainfo[1] in DDC port is 0 at most of time, we need to know what Tx wrote.

Write to 0xC4-C1 should be accessed by writing 0xC4-C4

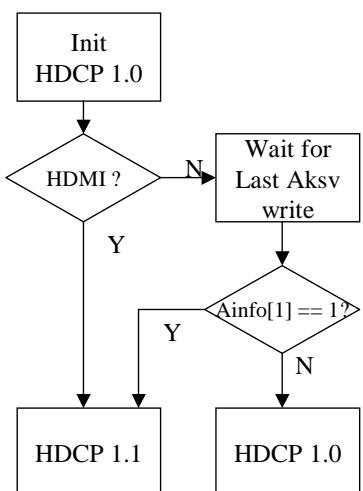
Register::: HDCP_SLAVE_ADD 0xC4-C2				
Name	Bits	R/W	Reset	Comments

			State	
OEES_EESS S	7	R/W	0	OEES_EESS mode select: 0:FW mode: hdmi_feature = register setting(old mode) 1:HW mode: hdmi_feature = hdmi_md ok(new mode: DVI format is set to OEES/HDMI format is set to EESS)
Slave_AdDR	6:0	R/W	3A	HDCP Slave_Addr[6:0] Ex. HDCP address = 0x74, 8'b 0111 0100 Reg_Slave_Addr[6:0] = 0111 010 ... the last bit is ignored.

HDCP 1.1/1.0 decide flow:

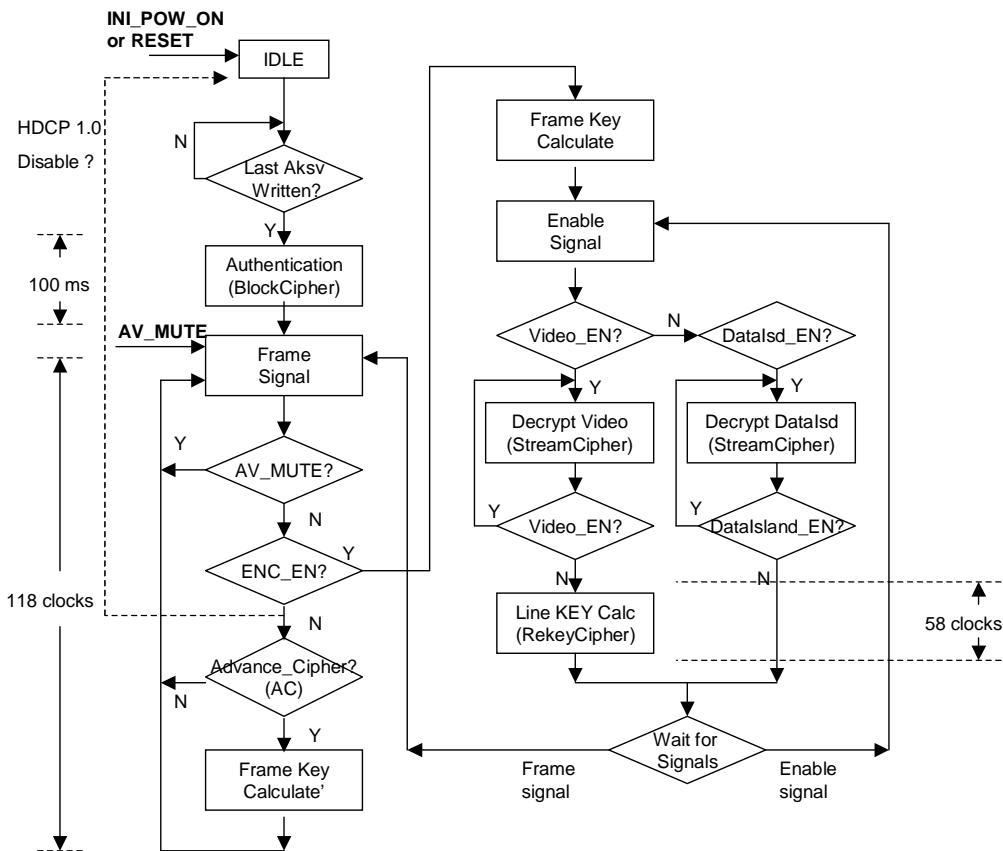
1. If HDMI conditions happen, HDCP 1.1 is used.
2. When last byte of Aksv is written, Ainfo[1] indicates HDCP 1.0/1.1 mode.

OEES is the same as HDCP 1.0. We could tell it by Ainfo[1] in DDC.

**HDCP 1.0/1.1 decide flow
(Before Auth)**


Initial flow.

HDCP Total Flow



HDCP 1.0/1.1 difference

Item	Description	HDCP 1.0	HDCP 1.1
1	Fast Reset	No constraint in 1.0	It must be done
2	DDC : Ainfo	Useless	Double buffer
3	DDC : Pj	No this feature	Update per 16 frames
4	DDC : Bcaps[1]	No this feature	It is used to tell if Rx supports 1.1
5	DDC : Bstatus	No this feature	HDMI mode mapping
6	DDC : short read	Read Ri.	Read Ri & Pj.
7	OEES/EESS	Only OEES compatible	Depend on DDC info. Sync.
8	Support protocol	DVI (DE only)	DVI & HDMI (DE & DIEN)
9	CTLx position	CTL3 follows VS	All info must be in opp. window.
10	Error correction	No the requirement	Error correction for ENC_EN/DIS
11	VS polarity distinction	No clear description	1. init is neg. 2. VS debouncing before DE. 3. VS por for open opp window.

Frame counter

HDCP 1.0 : Increase by VS(CTL3).

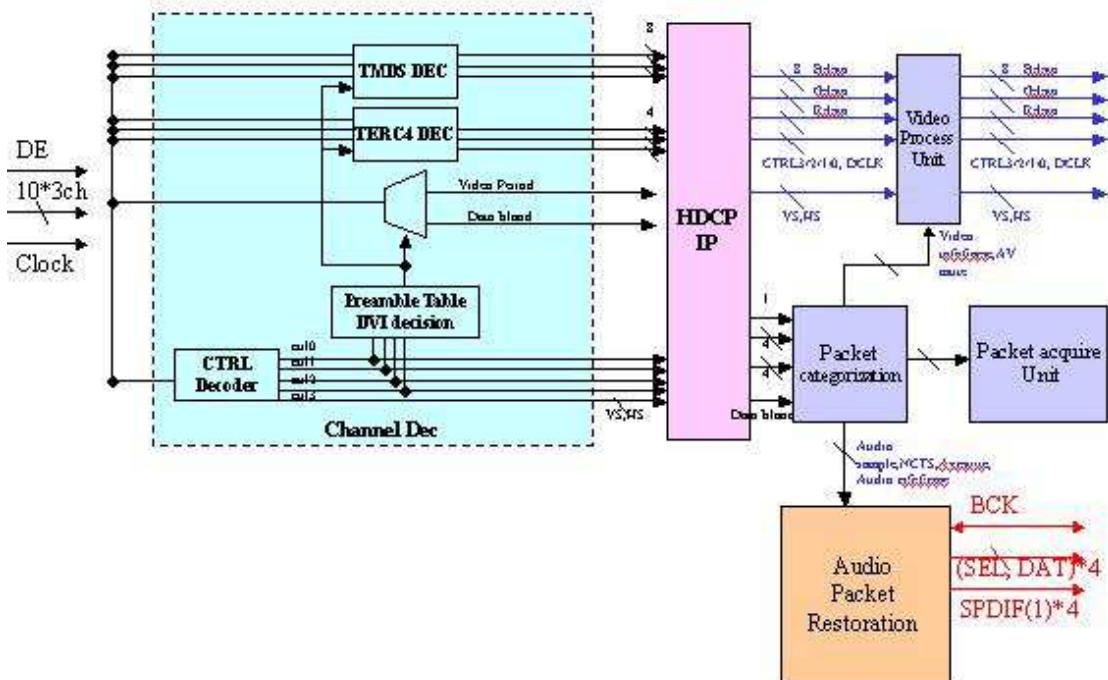
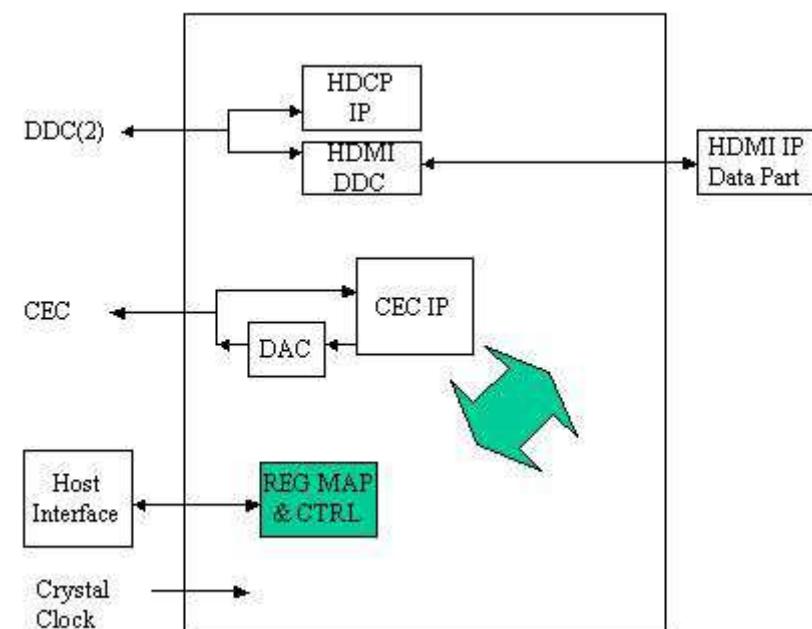
HDCP 1.1 : In OEES mode, increase by ENC_EN

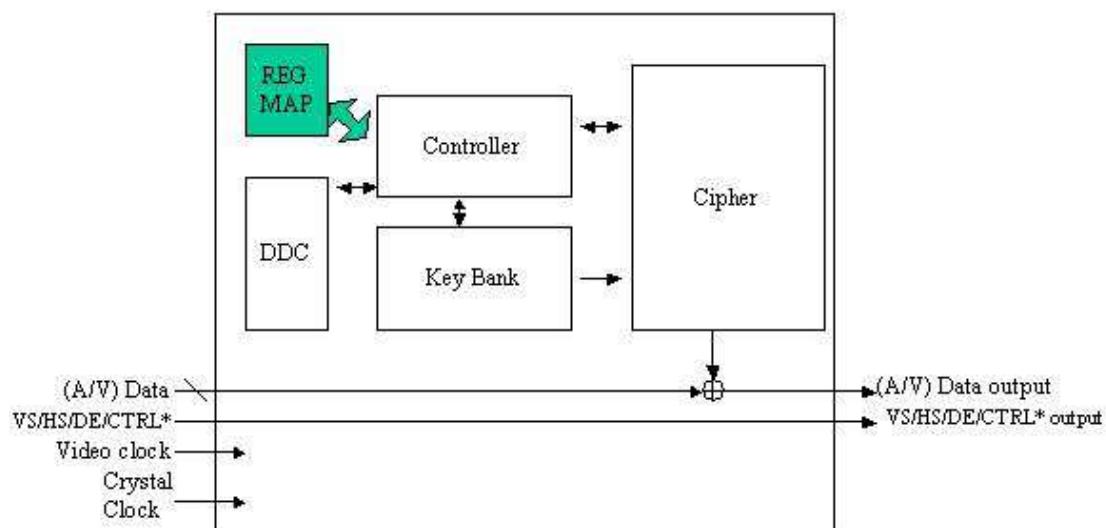
In EESS mode, increase when a. AV_MUTE = false. & b. AC = 1 or ENC_EN = 1.

NOTE :

1. HDCP output must be always enable for DVI/HDMI.
2. The sub-descriptions i of Ri & j of Pj are the same.

HDMI Video and Audio Part (Page 2)

HDMI IP Data Part

HDMI IP Control Part


HDCP IP


Register:: HDMI_AP 0xC8				
Name	Bits	R/W	Reset State	Comments
Reserved	7:1	R/W	0	Reserved to 0
AAIF	0	R/W	0	Address auto increase function 0: If read/write “HDMI data port” continuously without assign “HDMI address port”, address would be not added by one automatically. 1: If read/write “HDMI data port” continuously without assign “HDMI address port”, address would be added by one automatically.

Register:: HDMI_AP 0xC9				
Name	Bits	R/W	Reset State	Comments
AP	7:0	R/W	0	Address port for HDMI

Register:: HDMI_DP 0xCA				
Name	Bits	R/W	Reset State	Comments
DP	7:0	R/W	0	Data port for HDMI

HDMI Register in Address Data Port

Access Addr.	Name	Description
0x00	HDMI_SCR	System Control
0x01	HDMI_N_VAL	N times of Condition A
0x02	HDMI_BCHCR	BCH Control Bits
0x03	HDMI_AFCR	Audio Flow Control
0x04	HDMI_AFSR	Audio FIFO Status
0x05	HDMI_MAGCR	Manual Audio Gain Coefficient
0x06	HDMI_AAGCR	Auto Audio Gain Control
0x07	HDMI_MAG_M_FINAL	Audio Final Gain Control
0x08	HDMI_MAG_L_FINAL	HDMI Left Channel Final Gain

0x09	HDMI_MAG_R_FINAL	HDMI Right Channel Final Gain
0x0A	AUDIO_LD_P_TIME_M	Audio Waiting Time
0x0B	AUDIO_LD_P_TIME_N	Audio Waiting Time
0x0C	ZCD_CTRL	Zero Crossing Control of Final Gain
0x0D	ZCD_TIME_OUT	Time Out to Force Final Gain
0x0E	ZCD_STATUS	Zero Crossing Detect Status
0x10	HDMI_CMCR	Clock MUX Control
0x11	HDMI_MCAPR	M Code of Audio PLL
0x12	HDMI_SCAPR	S Code of Audio PLL
0x13	HDMI_DCAPR0	MSB of D Code of Audio PLL
0x14	HDMI_DCAPR1	LSB of D Code of Audio PLL
0x15	HDMI_PSCR	Phase Swallow Control
0x16	HDMI_FDDR	FIFO Depth at DE Rising
0x17	HDMI_FDDF	FIFO Depth at DE Falling
0x18	HDMI_MFDDR	Maximum FIFO Depth at DE Rising
0x19	HDMI_MFDDF	Minimum FIFO Depth at DE Falling
0x1A	HDMI_FTR	FIFO Trend Register
0x1B	HDMI_FBR	FIFO Boundary Register
0x1C	HDMI_ICPSNCR0	I Code of Phase Swallow and N/CTS Register 0
0x1D	HDMI_ICPSNCR1	I Code of Phase Swallow and N/CTS Register 1
0x1E	HDMI_PCPSNCR0	P Code of Phase Swallow and N/CTS Register 0
0x1F	HDMI_PCPSNCR1	P Code of Phase Swallow and N/CTS Register 1
0x20	HDMI_ICTPSR0	I Code of Trend for Phase Swallow Register 0
0x21	HDMI_ICTPSR1	I Code of Trend for Phase Swallow Register 1
0x22	HDMI_PCTPSR0	P Code of Trend for Phase Swallow Register 0
0x23	HDMI_PCTPSR1	P Code of Trend for Phase Swallow Register 1
0x24	HDMI_ICBPSR0	I Code of Boundary for Phase Swallow Register 0
0x25	HDMI_ICBPSR1	I Code of Boundary for Phase Swallow Register 1
0x26	HDMI_PCBPSR0	P Code of Boundary for Phase Swallow Register 0
0x27	HDMI_PCBPSR1	P Code of Boundary for Phase Swallow Register 1
0x28	HDMI_NTx1024TR0	Number of Tx in 1024 Tv Register 0
0x29	HDMI_PCBPSR1	Number of Tx in 1024 Tv Register 1
0x2A	HDMI_STBPR	Stop Time for Boundary PE Register
0x2B	HDMI_NCPER	N and CTS Phase Error Register
0x2C	HDMI_PETR	Phase Error Threshold Register
0x2D	HDMI_AAPNR	Action for Audio PLL Non-Lock Register
0x2E	HDMI_APDMCR	Audio PLL Debug Mode Control Register
0x30	HDMI_AVMCR	Audio and Video Mute Control Register
0x31	HDMI_WDCR0	Watch Dog Control Register 0
0x32	HDMI_WDCR1	Watch Dog Control Register 1
0x33	HDMI_WDCR1	Watch Dog Control Register 2
0x34	HDMI_DBCR	HDMI Double Buffer Control Register
0x35	HDMI_APTMCR0	Audio PLL Test Mode Control Register 0
0x36	HDMI_APTMCR1	Audio PLL Test Mode Control Register 1
0x38	HDMI_DPCR0	DPLL Control Register 0
0x39	HDMI_DPCR1	DPLL Control Register 1
0x3A	HDMI_DPCR2	DPLL Control Register 2
0x3B	HDMI_DPCR3	DPLL Control Register 3
0x3C	HDMI_SUMCM	SDM SumC
0x3D	HDMI_SUMCL	SDM SumC
0x40	HDMI_AWDSR	Audio Watch Dog Status Register

0x41	HDMI_VWDSR	Video Watch Dog Status Register
0x42	HDMI_PAMICR	Packet Acquire Mechanism Interrupt Control Register
0x43	HDMI_PTRSV1	Packet Type of RSV1 Packet
0x44	HDMI_PTRSV2	Packet Type of RSV2 Packet
0x45	HDMI_PVGCR0	Packet Variation Global Control Register 0
0x46	HDMI_PVGCR1	Packet Variation Global Control Register 1
0x47	HDMI_PVGCR2	Packet Variation Global Control Register 2
0x48	HDMI_PVSR0	Packet Variation Status Register 0
0x49	HDMI_PVSR1	Packet Variation Status Register 1
0x4A	HDMI_PVSR2	Packet Variation Status Register 2
0x50	HDMI_VCR	Video Control Register
0x51	HDMI_ACRCR	ACR Control Register
0x52	HDMI_ACRSR0	ACR Status Register 0
0x53	HDMI_ACRSR1	ACR Status Register 1
0x54	HDMI_ACRSR2	ACR Status Register 2
0x55	HDMI_ACRSR3	ACR Status Register 3
0x56	HDMI_ACRSR4	ACR Status Register 4
0x57	HDMI_ACS0	Audio Channel Status 0
0x58	HDMI_ACS1	Audio Channel Status 1
0x59	HDMI_ACS2	Audio Channel Status 2
0x5A	HDMI_ACS3	Audio Channel Status 3
0x5B	HDMI_ACS4	Audio Channel Status 4
0x60	HDMI_INTCR	HDMI Interrupt Control Register
0x61	HDMI_ALCR	Audio Layout Control Register
0x62	HDMI_AOCR	Audio Output Control Register
0x70	HDMI_BCSR	HDMI Basic Coding Status Register
0x71	HDMI_ASRO	Audio Status Register 0
0x72	HDMI_ASRI	Audio Status Register 1
0x80	TMDS_DPC_SET0	Deep Color Setting 0
0x81	TMDS_DPC_SET1	Deep Color Setting 1
0x82	TMDS_DPC_SET2	Deep Color Setting 2
0x83	TMDS_DPC_SET3	Deep Color Setting 3
0x84	TMDS_DET_0	TMDS Decoding Error Detection 0
0x85	TMDS_DET_1	TMDS Decoding Error Detection 1
0x86	TMDS_DET_2	TMDS Decoding Error Detection 2
0x87	TMDS_DET_3	TMDS Decoding Error Detection 3
0x88	TMDS_DET_4	TMDS Decoding Error Detection 4
0x90	AUDIO_FREQDET	Audio Frequency Detect
0x91	AUDIO_FREQDET_RESULT_M	Audio Frequency Detect Result
0x92	AUDIO_FREQDET_RESULT_L	Audio Frequency Detect Result
0x93	XTAL_DIV	Crystal Divider
0x94	RANGE0_M	Threshold of Range 0 Detection
0x95	RANGE0_L	Threshold of Range 0 Detection
0x96	RANGE1_L	Threshold of Range 1 Detection
0x97	RANGE2_M	Threshold of Range 2 Detection
0x98	RANGE2_L	Threshold of Range 2 Detection
0x99	RANGE3_L	Threshold of Range 3 Detection
0x9A	RANGE4_M	Threshold of Range 4 Detection
0x9B	RANGE4_L	Threshold of Range 4 Detection
0x9C	RANGE5_L	Threshold of Range 5 Detection

0x9D	PRESET_S_CODE_0	S Code of Range 0
0x9E	PRESET_S_CODE_1	S Code of Range 1
0x9F	PRESET_S_CODE_2	S Code of Range 2
0xA0	PRESET_S_CODE_3	S Code of Range 3
0xA1	PRESET_S_CODE_4	S Code of Range 4
0xA2	PRESET_S2_CODE	S1 MSB Code of All Range
0xA3	AFSM_MOD	Audio FSM Mode
0xA4	HDMI_DYNAMIC_I_CTRL	Dynamic I Code Control
0xA5	HDMI_INI_ICB_M	Initial I Code
0xA6	HDMI_INI_ICB_L	Initial I Code

Register:: HDMI_SR 0xCB				
Name	Bits	R/W	Reset State	Comments
AVMUTE_BG	7	R	0	AV_MUTE Flag under Background (write 1 clear) 1: Means HW receive Set_AVMUTE flag of General Control packet
AVMUTE	6	R	0	AV_MUTE flag of General Control Packet 0: If HW receive Clear_AVMUTE flag of General Control Packet ,this bit shall assign to 0 until HW receive Set_AVMUTE 1: If HW receive Set_AVMUTE flag of General Control Packet ,this bit shall assign to 1 until HW receive Clear_AVMUTE Note : If HW never receives “General Control Packet”, this bit shall set to 0. If HW receive “General Control Packet” with Clear_AVMUTE flag = 0 & Set_AVMUTE flag = 0, this bit shall keep previous value. If HW receive “General Control Packet” with Clear_AVMUTE flag = 1 & Set_AVMUTE flag = 1, this bit shall keep previous value, but set “General Control Packet error flag”.
VIC	5	R	0	If VIC(In AVI Infoframe) is different with pervious value ,this bit would be assigned to 1 until clear this bit. (write 1 clear for each bit)
SPDIFTYPE	4	R	0	SPDIF coding type 0: LPCM 1: Non-LPCM
PLLSTS	3	R	0	PLL status. This bit is global status, we could watch more detail information in PLL detail status byte. (write 1 clear for each bit) 1: non-lock 0: lock
AFIFOOF	2	R	0	0: Audio FIFO isn't overflow for X samples 1: Audio FIFO is overflow for X sample (write 1 clear for each bit) If audio FIFO has stayed at overflow state for X-sample periods, this bit would be set to ‘1’ until F/W clear this bit.
AFIFOUF	1	R	0	0: Audio FIFO isn't underflow for Y samples 1: Audio FIFO is underflow for Y sample (write 1 clear for each bit) If audio FIFO has stayed at underflow state for Y-sample periods, this bit would be set to ‘1’ until F/W clear this bit.
MODE	0	R	0	HDMI/DVI mode detected by auto function, even in manual mode, this bit could indicate decision of auto function. 0: DVI 1: HDMI

FW should read “PLL status” after 0.66ms~3 ms from FW clear this bit.

Register:: HDMI_GPVS 0xCC				
Name	Bits	R/W	Reset State	Comments

NPS	7	R	0	Null Packet Status
PIS	6:5	R	0	Packet Input Status 6: RSV1 received(Write 1 clear) 5: RSV0 received(Write 1 clear)
PVS	4:0	R	0	Packet Variation Status(Wrie 1 clear) 0: AVI infoframe 1: Audio infoframe 2: ACP 3: ISRC1 4: MPEG infoframe

Note. Write 1 Clear

“Packet variation status”:

1. “Packet variation status” means packet content variation, bit4 ~ bit 0 corresponds to AVI info-frame, audio info-frame, ACP, ISRC1, and MPEG info-frame respectively.
2. Before FW process the corresponding action item, FW should clear the corresponding bit of “Global Packet variation status”.
3. Then FW read the content of the corresponding packet, polling “Global Packet variation status”, check if corresponding bit of “Global Packet variation status” is 0, and execute follow-up action item if this bit is 0.
4. Jump to step 2 if this bit is 1.
5. The variation result appears in “Global Packet variation status” after the corresponding packet finish transmitting.

“Packet input status”:

1. “Packet input status” represents updated status of RSV1, RSV0 respectively. If it is updated, “Packet input status” is assigned to 1 until F/W clear this bit.
2. “Null Packet status” :When receive null packet , “Null Packet status” is assigned to 1until F/W clear this bit
3. If one bit of “Packet variation status” is cleared, the corresponding bit of “local variation flag for detail info” is also cleared.

Register:: HDMI_PSAP 0xCD				
Name	Bits	R/W	Reset State	Comments
APSS	7:0	R/W	0	Address for Packet Storage SRAM

Register:: HDMI_PSDP 0xCE				
Name	Bits	R/W	Reset State	Comments
DPSS	7:0	R	0	Data Port for Packet Storage SRAM

BCH is stored in the 1st address of each packet type, its content is stated as following:

Bit0: 2-bit error for bch header (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit1: 2-bit error for bch block 0 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit2: 2-bit error for bch block 1 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit3: 2-bit error for bch block 2 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit4: 2-bit error for bch block 3 (0: 2-bit error doesn't occur; 1: 2-bit error occurs)
 Bit5: checksum result (0: checksum error doesn't occur; 1: checksum error occurs)

Packet Type and Address

Packet type	Variation status	Storage (byte) (+ means BCH)	Address needed (8 bits/add)	Address
AVI info	12+1(global)	16+	17	0~16
Audio info	4+1	8+	9	17~25
ACP	3+1	4+	5	26~30
ISRC1	1+1	18+	19	31~49
ISRC2	X	18+	19	50~68
MPEG info	3+1	8+	9	69~77
RSV0	1, only global	30+	31	78~108
RSV1	1, only global	30+	31	109~139
RSV2	1, only global	30+	31	140~170
RSV3	1, only global	30+	31	171~201
VSPS	2+1	18+	19	202~220

GMPS	6+1	30+	31	221~251
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Table 2 Packet Type and Address SRAM map Table

Following register is assigned by “HDMI-address port”, “HDMI-data port”

Register:: HDMI_SCR 0xCA-00				
Name	Bits	R/W	Reset State	Comments
PIS2	7	R	0	Packet Input Status RSV2 received(Write 1 clear)
PIS1	6	R	0	Packet Input Status RSV3 received(Write 1 clear)
DVI_ACL_K_MODE	5	R/W	1	When switch to DVI mode, select audio clock control mode 0: Old mode (Gate audio PLL output clk, FIFO R/W & Data output) 1: New mode (Audio PLL output clk remains, but FIFO R/W & Data output are gated)
REG_PAC_KET_IGN_ORE	4	R/W	0	HDMI/DVI Mode Detection Method Selection 0: Detect by both Video and Data Island Guard Band. 1: Detect by only Video Guard Band. (Can't be used when auto mode)
MODE	3	R/W	0	HDMI/DVI switch mode 0: Auto detect flow is as Fig.1 1: Manual, determined by bit[2]
MSMODE	2	R/W	0	When manual mode, select HDMI or DVI 0: DVI 1: HDMI
CABS	1	R/W	0	DVI/HDMI condition A, B select 0: condition A: Detect data island preamble + data island guard band (appear count is decided by “N”) condition B: Detect if data island preamble + data island guard band appear in continuous 30 or 2 frames(decide by bit 0) 1: condition A: Detect data island preamble + data island guard band & video preamble + video guard band(appear count is decided by “N”) condition B: Detect if data island preamble + data island guard band & video preamble + video guard band appear in continuous 30 or 2 frames(decide by bit 0)
FCDDIP	0	R/W	0	Frame count to detect data island packet (Condition B) 0: 2 frames 1: 30 frames

1. HDMI/DVI auto switch mode , the information must be passed to HDCP :
DVI/HDMI decision flow is shown as below.

DVI/ HDMI decide flow

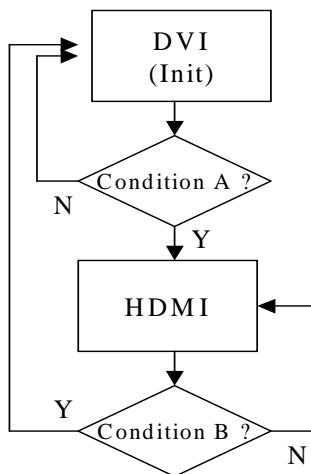


Fig 1

2. Power Saving for HDMI/HDCP :

In Power saving mode, TMDS channel Green/Red are always turn off. HDMI is power down.
There are only TMDS clock input frequency detect and channel blue DE decoder working.
The channel blue DE decoder is active after clock frequency is OK.

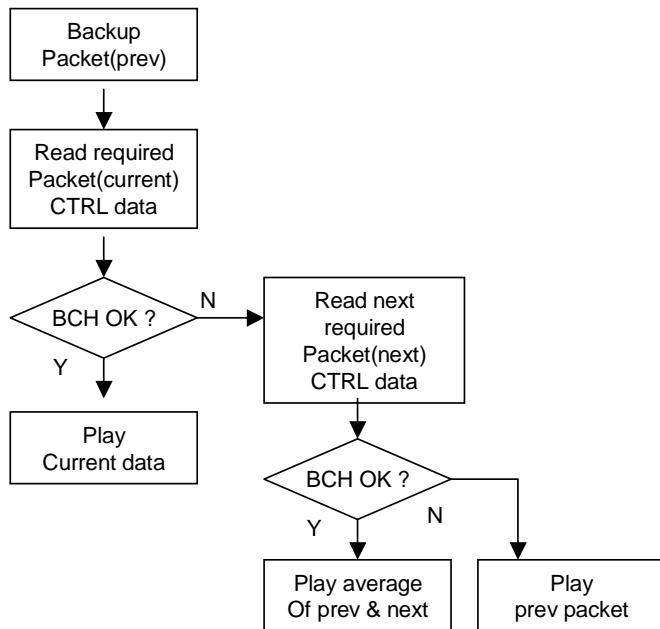
Register::: HDMI_N_VAL 0xCA-01				
Name	Bits	R/W	Reset State	Comments
NVAL	7:0	R/W	1	The N value used to detect guard band (refer to 0xC9-00) N= 00 : X 01 : 1 FF : 255 N = 1 ~ 255 , N can't be assigned to 0x00

Register::: HDMI_BCHCR 0xCA-02				
Name	Bits	R/W	Reset State	Comments
BCH_IRQ	7	R/W	0	IRQ when 2bit BCH error occur enable 0:Disable 1:Enable
BCH_FLAG_CLR_DVI	6	R/W	0	In DVI mode, clear BCH error flag (0xCA-02[2:1]) 0: keep old method (write 0 to clear) 1: auto clear BCH flag
SPCSS	5	R/W	0	SPDIF preamble channel status Source (Can be used when PL) 0: Input audio sample (normal) 1: Internal system
ENRWE	4	R/W	0	Enable noise reduction when BCH error is greater than one. 1: Enable noise reduction 0: Disable noise reduction
BCHE	3	R/W	1	BCH function enable 1: Enable BCH function 0: Disable BCH function, bit[2:1] are always 2'b00.
BCHES	2	R	0	BCH function's result, one bit error. It is set by this case, and This bit is the result of ORing 5 bits BCH 1 bit error. 1: One bit error occurs. 0: No error occurs

				Note: If BCH detect 1-bit error, this bit would be assigned to 1 until next frame.
BCHES2	1	R	0	BCH function's result, two bits error. It is set by this case, and This bit is the result of ORing 5 bits BCH 1 bit error. 1: 2-bit error occurs 0: 2-bit error don't occurs If BCH detect 2-bit error, this bit would be assigned to 1 until next frame.
PE	0	R/W	0	The processing for Packet with two or more BCH error (not including I2S) 1: Block Info frame message 0: As correct frame, decided by F/W NOTE! Audio samples always go to FIFO

Register:: HDMI_AFCR 0xCA-03				
Name	Bits	R/W	Reset State	Comments
TST_I2S_SW	7	R/W	0	Switch of Embedded Test Signal for I2S and DAC 0: Old version, using test_cnt[5:1] as reference counter. 1: New version, using test_cnt[4:0] as reference counter.
AOEM	6	R/W	1	Audio Output Enable mode 1: Auto audio output flow, bit[5:0] could be assigned by HW, but couldn't be assigned by FW. 0: Manual audio output flow, bit[5:0] could be assigned by FW, but couldn't be assigned by HW.
AOC	5	R	0	Audio output on/off control 0: Audio output off, cut off audio output immediately in “manual audio output flow”, and audio output is turned on by auto audio output flow gradually in “auto audio output flow”. 1: Audio output on, switch on audio output immediately in “manual audio output flow”, and audio output is turned on by auto audio output flow gradually in “auto audio output flow”.
AUDIO_TEST_ENABLE	4	R/W	1	0:Disable 1:Generate sine wave to IIS/SPDIF internally This is assigned to “1” in IIS/SPDIF test mode, but it is assigned to “0” in normal mode.
MGC	3	R/W	0	Manual Gain control 1: Enable gain control, gain is decided by “Manual Audio Gain coefficient” 0: Disable gain control, gain = 1
AFIFOWE	2	R/W	0	Audio FIFO write enable (FIFO pointer will be reset when disable) 0: Disable, no audio sample would go in audio FIFO. This bit would clear Audio FIFO status, including read/write address, ovfl, unfl, and etc. 1: Enable FIFO audio Write, and enable bit[1:0] function, read control . (If buffer write to target depth, new data read out action is controlled by bit1).
AFIFORE	1:0	R/W	0	Audio FIFO read enable, this bit is only active when bit[2] = 1, 00: No audio frequency read, only drop old data when new data in. 01: Audio sample which read from FIFO repeats previous sample, only drop old data when new data in. 1x: Use audio frequency to read out FIFO.

Audio noise reduction 1



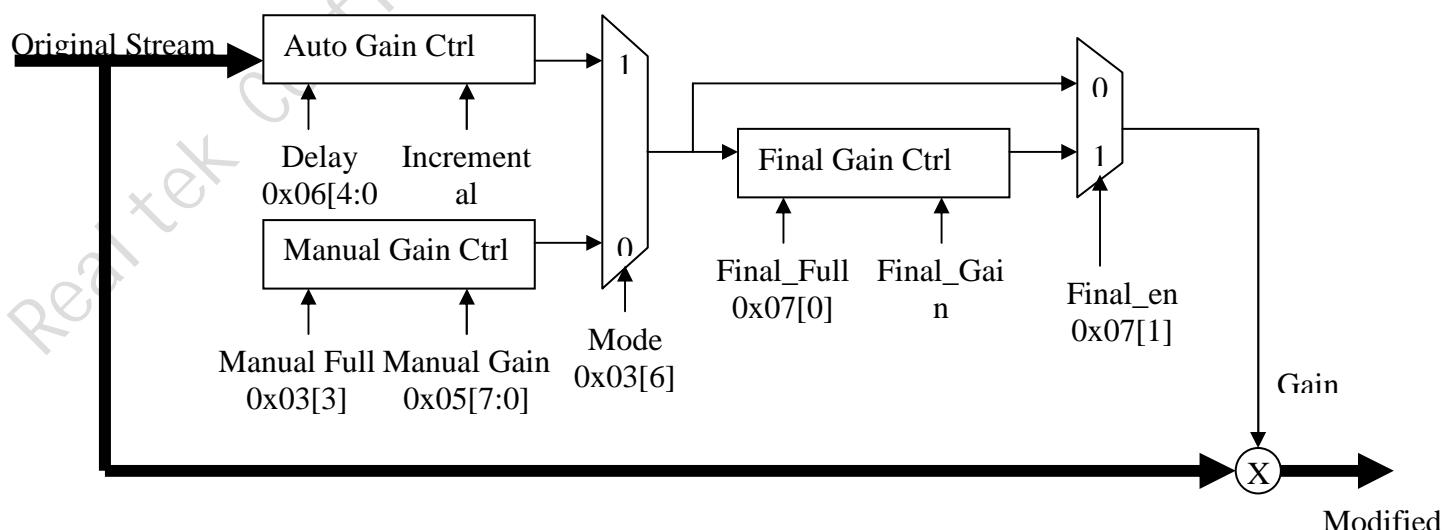
Register:: HDMI_AFSR 0xCA-04				
Name	Bits	R/W	Reset State	Comments
BCH_Watdog	7	R/W	0	Watchdog when 2bit BCH error occur enable 0: disable 1: enable
Reserved	6	R/W	0	Reserved
BISTR	5	R	1	Audio FIFO BIST Result 0: fail 1: success
BISTS	4	R/W	0	Audio FIFO BIST Start (embedded test pattern) 0: stop 1: start(auto clear)
AFIFOF	3	R	0	Audio FIFO Full (write clear) 0: Indicate FIFO is not full. 1: Indicate FIFO is full.
AFIFOE	2	R	0	Audio FIFO Empty(write clear) 0: Indicate FIFO is not empty. 1: Indicate FIFO is empty.
AFIFO_DEPTH_REACH	1	R	0	Current Audio FIFO Depth Reach Target Depth 0: Not yet reached 1: Reached (Target Depth is set at 0xCA-1B[7:3])
Reserved	0 1:0	---	0	Reserved to 0

Register:: HDMI_MAGCR 0xCA-05				
Name	Bits	R/W	Reset State	Comments
MG	7:0	R/W	0	Manual Gain. Unsigned floating. NOTE, gain value here is always less than 1. 8'h00 = 0 8'hFF = 1 - 2^-8

Only valid when “Manual Gain control” is enabled in “manual audio output flow”

Register:: HDMI_MAGCR 0xCA-06				
Name	Bits	R/W	Reset State	Comments
AGI	7:5	R/W	4	Auto Gain Incremental 000 : 2^{-8} 001 : 2^{-7} 010 : 2^{-6} ... 111 : 2^{-1}
AGD	4:0	R/W	4	Auto Gain Delay 00000 : 2^0 sample 00001 : 2^1 samples 00010 : 2^2 samples ... 00111 : 2^7 samples 01000 : 2^8 samples 01001 : 2^9 samples 01010 : 2^{10} samples ... 01111: 2^{15} samples 10000: 2^{16} samples 10001: 2^{17} samples 10010: 2^{18} samples 10011: 2^{19} samples 10100: 2^{20} samples Others: Not used. The total meanings of this byte are: When Auto audio function is on, gain increase from 0 to 1 with ‘incremental’ per ‘delay’. When Auto audio function is off, gain decrease from 1 to 0 with ‘-inc’ per ‘delay’. So that the default value means increase 2^{-5} per 16 samples.

Only valid in “auto audio output flow”



Register:: HDMI_MAG_M_FINAL 0x CA-07				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	--	0	Reserved.
AUTO_DLY_MOD	3	R/W	1	Automatically modify the “Auto Gain Delay” 0: Keep original “Auto Gain Delay” 1: According the Auto Audio Sampling Rate Detection Function to adjust the “Auto Gain Delay” automatically. If AFREQ_MEAS_RANGE == 000: Auto Gain Delay’ = Auto Gain Delay 001: Auto Gain Delay’ = Auto Gain Delay/4 010: Auto Gain Delay’ = Auto Gain Delay/4 011: Auto Gain Delay’ = Auto Gain Delay/2 100: Auto Gain Delay’ = Auto Gain Delay 101: Auto Gain Delay’ = Auto Gain Delay Others: Auto Gain Delay’ = Auto Gain Delay
FG_EN	2	R/W	1	Enable Final Gain control 1'b0: Original Design 1'b1: Enable Final Gain Control
FFG_L	1	R/W	1	Left Channel F Gain. Full gain 1'b0: Gain is controlled by 0x08 1'b1: Full gain.
FFG_R	0	R/W	1	Right Channel F Gain. Full gain 1'b0: Gain is controlled by 0x09 1'b1: Full gain.

Register:: HDMI_MAG_L_FINAL 0x CA-08				
Name	Bits	R/W	Reset State	Comments
FG_L	7:0	R/W	0	F Gain. Unsigned floating. NOTE, gain value here is always less than 1. 8'h00 = 0 8'hFF = 1 - 2^-8

Register:: HDMI_MAG_R_FINAL 0x CA-09				
Name	Bits	R/W	Reset State	Comments
FG_R	7:0	R/W	0	F Gain. Unsigned floating. NOTE, gain value here is always less than 1. 8'h00 = 0 8'hFF = 1 - 2^-8

Register:: AUDIO_LD_P_TIME_M CA-0x0A				
Name	Bits	R/W	Reset State	Comments
RESERVED	7:3	--	0	Reserved.
LDP_TIME_MODE	2	R/W	1	The mode of Wait-TIME for loading parameter 0: Old mode: 1024*Xclk 1: New mode: LDP_TIME * 200us
LDP_TIME[9:8]	1:0	R/W	0	Wait-time for HW getting stable. (Base clock is 5kHz), During this period, there'll be no audio outputted. 0: 200us 1: 400us ... 1023: 0.2048s

Note: the LDP_TIME[9:8] will be double-buffered when 0x0B is written.

Register:: AUDIO_LD_P_TIME_N CA-0x0B				
Name	Bits	R/W	Reset State	Comments
LDP_TIME[7:0]	7:0	R/W	2	Wait-time for HW getting stable. (Base clock is 5kHz)

				0: 200us 1: 400us ... 1023: 0.2048s
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Zero-Crossing Detection & Application of Final Gain

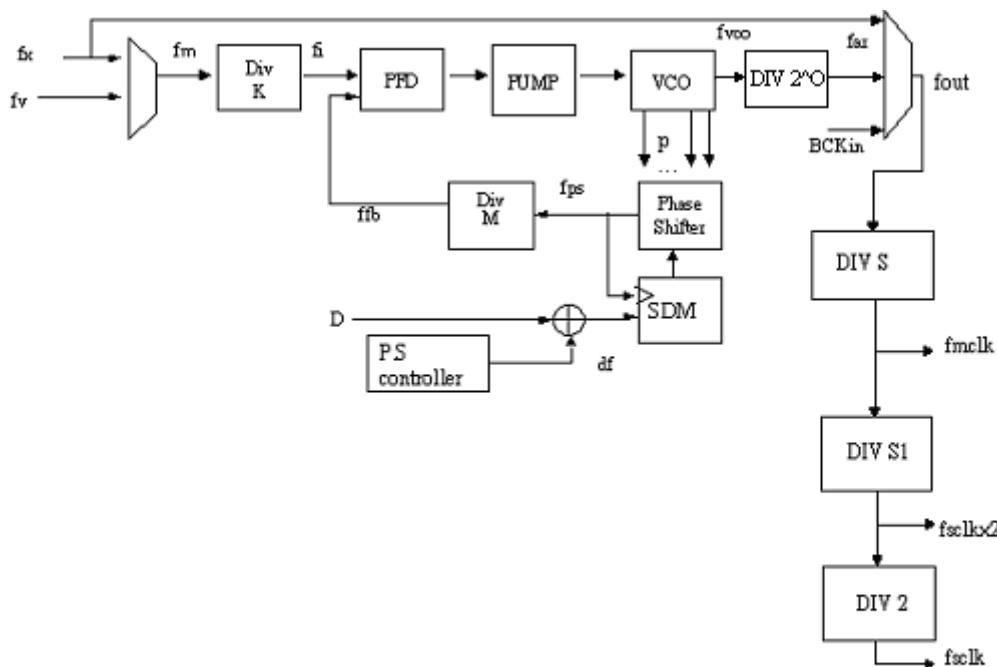
Register:: ZCD_CTRL 0x CA-0C				
Name	Bits	R/W	Reset State	Comments
ZCD_EN	7	R/W	1	Final Gain controlled by zero crossing detection 0: Disabled. 1: Enabled. (0x07[1:0] & 0x08 & 0x09 are applied when zero-crossing)
ZCD_SEP_8CH	6	R/W	1	Final Gain (8-ch) 0: 8-channel volumes are controlled at the same time. (Once any one of 8-channel detects zero-crossing, then apply the final gain to all channels) 1: Determined by .0x0C[5]
ZCD_SEP_ST	5	R/W	1	Final Gain (Stereo) 0: L/R volumes are controlled at the same time. (Once L or R detects zero-crossing, then apply the final gain to both channels) 1: L/R volumes are controlled separately.
RESERVED	4:0	R/W	0	Reserved

Register:: ZCD_TIMEOUT 0x CA-0D				
Name	Bits	R/W	Reset State	Comments
RESERVED	7	R/W	0	Reserved
ZCD_TIMEOUT	6:0	R/W	3	Force to apply final gain when time-out. Interval = Xtal * 512 Timeout = Interval * {(ZCD_TIMEOUT +1), 3'b000}

ZCD_CHx_DONE is cleared when new gain value is set.

Register:: ZCD_STATUS 0x CA-0E				
Name	Bits	R/W	Reset State	Comments
ZCD_CH7_DONE	7	R	--	ZCD of Channel 7 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH6_DONE	6	R	--	ZCD of Channel 6 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH5_DONE	5	R	--	ZCD of Channel 5 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH4_DONE	4	R	--	ZCD of Channel 4 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH3_DONE	3	R	--	ZCD of Channel 3 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH2_DONE	2	R	--	ZCD of Channel 2 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH1_DONE	1	R	--	ZCD of Channel 1 has been detected and Gain has been also applied. Write 1 to clear.
ZCD_CH0_DONE	0	R	--	ZCD of Channel 0 has been detected and Gain has been also applied. Write 1 to clear.

Audio Clock Regeneration



Definition :

fx : frequency of crystal
 fv : frequency of video
 fa : audio frequency
 fout : $128 * fa$
 far : recovered $128 * fa$
 fm : freq. of mux-clock
 fyco : frequency after V

fps : frequency after P.S
ffb : feed back frequency
P.S : Phase Swallow
p : number of phase
D : P.S density, shift D phase per cycle
df : fine tune of D
T* : Period of f*

NOTE!!! Signed number and detail procedures are not ready.

Register:: HDMI_CMCR					0x CA-10
Name	Bits	R/W	Reset State	Comments	
ICMUX	7	R/W	0	Input Clock MUX 1: use video clock as input 0: use crystal clock as input	
OCS	6:5	R/W	2	Output Clock Select 00: use crystal clock as output clock. 01: use BCKin as output clock 1X: use generated clock, far, as output clock (must set when power-saving)	
DBDCB	4	R/W	0	Double Buffer Download Control Bit Enable is also triggered by HW, ref. "Phase error mode". 1: write current data to active buffer. 0: after write done, this bit would be cleared automatically. When set this bit to 1, "K", "S", "S1", "M", "D", "O", "DPLLBN", "In/out clk mux", "Phase tracking enable control bits" would fill in after finish current audio PLL cycle and then set this bit to 0.	
KCAPLL	3:0	R/W	3	K Code of Audio PLL , the value set here adding 1 is real div value 0000: div 2 1111: div 17 If "DPLLBN" == 1'b1, no div, else, div number is decided by these four bits.	

NOTE:

- When reading the registers with double buffers, the read-out value is the value in the 2nd buffer, not the value just

- written.
2. The meaning of default value of registers with double buffers is that default values of both 1st registers and 2nd buffer are the value written in spec.

Register:: HDMI_MCAPR					0x CA-11
Name	Bits	R/W	Reset State	Comments	
MC	7:0	R/W	4E	M Code 00: div 2 FF: div 257	

Register:: HDMI_SCAPR					0x CA-12
Name	Bits	R/W	Reset State	Comments	
SLC	7	R/W	0	S1 code 0: div 1 1: div 2	
SC	6:0	R/W	5	S2 code	

Register:: HDMI_DCAPR0					0x CA-13
Name	Bits	R/W	Reset State	Comments	
DCAPR	7:0	R/W	0	D[15:8]	

Register:: HDMI_DCAPR1					0x CA-14
Name	Bits	R/W	Reset State	Comments	
DCAPR	7:0	R/W	0	D[7:0]	

Register:: HDMI_PSCR					CA-0x15
Name	Bits	R/W	Reset State	Comments	
FDINT	7:5	R/W	7	When max. FIFO depth increase for n times or min. FIFO depth decrease for n times, turn FIFO tracking mechanism 000 : xx 001 : n=2, don't use this value for normal case 010 : n=3 011 : n=4 100 : n=5 101 : n=6 110 : n=7 111 : n=8	
ETCN	4	R/W	0	Enable tracking of CTS & N 0: disable. 1: enable.	
ETFD	3	R/W	0	Enable tracking of the trend of FIFO depth 0: disable. 1: enable.	
ETFBC	2	R/W	0	Enable tracking of FIFO boundary condition (This bit is suggested to be 1) 0: disable. 1: enable.	
PECS	1:0	R/W	1	Phase error count source(CTS & N) 00 : phase error counted by video clock 01 : phase error counted by crystal clock 10 : phase error counted by fps/4, fdds 11 : It is too fast, about 500MHz,to be used	

Note. Phase tracking control bits is bit4~bit2.

Total FIFO depth is 32 samples

Register:: HDMI_FDDR 0x CA-16				
Name	Bits	R/W	Reset State	Comments
FDDR	7:0	R	0	FIFO depth at DE rising , this unit is number of samples,

Register:: HDMI_FDDF 0x CA-17				
Name	Bits	R/W	Reset State	Comments
FDDF	7:0	R	0	FIFO depth at DE falling

Register:: HDMI_MFDDR 0x CA-18				
Name	Bits	R/W	Reset State	Comments
MFDDR	7:0	R	0	Max. FIFO depth at DE rising. Auto clear to 0x00 when up-trend is confirmed and frequency up is triggered. Write 1 to clear this byte as 0x00.the clear action needs video clock to work.

Register:: HDMI_MFDDF 0x CA-19				
Name	Bits	R/W	Reset State	Comments
MFDDF	7:0	R	0	Min. FIFO depth at DE falling. Auto clear to 0xFF when down-trend is confirmed and frequency down is triggered. Write 1 to clear this byte as 0x00.the clear action needs video clock to work. Write 1 to clear.

Register:: HDMI_FTR 0x CA-1A				
Name	Bits	R/W	Reset State	Comments
TL2DER	7:6	R	0	Trend of latest 2 DE rising. 0X: the same 10: trend down, which means FIFO depth goes lower and lower. 11: trend up, which means FIFO depth goes larger and larger.
TL2DEF	5:4	R	0	Trend of latest 2 DE falling. 0X: the same 10: trend down, which means FIFO depth goes lower and lower. 11: trend up, which means FIFO depth goes larger and larger.
TT	3:0	R/W	7	Target times for summation of one trend to decide the trend. Times = value set + 1 0000 : 1, 1111 : 16

Register:: HDMI_FBR 0x CA-1B				
Name	Bits	R/W	Reset State	Comments
TFD	7:3	R/W	E	Target FIFO depth , the unit is 4 address, and 16 bits in one address.
BAD	2:0	R/W	2	Boundary address distance for triggering Audio PLL tracking where boundary address= value set * 4, and 16 bits per address. 4 bytes*16 bits is one sample. When the value is 2,number of sample is 0,1,31,and 32 will trigger boundary condition. Value 0 can't be used.

PI Code is double buffered when LSB is written

Register:: HDMI_ICPSNCR0 0x CA-1C				
Name	Bits	R/W	Reset State	Comments
IC	7:0	R/W	0	I code of N/CTS [15:8]

Register:: HDMI_ICPSNCR1 0x CA-1D				
Name	Bits	R/W	Reset State	Comments

IC	7:0	R/W	0	I code of N/CTS [7:0]
Register:: HDMI_PCPSNCR0 0x CA-1E				
Name	Bits	R/W	Reset State	Comments
PC	7:0	R/W	0	P code of N/CTS [15:8]
Register:: HDMI_PCPSNCR1 0x CA-1F				
Name	Bits	R/W	Reset State	Comments
PC	7:0	R/W	0	P code of N/CTS [7:0]
Register:: HDMI_ICTPSR0 0x CA-20				
Name	Bits	R/W	Reset State	Comments
ICT	7:0	R/W	0	I code of trend [15:8]
Register:: HDMI_ICTPSR1 0x CA-21				
Name	Bits	R/W	Reset State	Comments
ICT	7:0	R/W	0	I code of trend [7:0]
Register:: HDMI_PCTPSR0 0x CA-22				
Name	Bits	R/W	Reset State	Comments
PCT	7:0	R/W	0	P code of trend [15:8]
Register:: HDMI_PCTPSR1 0x CA-23				
Name	Bits	R/W	Reset State	Comments
PCT	7:0	R/W	0	P code of trend [7:0]
Register:: HDMI_ICBPSR0 0x CA-24				
Name	Bits	R/W	Reset State	Comments
ICB	7:0	R/W	0	I code of boundary [15:8]
Register:: HDMI_ICBPSR1 0x CA-25				
Name	Bits	R/W	Reset State	Comments
ICB	7:0	R/W	0	I code of boundary [7:0]
Register:: HDMI_PCBPSR0 0x CA-26				
Name	Bits	R/W	Reset State	Comments
PCB	7:0	R/W	0	P code of boundary [15:8]
Register:: HDMI_PCBPSR1 0x CA-27				
Name	Bits	R/W	Reset State	Comments
PCB	7:0	R/W	0	P code of boundary [7:0]
Register:: HDMI_NTx1024TR0 0x CA-28				
Name	Bits	R/W	Reset State	Comments
Reserved	7:6	---	0	Reserved to 0
AUDIO_NCTS_EN	5	R/W	0	When Tx's audio clock regeneration packet N = 0/CTS = 0, decide whether update the tracking N/CTS value or not

				0: update 1: not update
S1_CODE_MSB	4	R/W	0	S1 Code MSB bit 0: Depends on LSB bit 1: div 4
RM	3	R/W	0	Restart measure. Measure the length of 1024 Tv by crystal. The result is readable from the following bits. 1: enable measure. Writing 1 would clear the answer. This bit would be auto cleared after measure done. 0: indicating measure is done.
NT	2:0	R	0	Number of Tx for 1024 Tv [10:8], (How many Tx = 1024 * Tv)

Register:: HDMI_NTx1024TR1 0x CA-29				
Name	Bits	R/W	Reset State	Comments
NT	7:0	R/W	0	Number of Tx for 1024 Tv [7:0], (How many Tx = 1024 * Tv)

Register:: HDMI_STBPR 0x CA-2A				
Name	Bits	R/W	Reset State	Comments
FTB	7:0	R/W	0	The fast time for boundary df repeating. The unit is 16 crystal clock. 8'h00: 16 crystal clock. 8'h7F: 128 * 16 crystal clock.

Register:: HDMI_NCPER 0x CA-2B				
Name	Bits	R/W	Reset State	Comments
NCPER	7:0	R	0	Phase error equals how many numbers of measuring clock, PE[7:0]

NOTE!! The active PI code of CTS&N would have proportional alike relation with Phase error.

The value of this byte is record of the maximum value after last write.

Write this byte when fpec exists would clear the value to 0.

When “pe_mode”==1, delay mode, the max value of phase error is 40.

When “pe_mode”==1, clock mode, the max value of phase error is FF.

Register:: HDMI_PETR 0x CA-2C				
Name	Bits	R/W	Reset State	Comments
PETR	7:0	R/W	FF	Phase error threshold of audio PLL non-lock

If “Phase error” is greater than phase error threshold, “PLL status” would be automatically assigned to 1 until FW clear it.

Register:: HDMI_AAPNR 0x CA-2D				
Name	Bits	R/W	Reset State	Comments
CMVTC	7	R/W	0	Clear max value (18, 19) when trend condition is true. 1: Enable trend to clear max value 0: Disable this function
CMVBC	6	R/W	0	Clear max value (18, 19) when boundary condition is true. 1: Enable boundary to clear max value 0: Disable this function
SSDMOU	5	R	0	Flag of sum_r of SDM overflow/underflow (Read only) 1: Overflow or underflow happened 0: No overflow, no underflow
TEF	4	R/W	0	Trend Error Flag 1: Detect up and down at the same time. Clear only when disable SDM (2D[1] = 0) 0: Trend is ok.
W1C5	3	W	0	Write 1 to clear bit [5]
PEM	2	R/W	0	Phase Error Mode, 1: Use delay to calculate, each unit is 0.1 ns.

				0: Use clock to calculate, the clock select is at “PE count source”.
ESDM	1	R/W	0	Enable SDM (phase swallow) 1: Enable 0: Disable, there won't be phase swallow operating in the loop of PLL.
Reserved	0	---	0	Reserved

Register:: HDMI_APDMCR 0x CA-2E				
Name	Bits	R/W	Reset State	Comments
Reserved	7:6	---	0	Reserved
EDM	5	R/W	0	Enable Debug Mode 0: Normal run 1: Enable when test mode
PST	4	R/W	0	Phase swallow trend 0: Fast direction 1: Slow direction
PSC	3:0	R/W	0	Phase Swallow Cycle. Any bit is set to 1 for swallow, 0 for hold.

Behavior description of audio PLL non-clock

When system receive new audio or video timing , audio PLL would non-lock ,and watch dog mechanism would force audio output to mute state(I2S DAC: MCLK,SCLK, and LRCK normal output, but SDATA output zero),so system should provide a stable fout to I2S DAC in audio mute state.

In the transition form normal fout to mute fout , fout frequency couldn't change too much, for this reason ,HW provide double buffers of mechanism of “ K”, “S”, “S1”, “M”, “D”, “O”, “DPLLBN”, “In/out clk mux”, “Phase tracking enable control bits”.

For initial state, a stable fv input to audio PLL, and audio PLL would lock by use suitable “KMSDO”&PI code.The suitable “KMSDO” could be named as “KMSDO1”,and it would save in 2nd buffer(The value of 2nd buffer could be applied to audio PLL directly , and that of 1st buffer is used to backup, when “double buffer download control bit” is assigned to 1,the value of 1st buffer would be downloaded to 2nd buffer).F/W should calculate “KMSDO2” of crystal clock input to produce a fout which is the same as present fout ,then save KMSDO2 in 1st buffer of KMSDO, F/W also assign “phase tracking control bits” to 000'b in 1st buffer, and assign “input clock mux” to “crystal input” in 1st budder.

When audio PLL is non-lock(change audio frequency or video frequency),the 1st buffer content of “KMSDO”, “phase tracking control bits”, and “input clock mux” would download to their corresponding 2nd buffers. Then audio PLL would switch input to crystal in, apply KMSDO2, and disable phase tracking at the same time, and provide a stable fout to I2SDAC foe mute state.

In mute state, F/W calculate KMSDO(KMSDO3) of new audio or video timing, assign KMSDO3 in 1st buffer of KMSDO, F/W also assign “enable setting” in 1st buffer of phase tracking enable control, and assign “video input” to second buffer of input clock mux.

Assign PI code, then double buffer download control bit is assigned to 1, audio PLL would switch input to video in, apply KMSDO3, and disable phase tracking at the same time, and provide a fout for new video and audio timing.

Register:: HDMI_AVMCR 0x CA-30				
Name	Bits	R/W	Reset State	Comments
AVMUTE_WIN_EN	7	R/W	0	Avmute Window Enable 1: Enable 0: Disable If this bit is enabled, avmute signal will be blocked when in the invalid region. The valid region depends on the setting of register 0xA8
AOC	6	R/W	0	Audio output enable/disable control 1: Enable 0: Disable

				If this bit is enabled, audio output signal would be controlled by bit4. When FW set this bit to 1, then HW will return this bit to 0 if audio PLL non-lock if audio PLL non-lock.
AOMC	5	R/W	0	Audio Output Mute Control 1: Normal output 0: Mute If bit 5 is 0, output of I2S & SPDIF shall be disabled regardless of 1 or 0 in this bit for “auto audio output flow”. When FW set this bit to 1, then HW will return this bit to 0 if audio PLL is non-lock
AWD	4	R/W	0	If Audio Watch Dog event occur, audio output would be 0: Mute 1: Disable
VE	3	R/W	0	Video clock output Enable. When video watch dog occurs, this bit will be reset to 0. 1: Enable video clock output 0: disable video clock output
AMPIC	2	R/W	0	Audio Mute Pin Invert Control, execute when mute/disable happens. 0: when event (audio mute or disable) occur, set this pin to low voltage, others maintain high. 1: when event (audio mute or disable) occur, set this pin to high voltage, others maintain low
VDPIC	1	R/W	0	Video Disable Pin Invert Control 0: when event (video disable) occurred, set this pin to low voltage, others maintain high. 1: when event (video disable) occurred, set this pin to high voltage, others maintain low.
NFPSS	0	R/W	0	IRQ Output Pin Polarity Inverse 0: no inverse, which means H : IRQ, L : no IRQ 1: inverse, which means H : no IRQ L : IRQ

Definition:

Disable Video Assign “DE pins”, “VS pin”, “HS pin”, “CTRL(4) pins”, “CLK pin”, “Data(24) pins” to zero , refer to “Global System”

- Mute Audio**
1. In I2S application, keep MCLK*4, SCLK*4, and LRCK*4 to normal output, but cut SDATA*4 to zero.
 2. In SPDIF application, keep preamble(M,B,W) to normal output, but cut other bits to zero.

Disable Audio I2S => assign MCLK*4, SCLK*4, and LRCK*4 and SDATA*4 to zero.
SPDIF => Assign all bits to zero.

Register::: HDMI_WDCR0 0x CA-31				
Name	Bits	R/W	Reset State	Comments
ASMFE	7	R/W	1	Auto SET_AVMUTE function enable 0: If HW receives SET_AVMUTE flag, don't mute/disable audio & disable video by HW. 1: If HW receives SET_AVMUTE flag, mute/disable audio & disable video by HW. <i>Note:</i> If “CLEAR_AVMUTE” and “SET_AVMUTE” of the General Control Packet are all 1, keep previous A/V output state, and pull up “General Control Packet error flag”
load_d_code	6	R/W	0	Enable Load DCode 0: disable 1: enable
audio_wd_by_vic	5	R/W	0	In audio FIFO tracking process(trend and boundary tracking), when phase

				error occurs, the behavior of I/P code: 0: I/P code doesn't work, i.e., I/P code of HW use = 16'b0 1: I/P code work, i.e., I/P code of HW use = register setting
AWDCT	4	R/W	0	Audio watch dog for audio coding type(Decode from SPDIF, code type only include LPCM or Non-LPCM) 0: If coding type is different with previous type, don't mute/disable audio by HW. 1: If coding type is different with previous type, mute/disable audio by HW.
AWDAP	3	R/W	0	Audio Watch dog enable for audio PLL 0: If audio PLL is non-lock, don't mute/disable audio by HW. 1: If audio PLL is non-lock, mute audio , mute/disable audio by HW.
AWDFO	2	R/W	0	Audio watch dog function for audio FIFO overflow for "X" sample. 0: If audio FIFO is overflow for X samples , don't mute/disable audio by HW. 1: If audio FIFO is overflow for X samples, mute/disable audio by HW.
AWDFU	1	R/W	0	Audio watch dog function for audio FIFO underflow for "Y" sample. 0: If audio FIFO is underflow for Y samples, don't mute/disable audio by HW. 1: If audio FIFO is underflow for Y samples, mute/disable audio by HW.
CT	0	R/W	0	"SPDIF coding type" is decoded by 0: Channel status bit 1 1: Valid bit

Audio/Video watch dog for “packet acquire mechanism” is listed in Packet acquire mechanism Unit.

Register:: HDMI_WDCR1 0x CA-32				
Name	Bits	R/W	Reset State	Comments
AWDCK	7	R/W	0	Audio Watch Dog For TMDS clock 1: If TMDS clock disappears, mute or disable audio. 0: If TMDS clock disappears, doesn't mute or disable audio.
AWDLF	6	R/W	0	Audio Watch Dog For Layout Field Of Audio Sample Packet 1: If layout field is different with previous value, mute or disable audio. 0: If layout field is different with previous value, don't mute or disable audio.
Rev VWDMOD	5	R/W	0	Reserved Video Watch Dog Mode 0: Old Mode (Gated Clk) 1: New Mode (RGB Output Disable)
VWDACT	4	R/W	0	Video Watch Dog For Audio Coding Type 1: If coding type is different with previous type, disable video 0: If coding type is different with previous type, don't disable video
XV	3:0	R/W	0	X Value 0000: 1 0001: 3 ~ 1111: 31

Register:: HDMI_WDCR2 0x CA-33				
Name	Bits	R/W	Reset State	Comments
VWDAP	7	R/W	0	Video Watch dog enable for audio PLL 1: If audio PLL is non-lock, disable video 0: If audio PLL is non-lock, don't disable video
VWDLF	6	R/W	0	Video watch dog for layout field of audio sample packet 1: If layout field is different with previous value, disable Video. 0: If layout field is different with previous value, don't disable Video.
VWDAFO	5	R/W	0	Video watch dog function for audio FIFO overflow. 1: If audio FIFO is overflow for "X" samples, disable Video. 0: If audio FIFO is overflow for "X" samples, don't disable Video.
VWDAFU	4	R/W	0	Video watch dog function for audio FIFO underfloww . 1: If audio FIFO is underflow for "Y" samples, disable Video. 0: If audio FIFO is overflow for "Y" samples, don't disable Video
YV	3:0	R/W	0	Y value 0000:1

				0001:3 ~ 1111:31
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Register:: HDMI_DBCR 0x CA-34				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	R/W	0	Reserved
ALDBFv	3	R/W	0	<p>Auto Load Double Buffer when TMDS clock disappear (0xC9-10[4])</p> <p>0: If TMDS clock disappear , don't assign "double buffer download control bit" to 1 by HW</p> <p>1: If TMDS clock disappear, assign "double buffer download control bit" to 1 by HW.</p> <p><i>Note:</i></p> <p>If this bit is 0, "phase tracking control bits" shall be downloaded to 2nd buffer by assigned "double buffer download control bit" to 1.</p> <p>If this bit is 1, "phase tracking control bits" shall be downloaded to 2nd buffer by HW if fv < 25MHz or fv > 165MHz.</p>
ALDBFO	2	R/W	0	<p>Auto Load Double Buffer when FIFO overflow is for X samples.</p> <p>0: If audio FIFO is overflow for X samples, don't assign "double buffer download control bit" to 1 by HW</p> <p>1: If FIFO is overflow for X samples, assign "double buffer download control bit" to 1 by HW.</p> <p><i>Note:</i></p> <p>If this bit is 0, "phase tracking control bits" shall be downloaded to 2nd buffer by assigned "double buffer download control bit" to 1.</p> <p>If this bit is 1, "phase tracking control bits" shall be downloaded to 2nd buffer by HW if FIFO is overflow for X samples.</p>
ALDBFU	1	R/W	0	<p>Auto Load Double Buffer when FIFO underflow is for Y samples.</p> <p>0: If audio FIFO is underflow for Y samples, don't assign "double buffer download control bit" to 1 by HW</p> <p>1: If FIFO is underflow for Y samples, assign "double buffer download control bit" to 1 by HW.</p> <p><i>Note:</i></p> <p>If this bit is 0, "phase tracking control bits" shall be downloaded to 2nd buffer by assigned "double buffer download control bit" to 1.</p> <p>If this bit is 1, "phase tracking control bits" shall be downloaded to 2nd buffer by HW if FIFO is underflow for Y samples.</p>
ALDBPN	0	R/W	0	<p>Auto Load Double Buffer when PLL non-lock.</p> <p>This function needs crystal clock to work, which means it can't work when power down.</p> <p>After PLL non-lock,</p> <p>0: If audio PLL non-lock occurred, don't assign "double buffer download control bit" to 1 by HW</p> <p>1: If audio PLL non-lock occurred, assign "double buffer download control bit" to 1 by HW.</p> <p><i>Note:</i></p> <p>If this bit is 0, "phase tracking control bits" shall be downloaded to 2nd buffer by assigned "double buffer download control bit" to 1.</p> <p>If this bit is 1, "phase tracking control bits" shall be downloaded to 2nd buffer by HW if "PLL status" is non-lock.</p>

Register:: HDMI_APTMCR0 0x CA-35				
Name	Bits	R/W	Reset State	Comments
FPS	7:4	R/W	0	1st phase shift amount for a step
SPS	3:0	R/W	0	2nd phase shift amount for a step

Register:: HDMI_APTMCR1 0x CA-36				
Name	Bits	R/W	Reset State	Comments

audio_trans	7	R/W	1	DAC FT reg_tst_sinewave_sel (default is new parameter) 0:old parameter 1:new parameter
PLLTM	6	R/W	0	PLL test mode enable 1: enable 0: disable
FPSD	5	R/W	0	1st phase shift direction 0: upwards 1: downwards
SPSD	4	R/W	0	2nd phase shift direction 0: upwards 1: downwards
NFPSS	3:0	R/W	0	Number of 1st phase shift step

In test mode, PLL shift its phase by 16 steps periodically. The steps which are performed in 1st phase each 16 steps could be assigned by “Number of 1st phase shift step”, remaining steps are performed in 2nd phase.

Register:: HDMI_DPCR0 0x CA-38				
Name	Bits	R/W	Reset State	Comments
DPLLC2	7	R/W	1	DPLLPWDN 0: power up 1: power down
DPLLC1	6	R/W	0	DPLLFREEZE 0: normal 1: freeze
DPLLC0	5:4	R/W	1	DPLLO div 2^(DPLLO)
DPLL_CALBP	3	R/W	0	DPLL bypass calibration(active high)
DPLL_CALSW	2	R/W	0	calibration validated (go high after power on 1200us)
DPLL_CALLCH	1	R/W	0	latch calibration (go high after power on 1100us)
DPLL_CMPEN	0	R/W	0	cmp enable (go high after power on 1000us)

Register:: HDMI_DPCR1 0x CA-39				
Name	Bits	R/W	Reset State	Comments
DPLL_RS	7:5	R/W	3	DPLL Loop Filter Resister Control RS: 000:16K 001:18K 010:20K 011:22K 100: 24K 101: 26K 110:28K 111:30K
DPLL_CS	4:3	R/W	2	DPLL Loop Filter Capacitor Control CS= 00:18p, 01:20p, 10:24p, 11:28p
DPLL_IP	2:0	R/W	2	DPLL Charge Pump Current Control Icp=(2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]) Keep DPM/Icp constant=10.67

Register:: HDMI_DPCR2 0x CA-3A				
Name	Bits	R/W	Reset State	Comments
DPLLSTATUS	7	R	0	DPLLSTATUS(DPLL WD Status) 0:Normal 1:Abnormal Write 1 to clear.(WD enable when Audio PLL power on)
DPLLWDRST	6	R/W	0	DPLLWDRST(DPLL WD Reset) 0:Normal 1:Reset
DPLLWDSET	5	R/W	0	DPLLWDSET(DPLL WD Set) 0:Normal 1:Set

DPLLVCOMD	4:3	R/W	3	DPLL VCO Default mode 00: VCO slowest, 11: VCO fastest
DPLLRESERVE	2	R/W	1	DPLLRESERVE, phase swallow circuit clock select 0: fvco, default is 1 1: fps
DPLLSTOP	1	R/W	1	DPLLSTOP(DPLL Frequency Tuning Enable) 0:Disable 1:Enable
DPLL_CP	0	R/W	0	CP Control 0:CP=1.77pF 1:CP=2.1pF

Register:: HDMI_DPCR3 0x CA-3B				
Name	Bits	R/W	Reset State	Comments
DPLL_VO2	7	R	0	DPLL CAL OUT2
DPLL_VO1	6	R	0	DPLL CAL OUT1
DPLL_CAL	5:4	R	0	DPLL calibrated VCO code
RESERVED	3	R/W	0	Reserved.
DPLLBNP	2	R/W	0	DPLLBNP 0: divider K enable 1: divider K disable(K=1)
DPLL_RESERVED1	1	R/W	0	DPLL_RESERVED1
DPLLVCORSTB	0	R/W	0	RESET VCO (active high)

Register:: HDMI_SUMCM 0x CA-3C				
Name	Bits	R/W	Reset State	Comments
SUMC[15:8]	7:0	R	-	SDM SUMC[15:8]

Register:: HDMI_SUMCL 0x CA-3D				
Name	Bits	R/W	Reset State	Comments
SUMC[7:0]	7:0	R	-	SDM SUMC[7:0]

Packet Acquire Mechanism

Register:: HDMI_AWDSR 0x CA-40				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
AWDPVSB	4:0	R/W	0	Audio watch dog for Packet variation status bit

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, audio output will be disabled/muted.

Register:: HDMI_VWDSR 0x CA-41				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
VWDPVSB	4:0	R/W	0	Video watch dog for Packet variation status bit

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, video output will be disabled.

Register:: HDMI_PAMICR 0x CA-42				
Name	Bits	R/W	Reset State	Comments
Reserved	7:5	---	0	Reserved to 0
ICPVS	4:0	R/W	0	IRQ control for Packet variation status bit

If a bit is assigned to 1 and the corresponding bit of “Global Packet variation status” is 1, issue IRQ signal.

Note: The corresponding bit of “Global Packet variation status” means bit0 maps to bit 0 of “Global Packet variation status ,bit1” maps to bit 1 of “Global Packet variation status”,...etc.

Register:: HDMI_PTRSV1 0x CA-43				
Name	Bits	R/W	Reset State	Comments
PT	7:0	R/W	0	Packet Type of RSV0 packet

Register:: HDMI_PTRSV2 0x CA-44				
Name	Bits	R/W	Reset State	Comments
PT	7:0	R/W	0	Packet Type of RSV1 packet

Register:: HDMI_PVGCR0 0x CA-45				
Name	Bits	R/W	Reset State	Comments
	7	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit7(SC1,SC0)
	6	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit6(PR0 ~ PR6)
	5	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit5(VIC0 ~ VIC6)
	4	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit4(M0,M1)
	3	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit3(C0,C1)
	2	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit2(S0,S1)
	1	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit1(A0,R0,R1,R2,R3)
	0	R/W	1	packet variation status enable: refer to packet table, this byte,correspond to bit0(Y0Y1)

Register:: HDMI_PVGCR1 0x CA-46				
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Name	Bits	R/W	Reset State	Comments
	7	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit18(Copy_Permission, Copy_Number, Quality, & Transaction)
	6	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit17(DVD-audio_type_dependent_generation)
	5	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit16(ACP_Type)
	4	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit15(DM_INH)
	3	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit4(LSV0~LSV3)
	2	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit13(CA0~CA7)
	1	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit12(CC0~CC3)
	0	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit8(B0,B1,Top bar, bottom bar, left bar, right bar change)

Register:: HDMI_PVGCR2 0x CA-47				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	---	0	Reserved
	3	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit22(MF1, MF0)
	2	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit21(FR0)
	1	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit20(MB#3~MB#0)
	0	R/W	1	packet variation status enable: refer to packet table, this byte, correspond to bit19(ISRC_status change)

When the bits of enable “Packet Variation Global Control Register” are set, the corresponding “Packet Variation Status Register” bits will OR to “Packet Variation Global Control Register”.

Register:: HDMI_PVSR0 0x CA-48				
Name	Bits	R/W	Reset State	Comments
	7	R	0	packet variation status : refer to packet table, this byte, correspond to bit7(SC1, SC0)
	6	R	0	packet variation status : refer to packet table, this byte, correspond to bit6(PR0 ~ PR6)
	5	R	0	packet variation status : refer to packet table, this byte, correspond to bit5(VIC0 ~ VIC6)
	4	R	0	packet variation status : refer to packet table, this byte, correspond to bit4(M0, M1)
	3	R	0	packet variation status : refer to packet table, this byte, correspond to bit3(C0, C1)
	2	R	0	packet variation status : refer to packet table, this byte, correspond to bit2(S0, S1)

	1	R	0	packet variation status : refer to packet table, this byte,correspond to bit1(A0,R0,R1,R2,R3)
	0	R	0	packet variation status : refer to packet table, this byte,correspond to bit0(Y0Y1)

Register:: HDMI_PVSR1 0x CA-49				
Name	Bits	R/W	Reset State	Comments
	7	R	0	packet variation status : refer to packet table, this byte,correspond to bit18(Copy_Permission, Copy_Number,Quality,& Transaction)
	6	R	0	packet variation status : refer to packet table, this byte,correspond to bit17(DVD-audio_type_dependent_generation)
	5	R	0	packet variation status : refer to packet table, this byte,correspond to bit16(ACP_Type)
	4	R	0	packet variation status : refer to packet table, this byte,correspond to bit15(DM_INH)
	3	R	0	packet variation status : refer to packet table, this byte,correspond to bit4(LSV0~LSV3)
	2	R	0	packet variation status : refer to packet table, this byte,correspond to bit13(CA0~CA7)
	1	R	0	packet variation status : refer to packet table, this byte,correspond to bit12(CC0~CC3)
	0	R	0	packet variation status : refer to packet table, this byte,correspond to bit8(B0,B1,Top bar, bottom bar, left bar , right bar change)

Register:: HDMI_PVSR2 0x CA-4A				
Name	Bits	R/W	Reset State	Comments
Reserved	7:4	---	0	Reserved
	3	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit22(MF1, MF0)
	2	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit21(FR0)
	1	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit20(MB#3~MB#0)
	0	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit19(ISRC_status change)

HDMI Packet Acquire Mechanism

InfoFrame	Bit	Description
AVI	0	Y0Y1change
	1	A0,R0,R1,R2,R3 change
	2	S0,S1 any bit change
	3	C0,C1 change
	4	M0,M1 change
	5	VIC0 ~ VIC6 change
	6	PR0 ~ PR6 change
	7	SC1,SC0 change
	8	B0,B1,Top bar, bottom bar, left bar , right bar change
	9	EC2~EC0 change
	10	ITC,CN1~CN0 change
	11	Q1,Q0,YQ1,YQ0 change
Audio	12	CC0~CC3 change

	13	CA0~CA7 change
	14	LSV0~LSV3 change
	15	DM_INH any bit change
ACP	16	ACP_Type change
	17	DVD-audio_type_dependent_generation change
	18	Copy_Permission, Copy_Number, Quality, & Transaction change
ISRC1	19	ISRC_status change
MPEG	20	MB#3~MB#0 change
	21	FR0 change
	22	MF1, MF0 change
Vendor Specific	23	HDMI video formate change
	24	HDMI VIC, 3D structure change
Gamut Metadata	25	Affected Gamut Seq Num change
	26	GBD profile change
	27	Next Field change
	28	Current Gamut Seq Num change
	29	Packet Seq change
	30	N0 Cmt GBD change

Table3: HDMI Packet Type

There are 31 bits “Enable flags to global Packet variation”. Each bit is set to watching a standard type of received packet content, and checking if it changed from the previous received packet.

If received packet content changed from previous received one, the relative bit in “local variation flag for detail info.” register will be set, and it will trigger the “global packet variation status” set.

The following table presents the detail of “local variation flag for detail info.”

Register::: HDMI_VCR 0x CA-50				
Name	Bits	R/W	Reset State	Comments
EOI	7	R/W	0	EVEN/ODD Inverse 0: Normal 1: Inverse
EOT	6	R	0	EVEN/ODD Toggle (write 1 clear) 0: Progressive 1: Interlace
SE	5	R	0	EVEN/ODD signal error (write 1 clear) 0: Normal 1: Error
RS	4	R/W	0	The reference signal for executing Info-frame automatically. 0: DEN 1: VSYNC
DSC	3:0	R/W	0	Down sample control (only valid if Video Down Sampling Auto Mode Disable) 0000: pixel down sample for 1 time(no down sample) 0001: pixel down sample for 2 times 0010: pixel down sample for 3 times 0011: pixel down sample for 4 times 0100: pixel down sample for 5 times 0101: pixel down sample for 6 times 0110: pixel down sample for 7 times 0111: pixel down sample for 8 times

				1000: pixel down sample for 9 times 1001: pixel down sample for 10 times others : XXX
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Register:: HDMI_ACRCR 0x CA-51				
Name	Bits	R/W	Reset State	Comments
HDIRQ	7	R/W	0	HDMI/DVI change interrupt enable 0:disable 1:enable
CSAM	6	R/W	1	Color Space Translation 0: Manual 1: Auto
CSC	5:4	R/W	0	Color Space Control (if CSAM=1, CSC will be read-only) 00: RGB 01: YCrCb-422 10: YCrCb-444 11: Reserved
Reserved	3	--	0	Reserved to 0
PRDSAM	2	R/W	1	Pixel Repetition down sampling auto mode 1: auto, the circuit resolve the repeat number, and enable it in next frame. The result could be read in bits for repeat number. 0: manual, F/W sets repeat number, the number is set in bits for repeat number.
PUCNR	1	R/W	0	Pop up CTS&N result 0: No pop up 1: Pop up result (Pop up CTS&N which is acquired completely. If present N&CTS is acquiring, pop up previous complete N&CTS) If the info is updating, HW will refuse this command.
PUCSR	0	R/W	0	Pop up channel status result 0: No pop up 1: Pop up result (Pop up channel status which is acquired completely. If present channel status is acquiring, pop up previous complete channel status)

Register:: HDMI_ACRSR0 0x CA-52				
Name	Bits	R/W	Reset State	Comments
CTS	7:0	R	0	CTS in usage, CTS[19:12]

Register:: HDMI_ACRSR1 0x CA-53				
Name	Bits	R/W	Reset State	Comments
CTS	7:0	R	0	CTS in usage, CTS[11:4]

Register:: HDMI_ACRSR2 0x CA-54				
Name	Bits	R/W	Reset State	Comments
CTS	7:4	R	0	CTS in usage, CTS[3:0]
N	3:0	R	0	N in usage, N[19:16]

Register:: HDMI_ACRSR3 0x CA-55				
Name	Bits	R/W	Reset State	Comments
N	7:0	R	0	N in usage, N[15:8]

Register:: HDMI_ACRSR4 0x CA-56				
Name	Bits	R/W	Reset State	Comments
N	7:0	R	0	N in usage, N[7:0]

Register:: HDMI_ACS0 0x CA-57				
Name	Bits	R/W	Reset State	Comments
CS	7:0	R	0	Channel status bit7~ bit0

Register:: HDMI_ACS1 0x CA-58				
Name	Bits	R/W	Reset State	Comments
CS	7:0	R	0	Channel status bit 15~ bit 8

Register:: HDMI_ACS2 0x CA-59				
Name	Bits	R/W	Reset State	Comments
CS	7:0	R	0	Channel status bit23~ bit 16

Register:: HDMI_ACS3 0x CA-5A				
Name	Bits	R/W	Reset State	Comments
CS	7:0	R	0	Channel status bit 31~ bit 24

Register:: HDMI_ACS4 0x CA-5B				
Name	Bits	R/W	Reset State	Comments
CS	7:0	R	0	Channel status bit 39~ bit 32

Register:: HDMI_INTCR 0x CA-60				
Name	Bits	R/W	Reset State	Comments
PENDING	7	R	0	When IRQ occurred, this bit would be assigned to 1 by HW, and IRQ would be pended until FW clear this bit. (write 1 clear) (to MCU)
AVMUTE	6	R/W	0	If get General control packet and the corresponding Set_AVMUTE flag & Clear_AVMUTE flag is different with previous values 0: IRQ don't occur. 1: IRQ occur.
FIFOD	5	R/W	0	If FIFO depth reach Target (Used for manual audio flow) 0: IRQ don't occur 1: IRQ occur
ACT	4	R/W	0	Audio Coding Type 0: If audio coding type is different with previous value, IRQ doesn't occur. 1: If audio coding type is different with previous value, IRQ occurs.
APLL	3	R/W	0	Audio PLL 0: If audio PLL is non-lock, IRQ doesn't occur 1: If audio PLL is non-lock, IRQ occurs
AFIFO0	2	R/W	0	Audio FIFO Overflow 0: If audio FIFO is overflow for X samples , IRQ doesn't occur. 1: If audio FIFO is overflow for X samples , IRQ occurs.
AFIFOU	1	R/W	0	Audio FIFO Underflow 0: If audio FIFO is underflow for Y samples , IRQ doesn't occur. 1: If audio FIFO is underflow for Y samples , IRQ occurs.
VC	0	R/W	0	1: If video clock is higher than 165Mhz or lower than 25Mhz (refer to NL), IRQ doesn't occur. 0: If video clock is higher than 165Mhz or lower than 25Mhz (refer to NL), IRQ occurs.

Register:: HDMI_ALCR 0x CA-61				
Name	Bits	R/W	Reset State	Comments
LO1	7:6	R/W	0	Speaker location of I2S #1 & SPDIF OUT#1 00: from SubPacket0 of Audio Sample Packet

				01: from SubPacket1 of Audio Sample Packet 10: from SubPacket2 of Audio Sample Packet 11: from SubPacket3 of Audio Sample Packet
LO2	5:4	R/W	1	Speaker location of I2S #2 & SPDIF OUT #2
LO3	3:2	R/W	2	Speaker location of I2S #3 & SPDIF OUT #3
LO4	1:0	R/W	3	Speaker location of I2S #4 & SPDIF OUT #4

Register:: HDMI_AOCR 0x CA-62				
Name	Bits	R/W	Reset State	Comments
SPDIFO1	7	R/W	0	SPDIF 1 Output Switch 0: cutoff 1: normal
SPDIFO2	6	R/W	0	SPDIF 2 Output Switch
SPDIFO3	5	R/W	0	SPDIF 3 Output Switch
SPDIFO4	4	R/W	0	SPDIF 4 Output Switch
I2SO1	3	R/W	0	I2S 1 Output Switch 0: cutoff 1: normal
I2SO2	2	R/W	0	I2S 2 Output Switch
I2SO3	1	R/W	0	I2S 3 Output Switch
I2SO4	0	R/W	0	I2S 4 Output Switch

Register:: HDMI_BCSR 0x CA-70				
Name	Bits	R/W	Reset State	Comments
Reserved	7:6	---	0	Reserved to 0
NVLGB	5	R	0	Video No Leading Guard Band If no leading GB after video preamble (It is only triggered in HDMI mode), this bit would be assigned to 1 until clear this bit Write 1 to clear.
NALGB	4	R	0	Audio No Leading Guard Band If no leading GB after audio preamble (It is only triggered in HDMI mode), this bit would be assigned to 1 until clear this bit Write 1 to clear.
NATGB	3	R	0	Audio No Trailing Guard Band If audio packets without trailing GB, this bit would be assigned to 1 until clear this bit. Write 1 to clear.
NGB	2	R	0	No Guard Band If any type of GB is not synchronous in 3 channels(audio is only 2 channel), this bit would be assigned to 1 until clear this bit. Write 1 to clear.
PE	1	R	0	Packet Error If size of Data Island Packet is not times of 32, this bit would be assigned to 1 until clear this bit. Write 1 to clear.
GCP	0	R	0	General Control Packet error flag: If HW receive General Control Packet with Clear_AVMUTE=1 & Set_AVMUTE=1 ,assign this bit to 1 until clear this bit Write 1 to clear.

Register:: HDMI_ASR0 0x CA-71				
Name	Bits	R/W	Reset State	Comments
Reserved	7:3	---	0	Reserved to 0
FsRE	2	R	0	Fs Regeneration Error If CTS & N received 0, this bit would be assigned to 1 until clear this bit Write 1 to clear.
FsIF	1	R	0	Fs from InfoFrame

				If audio frequency from InfoFrame ready, this bit would be assigned to 1 until clear this bit Write 1 to clear.
FsCS	0	R	0	Fs from Channel Status If audio frequency from Channel Status ready, this bit would be assigned to 1 until clear this bit Write 1 to clear.

Register:: HDMI_ASR1 0x CA-72				
Name	Bits	R/W	Reset State	Comments
Reserved	7	---	0	Reserved
FBIF	6:4	R	0	Frequency bits from info frame 000: refer to channel status bits 001: 32k 010: 44.1k 011: 48k 100: 88.2k 101: 96k 110: 176.4k 111: 192k
FBCS	3:0	R	0	Frequency bits from channel status. (pop up with channel status simultaneously) 0000:44.1k 0010:48k 0011:32k 0100:22.05k 0110:24k 1000:88.2k 1010:96k 1100:176.4k 1110:192k 0001:Sampling frequency not indicated

Register:: TMDS_DPC_SET0 0x CA-80				
Name	Bits	R/W	Reset State	Comments
dpc_en	7	R/W	0	Enable deep color mode
phase_errcnt_in	6:4	R/W	0	Max. times of dpc pll phase error to rise error flag 3'b000 → count 8 times 3'b001~3'b111 → count 1~7 times
phase_clrnt_in	3:1	R/W	0	Max. times of sync. Signal to clear the phase error counter according to “phase_clr_sel” 3'b000 → count 8 times 3'b001~3'b111 → count 1~7 times
phase_clr_sel	0	R/W	0	Unit of “phase_clrnt_in” 0: Use V sync 1: Use H sync

Register:: TMDS_DPC_SET1 0x CA-81				
Name	Bits	R/W	Reset State	Comments
set_full_noti	7:4	R/W	0	Set full notify level (recommend: 3'd7) 3'b000~3'b111 → set 0~7
set_empty_noti	3:0	R/W	0	Set empty notify level (recommend: 3'd3)

			3'b000~3'b111 → set 0~7
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Register:: TMDS_DPC_SET2 0x CA-82				
Name	Bits	R/W	Reset State	Comments
fifo_errcnt_in	7:5	R/W	0	Max. times of FIFO error to rise error flag 3'b000 → count 8 times 3'b001~3'b111 → count 1~7 times
clr_phase_flag	4	R/W	0	Clear phase error flag
clr_fifo_flag	3	R/W	0	Clear FIFO error flag
dpc_phase_ok	2	R	0	Phase locking OK
dpc_phase_err_flag	1	R	0	Become 1 when phase error than “phase_errcnt_in” number
dpc_fifo_err_flag	0	R	0	Become 1 when fifo error than “fifo_errcnt_in” number

Register:: TMDS_DPC_SET3 0x CA-83				
Name	Bits	R/W	Reset State	Comments
dpc_fifo_over_flag	7	R	0	Become 1 when internal FIFO receive writing signal while it is full.
dpc_fifo_under_flag	6	R	0	Become 1 when internal FIFO receive reading signal while it is empty.
dpc_fifo_over_xflag	5	R	0	Become 1 when internal FIFO receive writing signal while it is full. If (fifo_under_xflag=1), this flag is not active.
dpc_fifo_under_xflag	4	R	0	Become 1 when internal FIFO receive reading signal while it is empty. If (fifo_over_xflag=1), this flag is not active.
Reserved	3:0	--	0	reserved

TMDS Decoding Error Detection

Register:: TMDS_DET_0 0xCA-84				
Name	Bits	R/W	Reset State	Comments
Reserved	7	---		Reserved
DE_SEL	6	R/W	0	Source of DE Selection 0: Choose DE from Post Stage (After LPF) 1: Choose DE from Pre-Stage
POS_DE_LOWBD	5:0	R/W	36	DE =1 Low Bound Setting Setting Positive DE Period Low Bound Value 0~63

Register:: TMDS_DET_1 0xCA-85				
Name	Bits	R/W	Reset State	Comments
NEG_DE_LOWBD	7:1	R/W	12	DE =0 Low Bound Setting Setting Negative DE Period Low Bound Value 0~127
RED_TRAN_ERR_FLAG	0	R	0	RED Channel Transition Error Flag (write 1 clear) 0: Means No Transition Error Occurs at Red Channel 1: Means Transition Error occurs

Register:: TMDS_DET_2 0xCA-86				
Name	Bits	R/W	Reset State	Comments
GRN_TRAN_ERR_FLAG	7	R	0	Green Channel Transition Error Flag (write 1 clear) 0: Means No Transition Error Occurs at Green Channel

				1: Means Transition Error occurs
BLU_TRAN_ERR_FLAG	6	R	0	Blue Channel Transition Error Flag (write 1 clear) 0: Means No Transition Error Occurs at Blue Channel 1: Means Transition Error occurs
RED_POS_DE_ERR_FLAG	5	R	0	Red Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Red Channel 1: Means DE Period is Invalid under Red Channel
GRN_POS_DE_ERR_FLAG	4	R	0	Green Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Green Channel 1: Means DE Period is Invalid under Green Channel
BLU_POS_DE_ERR_FLAG	3	R	0	Blue Channel Positive DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Blue Channel 1: Means DE Period is Invalid under Blue Channel
RED_NEG_DE_ERR_FLAG	2	R	0	Red Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Red Channel 1: Means DE Period is Invalid under Red Channel
GRN_NEG_DE_ERR_FLAG	1	R	0	Green Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Green Channel 1: Means DE Period is Invalid under Green Channel
BLU_NEG_DE_ERR_FLAG	0	R	0	Blue Channel Negative DE Period Measurement Flag (write 1 clear) 0: Means DE Period is Valid under Blue Channel 1: Means DE Period is Invalid under Blue Channel

Register:: TMDS_DET_3					0xCA-87
Name	Bits	R/W	Reset State	Comments	
TRAN_ERR_THRD	7:4	R/W	0	Transition Error Count Threshold Value Setting 0-15 0-14 Zero value means at least one error	
POS_DE_ERR_THRD	3:0	R/W	0	Positive DE Error Count Threshold Value Setting 0-15 0-14 Zero value means at least one error	

Register:: TMDS_DET_4					0xCA-88
Name	Bits	R/W	Reset State	Comments	
Rev	7:4	---		Reserved	
NEG_DE_ERR_THRD	3:0	R/W	0	Negative DE Error Count Threshold Value Setting 0-15 0-14 Zero value means at least one error	

Register:: AUDIO_FREQDET					0xCA-90
Name	Bits	R/W	Reset State	Comments	
AUDIO_FREQ_DETECT	7	R/W	0	Enable the detection of the audio sampling rate.	
AUTO_LOAD_SCODE	6	R/W	0	Auto load s-code.	
AWD_BY_FREQCHANGE	5	R/W	0	Audio watch dog triggered by audio sampling rate changed.	
AWD_BY_NOAUDIO	4	R/W	0	Audio watch dog triggered by no_audio_in.	
IRQ_BY_FREQCHANGE	3	R/W	0	IRQ triggered by audio sampling rate changed.	
IRQ_BY_NOAUDIO	2	R/W	0	IRQ triggered by no_audio_in.	
FREQCHANGE	1	R	0	Audio sampling rate changed, including change to no audio(Write 1 to clear)	
NOAUDIO	0	R	0	No any audio packet transmitted. Need 2ms for measurement to be asserted (Write 1 to clear)	

By measuring the number of received audio packets within 1ms (xtal clock divided by “32*XTAL_DIV”) to determine the audio sampling rate. The measured result should be the same for 2 times (2ms) for

sampling rate determination.

Register:: AUDIO_FREQDET_RESULT_M					0x CA-91
Name	Bits	R/W	Reset State	Comments	
AFREQ_MEAS_RANGE	7:5	R	0	Automatic detection of audio sampling rate. 3'b000: Range 0 (Default for no_audio) 3'b001: Range 1 (Default for 32kHz) 3'b010: Range 2 (Default for 44.1kHz & 48kHz) 3'b011: Range 3 (Default for 88.2kHz & 96kHz) 3'b100: Range 4 (Default for 176.4kHz & 192kHz) 3'b101: Range 5 (For future extention) Other: Not used.	
POPUP_AFREQ_MEAS_RESULT	4	R/W	0	Pop-up the current number of audio packets in 1ms	
AFREQ_MEAS_RESULT[11:8]	3:0	R	0	The number of audio packets in 1ms	

Register:: AUDIO_FREQDET_RESULT_L					0x CA-92
Name	Bits	R/W	Reset State	Comments	
AFREQ_MEAS_RESULT[7:0]	7:0	R	0	The number of audio packets in 1ms	

Register:: XTAL_DIV					0x CA-93
Name	Bits	R/W	Reset State	Comments	
XTAL_DIV	7:0	R/W	0x98	Select the most proper divider that the output clock will approximate 5kHz: Eq: Fx/32/Xtal_div ~= 5kHz For example: 14.318MHz: Xtal_div = 89 24.000MHz: Xtal_div = 150 24.300MHz: Xtal_div = 152 24.576MHz: Xtal_div = 154 27.000MHz: Xtal_div = 169	

Register:: RANGE0_M					0x CA-94
Name	Bits	R/W	Reset State	Comments	
RANGE0_TH[11:8]	7:4	R/W	0	The number of audio packets in 1ms less than RANGE0_TH or larger than RANGE5_TH will be regarded as Range0	
RANGE1_TH[11:8]	3:0	R/W	0	The number of audio packets in 1ms larger than RANGE0_TH and less than RANGE1_TH will be regarded as Range1	

Register:: RANGE0_L					0x CA-95
Name	Bits	R/W	Reset State	Comments	
RANGE0_TH[7:0]	7:0	R/W	0x10	The number of audio packets in 1ms less than RANGE0_TH or larger than RANGE5_TH will be regarded as Range0	

Register:: RANGE1_L					0x CA-96
Name	Bits	R/W	Reset State	Comments	
RANGE1_TH[7:0]	7:0	R/W	0x26	The number of audio packets in 1ms larger than RANGE0_TH and less than RANGE1_TH will be regarded as Range1	

Register:: RANGE2_M					0x CA-97
Name	Bits	R/W	Reset State	Comments	

RANGE2_TH[11:8]	7:4	R/W	0	The number of audio packets in 1ms larger than RANGE1_TH and less than RANGE2_TH will be regarded as Range2
RANGE3_TH[11:8]	3:0	R/W	0	The number of audio packets in 1ms larger than RANGE2_TH and less than RANGE3_TH will be regarded as Range3

Register:: RANGE2_L					0x CA-98
Name	Bits	R/W	Reset State	Comments	
RANGE2_TH[7:0]	7:0	R/W	0x44	The number of audio packets in 1ms larger than RANGE1_TH and less than RANGE2_TH will be regarded as Range2	

Register:: RANGE3_L					0x CA-99
Name	Bits	R/W	Reset State	Comments	
RANGE3_TH[7:0]	7:0	R/W	0x88	The number of audio packets in 1ms larger than RANGE2_TH and less than RANGE3_TH will be regarded as Range3	

Register:: RANGE4_M					0x CA-9A
Name	Bits	R/W	Reset State	Comments	
RANGE4_TH[11:8]	7:4	R/W	0	The number of audio packets in 1ms larger than RANGE3_TH and less than RANGE4_TH will be regarded as Range4	
RANGE5_TH[11:8]	3:0	R/W	0x1	The number of audio packets in 1ms larger than RANGE4_TH and less than RANGE5_TH will be regarded as Range5	

Register:: RANGE4_L					0x CA-9B
Name	Bits	R/W	Reset State	Comments	
RANGE4_TH[7:0]	7:0	R/W	0xF0	The number of audio packets in 1ms larger than RANGE3_TH and less than RANGE4_TH will be regarded as Range4	

Register:: RANGE5_L					0x CA-9C
Name	Bits	R/W	Reset State	Comments	
RANGE5_TH[7:0]	7:0	R/W	0xA4	The number of audio packets in 1ms larger than RANGE4_TH and less than RANGE5_TH will be regarded as Range5	

Register:: PRESET_S_CODE0					0x CA-9D
Name	Bits	R/W	Reset State	Comments	
PRE_SET_S1_CODE0	7	R/W	0	Once the determination of audio sampling rate is Range 0, the S1 code will be automatically replaced by this value.	
PRE_SET_S_CODE0	6:0	R/W	0x06	Once the determination of audio sampling rate is Range 0, the S code will be automatically replaced by this value.	

Register:: PRESET_S_CODE1					0x CA-9E
Name	Bits	R/W	Reset State	Comments	
PRE_SET_S1_CODE1	7	R/W	0	Once the determination of audio sampling rate is Range 1, the S1 code will be automatically replaced by this value.	
PRE_SET_S_CODE1	6:0	R/W	0x04	Once the determination of audio sampling rate is Range 1, the S code will be automatically replaced by this value.	

Register:: PRESET_S_CODE2					0x CA-9F
Name	Bits	R/W	Reset	Comments	

			State	
PRE_SET_S1_CODE2	7	R/W	0	Once the determination of audio sampling rate is Range 2, the S1 code will be automatically replaced by this value.
PRE_SET_S_CODE2	6:0	R/W	0x02	Once the determination of audio sampling rate is Range 2, the S code will be automatically replaced by this value.

Register:: PRESET_S_CODE3 0x CA-A0				
Name	Bits	R/W	Reset State	Comments
PRE_SET_S1_CODE3	7	R/W	0	Once the determination of audio sampling rate is Range 3, the S1 code will be automatically replaced by this value.
PRE_SET_S_CODE3	6:0	R/W	0x01	Once the determination of audio sampling rate is Range 3, the S code will be automatically replaced by this value.

Register:: PRESET_S_CODE4 0x CA-A1				
Name	Bits	R/W	Reset State	Comments
PRE_SET_S1_CODE4	7	R/W	0	Once the determination of audio sampling rate is Range 4, the S1 code will be automatically replaced by this value.
PRE_SET_S_CODE4	6:0	R/W	0x00	Once the determination of audio sampling rate is Range 4, the S code will be automatically replaced by this value.

Register:: PRESET_S2_CODE 0x CA-A2				
Name	Bits	R/W	Reset State	Comments
PRE_SET_SM_CODE0	7	R/W	1	Once the determination of audio sampling rate is Range 0, the S1_MSB code will be automatically replaced by this value.
PRE_SET_SM_CODE1	6	R/W	1	Once the determination of audio sampling rate is Range 1, the S1_MSB code will be automatically replaced by this value.
PRE_SET_SM_CODE2	5	R/W	1	Once the determination of audio sampling rate is Range 2, the S1_MSB code will be automatically replaced by this value.
PRE_SET_SM_CODE3	4	R/W	1	Once the determination of audio sampling rate is Range 3, the S1_MSB code will be automatically replaced by this value.
PRE_SET_SM_CODE4	3	R/W	1	Once the determination of audio sampling rate is Range 4, the S1_MSB code will be automatically replaced by this value.
NOAUDI_O_FSM	2	R/W	0	Audio FSM rerun when no audio enable 0: old mode: no volume adjust 1: new mode: volume adjust)
Audio_double_buffer	1	R	0	Read double buffer apply(Write 1 clear)
Auto_Manual_gain	0	R	0	Select gain by Auto or Manual 0:auto gain 1:manual gain

Register:: AFSM_MOD 0x CA-A3				
Name	Bits	R/W	Reset State	Comments
DP_ABUF_WR_MOD_EN	7	R/W	1	Before HW confirms there has been any audio-input, HW stops the dp-abuf write process.
AUTO_STOP_TRK_EN	6	R/W	1	HW automatically pause the FIFO tracking process right after no audio has been detected.
TRK_MOD_EN	5	R/W	1	FIFO tracking (trend & boundary) is activated only when Audio FSM is within normal state.

AFSM_MOD_EN	4	R/W	1	As long as no audio has been detected, HW automatically turn down the audio volume gradually.
HDMI_AUDIO_RESET	3	R/W	0	HDMI Audio Reset: Use FW reset HDMI audio related module: afifo_ctrl、audio_freqdet、audio_fsm、audio_trans、bch.
AFREQ_RESERVED1	2:0	R/W	0	Reserved.

HDMI Reserver Packet Type Register 2

Register:: HDMI_PTRSV_2 0x CA-A4				
Name	Bits	R/W	Reset State	Comments
packet_port2	7:0	R/W	0	Packet Type of RSV2 packet

HDMI Reserver Packet Type Register 3

Register:: HDMI_PTRSV_3 0x CA-A5				
Name	Bits	R/W	Reset State	Comments
packet_port3	7:0	R/W	0	Packet Type of RSV3 packet

DMI Reserver Packet Reserved Register

Register:: HDMI_PTRSV_3 0x CA-A6				
Name	Bits	R/W	Reset State	Comments
hdmi_parsv_rsv	7:0	R/W	0	Reserved

Register:: HDMI_GPVS_0 0x CA-A7				
Name	Bits	R/W	Reset State	Comments
new_pck_gmps_ocr_keep	7	R	0	Gamut Metadata Packet Status (Write 1 Clear)
new_pck_vsps_ocr_keep	6	R	0	Vendor Specific Packet Status (Write 1 Clear)
chg_pck_vsps_ocr	5	R	0	Packet Variation Status: Vendor Specific Packet
chg_pck_gmps_ocr	4	R	0	Packet Variation Status: Gamut Metadata Packet
Reserved	3:0	---	---	Reserved

The following is to read packet variation status.

Packet change flag is cleared as follows: ref.0xCC[4:0]

- (1) AVI packet change variation flag is clear by 0xCC[0]
- (2) AUD packet change variation flag is clear by 0xCC[1]
- (3) ACP packet change variation flag is clear by 0xCC[2]
- (4) ISRC1 packet change variation flag is clear by 0xCC[3]
- (5) MPG packet change variation flag is clear by 0xCC[4]

Register:: HDMI_PVSR_3 0x CA-A8				
Name	Bits	R/W	Reset State	Comments
chg_avi_enc	7	R	0	packet variation status: refer to packet table, this byte, correspond to bit9(ENC2~ENC0)
chg_avi_itc	6	R	0	packet variation status: refer to packet table, this byte, correspond to bit10(ITC,CN1~CN0)
chg_avi_q	5	R	0	packet variation status: refer to packet table, this byte, correspond to bit11(Q1,Q0,YQ1,YQ0)
chg_vsc_video	4	R	0	packet variation status: refer to packet table, this byte, correspond to bit23(HDMI video formate)
chg_vsc_vic	3	R	0	packet variation status: refer to packet table, this byte, correspond to bit24(HDMI VIC,3D structure)
chg_gmt_gmt	2	R	0	packet variation status: refer to packet table, this byte, correspond to

				bit25(Affected Gamut Seq Num)
chg_gmt_gbd	1	R	0	packet variation status: refer to packet table, this byte,correspond to bit26(GBD profile)
chg_gmt_nextf	0	R	0	packet variation status: refer to packet table, this byte,correspond to bit27(Next Field)

Register:: HDMI_PVSR_4					0x CA-A9
Name	Bits	R/W	Reset State	Comments	
chg_gmt_cgsn	7	R	0	packet variation status: refer to packet table, this byte,correspond to bit28(Current Gamut Seq Num)	
chg_gmt_psc	6	R	0	packet variation status: refer to packet table, this byte,correspond to bit29(Packet Seq)	
Chg_gmt_nocmt	5	R	0	packet variation status: refer to packet table, this byte,correspond to bit30(N0 Cmt GBD)	
Reserved	4:0	R	0	Reserved	

HDMI_PVGCR3					0x CA-AA
Name	Bits	R/W	Reset State	Comments	
chg_avi_enc_en	7	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit9(ENC2~ENC0)	
chg_avi_itc_en	6	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit10(ITC,CN1~CN0)	
chg_avi_q_en	5	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit11(Q1,Q0,YQ1,YQ0)	
chg_vsc_video_en	4	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit23(HDMI video formate)	
chg_vsc_vic_en	3	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit24(HDMI VIC,3D structure)	
chg_gmt_gmt_en	2	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit25(Affected Gamut Seq Num)	
chg_gmt_gbd_en	1	R	0	packet variation status enable :refer to packet table, this byte,correspond to bit26(GBD profile)	
chg_gmt_nextf_en	0	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit27(Next Field)	

HDMI_PVGCR4					0x CA-AB
Name	Bits	R/W	Reset State	Comments	
chg_gmt_cgsn	7	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit28(Current Gamut Seq Num)	
chg_gmt_psc	6	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit29(Packet Seq)	
Chg_gmt_nocmt	5	R	0	packet variation status enable: refer to packet table, this byte,correspond to bit30(N0 Cmt GBD)	
Reserved	4:0	R	0	Reserved	

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AUX Power Saving Mode (Page 2)

Register:: AUX_PS_CTRL 0xE0					
Name	Bits	R/W	Default	Comments	Config
Aux_ps_en	7	R/W	0	Used in power saving mode 1:enable aux detection 0:disable aux detection	
Auxps_clksel	6:5	R/W	0	Aux clk select 00: 27M 01: 26M 10: 24.576M 11: 14.318M	
Auxps_int_en	4	R/W	0	Aux power saving interrupt enable	
Auxps_int_st	3:1	R/W	3	Auxps_int flag is trigger by encounter what state 001:sync0 state 010:sync1 state 011:data state 100:end state 101:precharge state	
Auxps_int	0	R	0	Auxps interrupt flag	Wclr_out

Register:: AUX_PS_REPLY 0xE1					
Name	Bits	R/W	Default	Comments	Config
Aux_ctrl_fpga	7	R/W	0	AUX handshake by FPGA	
Aux_ps_en_ctrl	6	R/W	0	0: E0[7] is double buffered by H/W 1: E0[7] is not double buffered	
Xtal_sel4gdi	5	R/W	1	1: from m2pll 0 : from xtal	
Auxps_reply_en	4	R/W	0	Aux power saving reply enable 1: reply cmd refer to E1[3:0]	
Auxps_reply_cmd	3:0	R/W	2	Active when bit4 = 1 0000 : aux ack/i2c ack 0001 : aux_nack 0010 : aux defer 0100 : i2c nack 1000 : i2c defer	

Register:: AUX_PS_DUMMY1 0xE2					
Name	Bits	R/W	Default	Comments	Config
Auxps_dummy1	7:3	R/W	0x1E	Reserved	
PS_ERROR_HANDLE_EN	2	R/W	0	1:if receiving error , no reply any command 0:whether receiving errors, reply command.	
PS_AUTO_RESET_EN	1	R/W	0	1: when receive aux signal, auto reset F1[1], F2[7], F3[7:6] 0: origin mode	
Single-ended	0	R/W	0	1: single ended mode (aux_d2 = ~aux_d1) 0: origin	

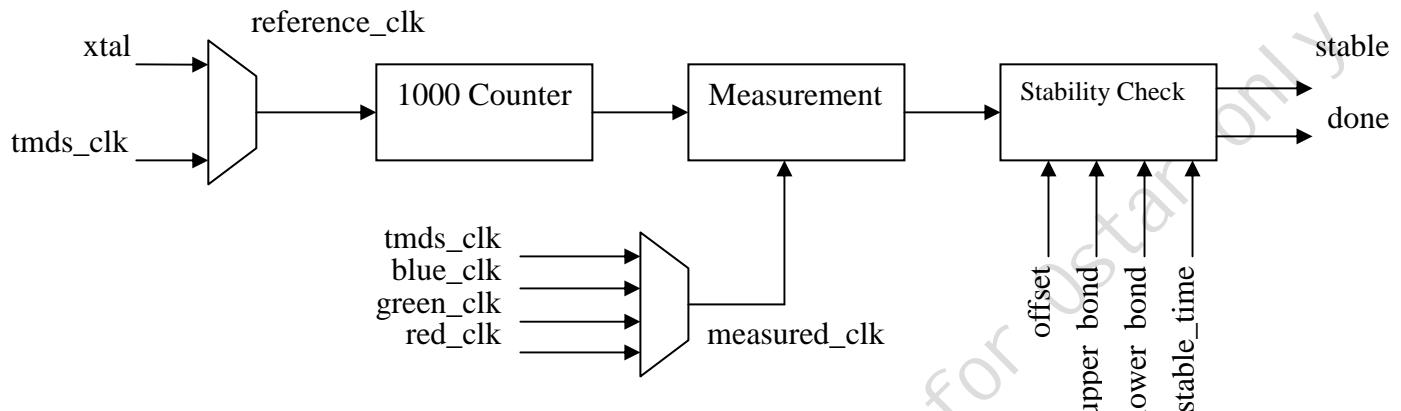
Register:: AUX_PS_DUMMY2 0xE3					
Name	Bits	R/W	Default	Comments	Config
Auxps_timeout_tgt	7:4	R/W	0	aux power saving mode timeout target Timeout = XCLK_period * {timeout_tgt,9'h1FF}	
Auxps_rd_dummy	3:0	R		Read only reserved	

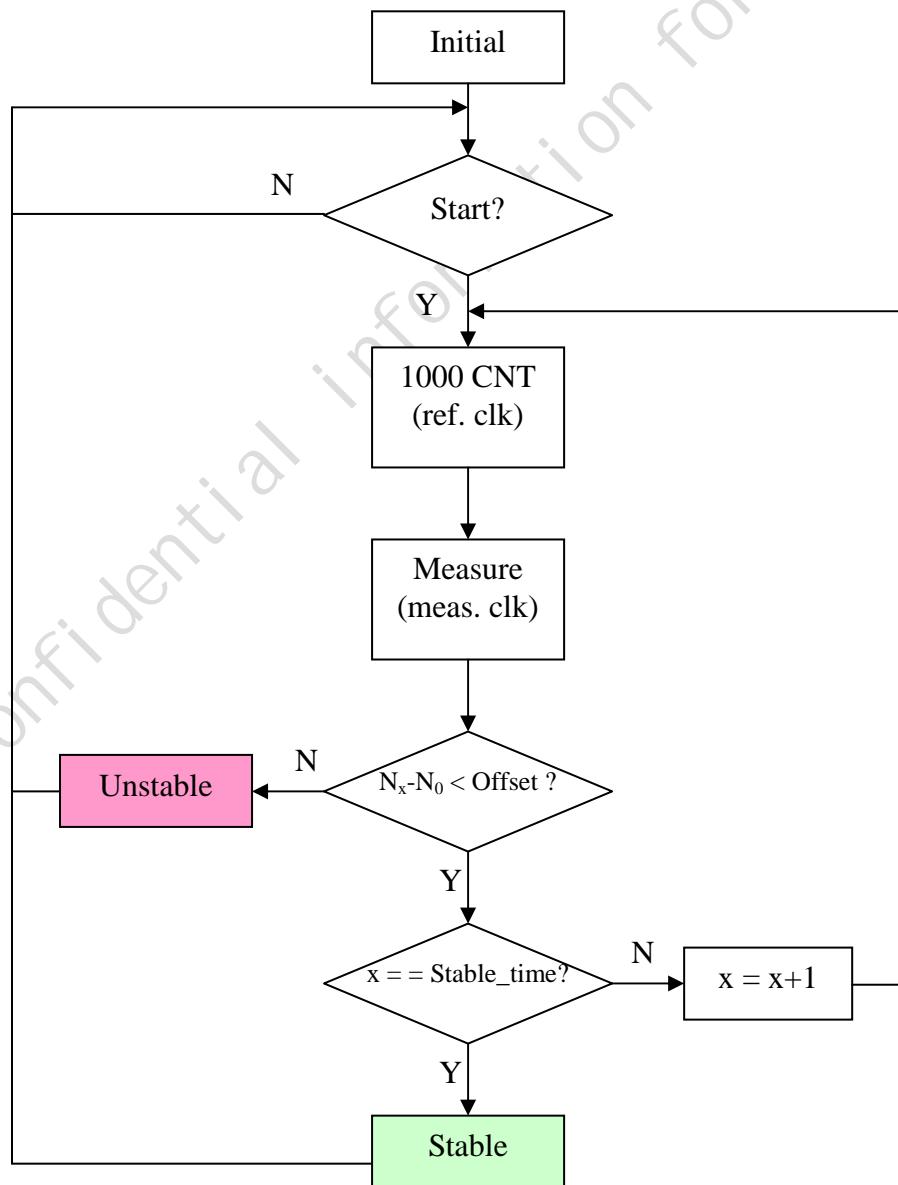
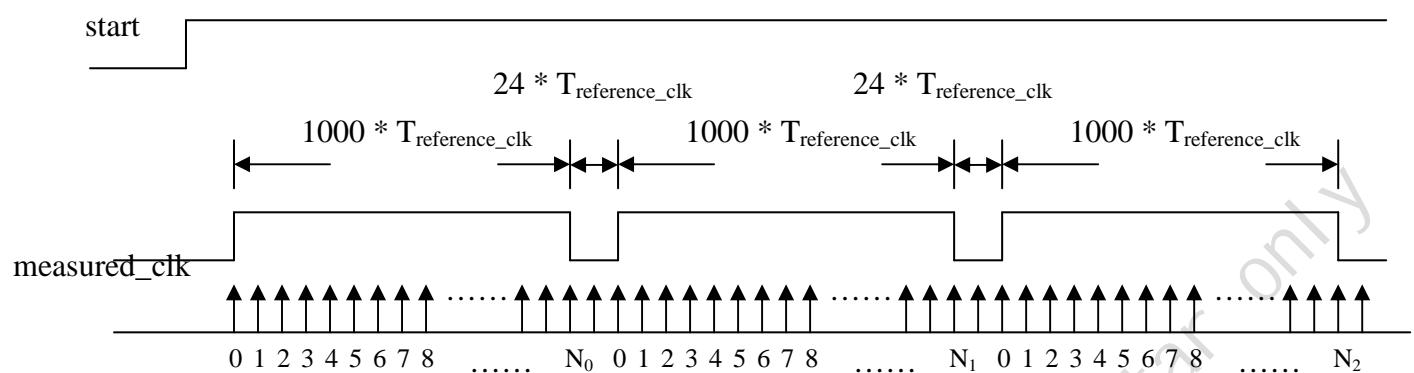
Register:: AUX_PS_RX_SIGNAL1 0xE4					
Name	Bits	R/W	Default	Comments	Config
Rx_cmd	7:4	R	0	Aux Rx. command	
Rx_data	3:0	R	0	Receive first data [3:0]	

Register:: AUX_PS_RX_SIGNAL2 0xE5					
Name	Bits	R/W	Default	Comments	Config
Rx_addr[7:4]	7:4	R	0	Receive 20 bits address[15:8]	
Rx_addr[3:0]	3:0	R	0	Receive 20 bits address[3:0]	

Power-Saving Mode Domain Input Video clock frequency detection

Frequency detection formula: $1000 \times T_{ref_clk} = counter \times T_{measure_clk}$





Register:: HDMI_FREQDET_CTRL 0xE6					
Name	Bit	R/W	Default	Description	Config
FREQDET_START	7	R/W	0	Start the frequency detection process. Once the bit has been set, this process won't stop until disabling this bit. 0: Disabled 1: Started	
FREQDET_DONE	6	R	0	The first frequency detection process has done. 0: Not done yet. 1: Done.	
FREQ_SOURCE	5:4	R/W	0	Choose which clock to be measured. 00: TMDS clock. 01: Blue channel clock. 10: Green channel clock. 11: Red channel clock.	
FREQ_REFERENCE	3	R/W	0	Choose which clock as reference clock. 0: Xtal clock. 1: TMDS clock.	
FREQ_UNSTABLE	2	R	0	The freq status has been unstable. (Write 1 to clear) 0: Disabled 1: Enabled	
IRQ_FREQ_UNSTABLE	1	R/W	0	Interrupt as long as the freq is unstable. 0: Disabled 1: Enabled	
VWD_FREQ_UNSTABLE	0	R/W	0	Trigger video watch-dog as long as the freq is unstable. 0: Disabled 1: Enabled	WportRport

Register:: HDMI_FREQDET_OFFSET 0xE7					
Name	Bit	R/W	Default	Description	Config
MEAS_CLK_SEL	7	R/W	0	The selection of measure clk 0: determined by 0xE6[5:4] 1: determined by hdmi_cp_clk	
FREQDET_OFFSET	6:0	R/W	2	Determine the pre-set threshold, within which means the frequency is still stable. 0: No variation is allowed. 1: $\pm F_x / 1000$ 2: $\pm 2^* F_x / 1000$ 3: $\pm 3^* F_x / 1000$... 127: $\pm 127^* F_x / 1000$, where F_x is frequency of xtal clock.	

Register:: HDMI_FREQDET_UPPER_M 0xE8					
Name	Bit	R/W	Default	Description	Config
UPPER_BOUND[15:8]	7:0	R/W	2D	Once the frequency counter exceeds this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_UPPER_L 0xE9					
Name	Bit	R/W	Default	Description	Config
UPPER_BOUND[7:0]	7:0	R/W	ED	Once the frequency counter exceeds this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_LOWER_M 0xEA					
Name	Bit	R/W	Default	Description	Config
LOWER_BOUND[15:8]	7:0	R/W	2	Once the frequency counter is smaller than this value, then it will be treated as unstable.	

Register:: HDMI_FREQDET_LOWER_L 0xEB					
Name	Bit	R/W	Default	Description	Config

LOWER_BOUND[7:0]	7:0	R/W	F6	Once the frequency counter is smaller than this value, then it will be treated as unstable.	
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Register:: HDMI_FREQDET_STABLE					0xEC
Name	Bit	R/W	Default	Description	Config
RESULT_POPUP	7	W	0	POP UP the counter value in HW The result will be shown in 0xED[7], 0xED[6:0], 0xEE[7:0]	Wclr_out
STABLE_TIME	6:0	R/W	A	Determine how much times that freq needs to be within the pre-set threshold then the freq can be regarded as stable. 0: 1 time. 1: 2 time. 2: 3 times. ... 127: 128 times.	

Register:: HDMI_FREQDET_RESULT_M					0xED
Name	Bit	R/W	Default	Description	Config
NO_CLOCK	7	R	0	No input clock	
FREQDET_RESULT [14:8]	6:0	R		The result of frequency counter (bit 15 is in 0xEF[5])	

Register:: HDMI_FREQDET_RESULT_L					0xEE
Name	Bit	R/W	Default	Description	Config
FREQDET_RESULT [7:0]	7:0	R		The result of frequency counter	

Register:: HDMI_ERROR_TH					0xEF
Name	Bit	R/W	Default	Description	Config
FREQ_STABLE_IRQ_EN	7	R/W	0	Interrupt as long as the freq is stable. 0: Disabled 1: Enabled	
FREQ_STABLE	6	R	0	Determine if clock frequency is stable in measure process. 0: Not stable yet 1: Stable at least once. (write 1 clear)	write 1 clear
FREQDET_RESULT [15]	5	R/W	0	The result of frequency counter	
FREQ_ERROR_TH	4:0	R/W	0	Error Count Upper Limit When accumulated error below this value, frequency unstable will not occur. 0: means 1 error 1: means 2 errors 31: means 32 errors.	

LiveShow™ Control (Page 3)

Register::: LS_CTRL0					0xA1	
Name	Bits	Read/Write	Reset State	Comments	Config	
LS_BYPASS	7	R/W	0	LiveShow™ Enable 0: Bypass LiveShow™ Processing 1: Enable LiveShow™ Processing		
LS_BUF_EN	6	R/W	0	Enable SDRAM Buffer Access 0: Disable 1: Enable		
LS_PD_EST	5	R/W	0	Level Estimation 0: Disable 1: Enable		
Reserved	4	R/W	0	Reserved		
LS_GAIN_EN	3	R/W	0	Delta Gain Adjustment 0: Disable (Delta Gain=1) 1: Enable Delta Gain only take effect when LS_BYPOS_EN (0xB5[7]) = 1'b0		
Reserved	2	R/W	0	Reserved		

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SOURCE_RES	1:0	R/W	0	<p>Source Pixel Resolution (previous round) 00: 8bit 01: 6bit 10: 5bit 11: 4bit (Pixel Resolution after rounding in previous path. Pixel Resolution for Compression.) Note: Rounding precision of compressed color values in previous frame path when pixels are represented in RGB formats, or Y value in YUV format. Compressed UV values are of precision the same as Y value or 2 bit less depending on the setting of bit 4 in Register LS_FRAME2. The raw data size per pixel in the compressed frame is determined by this bit along with the compression method and UV round mode, as illustrated in the following table.</p> <table border="1"> <thead> <tr> <th>Source_res</th><th>8</th><th>6</th><th>5</th><th>4</th></tr> </thead> <tbody> <tr> <td>Compression format</td><td></td><td></td><td></td><td></td></tr> <tr> <td>rgb/yuv</td><td>24</td><td>18</td><td>15</td><td>12</td></tr> <tr> <td>yuv444 (uv_round)</td><td>20</td><td>14</td><td>11</td><td>8</td></tr> <tr> <td>yuv422</td><td>16</td><td>12</td><td>10</td><td>8</td></tr> <tr> <td>yuv422 (uv_round)</td><td>14</td><td>10</td><td>8</td><td>6</td></tr> <tr> <td>Super-pixel 1x2 / 1x3</td><td>12</td><td>9</td><td>7.5</td><td>6</td></tr> <tr> <td>yuv411</td><td>12</td><td>9</td><td>7.5</td><td>6</td></tr> <tr> <td>yuv411 (uv_round)</td><td>11</td><td>8</td><td>6.5</td><td>5</td></tr> <tr> <td>Super-pixel 1x4</td><td>6</td><td>4.5</td><td>3.75</td><td>3</td></tr> </tbody> </table>	Source_res	8	6	5	4	Compression format					rgb/yuv	24	18	15	12	yuv444 (uv_round)	20	14	11	8	yuv422	16	12	10	8	yuv422 (uv_round)	14	10	8	6	Super-pixel 1x2 / 1x3	12	9	7.5	6	yuv411	12	9	7.5	6	yuv411 (uv_round)	11	8	6.5	5	Super-pixel 1x4	6	4.5	3.75	3
Source_res	8	6	5	4																																																		
Compression format																																																						
rgb/yuv	24	18	15	12																																																		
yuv444 (uv_round)	20	14	11	8																																																		
yuv422	16	12	10	8																																																		
yuv422 (uv_round)	14	10	8	6																																																		
Super-pixel 1x2 / 1x3	12	9	7.5	6																																																		
yuv411	12	9	7.5	6																																																		
yuv411 (uv_round)	11	8	6.5	5																																																		
Super-pixel 1x4	6	4.5	3.75	3																																																		

Register:: LS_CTRL1					0xA2
Name	Bits	Read/Write	Reset State	Comments	Config
LS_IN_WIN	7	R/W	0	LiveShow™ Inside Highlight Window 0: Disable 1: Enable	
LS_OUT_WIN	6	R/W	0	LiveShow™ Outside Highlight Window 0: Disable 1: Enable	
LS_NR_THD_OFFSET	5	R/W	0	Low-Bit Noise Reduction Threshold Offset 0: Low-Bit Noise Reduction Threshold 1: Low-Bit Noise Reduction Threshold + 8	

LS_NR_EN	4	R/W	0	Low-Bit Noise Reduction 0: Disable 1: Enable	
LS_NR_MD	3	R/W	0	Low-Bit Noise Reduction Mode 0: RGB Independent Mode (Old mode: RTD2363-like) 1: RGB Related Mode (New Mode)	
LS_NR THD	2:0	R/W	0	Low-Bit Noise Reduction Threshold 000`b: 1 001`b: 2 010`b: 3 011`b: 4 100`b: 5 101`b: 6 110`b: 7 111`b: 8	

Register:: DELTA_GAIN					0xA3
Name	Bits	Read/Write	Reset State	Comments	Config
DELTA_GAIN	7:0	R/W	0	Delta Gain Setting : 0x00 → Gain = 0 0x40 → Gain = 1 0xFF → Gain = 255/64 (Effective only when LS_GAIN_EN=1)	

FIFO Setting (to be modified)

Register:: LS_STATUS0					0xA4
Name	Bits	Read/Write	Reset State	Comments	Config
LS_RBUF_FULL	7	R	0	Set if BUF_R is full (On-line monitor)	
LS_RBUF_EPTY	6	R	0	Set if BUF_R is empty (On-line monitor)	
LS_RBUF_UDFW	5	R	0	Set if BUF_R is underflow	
LS_WBUF_FULL	4	R	0	Set if BUF_W is full (On-line monitor)	
LS_WBUF_EPTY	3	R	0	Set if BUF_W is empty (On-line monitor)	
LS_WBUF_OVFW	2	R	0	Set if BUF_W is overflow	
Reserved	1	--	0	Reserved	
LS_STATUS0_RST	0	R/W	0	Write 1 to reset BUF and FIFO status (Auto clear after done)	

Register:: LS_STATUS1					0xA5
Name	Bits	Read/Write	Reset State	Comments	Config
LS_RFIFO_FULL	7	R	0	Set if FIFO_R is full (On-line monitor)	
LS_RFIFO_EPTY	6	R	0	Set if FIFO_R is empty (On-line monitor)	
LS_RFIFO_OVFW	5	R	0	Set if FIFO_R is overflow before LS_RFIFO_UDFW is set	
LS_RFIFO_UDFW	4	R	0	Set if FIFO_R is underflow before LS_RFIFO_OVFW is set	
LS_WFIFO_FULL	3	R	0	Set if FIFO_W is full (On-line monitor)	
LS_WFIFO_EPTY	2	R	0	Set if FIFO_W is empty (On-line monitor)	
LS_WFIFO_OVFW	1	R	0	Set if FIFO_W is overflow before LS_WFIFO_UDFW is set	
LS_WFIFO_UDFW	0	R	0	Set if FIFO_W is underflow before LS_WFIFO_OVFW is set	

Register:: LS_WTLVL_W					0xA6
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
LS_WTLVL_W	6:0	R/W	0x40	When FIFO depth is over WTLVL, FIFO write data ((NUM*LEN)+REM) * 64 = one frame/line data	

The assigned value multiplied by 2 is the real value.

Register:: LS_WTLVL_R
0xA7

Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
LS_WTLVL_R	6:0	R/W	0x40	When FIFO depth is over WTLVL, FIFO request data ((NUM*LEN)+REM) * 64 = one frame/line data The assigned value multiplied by 2 is the real value.	

Register:: LS_MEM_FIFO_RW_NUM_H
0xA8

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MFRW_NO_H	7:0	R/W	0x01	LS_MEM_FIFO_RW_NUM [15:8] The Read/Write times of total memory access.	

Register:: LS_MEM_FIFO_RW_NUM_L
0xA9

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MFRW_NO_L	7:0	R/W	0x00	LS_MEM_FIFO_RW_NUM [7:0] The Read/Write times of total memory access.	

Register:: LS_MEM_FIFO_RW_LEN
0xAA

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MFRW_LEN	7:0	R/W	0x80	LS_MEM_FIFO_RW_LEN [7:0] The Read/Write number of words in each memory access.	

Register:: LS_MEM_FIFO_RW_REMAIN
0xAB

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MFRW_RM	7:0	R/W	0x80	LS_MEM_FIFO_RW_REMAIN [7:0] The Read/Write number of words at the last access. This register must be 4X.	

Register:: LS_MEM_START_ADDR_H
0xAC

Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved	
LS_MEM_ADR_H	6:0	R/W	0x00	LS_MEM_START_ADDR [22:16] Start address of LS memory block (Total 22/23 bits) .	

If the columns per bank are 256, and Bank = 4 , SDRAM address [22:0] is: 1'b0+R[11:0]+B[1:0]+C[7:0]

If the columns per bank are 256, and Bank = 2 , SDRAM address [22:0] is: 2'b0+R[11:0]+B[0]+C[7:0]

If the columns per bank are 512, and Bank = 4 , SDRAM address [22:0] is: R[11:0]+B[1:0]+C[8:0]

If the columns per bank are 512, and Bank = 2 , SDRAM address [22:0] is: 1'b0+R[11:0]+B[0]+C[8:0]

Register:: LS_MEM_START_ADDR_M
0xAD

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MEM_ADR_M	7:0	R/W	0x00	LS_MEM_START_ADDR [15:8] Start address of LS memory block (Total 22/23 bits)	

Register:: LS_MEM_START_ADDR_L
0xAE

Name	Bits	Read/Write	Reset State	Comments	Config
LS_MEM_ADR_L	7:0	R/W	0x00	LS_MEM_START_ADDR [7:0] Start address of LS memory block (Total 22/23 bits)	

Register:: LS_BIST_CTRL
0xAF

Name	Bits	Read/Write	Reset State	Comments	Config
LS_TEST	7:6	R/W	0	Reserved for testing	
Reserved	5	R/W	0	Reserved	
FREEZE_MODE	4	R/W	0	Freeze mode enable	

LS_TEST_EN	3	R/W	0	LiveShow™ Test Enable. 0: Disable 1: Enable	
LS_TEST_MODE	2	R/W	0	LiveShow™ Test Mode. 0: Bypass interpolated delta 1: Bypass LUT4 value	
LS_BIST_START	1	R/W	0	LiveShow™ Memory BIST Start. Set 1 to start and auto-clear after finished.	
LS_BIST_RESULT	0	R	0	LiveShow™ Memory BIST Result. 0: Failed 1: Pass	

Compression

Register:: LS_FRAME0 0xB0					
Name	Bits	Read/Write	Reset State	Comments	Config
CUR_BYPASS_EN	7	R/W	0	In Current frame path, By Pass the conversion path and go through OD_LUT directly: 0: Disable 1: Enable	
CUR_COMP_MODE	6	R/W	0	In Current frame path, compression mode: 0: Interpolation Mode (Average Mode)(Mode 1) 1: Duplication Mode(Drop Mode) (Mode 2)	
CUR_RGB2YUV_EN	5	R/W	0	In Current frame path, RGB to YUV: 0: Disable 1: Enable	
CUR_COMP_EN	4	R/W	0	In Current frame path compression enable: 0: Disable 1: Enable	
CUR_COMP_METHOD	3:1	R/W	0	Current frame path compression method: 000: YUV444to422 (for YUV mode) 001: YUV444to411 (for YUV mode) 010: Super Pixel 1x2 compression (for RGB mode) 011: Super Pixel 1x3 compression (for RGB mode) 100: Super Pixel 1x4 compression (for RGB mode) Others: Reserved	
UV_MODE	0	R/W	0	In Current/Previous frame path, 444to422 U/V type 0: U0 V0 U2 V2 U4 V4 ... 1: U0 V1 U2 V3 U4 V5 ... Only take effect when CUR_COMP_METHOD set 3'b000 (YUV444to422 mode) and CUR_COMP_MODE set 1'b1	

Compression Method:

YUV444to422:

Average Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0((U0+U1)/2)((V0+V1)/2), Y1, Y2((U2+U3)/2)((V2+V3)/2), Y3, Y4((U4+U5)/2)((V4+V5)/2)...

Drop Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0U0V0, Y1, Y2U2V2, Y3, Y4U4V4...

YUV444to422 (uv_mode=1):

Average Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0((U0+U1)/2)((V0+V1)/2), Y1, Y2((U2+U3)/2)((V2+V3)/2), Y3, Y4((U4+U5)/2)((V4+V5)/2)...

Drop Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0U0V1, Y1, Y2U2V3, Y3, Y4U4V5...

YUV444to411:

Average Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0((U0+U1+U2+U3)/4) ((V0+V1+V2+V3)/4), Y1, Y2, Y3, Y4((U4+U5+U6+U7)/4) ((V4+V5+V6+V7)/4), Y5Y6Y7, Y8U8V8...

Drop Mode:

Original sequence: Y0U0V0, Y1U1V1, Y2U2V2, Y3U3V3, Y4U4V4...

Final sequences: Y0U0V0, Y1Y2Y3, Y4U4V4, Y5Y6Y7, Y8U8V8...

Super Pixel 1x2:

Method 1(Average Mode):

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: ((R0+R1)/2)((G0+G1)/2)((B0+B1)/2), ((R2+R3)/2)((G2+G3)/2)((B2+B3)/2)...

Mode 2(Drop Mode) :

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: R0G0B0, R2G2B2, R4G4B4...

Super Pixel 1x3:

Method 1(Average Mode):

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: ((R0+2R1+R2)/4)((G0+2G1+G2)/4)((B0+2B1+B2)/4), ((R2+2R3+R4)/4)((G2+2G3+G4)/4)((B2+2B3+B4)/4)...

Mode 2(Drop Mode) :

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: R1G1B1, R3G3B3, R5G5B5...

Super Pixel 1x4:

Method 1(Average Mode):

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: ((R0+R1+R2+R3)/4) ((G0+G1+G2+G3)/4) ((B0+B1+B2+B3)/4), ((R5+R6+R7+R8)/4) ((G5+G6+G7+G8)/4) ((B5+B6+B7+B8)/4)...

Mode 2(Drop Mode) :

Original sequence: R0G0B0, R1G1B1, R2G2B2, R3G3B3, R4G4B4...

Final sequences: R0G0B0, R4G4B4...

Register::: LS_FRAME1					0xB1	
Name	Bits	Read/Write	Reset State	Comments	Config	
CUR_DECOMP_EN	7	R/W	0	In Current frame path, decompression: 0: Disable 1: Enable		
CUR_DECOMP_MODE	6	R/W	0	In Current frame path, Decompression mode: 0: Interpolation Mode (Mode 1) 1: Duplication Mode (Mode 2)		
CUR_YUV2RGB_EN	5	R/W	0	In Current frame path, YUV to RGB: 0: Disable 1: Enable		
Reserved	4	R/W	0	Reserved		
PRE_DECOMP_EN	3	R/W	0	In Previous frame path, decompression: 0: Disable 1: Enable		
PRE_DECOMP_MODE	2	R/W	0	In Previous frame path, Decompression mode: 0: Interpolation Mode (Mode 1) 1: Duplication Mode (Mode 2)		
PRE_YUV2RGB_EN	1	R/W	0	In Previous frame path, YUV to RGB: 0: Disable 1: Enable		

Reserved	0	R/W	0	Reserved	
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Decompression method will follow compression setting (0x6016[3:1])

Decompression Method:

YUV422to444:

Interpolation Mode:

Original sequence: Y0U0V0, Y1, Y2U2V2, Y3, Y4U4V4, Y5,....

Final sequences: Y0U0V0, Y1((U0+U2)/2)((V0+V2)/2), Y2U2V2, Y3((U2+U4)/2)((V2+V4)/2), Y4U4V4, ...

Duplication Mode:

Original sequence: Y0U0, Y1V0, Y2U2, Y3V2, Y4U4, Y5V4,....

Final sequences: Y0U0V0, Y1U0V0, Y2U2V2, Y3U2V2, Y4U4V4, Y5U5V5,...

YUV422to444 (uv_mode=1):

Interpolation Mode:

Original sequence: Y0U0V1, Y1, Y2U2V3, Y3, Y4U4V5, Y5,....

Final sequences: Y0U0V0, Y1((U0+U2)/2)((V0+V2)/2), Y2U2V2, Y3((U2+U4)/2)((V2+V4)/2), Y4U4V4, ...

Duplication Mode:

Original sequence: Y0U0V1, Y1, Y2U2V3, Y3, Y4U4V5, Y5,....

Final sequences: Y0U0V1, Y1U0V1, Y2U2V3, Y3U2V3, Y4U4V5, Y5U4V5,...

YUV411to444:

Interpolation Mode:

Original sequence: Y0U0V0, Y1, Y2, Y3, Y4U4V4...

Final sequences: Y0U0V0, Y1((3U0+U4)/4)((3V0+V4)/4), Y2((2U0+2U4)/4)((2V0+2V4)/4), Y3((U0+3U4)/4)((V0+3V4)/4), Y4U4V4...

Duplication Mode:

Original sequence: Y0U0V0, Y1, Y2, Y3, Y4U4V4...

Final sequences: Y0U0V0, Y1U0V0, Y2U0V0, Y3U0V0, Y4U4V4...

Super Pixel 1x2:

Mode 1 (Duplicate Mode):

Original sequence: R0G0B0, R2G2B2, R4G4B4...

Final sequences: R0G0B0, R0G0B0, R2G2B2, R2G2B2, R4G4B4...

Mode 2 (Interpolation Mode) :

Original sequence: R0G0B0, R2G2B2, R4G4B4...

Final sequences: R0G0B0, ((R0+R2)/2)((G0+G2)/2)((B0+B2)/2), R2G2B2, ((R2+R4)/2)((G2+G4)/2)((B2+B4)/2)...

Super Pixel 1x3:

Mode 1 (Duplicate Mode):

Original sequence: R1G1B1, R3G3B3, R5G5B5...

Final sequences: (R1G1B1), R1G1B1, R1G1B1, R3G3B3, R3G3B3, R5G5B5, R5G5B5...

(repeat boundary)

Mode 2 (Interpolation Mode) :

Original sequence: R1G1B1, R3G3B3, R5G5B5...

Final sequences: (R1G1B1), R1G1B1, ((R1+R3)/2)((G1+G3)/2)((B1+B3)/2), R3G3B3, ((R3+R5)/2)((G3+G5)/2)((B3+B5)/2), R5G5B5...

Super Pixel 1x4:

Mode 1 (Duplicate Mode):

Original sequence: R0G0B0, R4G4B4, R8G8B8...

Final sequences: R0G0B0, R0G0B0, R0G0B0, R0G0B0, R4G4B4, R4G4B4, R4G4B4, R4G4B4...

Mode 2 (Interpolation Mode) :

Original sequence: R0G0B0, R4G4B4, R8G8B8...

Final sequences: R0G0B0, ((3R0+R4)/4)((3G0+G4)/4)((3B0+B4)/4), ((2R0+2R4)/4)((2G0+2G4)/4)((2B0+2B4)/4), ((R0+3R4)/4)((G0+3G4)/4)((B0+3B4)/4), R4G4B4...

Register::: LS_FRAME2						0xB2
Name	Bits	Read/Write	Reset State	Comments		Config
CUR_ROUND	7:6	R/W	0	The Current Pixel after RGB->YUV, 444->422 rounding mode setting 00: 8bit rounding 01: 6bit rounding 10: 5bit rounding 11: 4bit rounding Note: Rounding precision of compressed color values in current frame path when pixels are represented in RGB formats, or Y value in YUV format. Compressed UV values are of precision the same as Y value or 2 bit less depending on the setting of bit 5 in this Register.		
CUR_UV_ROUND	5	R/W	0	Current frame path UV rounding mode. When enabled, round additional 2 bits off UV data then the rounding bit specified by CUR_ROUND. (Only valid when CUR_ROUND != 2'b00) 0: Disable 1: Enable		
PRE_UV_ROUND	4	R/W	0	Previous frame path UV rounding mode. When enabled, round additional 2 bits off UV data then the rounding bit specified by SOURCE_RES. 0: Disable 1: Enable		
Reserved	3	R/W	0	Reserved		
CUR_RGB2YUV_SIM	2	R/W	0	Enable use of simplified formula for RGB to YUV conversion in current frame path. Should be set along with bit 1 and bit 0 in this register accordantly to get consistent color conversion results. 0: Disable 1: Enable RGB to YUV: $Y = (R+2G+B) / 4$ $U = (R-2G+B) / 4$ $V = (2R - 2B) / 4$		
CUR_YUV2RGB_SIM	1	R/W	0	Enable use of simplified formula for YUV to RGB conversion in current frame path. 0: Disable 1: Enable YUV to RGB: $R = Y + U + V$ $G = Y - U$ $B = Y + U - V$		
PRE_YUV2RGB_SIM	0	R/W	0	Enable use of simplified formula for YUV to RGB conversion in previous frame path. 0: Disable 1: Enable		

Level Estimation

Register::: LS_FRAME4						0xB3
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:6	R/W	0	Reserved		
EST_RANGE	5:4	R/W	0	Max error level correction calculate range: 00: Bypass 01: 8 pixels (add bandwidth 1 bit /pixel) 10: 16 pixels (add bandwidth 0.5 bit /pixel) 11: 32 pixels (add bandwidth 0.25 bit /pixel)		
EST_GAIN	3:0	R/W	0	User defined level estimation gain. Value: 0~15 Note: Take effect when level estimation is in threshold		

			mode, i.e. current compression enabled or current rgb to yuv conversion enabled. Working along with bit 5:0 of Register LS_FRAME5, this register defines the level estimation threshold locally, using the information obtained via comparison between original uncompressed and compressed frames, as described by following formula. Threshold = (Est_gain*grp_max_err>>3) + Est_value.	
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Note:

When using group maximum level estimation mode, the valid estimation range depends on the compression method selected. The setting in registers SOURCE_RES, CUR_COMP_METHOD, CUR_COMP_EN, and CUR_UV_ROUND all affect the compression ratio and thus the estimation range possible setting. Following table gives the valid value of register EST_RANGE. If value is out of the valid range, the reorder fifos may overflow or malfunction.

EST_RANGE valid values

SOURCE_RES	8	6	5	4
CUR_COMP_EN, CUR_COMP_METHOD, CUR_UV_ROUND				
Disabled, method = x, uv_round = 0 (RGB)	8	8,16	8,16	8,16
Disabled, method = x, uv_round = 1 (YUV444 + uv_rnd)	8	8,16	8,16,32	8,16,32
Enabled , method = 0, uv_round = 0 (YUV422)	8,16	8,16	8,16,32	8,16,32
Enabled , method = 0, uv_round = 1 (YUV422 + uv_rnd)	8,16	8,16,32	8,16,32	8,16,32
Enabled , method = 2 or 3, uv_round = 0 (super-pixel 1x2 / 1x3)	8,16	8,16,32	16,32	8,16,32
Enabled , method = 1, uv_round = 0 (YUV411)	8,16	8,16,32	16,32	8,16,32
Enabled , method = 1, uv_round = 1 (YUV411 + uv_rnd)	8,16,32	8,16,32	16,32	8,16,32
Enabled , method = 4, uv_round = 0 (super-pixel 1x4)	8,16,32	16,32	32	8,16,32

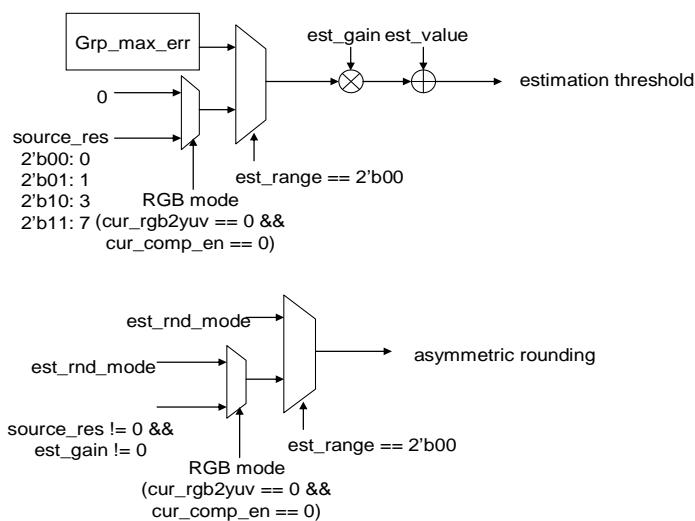
Register:: LS_FRAME5						0xB4
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7	R/W	0	Reserved		
EST_RND_MODE	6	R/W	0	Estimation value rounding mode. 0: Symmetric rounding estimation 1: Asymmetric estimation (with negative level estimation threshold=positive estimation threshold+1) Note: In normal rounding operation, maximum round-off error in negative direction is always 1 LSB larger than its counterpart in positive direction. But after color conversion and down-sampling this behavior does not always remain.		
EST_VALUE	5:0	R/W	0	User Defined Level Estimation Value: 0~63 (When Level Estimation Enabled, i.e. bit 5 in Register LS_CTRL0 = 1.)		

Note:

If user want to use original threshold mode, set EST_GAIN = 0.

If user want to use original estimation mode, set EST_GAIN = 1 and EST_VALUE = 0.

The final level estimation threshold and rounding mode applied on to the previous frame are decided as following figure.



Recommended usage:

1) In RGB mode,

`est_range = 0,`
`est_gain = 8,`
`est_value = 0.`

Description: estimation using fixed rounding error upper and lower bound calculated from applied source resolution.

2) In yuv or super-pixel modes,

`est_range = 0,`
`est_gain = 0,`
`est_value = "preferred value".`

Description: estimation using user defined value.

3) In yuv or super-pixel modes,

`set est_range = 1 or 2 or 3`
`est_gain = 8,`
`est_value = 0 :`

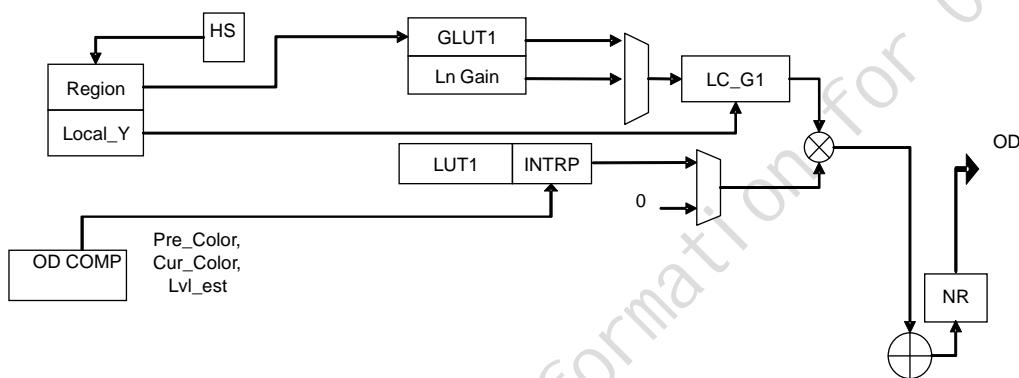
Description: estimation using dynamically calculated group maximum value.

By Position OverDrive

Register::: LS_BYPOS0	0xB5				
Name	Bits	Read/Write	Reset State	Comments	Config
LS_BYPOS_EN	7	R/W	0	Enable By Position Over Drive functions. Note: When disabled, traditional OD method is used with RGB mode turned on regardless bit 3 of this register and the local gain constantly set to 1. Other registers in this section only take effect when this bit enabled 1'b0 : Disable 1'b1 : Enable	
LS_BYPOS_REGION	6:5	R/W	0	Number of lines in each vertical region. Note: By Position Over Drive functions based on vertical regions in every frame. Inside each region the over drive value and also the local gain which obtained from LUTs are interpolated to get precision for each line. 2'b00: Region_size = 16 2'b01: Region_size = 32 2'b10: Region_size = 64 2'b11: Region_size = 128	
Reserved	4:3	R/W	0	Reserved	

LS_LAST_REGION_MODE	2	R/W	0	Last region LUT mode. Note: When enabled interpolation between OD LUT is not performed for the last region in every frame, instead, the OD value from the LUT assigned the first line of that region is used for the whole region. 1'b0 : Disable 1'b1 : Enable	
Reserved	1:0	R/W	0	Reserved	

When by position OD modes are enabled, each RTC channel outputs the over drive delta from the product of the OD LUT and the local gain, i.e. the OD delta = LUT1 * LC_G1. Noise reduction is applied to the OD delta before it is output from RTC channel and applied to the corresponding pixel value. Following is a block diagram depicts By Position Over Drive for a single RTC color channel. All 3 color channels share the same LUT and GLUT.



LUT size:

1. The table LUT1 consists of 17 x 16 8-bit elements, arranged in a matrix with 17 rows and 17 columns with diagonal elements vanish. Each row represents a current frame target color value running from 0 to 256 with a step of 16, while each column represents a previous frame color value covering the same range as current color value. Each 8-bit LUT element represents the magnitude of the corresponding Over Drive value.
 2. The tables GLUT1 consists of 32 7-bit elements, each of which represents a local Over Drive gain factor that is going to be applied to the OD value in the corresponding path. The 80 elements correspond to local gain of the first lines of number 0 to 79 region by default. This means up to 31 regions can be assigned within each of which interpolation between local gains corresponding to the first lines of current and next region is preformed to obtain precious local gain for every line.
- Vertical supports 512(16*32) to 4096(128*32) lines.

By Position OD operation Modes:

Register:: LS_BYPOS1					0xB6	
Name	Bits	Read/Write	Reset State	Comments	Config	
LS_LUT_EN_1	7	R/W	1	Enable Over Drive LUT in path 1. Note: This bit only takes effect when RGB mode is turned off. When enabled, Over Drive value in the path is interpolated from the 2D LUT1 with previous and current color value from RTC compression / decompression module. Otherwise Over Drive value is set to null in this path. 1'b0: Disable 1'b1: Enable Mode 1: enable Mode 2: enable Mode 3: enable		
LS_GLUT_1	6	R/W	0	Enable Non-Linear Gain LUT in path 1.		

				Note: When enabled, local gain in the path is interpolated from the non-linear gain table GLUT1, with the vertical region current pixel resides in (Region) and the local vertical position within the region (Local_Y). Otherwise local gain is interpolated from the user-defined gain in register LS_BYPOS_GAIN1, with the local vertical position. 1'b0: Disable 1'b1: Enable	
LS_GAIN_RND_1	5:3	R/W	0	Number of rounded bits for local gain in path 1. Note: Rounding is applied to the interpolated local gain with various range set by this option. The rounding bit number should be decided regarding the region size and the normalization of the corresponding GLUT or linear gains. If not rounded properly overflow may not be handled properly in this path. 3'b000: No rounding 3'b001: 1-bit rounding 3'b010: 2-bit rounding 3'b011: 3-bit rounding 3'b100: 4-bit rounding 3'b101: 5-bit rounding 3'b110: 6-bit rounding	
Reserved	2:0	R/W	0	Reserved.	

Register:: LS_BYPOS_GAIN1 0xB7					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved.	
LS_GAIN_BASE_1	6:0	R/W	0	7-bit unsigned linear gain base for path 1. Note: Defined as gain of the first line in Region 0. Combining bit 5:0 in register LS_BYPOS_SLOPE1 it defines the linear gain of this path. Takes effect only when LS_GLUT_1 and LS_BYPOS_AUTOUPDT are disabled.	

Register:: LS_BYPOS_SLOPE1 0xB8					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:6	R/W	0	Reserved.	
LS_GAIN_SLOPE_1	5:0	R/W	0	6-bit signed linear gain slope for path 1. Note: Together with bit 6:0 in register LS_BYPOS_GAIN1, the linear gain of the first line in each region is defined as Gain_base + (Region * Gain_slope >> Shift_bit), where the parameter Shift_bit equals 4, 3, or 2 when Region_size is set to 16, 32, or 64 respectively. This value is clamped to 0~127, as 7bits as GLUT1. Takes effect only when LS_GLUT_1 and LS_BYPOS_AUTOUPDT are disabled.	

Register:: LS_LUT_CTRL 0xBF					
Name	Bits	Read/Write	Reset State	Comments	Config
LS_LUT_WEN	7	R/W	0	Enable write to the selected LUT through LS_LUT_DATA access port. This bit should be enabled only when RTC function is disabled to avoid undefined behavior during LUT writing. Complete contains for a single LUT, which means 289 bytes for OD LUTs or 80 bytes for GLUTs should be written to the access port sequentially before	

				disabling this bit or changing the selection of LUTs. 1'b0: Disable 1'b1: Enable	
LS_LUT_SEL	6	R/W	0	Select which set of LUTs to be written or read. 1'b0: Over Drive LUTs 1'b1: Non-Linear Gain LUTs	
Reserved	5:2	R/W	0	Reserved	
LS_LUT_INCMPL	1	R	0	LUT incomplete flag. Indicate that one of the OD LUTs is not completely written with 289 bytes of data. Should not turn on RTC function when this bit is set. Incomplete GLUTs writing does not trigger this bit, and RTC function should operate normally if properly set so that in every by position region reasonable local gain is applied. 1'b0: Normal 1'b1: LUT incomplete	
Reserved	0	R/W	0	Reserved.	

Register:: LS_LUT_READ 0xC0					
Name	Bits	Read/Write	Reset State	Comments	Config
LS_LUT_READ_EN	7	R/W	0	Enable OD LUT and GLUT read function. The Over Drive functions should be disabled (A1[7] = 0), or otherwise OD delta may be incorrect for certain color channels.	
Reserved	6:0	R/W	0	Reserved	

Register:: LS_LUT_ROW 0xC1					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:5	R/W	0	Reserved.	
LS_LUT_READ_ROW	4:0	R/W	0	Read OD LUTs: Specify the row address of the element to be read. Address increment is automatic in reading process, right after every read with column address = 16. Row address wraps around when increasing beyond 16. Reset when LS_LUT_READ_EN disabled. 0 to 16: current color value 0 to 256 17 to 31: reserved Read GLUTs: No use.	

Register:: LS_LUT_COL 0xC2					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved.	
LS_LUT_READ_COL	6:0	R/W	0	When reading OD LUTs, specify the column address of the element to be read. Address increment is automatic in reading process, right after every read. Column address wraps around when increasing beyond 16. Reset when LS_LUT_READ_EN disabled. 0 to 16: previous color value 0 to 256 17 to 127: reserved When reading GLUTs, Specify the address of the element to be read. (Auto increment, wraps around beyond 79, and reset when read disabled.) (= LS_GLUT_READ_ADDR[6:0]) 0 to 31: address 32 to 127: reserved	

Register:: LS_LUT_DATA					0xC3	
Name	Bits	Read/Write	Reset State	Comments	Config	
LS_LUT_DATA	7:0	R/W	0	LUT data port. The value written to this register is pushed into the selected LUT when LS_LUT_WEN is 1. Reading this register gets the value from the selected LUT with address specified in register LS_LUT_ROW and LS_LUT_COL, while the address increase automatically after every read.	wport rport	

SDRAM Control (Page 4)

Register:::SDR_CTRL0						0xA1
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSV_A1_76	7:6	R/W	0	Reserved		
SDR_RD_DELAY	5:3	R/W	'b011	Delay from Row Active to Data Valid 000: Reserved 001: Reserved 010: Reserved 011: 3 MCLK 100: 4 MCLK 101: 5 MCLK 110: Reserved 111: Reserved		
SDR_WR_DELAY	2:0	R/W	'b011	Delay from Row Active to Write 000: Reserved 001: Reserved 010: 2 MCLK 011: 3 MCLK 100: 4 MCLK 101: 5 MCLK 110: Reserved 111: Reserved		

Register:::SDR_CTRL1						0xA2
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_CL	7:5	R/W	'b011	CAS Latency of SDRAM 000: Reserved 001: Reserved 010: 2 MCLK 011: 3 MCLK 100: Reserved 101: Reserved 110: Reserved 111: Reserved If MCLK >100MHz, SDR_CL should be 3 MCLK.		
SDR_RSV_A2_40	4:0	R/W	4	Reserved		

Register:::SDR_AREF_TIME						0xA3
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_AREF_TIME	7:0	R/W	0x0D	Auto Refresh Time. (The period of initial refresh time in MCLK cycle)		

Register:::SDR_PRCG						0xA4
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_PRCG_BIT	7	R/W	1'b1	Precharge All Banks by 0: A8 1: A10		

SDR_PRCG_DO	6	R/W	0	Force to Precharge All Banks	
SDR_COL_NUM	5	R/W	0	Columns per Bank 0: 256 1: 512	
SDR_RESET	4	R/W	0	SDR Reset 0: Normal 1: Reset	
SDR_PRCG_DLY	3:0	R/W	3	Precharge Delay Cycle (The interval from precharge to next valid command)	

Register::SDR_MEM_TYPE 0xA5					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_MEM_SIZE	7:6	R/W	0x02	SDRAM Memory Size 00: 1Mx16x1pcs 01: 1Mx16x2pcs 10: 2Mx32x1pcs 11: Reserved	
SDR_BANK_SEL	5	R/W	0	Banks per SDRAM 0: 4 bank 1: 2 bank	
SDR_ABR_STATUS	4	R	0	Arbiter Recovery Happen	
SDR_ABR_REC_EN	3	R/W	0	Arbiter Recovery Enable, Reset State Machine	
SDR_CAS_LATN	2:0	R/W	1	CAS Latency for Controller 000: Reserved 001: 1 010: 1 011: 2 100: 2 101: 3 110: 3 111: 4	

Register::SDR_SLEW_RATE 0xA6					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_RSV_A6_73	7:3	R/W	0	Reserved	
SDR_AUTO_GATING	2	R/W	0	Auto gating CKE 0: Disable 1: Enable	
SDR_CKE_L	1	R/W	0	Force CKE Low (for power-down mode) 0: Disable 1: Enable	
SDR_CKE_H	0	R/W	0	Force CKE High (for testing) 0: Disable 1: Enable	

Register::SDR_AREF_CNT 0xA7					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_AREF_CNT8	7:0	R/W	0x81	Periodic refresh command interval time. (N x 256 x MCLK period) This setting need to meet all rows in all banks must be refreshed at least once every t _{REF} time	reg_aref_cn t[7:0]

Register::RESERVED						0xA8
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:0	R/W	0	Reserved		

Register::RESERVED						0xA9
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:0	R/W	0	Reserved		

Register::SDR_RSC_AREF						0xAA
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC_AREF	7:0	R/W/D	0xFF	Token Ring Bit[7:0]		

Register::SDR_RSC MCU						0xAB
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC MCU	7:0	R/W/D	0x20	Token Ring Bit[7:0]		

Register::SDR_RSC_CAP1						0xAC
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC_CAP1	7:0	R/W/D	0xAA	Token Ring Bit[7:0]		

Address 0xAD reserved

Register::SDR_RSC_MAIN						0xAE
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC_MAIN	7:0	R/W/D	0x55	Token Ring Bit[7:0]		

Address 0xAF reserved

Register::SDR_RSC_RTC_RD						0xB0
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC_RTC_RD	7:0	R/W/D	0xAA	Token Ring Bit[7:0]		

Register::SDR_RSC_RTC_WR						0xB1
Name	Bits	Read/ Write	Reset State	Comments	Config	
SDR_RSC_RTC_WR	7:0	R/W/D	0x55	Token Ring Bit[7:0]		

- *(Double-Buffer) Token-Ring access before AREF*

Register::RESERVED						0xB2
Name	Bits	Read/ Write	Reset State	Comments	Config	

Reserved	7:0	R/W	0	Reserved	
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Register::RESERVED					0xB3
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register::SDR_ABTR_STATUS0					0xB4
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_ABTR_RTCR	7	R	0	RTC Read Arbiter Status	
SDR_ABTR_RTCW	6	R	0	RTC Write Arbiter Status	
SDR_ABTR_MAIN	5	R	0	MAIN Read Arbiter Status	
Reserved	4	--	0	Reserved	
SDR_ABTR_CAP1	3	R	0	CAP1 Write Arbiter Status	
Reserved	2	--	0	Reserved	
SDR_ABTR MCU	1	R	0	MCU R/W Arbiter Status	
SDR_ABTR_AREF	0	R	0	AREF Arbiter Status	

- Write-clear

Register::SDR_ABTR_STATUS 1					0xB5
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:1	--	0	Reserved	
SDR_RESET_RDY	0	R	0	SDR Reset Ready	

Register::RESERVED					0xB6
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: SDR_POWER_CTRL0					0xB7
Name	Bits	Read/ Write	Reset State	Comments	Config
precharge_pwr_down	7	R/W	0	Make SDRAM enter precharge power down mode 1: activated 0: inactivated	
pwr_down_rdy	6	R	0	SDR power down ready	
SDR_POWDN_CMD	5:4	R/W	0	Enter different mode when 0xB7[7] set to 1'b1 00: precharge power down (default) 01: reserved 10:deep power down 11:self refresh	
SDR_CKE_HIGH	3	R/W	0	Force Cke pin of SDRAM High 1 : Enable 0 : Disable	
Reserved	2:0	R/W	0	Reserved	

Register::SDR_ADDR_H					0xB8
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Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
SDR_ADDR_H	6:0	R/W	0	SDR_ADDR [22:16] If the columns per bank are 256, bit[5:0] is assigned to R[11:6] and bit[6] is reserved. If the columns per bank are 512, bit[6:0] is assigned to R[11:5]	

If the columns per bank are 256, SDRAM address [22:0] is: R[11:0]+B[1:0]+C[7:0]

If the columns per bank are 512, SDRAM address [22:0] is: R[11:0]+B[1:0]+C[8:0]

Register::SDR_ADDR_M 0xB9					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_ADDR_M	7:0	R/W	0	SDR_ADDR [15:8] If the columns per bank are 256, bit[7:2] is assigned to R[5:0] bit[1:0] is assigned to B[1:0] If the columns per bank are 512,bit bit[7:3] is assigned to R[4:0] bit[2:1] is assigned to B[1:0] bit[0] is assigned to C[8]	

Register::SDR_ADDR_L 0xBA					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_ADDR_L	7:0	R/W	0	SDR_ADDR [7:0] Bit[7:0] is assigned to C[7:0] regardless of columns per bank are 256 or 512.	

Register::SDR_ACCESS_CMD 0xBB					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_ACS_CMD	7:5	R/W	0	SDR_ACCESS_COMMAND (clear to 000 after finish) 000: NOP or Finish 001: Pre-charge (all bank or single bank) 010: Auto-Refresh (step by step or auto arbiter) 011: Load Mode Register (step by step or auto initialization) (Load Mode Register will reset DLL of DRAM, we must idle ~200cycles before next "READ") 100: WRITE command (Buf→SDR) 101: READ command (SDR→Buf) 110: Reserved 111: Reserved	
SDR_DBUF_IDX	4:0	R/W	0	DATA_BUFFER_INDEX Specifies the next access byte in the buffer.	

Register::SDR_DATA_BUF 0xBC					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_DATA_BUF	7:0	R/W	0	SDR_DATA_BUFFER Sequential 8-word (32 byte) READ/WRITE from low to high address auto-increase. DATA_BUFFER_INDEX specifies the next access byte in the buffer.	

- *SDR_ACCESS (Read/Write) can be used for MCU access*
- *How to modify only one-byte in SDR? Read 32 bytes, only modify one index-select byte, Write 32 bytes.*

Register::SDR MCU RD LEN 0xBD					
Name	Bits	Read/ Write	Reset State	Comments	Config

Mcurd_tst_en	7	R/W	0	On-line test mcurl SDRAM enable	
Mcurd_len	6:0	R/W	2	Mcu Read SRAM Length	

Register::phase calibration 0xBE					
Name	Bits	Read/ Write	Reset State	Comments	Config
reserve	7:5	R/W	0		
Ph_cal_up_sel	4	R/W	0	Phase calibration wait event select 0 : SDRAM write (not include MCU write to SDRAM) 1: display vertical front porch	
Phcal_wait_en	3	R/W	0	Calibration wait event (ref. CR_BE[4])	
Phcal_en	2	R/W	0	Phase calibration enable 0: finish 1: enable (auto-clear by HW)	
Rd_ph_db_en	1	R/W	0	Double buffer enable(Update SRAM DATAT DQS fine dly)	
Rd_ph_db_start	0	R/W	0	Start double buffer (ref. CR_BE[4]) 0: finish 1: start (auto clear by HW)	

Register::calibration_result 0xBF					
Name	Bits	Read/ Write	Reset State	Comments	Config
reserve	7	R	0		
Phcal_cnt	6:0	R	0		

Register::SDR_CLK_DLY1 0xC0					
Name	Bits	Read/ Write	Reset State	Comments	Config
mclk_inv	7	R/W/D	0	Mclk ouput invert 0 : non invert 1: inert	
reserve	6:0	R/W	0		

Register::SDR_CLK_DLY2 0xC1					
Name	Bits	Read/ Write	Reset State	Comments	Config
mclk_fine_tune	7:0	R/W/D	0	Mclk delay fine tune[7:0]	

Register::DQS0_DLY1 0xC2					
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_D0_LFT_OFF	7	R	0	SDRAM Data [15:0] Latch Fine-Tune Status 0: Activated 1: Inactivated	
dqs0_coarse_dly	6:5	R/W/D	0	SDRAM Data [15:0]coarse dly [1:0] 00: 0 01: 90 10: 180 11: 270	

reserve	4:0	R/W	0		
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Register::DQS0_DLY2					0xC3
Name	Bits	Read/ Write	Reset State	Comments	Config
dqs0_fine_dly	7:0	R/W/D	0	SDRAM Data[15:0] fine dly [7:0]	

Register::DQS1_DLY1					0xC4
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_D1_LFT_OFF	7	R	0	SDRAM Data [31:16] Latch Fine-Tune Status 0: Activated 1: Inactivated	
dqs1_coarse_dly	6:5	R/W/D	0	SDRAM Data[31:16] coarse dly [1:0] 00: 0 01: 90 10: 180 11: 270	
reserve	4:0	R/W	0		

Register::DQS1_DLY2					0xC5
Name	Bits	Read/ Write	Reset State	Comments	Config
dqs1_fine_dly	7:0	R/W/D	0	SDRAM Data[31:16] fine dly [7:0]	

Register::DQS2_DLY1					0xC6
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_D2_LFT_OFF	7	R	0	SDRAM Data [47:32] Latch Fine-Tune Status 0: Activated 1: Inactivated	
Dqs2_coarse_dly	6:5	R/W/D	0	SDRAM Data[47:32] coarse dly [1:0] 00: 0 01: 90 10: 180 11: 270	
reserve	4:0	R/W	0		

Note: reserve for 64 bits SDRAM

Register::DQS2_DLY2					0xC7
Name	Bits	Read/ Write	Reset State	Comments	Config
Dqs2_fine_dly	7:0	R/W/D	0	SDRAM Data[47:32] fine dly [7:0]	

Note: reserve for 64 bits SDRAM

Register::DQS3_DLY1					0xC8
Name	Bits	Read/ Write	Reset State	Comments	Config
SDR_D3_LFT_OFF	7	R	0	SDRAM Data [63:48] Latch Fine-Tune Status 0: Activated 1: Inactivated	

Dqs3_coarse_dly	6:5	R/W/D	0	SDRAM Data coarse dly [1:0] 00: 0 01: 90 10: 180 11: 270	
reserve	4:0	R/W	0		

Note: reserve for 64 bits SDRAM

Register::DQS3_DLY2	0xC9
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Name	Bits	Read/ Write	Reset State	Comments	Config
Dqs3_fine_dly	7:0	R/W/D	0	SDRAM Data[63:48] fine dly [7:0]	

Note: reserve for 64 bits SDRAM

Register::SEC_DQS0_DLY	0xCA
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Name	Bits	Read/ Write	Reset State	Comments	Config
Sec_dqs0_fine_dly	7:0	R/W	0	SDRAM Data[15:0] fine dly [7:0] Phase switch setting for on-line mcurd to check phase	

Register::SEC_DQS1_DLY	0xCB
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Name	Bits	Read/ Write	Reset State	Comments	Config
Sec_dqs1_fine_dly	7:0	R/W	0	SDRAM Data[31:16] fine dly [7:0] Phase switch setting for on-line mcurd to check phase	

Register::SEC_DQS2_DLY	0xCC
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Name	Bits	Read/ Write	Reset State	Comments	Config
Sec_dqs2_fine_dly	7:0	R/W	0	SDRAM Data[47:32] fine dly [7:0] Phase switch setting for on-line mcurd to check phase	

Note: reserve for 64 bits SDRAM

Register::SEC_DQS3_DLY	0xCD
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Name	Bits	Read/ Write	Reset State	Comments	Config
Sec_dqs3_fine_dly	7:0	R/W	0	SDRAM Data[63:48] fine dly [7:0] Phase switch setting for on-line mcurd to check phase	

Note: reserve for 64 bits SDRAM

Address: CE~FB Reserved

Register::extended_mode_register	0xFC
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Name	Bits	Read/ Write	Reset State	Comments	Config
EMR_first_b	7	R/W	0	Select which mode register programmed first when initialization sequence 0:EMR 1:MR	
Mcurd_crc_en	6	R/W	0	CRC Enable for MCU Read from SDRAM only	

EMR_addr	5:4	R/W	01	Define BA1 ,BA0 value to locate EMR	
Emr_config[11:8]	3:0	R/W	0	extended_mode_register[11:8]	

Register::extended_mode_register 0xFD					
Name	Bits	Read/Write	Reset State	Comments	Config
Emr_config[7:0]	7:0	R/W	0	extended_mode_register[7:0]	

Register::random_generator 0xFE					
Name	Bits	Read/Write	Reset State	Comments	Config
Rst_random_sel	7	R/W	0	SDRAM controller random generator reset 0: dvs 1: ivs	
Rst_crc_sel	6	R/W	0	SDRAM controller CRC reset 0: dvs 1: ivs	
Random_en	5	R/W	0	SDRAM controller random generator enable	
Crc_start	4	R/W	0	SDRAM controller CRC start 0: finish 1: start (auto-clear by HW)	
Crc_adr_port	3:0	R/W	0	Address port for CRFF	

Register::CRC_DATA_PORT 0xFF					
Name	Bits	Read/Write	Reset State	Comments	Config
Crc_data_port	7:0	R	0	CRC Data Port	

SDR_FIFO Control (Page 5)

Register::IN1_FIFO_STATUS					0xA1
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_BIST_DONE	7	R	0	IN1_BIST_DONE 0: BIST is done. 1: BIST is active	
IN1_BIST_OK	6	R	0	IN1_BIST_OK 0: Failed 1: Pass	
IN1_BIST_EN	5	R/W	0	IN1_BIST_EN Set 1 to trigger BIST function.	
IN1_FLAG_CLR	4	R/W	0	IN1_FLAG_CLEAR Write 1 to clear overflow and underflow (CRA1[1:0])	
IN1_FIFO_FULL	3	R	0	IN1_FIFO_FULL 0: FIFO is not full. 1: FIFO is full.	
IN1_FIFO_EPTY	2	R	0	IN1_FIFO_EMPTY 0: FIFO is not empty. 1: FIFO is empty.	
IN1_FIFO_OVFL	1	R	0	IN1_FIFO_OVERFLOW It will go high when overflow occurred, and cleared by IN1_FLAG_CLR.	
IN1_FIFO_UDFL	0	R	0	IN1_FIFO_UNDERFLOW It will go high when underflow occurred, and cleared by IN1_FLAG_CLR.	

Register::MAIN_FIFO_STATUS					0xA2
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_BIST_DONE	7	R	0	MN_BIST_DONE 0: BIST is done. 1: BIST is active	
MN_BIST_OK	6	R	0	MN_BIST_OK 0: Failed 1: Pass	
MN_BIST_EN	5	R/W	0	MN_BIST_EN Set 1 to trigger BIST function.	
MN_FLAG_CLR	4	R/W	0	MN_FLAG_CLEAR Write 1 to clear overflow and underflow (CRA21:0])	
MN_FIFO_FULL	3	R	0	MN_FIFO_FULL 0: FIFO is not full. 1: FIFO is full.	
MN_FIFO_EPTY	2	R	0	MN_FIFO_EMPTY 0: FIFO is not empty. 1: FIFO is empty.	
MN_FIFO_OVFL	1	R	0	MN_FIFO_OVERFLOW It will go high when overflow occurred, and cleared by MN_FLAG_CLR.	
MN_FIFO_UDFL	0	R	0	MN_FIFO_UNDERFLOW It will go high when underflow occurred, and cleared by MN_FLAG_CLR.	

Register::IN1_SFIFO_STATUS					0xA3
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Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	--	0	Reserved	
IN1_S_FLAG_CLR	2	W	0	IN1_S_FLAG_CLEAR Write 1 to clear sfifo overflow (CRA3[0])	
IN1_SFIFO_FULL	1	R	0	IN1_SFIFO_FULL 0: SFIFO is not full. 1: SFIFO is full.	
IN1_SFIFO_OVFL	0	R	0	IN1_SFIFO_OVERFLOW It will go high when overflow occurred, and cleared by IN1_S_FLAG_CLR	

Register::IN1_ONEF_STATUS					0xA4
Name	Bits	Read/ Write	Reset State	Comments	Config
NOT_W_CNT_SEL	7	R/W	0	The counter select 0: the max. continuous frames 1: the current continuous frames	
NOT_W_CNT	6:0	R	0	The counter to record the continuous frames not written in capture FIFO (depend on bit7) Note: write bit0 as 1 to clear the counter	

Register:: IN1_3D_FRC_CTL					0xA5
Name	Bits	R/W	Default	Comments	Config
WD_2Dto3D_EN	7	R/W	0	Watchdog for 2D to 3D enable: 0: disable 1: enable	
LR_FLAG_SYNC_I_MET_HOD	6	R/W	0	Input LR image block selection sync method (for cyberlink 3D, only effect when input slower) 0: drop mode 1: overwrite mode	
FRAME_MASK_EN	5	R/W	0	1/2 input frames mask enable 0: disable 1: enable	
IVS_MASK_EN	4	R/W	0	ivs between L&R mask enable (double buffer) 0: disable 1: enable	
LR_FLAG_SYNC_I_EN1	3	R/W	0	Input LR image block selection sync enable(for frame sequential, only effect when input slower) 0:disable 1:enable	
LR_FLAG_SYNC_I_EN2	2	R/W	0	Input LR image block selection sync enable (for cyberlink 3D, only effect when input slower) 0: disable 1: enable	
DB_FIELD_MERGE_EN	1	R/W	0	Double buffer field merge enable 0: disable 1: enable	
HALF_LINE_EN	0	R/W	0	Half line process for Side-by-side enable 0: disable 1: enable	

Register::IN1_PXL_NUM_H	0xA6
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Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
3D_HALF_LINE_OPTION	5	R/W	0	Half line process option for side by side: 0:generate 23-pipeline delay between L&R 1:generate 23-pipeline delay between R&L It's valid only when 0xA5-bit[0] is enable	
3D_INTERLACE_MODE_EN	4	R/W	0	Double buffer field merge for frame packing interlace mode: 0: disable 1: enable	
IN1_PXL_NUM_H	3:0	R/W	0	IN1_PIXEL_NUM [11:8] Pixel number of one line, for FIFO to fill dummy. (total 12-bits)	

Register::IN1_PXL_NUM_L 0xA7					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_PXL_NUM_L	7:0	R/W	0	IN1_PIXEL_NUM [7:0] Pixel number of one line, for FIFO to fill dummy. (total 12-bits)	

Register::IN1_WATER_LEVEL 0xA8					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_WTLVL	7:0	R/W	0x80	IN1_WTLVL [7:0] When FIFO depth is over WTLVL, FIFO write data.	

Register::IN1_WR_NUM_H 0xA9					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_WR_NUM_H	7:0	R/W	0x08	IN1_WRITE_NUM[15:8] Number of length to fill in the SDR memory.	

Register:: IN1_WR_NUM_L 0xAA					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_WR_NUM_L	7:0	R/W	0xFF	IN1_WRITE_NUM[7:0] Number of length to fill in the SDR memory.	

Register::IN1_WR_LEN 0xAB					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_WR_LEN	7:0	R/W	0x80	IN1_WRLEN[7:0] Length of data to fill in the SDR memory once. (unit : 64 bit)	

Register::IN1_WR_REMAIN 0xAC					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_WR_REMAIN	7:0	R/W	0x80	WRITE_REMAIN [7:0]	

				The remained part that can't make a complete length. (unit : 64 bit)	
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- Formula : (bits of one frame or one line data) / 64 = ((NUM*LEN)+REM)
- Restriction :
 - ✓ When total data = n * 64, it must be configured to num=0, remain = n.
 - ✓ Both LEN and REM must be times of 4. REM is not necessary smaller than LEN but can't be 0.

Register::IN1_MEM_ADDR_H					0xAD
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
IN1_MADR_H	6:0	R/W	0	IN1_WRI_MEM_START[22:16] The initial write address of SDR.(Total 23 bits)	

Register:: IN1_MEM_ADDR_M					0xAE
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_MADR_M	7:0	R/W	0x00	IN1_WRI_MEM_START[15:8] The initial write address of SDR. (Total 23 bits)	

Register:: IN1_MEM_ADDR_L					0xAF
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_MADR_L	7:0	R/W	0x00	IN1_WRI_MEM_START[7:0] The initial write address of SDR. (Total 23 bits)	

- The initial write address total 23 bits.
- Write initial address[22:0] = Row[11:0] + Bank[1:0] + C(1) + Column[7:0]

Register::IN1_LINE_STEP_H					0xB0
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
IN1_LSTEP_H	5:0	R/W	0	IN1_LINE_STEP[13:8] The distance between two lines of SDR. (Total 14 bits)	

Register::IN1_LINE_STEP_L					0xB1
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_LSTEP_L	7:0	R/W	0x00	IN1_LINE_STEP [7:0] The distance between two lines of SDR. (Total 14 bits)	

- Line step total 14 bits[13:0] = one more row[2:0] + bank[1:0] + C(1) + Column [7:0]

- Line step = horizontal pixel bits /"32"

Sdr addr = {row[11:0], bank[1], bank[0], col[8], col[7:0]}

If SDR is 256-column(0xA4[5]==0), Col[8] of line step or block step is useless

If SDR is 2-bank(0xA5[5]==1), Bank[1] of line step or block step is useless

(page 5: 0xB0 0xB1 0xB2 0xB3 0xB4 0xB5 0xB6 0xC9 0xCA 0xCB 0xCC)

Register::IN1_BLOCK_STEP_H					0xB2
Name	Bits	Read/ Write	Reset State	Comments	Config

Reserved	7:4	--	0	Reserved	
IN1_BSTEP_H	3:0	R/W	0	IN1_BLOCK_STEP[11:8] The distance between two blocks of SDR.(Total 12 bits)	

Register::IN1_BLOCK_STEP_L					0xB3
Name	Bits	Read/Write	Reset State	Comments	Config
IN1_BSTEP_L	7:0	R/W	0x00	IN1_BLOCK_STEP[7:0] The distance between two blocks of SDR. (Total 12 bits)	

- The unit is row. Use it to identify max. 4 blocks for merge.

Register::IN1_BL2_ADDR_H					0xB4
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
IN1_BL2_MADR_H	6:0	R/W	0	IN1_SEC_BL[22:16] Second block of SDR to progress the double buffer. The given address is the absolute one.	

Register::IN1_BL2_ADDR_M					0xB5
Name	Bits	Read/Write	Reset State	Comments	Config
IN1_BL2_MADR_M	7:0	R/W	0x00	IN1_SEC_BL[15:8] Second block of SDR to progress the double buffer. The given address is the absolute one.	

Register::IN1_BL2_ADDR_L					0xB6
Name	Bits	Read/Write	Reset State	Comments	Config
IN1_BL2_MADR_L	7:0	R/W	0x00	IN1_SEC_BL[7:0] Second block of SDR to progress the double buffer. The given address is the absolute one.	

- When double block, the second block is located here. When merged, the 3rd and 4th block will start here.
- double : 1st block starts at wr_add_sta, 2nd block starts at secblock.
- merge : 1st : wr_add_sta, 2nd : wr_add_sta + { blockstep, 11'h000 },
3rd : secblock, 4th secblock + { blockstep, 11'h000 }

Register::IN1_LINE_NUM_H					0xB7
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
IN1_BK_STA_SEL	6	R/W	0	IN1 start point to change block_sel 0: reference to ivs 1: reference to vertical active region Note : the register is only used at double buffer mode input faster case	
Zero	5	R/W	0	Useless, Must set to 0	
IN1_FRAME_MD	4	R/W	1	Frame Mode 0: Num*Length + Remain is line-access setting 1: Num*Length + Remain is frame-access setting	

				Line mode: It must be used for Double buffer mode and Filed merge mode Frame mode: It only be used if the SDR is regarded as frame buffer.	
IN1_LNUM_H	3:0	R/W	0	IN1_Line_Number [11:8] The total line-number of one image. (Total 12 bits)	

Register::IN1_LINE_NUM_L 0xB8					
Name	Bits	Read/Write	Reset State	Comments	Config
IN1_LNUM_L	7:0	R/W	0x00	IN1_Line_Number [7:0] The total line-number of one image. (Total 12 bits)	

Register::IN1_SDR_CTRL 0xB9					
Name	Bits	Read/Write	Reset State	Comments	Config
IN1_CAP_EN	7	R/W	1	IN1_Capture_Enable 0: Disable this capture block.(Frame-Sync can also disable memory access) 1: Enable this capture block.	
IN1_MRG_EN	6	R/W	0	IN1_Merge_Enable 0: Disable field merge function. 1: Enable field merge function, change to 4 blocks mode.	
IN1_DB_EN	5	R/W	0	IN1_Double_Enable (SDR memory block) 0: Single buffer (Only use 1 st memory block) 1: Double buffer or Field merge	
IN1_BLK_FREE	4	R/W	0	IN1_Block_Free 0: FRC mode 1: Block free toggle when double buffer enable	
IN1_SB_SEL	3	R/W	0	IN1_Single_Buffer_Select (Only active when Single-Buffer) 0: Single buffer(0)/Field merge buffer(0/1) 1: Single buffer(1)/Field merge buffer(2/3)	
IN1_FRZ_EN	2	R/W	0	IN1_Freeze_Enable 0: Disable freeze (Always start from 1 st block) 1: Enable freeze (Always freeze at 1st block)	
IN1_IVS_RST_EN	1	R/W	1	IN1_En_Vs_Rst Use IVS as synchronous reset, in this module, it must be 1	
Reserved	0	--	0	Reserved	

Register::IN1_MADDR_TOG_CTL 0xBA					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved	
IN1_MADR_DB_RDY	6	R/W	0	Hardware auto toggle M:N double buffer ready (both for capture/display)(auto clear): 1'b0: not ready 1'b1: ready	
IN1_MADR_DB_MN	5	R/W	0	Hardware auto toggle M:N double buffer (both for capture/display) (auto clear): 1'b0: disable 1'b1: enable	
IN1_MADR_TOG_EN	4	R/W	0	Hardware auto toggle among three initial write address:	

				1'b0: disable 1'b1: enable	
IN1_MADR_SEL	3:2	R/W	0	Three initial write address access port(0xAD&0xAE&0xAF): 2'b00: the 1st write address 2'b01: the 2nd write address 2'b10: the 3rd write address 2'b11: reserved	
IN1_MADR_CNT	1:0	R	0	The counter to record the current write address 2'b00: the current write address is the 1st 2'b01: the current write address is the 2nd 2'b10: the current write address is the 3rd	

Register::IN1_SDR_STATUS					0xBB
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_BLK_SEL	7:6	R	0	BLOCK_SELECT[1:0] Indicate the accessing block.	
IN1_FRZ_ON	5	R	0	FREEZE_ON 0: Capture is running 1: Freezing	
IN1_FPOL_ERR	4	R	0	Field Polarity Error (Write clear) 0: Normal 1: Field polarity error (not 0101)	
IN1_FPOL_STATUS	3:0	R	-	Field Polarity Status [3:0]	

Register::MN_PRRD_VST_H					0xBC
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	--	0	Reserved	
MN_PRRD_VST_H	2:0	R/W	0	MAIN_PRE_READ_V_START [10:8] Vertical start line of MAIN to pre-read input data. (total 11-bits)	

Register::MN_PRRD_VST_L					0xBD
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_PRRD_VST_L	7:0	R/W	2	MAIN_PRE_READ_V_START [7:0] Vertical start line of MAIN to pre-read input data. (total 11-bits)	

- Display FIFO starts to check FRC (DB_Status) and read-in data.
- Set the n-th DHS as pre-read timing, where n = pre-read [10:0].

Register::MN_PXL_NUM_H					0xBE
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_MADR_TOG_MUL	7:4	R/W	0	MAIN_MADR_TOG_MUL[3:0] Multiple of hardware auto toggle among three initial read address, it is (N/M - 1)	
MN_PXL_NUM_H	3:0	R/W	0	MAIN_PIXEL_NUM [11:8] Pixel number of one line, for FIFO to clear	

				garbage from capture side. (Equal to the length after scale-down). (total 11-bits)	
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Register::MN_PXL_NUM_L					0xBF
Name	Bits	Read/Write	Reset State	Comments	Config
MN_PXL_NUM_L	7:0	R/W	0	MAIN_PIXEL_NUM [7:0] Pixel number of one line, for FIFO to clear garbage from capture side. (Equal to the length after scale-down). (total 11-bits)	

Register::MN_WTLVL					0xC0
Name	Bits	Read/Write	Reset State	Comments	Config
MN_WTLVL	7:0	R/W	0	MAIN_WTLVL [7:0] When FIFO depth is under WTLVL, FIFO requests data.	

- One line data / 64 = ((NUM*LEN) + REM).

Register:: MN_MADDR_TOG_CTL					0xC1
Name	Bits	Read/Write	Reset State	Comments	Config
MN_MADR_TOG_Rem	7:5	R/W	0	MAIN_MADR_TOG_Rem[10:8] Remain of hardware auto toggle among three initial read address, and it is (N%M)/N * 2^10.(11bit in total)	
MN_MADR_TOG_EN	4	R/W	0	Hardware auto toggle among three initial read address: 1'b0: disable 1'b1: enable	
MN_MADR_SEL	3:2	R/W	0	Three initial read address access port(0xC6&0xC7&0xC8): 2'b00: the 1st read address 2'b01: the 2nd read address 2'b10: the 3rd read address 2'b11: reserved	
MN_MADR_CNT	1:0	R	0	The counter to record the current read address: 2'b00: the current read address is the 1st 2'b01: the current read address is the 2nd 2'b10: the current read address is the 3rd	

Register::MN_READ_NUM_H					0xC2
Name	Bits	Read/Write	Reset State	Comments	Config
MN_RD_NUM_H	7:0	R/W	0	MAIN_READ_NUM[15:8] Number of length to read from SDR in one-line.	

Register::MN_READ_NUM_L					0xC3
Name	Bits	Read/Write	Reset State	Comments	Config
MN_RD_NUM_L	7:0	R/W	0	MAIN_READ_NUM[7:0] Number of length to read from SDR in one-line.	

Register::MN_READ_LEN 0xC4					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_RD_LEN	7:0	R/W	0	MAIN_READ_LEN [7:0] The length of data to read from SDR once.	

Register::MN_READ_REMAIN 0xC5					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_RD_REMAIN	7:0	R/W	0	MAIN_READ_REMAIN [7:0] The remain part that can't be a complete length in one-line.	

- LEN must be times of 4, REM is not under this constraint but remain can't be 0

Register::MN_READ_ADDR_H 0xC6					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved	
MN_RD_ADDR_H	6:0	R/W	0	MAIN_READ_ADDR [22:16] The initial read address of SDR. (total 23-bits)	

Register::MN_READ_ADDR_M 0xC7					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_RD_ADDR_M	7:0	R/W	0	MAIN_READ_ADDR [15:8] The initial read address of SDR. (total 23-bits)	

Register::MN_READ_ADDR_L 0xC8					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_RD_ADDR_L	7:0	R/W	0	MAIN_READ_ADDR [7:0] The initial read address of SDR. (total 23-bits)	

- Total 23 bits = Row[11:0] + Bank[1:0] + C(1) + Column(7:0)

Register::MN_LINE_STEP_H 0xC9					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
MN_LSTEP_H	5:0	R/W	0	MAIN_LINE_STEP[13:8] Line step indicates the distance between two lines. (Total 14 bits)	

Register::MN_LINE_STEP_L 0xCA					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_LSTEP_L	7:0	R/W	0	MAIN_LINE_STEP[7:0] Line step indicates the distance between two lines. (Total 14 bits)	

- Line step total 14 bits[13:0] = one more row[2:0] + bank[1:0] + C(1) + Column [7:0]

- Line step = horizontal pixel bits /"32"

Sdr addr = {row[11:0], bank[1], bank[0], col[8], col[7:0]}

If SDR is 256-column(page4-0xA4[5]==0), Col[8] of line step or block step is useless

If SDR is 2-bank(page4-0xA5[5]==1), Bank[1] of line step or block step is useless

Register::MN_BLOCK_STEP_H _Row					0xCB
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_MADR_TOG_S HIFT	7:4	R/W	0	MAIN_MADR_TOG_SHIFT [3:0] IVS to DVS shift value for hardware auto toggle among three initial read address.	
MN_BSTEP_H_ROW	3:0	R/W	0	MAIN_BLOCK_STEP [22:19] Row address of block step: the distance between two blocks of SDR. (total 23-bits)	

Register::MN_BLOCK_STEP_L_Row					0xCC
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_BSTEP_L_ROW	7:0	R/W	0	MAIN_BLOCK_STEP [18:11] Row address of block step: the distance between two blocks of SDR. (total 23-bits)	

- Use it to identify max. 4 blocks for merge.
- Block step[22:0] = 12bit row address[22:11]+2bit bank address[10:9]+9bit column address[8:0]

Register::MN_LINE_NUM_H					0xCD
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
Zero	5	--	0	Useless, Must set to 0	
MN_FRAME_MD	4	R/W	1	Frame Mode 0: Num*Length + Remain is line-access setting 1: Num*Length + Remain is frame-access setting Line mode: It must be used for Double buffer mode and Filed merge mode Frame mode: It only be used if the SDR is regarded as frame buffer.	
MN_LNUM_H	3:0	R/W	0	MAIN_LINE_NUMBER [11:8] The total line-number of one image. (Total 12 bits)	

Register::MN_LINE_NUM_L					0xCE
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_LNUM_L	7:0	R/W	0	MAIN_LINE_NUMBER [7:0] The total line-number of one image. (Total 12 bits)	

Register::MN_DISP_CTRL					0xCF
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_IN_FMT	7	R/W	0	Input Format (Data format in SDR) 0: 24 bits	

				1: 16 bits	
MN_DB_EN	6	R/W	0	Double Buffer Enable (Double buffer enable) 0: Disable. 1: Enable	
MN_MRG_EN	5	R/W	0	Merge Enable (Merge enable) 0: Disable 1: Enable. Worked after sync by pre-read. It must the same with source.	
MN_BLK_FREE	4	R/W	0	Block Free (when double buffer enable) 0 : Decided by FRC controller 1 : Free toggle 2 blocks	
MN_FRC_STYLE	3	R/W	0	FRC Style 0: Input slower than display. 1: Input fast than display.	
MN_SRC_SEL	2:1	R/W	10	Source Select [1:0] 00: Use information from Capture. 01: Reserved 1x: Frame-sync mode	
MN_DISP_EN	0	R/W	1	Display Enable 0: Disable function of display main. 1: Enable function of display main.	

Register::MN_SDR_STATUS					0xD0
Name	Bits	Read/Write	Reset State	Comments	Config
MN_BLK_SEL	7:6	R	0	Block Select[1:0] Indicate the accessing block.	
MN_RB_EXT	5	R/W	0	MAIN Red(Pr)/Blue(Pb) extend value (Green/Y always 0x00) 0: 0x00 1: 0x80	
MN_DBWR_EN	4	R/W	0	MAIN Double-Buffer Write Enable 0: Finish 1: Enable write-in	
Reserved	3:2	R/W	0	Reserved	
MN_IN_FMT_411	1	R/W	0	Input Format 0: 24bits or 16bits or 18bits 1: 12bits(for yuv411 mode)	
MN_IN_FMT	0	R/W	0	Input Format 0:24bits or 16bits 1:18bits(for RGB 6-bit)	

Address: D1~D5 Reserved

Register:: ADC TEST						0xD6
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:1	R/W	00	Reserved		
ADC_TEST_REQ_DISP	0	R/W	0	For ADC test usage.		

Address: D7~E2 Reserved

Register::MN_FIFO_422_SET					0xE3
Name	Bits	Read/Write	Reset State	Comments	Config

Reserved	7:3	--	0	Reserved	
FIFO_411_FMT	2	R/W	0	Output 444 Format (only work in FIFO 411 In Mode) 1'b0: Duplication Mode $Y_0U_0V_2, Y_1U_0V_2, Y_2U_0V_2, Y_3U_0V_2,$ $Y_4U_4V_6, Y_5U_4V_6, Y_6U_4V_6, Y_7U_4V_6.$ 1'b1: Interpolation Mode $Y_0U_0V_2, Y_1U_0V_2,$ $Y_2(U_0*3/4+U_4*1/4)(V_2*3/4+V_6*1/4),$ $Y_3(U_0*2/4+U_4*2/4)(V_2*2/4+V_6*2/4),$ $Y_4(U_0*1/4+U_4*3/4)(V_2*1/4+V_6*3/4),$ $Y_5U_4V_6,$ $Y_6(U_4*3/4+U_8*1/4)(V_6*3/4+V_{10}*1/4),$ $Y_7(U_4*2/4+U_8*2/4)(V_6*2/4+V_{10}*2/4).$	
FIFO_444_FMT	1:0	R/W	0	Output 444 Format (only work in FIFO 422 In Mode) 00: Duplication Mode $Y_0U_0V_0, Y_1U_0V_0, Y_2U_2V_2, Y_3U_2V_2,$ 01: Reserved 10: Interpolation Mode 1 $Y_0U_0V_0, Y_1\boxed{U_0+U_2}/2\boxed{(V_0+V_2)/2}, Y_2U_2V_2,$ $Y_3\boxed{(U_2+U_4)/2}\boxed{(V_2+V_4)/2}...$ 11: Interpolation Mode 2 $Y_0U_0V_1, Y_1\boxed{U_0+U_2}/2V_1, Y_2U_2\boxed{(V_1+V_3)/2},$ $Y_3\boxed{(U_2+U_4)/2}V_3...$ (useless)	

Register:: MN_ONEF_DHF_H 0xE4					
Name	Bits	R/W	Default	Comments	Config
MN_ONEF_EN	7	R/W	0	One frame FRC enable (not support single merge) 0: disable 1: enable	
MN_ONEF_MODE	6	R/W	0	One frame FRC mode 0: manual mode 1: auto mode	
Reserved	5:4	R/W	0	Reserved	
DHF_pro_LEN[19:16]	3:0	R/W	0	DHF or (DHF – IHF) product Length [19:16] Input faster case : DHF * Length Input slower case : (DHF – IHF) * Length	

Register:: MN_ONEF_DHF_M 0xE5					
Name	Bits	R/W	Default	Comments	Config
DHF_pro_LEN[15:8]	7:0	R/W	0	DHF or (DHF – IHF) product Length [15:8] Input faster case : DHF * Length Input slower case : (DHF – IHF) * Length	

Register:: MN_ONEF_DHF_L 0xE6					
Name	Bits	R/W	Default	Comments	Config
DHF_pro_LEN[7:0]	7:0	R/W	0	DHF or (DHF – IHF) product Length [7:0] Input faster case : DHF * Length Input slower case : (DHF – IHF) * Length	

Register:: MN_ONEF_IHF 0xE7					
Name	Bits	R/W	Default	Comments	Config
ONEF_IHF	7:0	R/W	0	One frame FRC IHF_M Assume IHF_M = 37.48KHz, if input faster, IHF_M set 38, else set 37	

Register:: MN_LINE_MAGN_L 0xE8					
Name	Bits	R/W	Default	Comments	Config
LINE_MARGIN[7:0]	7:0	R/W	0	One frame FRC line margin [7:0] (12-bit, s11.0) Auto mode : margin to avoid frame tear, range from -2048 to 2047 Manual mode : decide whether write data to SDRAM or not	

Register:: MN_ONEF_MAGN_H 0xE9					
Name	Bits	R/W	Default	Comments	Config
LINE_MARGIN[11:8]	7:4	R/W	0	One frame FRC line margin [11:8] (12-bit, s11.0) Auto mode : margin to avoid frame tear, range from -2048 to 2047 Manual mode : decide whether write data to SDRAM or not	
PRRD_MARGIN[11:8]	3:0	R/W	0	One frame FRC pre-read margin [11:8] (12-bit) Input faster case : compared with pre_cnt[11:0] Input slower case : compared with line_cnt[11:0]	

Register:: MN_PRRD_MAGN_L 0xEA					
Name	Bits	R/W	Default	Comments	Config
PRRD_MARGIN[7:0]	7:0	R/W	0	One frame FRC pre-read margin [7:0] (12-bit) Input faster case : compared with pre_cnt[11:0] Input slower case : compared with line_cnt[11:0]	

Register:: MN_BLOCK_STEP_BANK 0xEB					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:3	R/W	0	Reserved	
MN_BSTEP_BANK	2:1	R/W	0	MAIN_BLOCK_STEP [10:9] Bank address of block step: the distance between two blocks of SDR. (total 2-bits)	
MN_BSTEP_H_COL	0	R/W	0	MAIN_BLOCK_STEP [8] Column address of block step: the distance between two blocks of SDR. (total 9-bits)	

Register:: MN_BLOCK_STEP_COL 0xEC					
Name	Bits	Read/Write	Reset State	Comments	Config
MN_BSTEP_L_COL	7:0	R/W	0	MAIN_BLOCK_STEP [7:0] Column address of block step: the distance between two blocks of SDR. (total 9-bits)	

- Block step[22:0] = 12bit row address[22:11]+2bit bank address[10:9]+9bit column address[8:0]

Register:: MN_3D_FRC_CTL 0xED					
Name	Bits	R/W	Default	Comments	Config
3D_field_swap_en	7	R/W	0	3D field signal swap enable(for interlace mode) 0:disable 1:enable	
3D_field_sync_en	6	R/W	0	3D field signal sync enable(for interlace mode) 0: disable 1: enable	
LR_FLAG_SYNC_EN	5	R/W	0	LR flag signal sync enable 0 : LR flag signal sync disable 1 : LR flag signal sync enable	

SWAP_LR_FLAG	4	R/W	0	LR flag definition swap enable 0: 1'b0 means L image, 1'b1 means R image. 1: swap LR flag definition	
LR_FLAG_SYNC_SEL	3:2	R/W	0	LR flag signal sync method 00: dvs sample 01: m-domain rebuild: single buffer 10:m-domain rebuild: double buffer without dvs mask 11:m-domain rebuild:double buffer with dvs mask	
DVS_MASK_EN	1	R/W	0	dvs between L&R mask enable 0: disable 1: enable	
MN_ANAGLYPH_EN	0	R/W	0	Anaglyph glass mode enable 0:disable 1:enable	

Register:: IN1_3D_ANAGLYPH_CTL 0xEE					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	R/W	--	Reserved	
IN1_ANAGLYPH_EN	5	R/W	0	Anaglyph glass mode enable 0: disable 1: enable	
ANAGLYPH_MODE	4:3	R/W	0	Anaglyph operation mode for different format: 2'b00: color drops every line(for line interleave & line interlace & side-by-side) 2'b01: color drop every half-frame (for frame packing & top-bottom) 2'b10: color drops every frame (for frame sequential & cyberlink) 2'b11: Reserved	
ANAGLYPH_COLOR_DROP	2:0	R/W	0	Color drop combination: 3'b000:G _L B _L & R _R 3'b001:R _L B _L & G _R 3'b010:R _L G _L & B _R 3'b011:Reserved 3'b100:R _L & G _R B _R 3'b101:G _L & R _R B _R 3'b110:B _L & R _R G _R 3'b111:Reserved	

- When ANAGLYPH_COLOR_DROP bit[2] is 1'b0, 0xA9~0xAC Num/Len/Rem must be 16-bit setting, 0xEF~0xF2 Num/Len/Rem must be 8-bit setting, and when it is 1'b1, the setting should be inverse.

Register::IN1_3D_WR_NUM_H 0xEF					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_3D_WR_NUM_H	7:0	R/W	0x08	IN1_3D_WRITE_NUM[15:8] Number of length to fill in the SDR memory.	

Register:: IN1_3D_WR_NUM_L 0xF0					
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_3D_WR_NUM_L	7:0	R/W	0xFF	IN1_3D_WRITE_NUM[7:0] Number of length to fill in the SDR memory.	

Register::IN1_3D_WR_LEN 0xF1					
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Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_3D_WR_LEN	7:0	R/W	0x80	IN1_3D_WRLLEN[7:0] Length of data to fill in the SDR memory once. (unit : 64 bit)	

Register::IN1_3D_WR_REMAIN					0xF2
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_3D_WR_REMA IN	7:0	R/W	0x80	3D_WRITE_REMAIN [7:0] The remained part that can't make a complete length. (unit : 64 bit)	

- Formula : (bits of one frame or one line data) / 64 = ((NUM*LEN)+REM)
- Restriction:
 - ✓ When total data = n * 64, it must be configured to num=0, remain = n.
 - ✓ Both LEN and REM must be times of 4. REM is not necessary smaller than LEN but can't be 0.

Register::IN1_3D_LINE_STEP_H					0xF3
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
IN1_3D_LSTEP_H	5:0	R/W	0	IN1_3D_LINE_STEP[13:8] The distance between two lines of SDR. (Total 14 bits)	

Register::IN1_3D_LINE_STEP_L					0xF4
Name	Bits	Read/ Write	Reset State	Comments	Config
IN1_3D_LSTEP_L	7:0	R/W	0x00	IN1_3D_LINE_STEP[7:0] The distance between two lines of SDR. (Total 14 bits)	

- Formula : (bits of one frame or one line data) / 64 = ((NUM*LEN)+REM)
 - ✓ The new added Num/Len/Rem & linestep setting are useful only when **Anaglyph glass mode** is enable.
 - ✓ In **Anaglyph glass mode**, the old write Num/ Len/ Rem linestep setting is for L image, and the new added write Num/ Len/ Rem & linestep is for R image.

Register::MN_3D_WTLVL					0xF5
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_WTLVL	7:0	R/W	0	MAIN_3D_WTLVL[7:0] When FIFO depth is under WTLVL, FIFO requests data.	

Register::MN_3D_READ_NUM_H					0xF6
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_NUM_ H	7:0	R/W	0	MAIN_3D_READ_NUM[15:8] Number of length to read from SDR in one-line.	

Register::MN_3D_READ_NUM_L					0xF7
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Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_NUM_L	7:0	R/W	0	MAIN_3D_READ_NUM[7:0] Number of length to read from SDR in one-line.	

Register::MN_3D_READ_LEN 0xF8					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_LEN	7:0	R/W	0	MAIN_3D_READ_LEN [7:0] The length of data to read from SDR once.	

Register::MN_3D_READ_REMAIN 0xF9					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_REMAIN	7:0	R/W	0	MAIN_3D_READ_REMAIN [7:0] The remain part that can't be a complete length in one-line.	

Register::MN_3D_READ_ADDR_H 0xFA					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved	
MN_3D_RD_ADDR_H	6:0	R/W	0	MAIN_3D_READ_ADDR [22:16] The initial read address of SDR. (total 23-bits)	

Register::MN_3D_READ_ADDR_M 0xFB					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_ADDR_M	7:0	R/W	0	MAIN_3D_READ_ADDR [15:8] The initial read address of SDR. (total 23-bits)	

Register::MN_3D_READ_ADDR_L 0xFC					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_RD_ADDR_L	7:0	R/W	0	MAIN_3D_READ_ADDR [7:0] The initial read address of SDR. (total 23-bits)	

- Total 23 bits = Row[11:0] + Bank[1:0] + C(1) + Column(7:0)

Register::MN_3D_LINE_STEP_H 0xFD					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
MN_3D_LSTEP_H	5:0	R/W	0	MAIN_3D_LINE_STEP[13:8] Line step indicates the distance between two lines. (Total 14 bits)	

Register::MN_3D_LINE_STEP_L 0xFE					
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_3D_LSTEP_L	7:0	R/W	0	MAIN_3D_LINE_STEP[7:0] Line step indicates the distance between two	

			lines. (Total 14 bits)	
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- Formula : (bits of one frame or one line data) / 64 = ((NUM*LEN)+REM)
 - ✓ The new added Num/Len/Rem & linestep setting are useful only when **Anaglyph glass mode** is enable.
 - ✓ In **Anaglyph glass mode**, the old read Num/ Len/ Rem linestep setting is for L image, and the new added read Num/ Len/ Rem & linestep is for R image.
 - ✓ In **Anaglyph glass mode**, 8-bit channel waterlevel & Length must be set half of the value 16-bit channel.

Register::MN_MADDR_TOG_Rem					0xFF
Name	Bits	Read/ Write	Reset State	Comments	Config
MN_MADR_TOG_Rem	7:0	R/W	0	MAIN_MADR_TOG_Rem[7:0] Remain of hardware auto toggle among three initial read address, and it is $(N\%M)/N$ $* 2^{10}$. (11bit in total)	

Internal OSC (Page 6)

Register::OSC_TRIM_CTRL0					0xA0
Name	Bits	R/W	Default	Comments	Config
TRIM_EN	7	R/W	0x0	Trimming Enable 0: Disable 1: Enable	
TRIM_DONE	6	R	0x1	Trimming is done 0: In progress 1: Done	
TRIM_RESOLUTION	5	R/W	0x0	Trimming Counter Set (counted by Tref) 0: 1000 1: 2000(higher resolution)	
TRIM_WCNT_1ms	4	R/W	0x1	Wait time for "Initial OSC stable" 0: 1* 2^10 *Tref 1: 15* 2^10 *Tref (1ms at Tref=70ns)	
TRIM_WCNT	3:2	R/W	0x1	Wait time for trimming" 00: 1* 2^10 *Tref 01: 2* 2^10 *Tref 10: 3 * 2^10 *Tref 11: 4 * 2^10 *Tref	
IOSC_DIV	1:0	R/W	0	IOSC Divider 00: Div 1 (default) 01: Div 2 10: Div 4 11: Div 8	

Register::OSC_TRIM_CTRL1					0xA1
Name	Bits	R/W	Default	Comments	Config
TRIM_TARGET_L	7:0	R/W	0xE8	Trimming Comparison Target (default when Tref = 70ns)	

Register::OSC_TRIM_CTRL2					0xA2
Name	Bits	R/W	Default	Comments	Config
TRIM_MANUAL_EN	7	R/W	0	Trimming Manual mode Enable 0: Trimming Auto Mode 1: Trimming Manual Mode	
TRIM_LT	6	R	0	0: Trimming Counter Result more than target 1: Trimming Counter Result less than target	
TRIM_VC_RESULT	5:3	R	0	Trimming VC Result	
TRIM_MOS_RESULT	2:0	R	0	Trimming MOS Result	

Register::EMBEDDED_OSC_CTRL					0xA3
Name	Bits	R/W	Default	Comments	Config

OSC_EN	7	R/W	1	EMB OSC ENABLE, (need waiting 1ms after enable) 0: DISABLE 1: ENABLE	
OSC_AUTO	6	R/W	1	0: manual mode (by A2[5:0]) 1: auto switch to trimming result	
OSC_VR_VC	5:3	R/W	0	bit[5:3] OSC VC Tune LSB active when manual mode (bit6=0)	
OSC_VR_MOS	2:0	R/W	0x3	bit[1:0] OSC MOS Tune MSB-bit 2 is useless active when manual mode (bit6=0)	

Register:: OSC_TRIM_CNT					0xA4
Name	Bits	R/W	Default	Comments	Config
TRIM_CNT_L	7:0	R	--	Trimming Counter(Low byte), to compare with the target clock	

Register:: EMB_BGRES					0xA5
Name	Bits	R/W	Default	Comments	Config
TRIM_CNT_H	7:4	R	--	Trimming Counter(High byte), to compare with the target clock	
TRIM_TARGET_H	3:0	R/W	0x3	Trimming Comparison Target (default when Tref = 70ns)	

Register:: EMB_BGRES					0xA6
Name	Bits	R/W	Default	Comments	Config
Reversed	7:2	--	--	Reversed	
REG_EMB_BGRES[1:0]	1:0	R/W	0x0	Value of temperature factor (01 for 14.318M, 10 for 27M) 00: smallest 11: largest	

Address 0xA7 ~ 0xAF reserved

AUDIO DAC (Page 6)

Register::: BB_POWER0 0xB0					
Name	Bits	R/W	Default	Comments	Config
BB_POW_AIN	7	R/W	0	Power down control for AIN buffer (0:power down, 1:power on)	
BB_POW_AINVOL	6	R/W	0	Power down control for AIN volume control (0:power down, 1:power on)	
BB_POW_AOUT	5	R/W	0	Power down control for AOUT amplifier (0:power down, 1:power on)	
BB_POW_DAC	4	R/W	0	Power down control for DAC (0:power down, 1:power on)	
BB_POW_DACVOL	3	R/W	0	Power down control for DAC volume control (0:power down, 1:power on)	
BB_POW_DACVREF	2	R/W	0	Power down control for DAC reference voltage buffer (0:power down, 1:power on)	
BB_POW_DF2SE	1	R/W	0	Power down control for DF2SE (0:power down, 1:power on)	
BB_POW_HPOUT	0	R/W	0	Power down control for HPOUT amplifier (0:power down, 1:power on)	

Register::: BB_POWER1 0xB1					
Name	Bits	R/W	Default	Comments	Config
Rev_b1_7_3	7:3	R/W	0	Reserved	
BB_EN_AIN	2	R/W	0	Enable AIN (0:disable, 1:enable)	
BB_POW_MBIAS	1	R/W	0	Power down control for bias generator (0:power down, 1:power on)	
BB_POW_VREF	0	R/W	0	Power down control for analog ground generator (0:power down, 1:power on)	

Register::: BB_ZCD_ANA 0xB2					
Name	Bits	R/W	Default	Comments	Config
BB_MBIAS_ZCD	7:6	R/W	2	Bias current selection for zero crossing comparator (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_POW_ZCD	5	R/W	0	Power down control for all zero crossing comparator (0:power down, 1:power on)	
BB_POW_ZCDCOMP	4:1	R/W	0	Power down control for VOL zero crossing comparator (0:power down, 1:power on) (Bit 4: AINVOL_L, Bit3: AINVOL_R, Bit2: DACVOL_L, Bit1: DACVOL_R)	
EN_POCD	0	R/W	0	Not Used	

Register::: AOUT_CONTROL 0xB3					
Name	Bits	R/W	Default	Comments	Config

BB_MUTE_AOUT_L	7	R/W	1	Mute control for AOUT_L (0:unmute, 1:mute) If C2 [4]=0, write this address could be read out immediately. Else, this value would be the final volume apply value	Rport wport
BB_MUTE_AOUT_R	6	R/W	1	Mute control for AOUT_R (0:unmute, 1:mute) If C2 [4]=0, write this address could be read out immediately. Else, this value would be the final volume apply value	Rport wport
BB_MUX_AOUT	5	R/W	0	Source selection for AOUT (0:from DAC, 1:from AIN)	
BB_OUTEN_AOUT	4	R/W	0	Output enable for AOUT (0: input mode, for start up de-pop) (1: output mode, for normal operation)	
Rev_b4_3_0	3:0	R/W	0	Reserved	

P.S Before set B3[5] & B3[3], make sure C2[5] is disable.

Register:: HPOUT_CONTROL 0xB4					
Name	Bits	R/W	Default	Comments	Config
BB_MUTE_HPOUT_L	7	R/W	1	Mute control for HPOUT_L (0:unmute, 1:mute) If C2 [5]=0, write this address could be read out immediately. Else, this value would be the final volume apply value.	Rport wport
BB_MUTE_HPOUT_R	6	R/W	1	Mute control for HPOUT_R (0:unmute, 1:mute) If C2 [5]=0, write this address could be read out immediately. Else, this value would be the final volume apply value	Rport wport
BB_MUX_HPOUT	5	R/W	0	ZCD reference input for HPOUT (Should be aligned with CA) 0:from DAC 1:from AIN	
BB_OUTEN_HPOUT	4	R/W	0	Output enable for HPOUT (0: input mode, for start up de-pop) (1: output mode, for normal operation)	
Rev_b5_3_0	3:0	R/W	0	Reserved	

P.S Before set B4[5] & B4[3], make sure C2[4] is disable.

Register:: MBIAS_CONTROL0 0xB5					
Name	Bits	R/W	Default	Comments	Config
BB_MBIAS_AMP	7:6	R/W	2	Bias current selection for output amplifier (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_DACVREF	5:4	R/W	2	Bias current selection for DACVREF (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_DAOP	3:2	R/W	2	Bias current selection for DAOP (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_DAREFBUF	1:0	R/W	2	Bias current selection for DAREFBUF (00b:10u, 01b:15u, 10b:20u, 11b:30u)	

Register:: MBIAS_CONTROL1 0xB6					
Name	Bits	R/W	Default	Comments	Config

BB_MBIAS_DF2SE	7:6	R/W	2	Bias current selection for DF2SE (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_IN_MC3	5:4	R/W	2	Bias current selection for input buffer (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_VOL	3:2	R/W	2	Bias current selection for volume control (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_VREF	1:0	R/W	2	Bias current selection for analog ground generator (00b:10u, 01b:15u, 10b:20u, 11b:30u)	

Register:: VREF_CONTROL 0xB7					
Name	Bits	R/W	Default	Comments	Config
BB_VREF_VAG	7:6	R/W	1	Analog ground voltage selection (00b:1.717 ,01b:1.65, 10b:1.58, 11b:1.51)	
BB_DACVREF_MODE	5	R/W	1	DAC reference voltage source (0:internal generation, 1:external given)	
Rev_b8_4_0	4:0	R/W	0	Reserved	

Register:: DAC_VOL_L 0xB8					
Name	Bits	R/W	Default	Comments	Config
BB_DACVOL_L	7:0	R/W	0	Volume control for DAC output (00h:-58.5dB~37h:24dB) If C2 [7]=0, write this address could be read out immediately. Else, this value would be the final volume apply value. Note : double buffered by B9	Rport wport

PS. Before setting this byte, make sure corresponding “Done L” signal (C4[7]) is 1.

Register:: DAC_VOL_R 0xB9					
Name	Bits	R/W	Default	Comments	Config
BB_DACVOL_R	7:0	R/W	0	Volume control for DAC output (00h:-58.5dB~37h:24dB) If C2 [7]=0, write this address could be read out immediately. Else, this value would be the final volume apply value.	Rport wport

PS. Before setting this byte, make sure corresponding “Done L & R ” signals (C4[7:6]) are both 1.

Note: B8 value is double buffered by B9

Register:: AIN_VOL_L 0xBA					
Name	Bits	R/W	Default	Comments	Config
BB_AINVOL_L	7:0	R/W	0	Volume control for AIN (00h:-58.5dB~37h:24dB) If C2[6]=0, write this address could be read out immediately. Else, this value would be the final volume apply value. Note : double buffered by BB	Rport wport

PS. Before setting this byte, make sure corresponding “Done L” signal (C4[5]) is 1.

Register:: AIN_VOL_R 0xBB						
Name	Bits	R/W	Default	Comments	Config	
BB_AINVOL_R	7:0	R/W	0	Volume control for AIN (00h:-58.5dB~37h:24dB) If C2[6]=0, write this address could be read out immediately. Else, this value would be the final volume apply value.	Rport wport	

PS. Before setting this byte, make sure corresponding “Done L & R ” signals (C4[5:4]) are both 1.

Note: BA value is double buffered by BB

Register:: ANA_RESERVE1 0xBC						
Name	Bits	R/W	Default	Comments	Config	
BB_MUX_AOUT_L	7:6	R/W	00	Source selection for AOUT_L 00: From DAC_L 01: From DAC_R 10: From AIN_L 11: From AIN_R		
BB_MUX_AOUT_R	5:4	R/W	00	Source selection for AOUT_R 00: From DAC_R 01: From DAC_L 10: From AIN_R 11: From AIN_L		
ANA_REV1	3:2	R/W	0	reserved		
ANA_REV1	1	R/W	0	0: As depop power down, ramp switch OFF 1: As depop power down, ramp switch ON		
BB_IMP_SEL<0>	0	R/W	0	It is only used in tradition de-pop mode (input mode, then output mode.) (According the value of external de-coupling capacitor , set different input impedance) 0: input impedance is 0.5K ohms. 1: input impedance is 3.5K ohms.		

Register:: ANA_RESERVE2 0xBD						
Name	Bits	R/W	Default	Comments	Config	
ANA_REV2	7:0	R/W	0	reserved		

POWER_OFF Region

Register:: MODULATOR_CONTROL 0xBE						
Name	Bits	R/W	Default	Comments	Config	
BB_MOD_CLK_RATE	7:6	R/W	00	00:mclk(256fs) 01:aclk(128fs) 10:sclk(64fs)	Rport Wport	
BB_MOD_RST_N	5	R/W	1	for second time to reset sigma-delta modulator(after reset up sample filter about 22*(1/fs)) 0: Reset 1: No Reset		

BB_DEBUG_EN	4	R/W	0	Debug Mode Enable 1:Enable 0:Disable	
BB_DEBUG_MODE	3:1	R/W	0	Support 8 sets debug mode.	
BB_OUT_L_R_SEL	0	R/W	0	Debug Mode, Adding L or R output 16bits in digital function 0: L 1: R	

POWER_OFF Region

Register::: BIST_CONTROL 0xBF					
Name	Bits	R/W	Default	Comments	Config
BB_BIST_MODE	7	R/W	0	1: Enable 0: Disable	
BB_BIST_RST_N	6	R/W	1	0: Reset 1: No Reset	
BB_BIST_DONE	5	R	0	1: BIST is done 0: BIST running	
BB_BIST_FAIL	4	R	0	1: SRAM fail 0: SRAM ok	
BB_FT_EN	3	R/W	0	For FT and test performance . 1: Input PCM data from test pin in. 0: PCM data from digital circuit.	
BB_48PIN_MODE	2	R/W	0	1:16bits TEST IN (PCM DATA). 0:22bits TEST IN. (PCM DATA)	
SDM_OUT_TEST_EN	1	R/W	0	SDM test enable. When set to 1, the DAC input will be forced SDM_OUT_TEST_VALUE	
HPF_EN	0	R/W	1	High pass filter enable. 1 : Enable 0 : Disable	

POWER_OFF Region

Register::: SDM_OUT_VALUE_MSB 0xC0					
Name	Bits	R/W	Default	Comments	Config
SDM_OUT_TEST_VALUE[15:8]	7:0	R/W	0xAA	Active when BF[1] = 1 , for verify	

POWER_OFF Region

Register::: SDM_OUT_VALUE_LSB 0xC1					
Name	Bits	R/W	Default	Comments	Config
SDM_OUT_TEST_VALUE[7:0]	7:0	R/W	0xAA	Active when BF[1] = 1 , for verify	

Register::: ZERO_CROSSING_CTRL 0xC2					
Name	Bits	R/W	Default	Comments	Config

ZCD_DAC_VOL_EN	7	R/W	1	DAC 1:Volume control by zero crossing enable 0: disable	
ZCD_AIN_VOL_EN	6	R/W	1	AIN 1:Volume control by zero crossing enable 0: disable	
ZCD_HPOUT_MUTE_EN	5	R/W	0	Head phone Including un-mute and mute 1:mute control by zero crossing enable 0:disable	
ZCD_AOUT_MUTE_EN	4	R/W	0	Speaker Including un-mute and mute 1:mute control by zero crossing enable 0:disable	
ZCD_DAC_VOL_SEP	3	R/W	1	DAC volume 1: LR controlled separately 0: LR controlled volume at the same time (if L or R encounter zero crossing, apply volume/mute to another one)	
ZCD_AIN_VOL_SEP	2	R/W	1	Ain volume 1: LR controlled separately 0: LR controlled volume at the same time (if L or R encounter zero crossing, apply volume/mute to another one)	
ZCD_HP_MUTE_SEP	1	R/W	1	Head phone mute 1: LR controlled separately 0: LR controlled volume at the same time (if L or R encounter zero crossing, apply volume/mute to another one)	
ZCD_AOUT_MUTE_SEP	0	R/W	1	Speaker mute 1: LR controlled separately 0: LR controlled volume at the same time (if L or R encounter zero crossing, apply volume/mute to another one)	

Register:: ZCD_TIMEOUT 0xC3					
Name	Bits	R/W	Default	Comments	Config
ZCD_TEST_INPUT	7	R/W	0	Test input. When F7[4] is 1, the input square wave will be switched to this register bit.	
ZCD_TIMEOUT	6:0	R/W	3	Setting range 0~7E Clock_base is xtal * 512 = 35.84us Timeout target is clock_base*{(ZCD_TIMEOUT+1),3'b0}	

Register:: ZCD_STATUS 0xC4					
Name	Bits	R/W	Default	Comments	Config
ZCD_DAC_L_VOL_DONE	7	R	1	Active when ZCD_DAC_VOL_EN = 1	
ZCD_DAC_R_VOL_DONE	6	R	1	Active when ZCD_DAC_VOL_EN = 1	
ZCD_AIN_L_VOL_DONE	5	R	1	Active whe ZCD_AIN_VOL_EN = 1	
ZCD_AIN_R_VOL_DONE	4	R	1	Active whe ZCD_AIN_VOL_EN = 1	

ZCD_HPOUT_L_MUTE_DONE	3	R	1	Active when ZCD_HPOUT_MUTE_EN = 1	
ZCD_HPOUT_R_MUTE_DONE	2	R	1	Active when ZCD_HPOUT_MUTE_EN = 1	
ZCD_AOUT_L_MUTE_DONE	1	R	1	Active whe ZCD_AOUT_MUTE_EN = 1	
ZCD_AOUT_R_MUTE_DONE	0	R	1	Active whe ZCD_AOUT_MUTE _EN = 1	

POWER_OFF Region

Register::: DIG_RESERVE1 0xC5					
Name	Bits	R/W	Default	Comments	Config
DIG_REV1	7:0	R/W	0	reserved	

POWER_OFF Region

Register::: DIG_RESERVE2 0xC6					
Name	Bits	R/W	Default	Comments	Config
DA_CLK_EN	7	R/W	1	da_clk enable.	
DIG_REV2	6:0	R/W	3F	reserved	

POWER_OFF Region

Register::: DIG_RESERVE_RONLY 0xC7					
Name	Bits	R/W	Default	Comments	Config
DIG_REV3	7:0	R	0	reserved	

Register:::DEPOP_CTRL0 0xC8					
Name	Bits	R/W	Default	Comments	Config
BB_POW_DEPOP	7	R/W	0	Power down control for De-pop (0:power down, 1:power on)	
BB_POW_DEPOP_CORE	6	R/W	0	Power down control for De-pop Core (0:power down, 1:power on)	
BB_POW_DEPOP_OP	5	R/W	0	Power down control for De-pop OP (0:power down, 1:power on)	
BB_POW_DEPOP_CKGEN	4	R/W	0	Power down control for De-pop CKGEN (0:power down, 1:power on)	
BB_EN_AOUT_NORM	3	R/W	0	Transfer De-pop mode to AOUT normal operation mode. 0: disable 1: Normal operation mode.	
BB_EN_INEN_AOUT	2	R/W	0	Enable input mode at AOUT 0 Disable 1: Enable input mode.	
BB_EN_AOUT_COPY[1:0]	1:0	R/W	0	Select Channel of AOUT 00b: Normal Stereo <Default>	

				01b: Normal Stereo 10b: L copy to R 11b: R copy to L	
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Register::DEPOP_CTRL1 0xC9					
Name	Bits	R/W	Default	Comments	Config
BB_EN_AMP	7	R/W	0	Enable HPOUT AMP 0: disable(10k loading) 1: enable(32 loading)	
BB_EN_HP_NORM	6	R/W	0	Transfer De-pop mode to HPOUT normal operation mode. 0: disable 1: Normal operation mode.	
BB_EN_INEN_HPOUT	5	R/W	0	Enable input mode at HPOUT 0 Disable 1: Enable input mode.	
BB_EN_HPOUT_COPY[1:0]	4:3	R/W	0	Select Channel of HPOUT <u>(NO USE)</u> 00b: Normal Stereo <u><Default></u> 01b: Normal Stereo 10b: L copy to R 11b: R copy to L	
Reserved	2:0	R/W	0	Reserved to 0	

Register::DEPOP_CTRL2 0xCA					
Name	Bits	R/W	Default	Comments	Config
BB_MUX_HPOUT_L[3:0]	7:4	R/W	0	Source selection for HPOUT_L 1110: From DAC_L 1101: From AIN_L 1011: From DAC_R 0111: From AIN_R	
BB_MUX_HPOUT_R[3:0]	3:0	R/W	0	Source selection for HPOUT_R 1110: From DAC_R 1101: From AIN_R 1011: From DAC_L 0111: From AIN_L	

Register::DEPOP_CTRL4 0xCB					
Name	Bits	R/W	Default	Comments	Config
BB_MBIAS_DEPOP[1:0]	7:6	R/W	2	Bias current selection for DEPOP (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_DEPOP_OP1[1:0]	5:4	R/W	2	Bias current selection for DEPOP OP1 (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_MBIAS_DEPOP_OP2[1:0]	3:2	R/W	2	Bias current selection for DEPOP OP2 (00b:10u, 01b:15u, 10b:20u, 11b:30u)	
BB_VCM_READY	1	R/W	0	When VCM is charged to (AVDD/2), REG_BB_VCM_READY changes from L to H.	
Reserved	0	R/W	0	Reserved to 0	

Register::DEPOP_CTRL5 0xCC						
Name	Bits	R/W	Default	Comments	Config	
BB_DEPOP_SEL[1:0]	7:6	R/W	1	De-pop type selection 00: DEPOP1-original 01: DEPOP2-cap(Default) 10: DEPOP3-cap 11: DEPOP4-cap - high impedance		
BB_DEPOP_CUR_SEL[2:0]	5:3	R/W	2	Select the current at charge pump of the ramp wave generator. 000: 0.3125uA 001: 0.625uA 010: 1.25uA (Default) 011: 2.5uA 100: 5uA 101: 10uA		
BB_DEPOP_CAP_SEL[1:0]	2:1	R/W	3	Select the capacitor at charge pump of the ramp wave generator. 00: 6pF+6pF 01: 12pF+24pF 10: 18pF+24pF 11: 24pF+24pF (Default)		
Reserved	0	R/W	0	Reserved to 0		

Register::DEPOP_CTRL6 0xCD							
Name	Bits	R/W	Default	Comments	Config		
DEPOP_CK_DIV	7:4	R/W	0x4	Clock to De-pop circuit (14.318M / 64) 0000: 14.318MHz/64 = 223kHz 0001: 14.318MHz/128 = 111kHz 0010: 14.318MHz/256 = 55.75kHz (transition time=100ms) 0011: 14.318MHz/512 = 27.875kHz 0100: 14.318MHz/1024 = 13.9kHz (Default) 0101: 14.318MHz/2048 = 6.97kHz 0110: 14.318MHz/4096 = 3.48kHz (transition time=400ms) 0111: 14.318MHz/8192 = 1.74kHz 1000: 14.318MHz/16384 = 0.87kHz 1001: 14.318MHz/32768 = 0.435kHz			
DEPOP_CK_EN	3	R/W	0	Depop clock enable			
Reserved	2:0	R/W	0	Reserved to 0			

POWER_OFF Region

Register::LFSR_CTRL 0xCE						
Name	Bits	R/W	Default	Comments	Config	
LFSR_EN	7	R/W	0	24-bit LFSR (Random generator) in SDM input 1: enable 0: output -> all "1'b1"		

BIT2_LFSR_EN	6	R/W	0	1:SDM input[2] replaced by LFSR[23] 0:orginal input	
BIT1_LFSR_EN	5	R/W	0	1:SDM input[1] replaced by LFSR[15] 0:orginal input	
BIT0_LFSR_EN	4	R/W	0	1:SDM input[0] replaced by LFSR[7] 0:orginal input	
SMPL_LFSR_EN	3	R/W	0	24-bit LFSR in DAC input 1: enable 0: output -> all "1'b1"	
SMPL_BIT2_LFSR_EN	2	R/W	0	1:DAC input[2] replaced by LFSR[23] 0:orginal input	
SMPL_BIT1_LFSR_EN	1	R/W	0	1:DAC input[1] replaced by LFSR[15] 0:orginal input	
SMPL_BIT0_LFSR_EN	0	R/W	0	1:DAC input[0] replaced by LFSR[7] 0:orginal input	

Register::AUDIO_RES 0xCF					
Name	Bits	R/W	Default	Comments	Config
AUDIO_RES	7:0	R/W	0xF0	ANALOG reserved	

Vivid color-DCC (Page 7)

Register:: DCC_CTRL_0					0xc7	
Name	Bits	R/W	Default	Comments	Config	
DCC_EN	7	R/W	0	DCC_ENABLE 0: Disable 1: Enable		
Y_FORMULA	6	R/W	0	Y_FORMULA 0: Y = (2R+5G+B)/8 1: Y = (5R+8G+3B)/16		
SC_EN	5	R/W	0	SOFT_CLAMP 0: Disable 1: Enable		
DCC_MODE	4	R/W	0	DCC_MODE 0: Auto Mode 1: Manual Mode		
SCG_EN	3	R/W	0	SCENE_CHANGE 0: Disable Scene-Change Function 1: Enable Scene-Change Function in Auto Mode		
BWL_EXP	2	R/W	0	BWL_EXP 0: Disable Black/White Level Expansion 1: Enable Black/White Level Expansion in Auto Mode		
PAGE_SEL	1:0	R/W	0	DCC_PAGE_SEL 00: Page 0 (for Histogram / Ymin-max / Soft-Clamping / Scene-Change) 01: Page 1 (for Y-Curve / WBL Expansion) 10: Page 2 (for Calculation Parameter) 11: Page 3 (for Testing and Debug)		

Register:: DCC_CTRL_1					0xc8	
Name	Bits	R/W	Default	Comments	Config	
GAIN_EN	7	R/W	0	DCC gain control enable 0: Disable 1: Enable Note: DCC gain control enable must delay MOV_AVG_LEN frame after DCC enable.		
DCC_FLAG	6	R	0	1: time to write highlight window position & normalized factor, write to clear		
SAT_COMP_EN	5	R/W	0	Saturation Compensation Enable 0: Disable 1: Enable		
BLD_MODE	4	R/W	0	Blending Factor Control Mode 0: old mode 1: new mode (diff. regions have diff. blending factor)		
Reserved	3:0	--	0x00	Reserved to 0		

Register:: DCC Address Port					0xc9	
Name	Bits	R/W	Default	Comments	Config	
DCC_ADDR	7:0	R/W	0x00	DCC address		

Register:: DCC Data Port					0xca	
Name	Bits	R/W	Default	Comments	Config	
DCC_DATA	7:0	R/W	0x00	DCC data		

Register:: NOR_FACTOR_H (page0) (ACCESS[C9,CA])					0x00	
Name	Bits	R/W	Default	Comments	Config	
Reserved	7:6	--	--	Reserved		
NOR_FAC_H	5:0	R/W	0x00	Bit[21:16] of Normalized Factor; NF=(255/N)*(2^22)		

Register:: NOR_FACTOR_M (page0) (ACCESS[C9,CA]) 0x01				
Name	Bits	R/W	Default	Comments
NOR_FAC_M	7:0	R/W	0x00	Bit[15:8] of Normalized Factor; NF=(255/N)*(2^22)

Register:: NOR_FACTOR_L (page0) (ACCESS[C9,CA]) 0x02				
Name	Bits	R/W	Default	Comments
NOR_FAC_L	7:0	R/W	0x00	Bit[7:0] of Normalized Factor; NF=(255/N)*(2^22)

Register:: BBE_CTRL (page0) (ACCESS[C9,CA]) 0x03				
Name	Bits	R/W	Default	Comments
BBE_EN	7	R/W	0	BBE_ENA 0: Disable Black-Background Exception 1: Enable Black-Background Exception
Reserved	6:4	--	--	Reserved
BBE_THD	3:0	R/W	0x4	BBE_THD 8-bit RGB Threshold for Black-Background Exception

Register:: NFLT_CTRL (page0) (ACCESS[C9,CA]) 0x04				
Name	Bits	R/W	Default	Comments
HNFLT_EN	7	R/W	0	HNFLT_ENA 0: Disable Histogram Noise Filter 1: Enable Histogram Noise Filter
HNFLT_THD	6:4	R/W	0	HNFLT_THD Threshold for Histogram Noise Filter
YNFLT_EN	3	R/W	0	YNFLT_ENA 0: Disable Ymax / Ymin Noise Filter 1: Enable Ymax / Ymin Noise Filter
YNFLT_THD	2:0	R/W	0	YNFLT_THD Threshold for Ymax/Ymin Noise Filter (= 4*YNFLT_THD)

Register:: HIST_CTRL (page0) (ACCESS[C9,CA]) 0x05				
Name	Bits	R/W	Default	Comments
RH0_LIMITER	7	R/W	0	RH0_LIMITER 0: Disable RH0 Limiter 1: Enable RH0 Limiter
RH1_LIMITER	6	R/W	0	RH1_LIMITER 0: Disable RH1 Limiter 1: Enable RH1 Limiter
REAL_MA_LEN	5:3	R	--	Real MOV_AVG_LEN may be different with MOV_AVG_LEN, if SCG enable
MOV_AVG_LEN	2:0	R/W	0	MOV_AVG_LEN 000: Histogram Moving Average Length = 1 001: Histogram Moving Average Length = 2 010: Histogram Moving Average Length = 4 011: Histogram Moving Average Length = 8 100: Histogram Moving Average Length = 16 101~111: reserved

Register:: SOFT_CLAMP (page0) (ACCESS[C9,CA]) 0x06				
Name	Bits	R/W	Default	Comments
SOFT_CLAMP	7:0	R/W	0xB0	Slope of Soft-Clamping (= SOFT_CLAMP / 256)

Register:: Y_MAX_LB (page0) (ACCESS[C9,CA]) 0x07				
Name	Bits	R/W	Default	Comments
Y_MAX_LB	7:0	R/W	0xFF	Lower Bound of Y_MAX (= 4*Y_MAX_LB)

Register:: Y_MIN_HB (page0) (ACCESS[C9,CA]) 0x08					
Name	Bits	R/W	Default	Comments	Config
Y_MIN_HB	7:0	R/W	0x00	Higher Bound of Y_MIN (= 4*Y_MIN_HB)	

Register:: SCG_PERIOD (page0) (ACCESS[C9,CA]) 0x09					
Name	Bits	R/W	Default	Comments	Config
SCG_MODE	7	R/W	0	Scene-Change Control Mode 0: old mode (2553V) 1: new mode (2622)	
Reserved	6:5	--	--	Reserved	
SCG_PERIOD	4:0	R/W	0x10	Scene-Change Mode Period = 1~32. Note: SCG_PERIOD >= MOV_AVG_LEN, CRED-05[2:0](page0)	

Register:: SCG_LB (page0) (ACCESS[C9,CA]) 0x0A					
Name	Bits	R/W	Default	Comments	Config
SCG_LB	7:0	R/W	0x00	SCG_DIFF Lower Bound for Exiting Scene-Change Mode	

Register:: SCG_HB (page0) (ACCESS[C9,CA]) 0x0B					
Name	Bits	R/W	Default	Comments	Config
SCG_HB	7:0	R/W	0xFF	SCG_DIFF Higher Bound for Exiting Scene-Change Mode	

Register:: POPUP_CTRL (page0) (ACCESS[C9,CA]) 0x0C					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	--	Reserved	
POPUP_BIT	0	R	--	Reg[0D]~Reg[16] are updated every frame. Once POPUP_BIT is read, the value of Reg[0D] ~ Reg[16] will not be updated until Reg[16] is read.	

Register:: SCG_DIFF (page0) (ACCESS[C9,CA]) 0x0D					
Name	Bits	R/W	Default	Comments	Config
SCG_DIFF	7:0	R	--	= (Histogram Difference between Current Frame and Average) / 8	

Register:: Y_MAX_VAL (page0) (ACCESS[C9,CA]) 0x0E					
Name	Bits	R/W	Default	Comments	Config
Y_MAX_VAL	7:0	R	--	= Max { Y_MAX_LB, (Y Maximum in Current Frame / 4) }	

Register:: Y_MIN_VAL (page0) (ACCESS[C9,CA]) 0x0F					
Name	Bits	R/W	Default	Comments	Config
Y_MIN_VAL	7:0	R	--	= Min { Y_MIN_HB, (Y Minimum in Current Frame / 4) }	

Register:: S0_VALUE (page0) (ACCESS[C9,CA]) 0x10					
Name	Bits	R/W	Default	Comments	Config
S0_VALUE	7:0	R	--	Normalized Histogram S0 Value	

Register:: S1_VALUE (page0) (ACCESS[C9,CA]) 0x11					
Name	Bits	R/W	Default	Comments	Config
S1_VALUE	7:0	R	--	Normalized Histogram S1 Value	

Register:: S2_VALUE (page0) (ACCESS[C9,CA]) 0x12					
Name	Bits	R/W	Default	Comments	Config
S2_VALUE	7:0	R	--	Normalized Histogram S2 Value	

Register:: S3_VALUE (page0) (ACCESS[C9,CA]) 0x13				
--	--	--	--	--



Name	Bits	R/W	Default	Comments	Config
S3_VALUE	7:0	R	--	Normalized Histogram S3 Value	

Register:: S4_VALUE (page0) (ACCESS[C9,CA]) 0x14					
Name	Bits	R/W	Default	Comments	Config
S4_VALUE	7:0	R	--	Normalized Histogram S4 Value	

Register:: S5_VALUE (page0) (ACCESS[C9,CA]) 0x15					
Name	Bits	R/W	Default	Comments	Config
S5_VALUE	7:0	R	--	Normalized Histogram S5 Value	

Register:: S6_VALUE (page0) (ACCESS[C9,CA]) 0x16					
Name	Bits	R/W	Default	Comments	Config
S6_VALUE	7:0	R	--	Normalized Histogram S6 Value	

Register:: YHL_THD (page0) (ACCESS[C9,CA]) 0x17					
Name	Bits	R/W	Default	Comments	Config
YHL_THD	7:0	R/W	0x00	Y_H and Y_L Threshold When DIFF[10:0] < YHL_THD[7:0], Y_H and Y_L keep the previous values	

Register:: DEF_CRV[01] (page1) (ACCESS[C9,CA]) 0x00					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV01	7:0	R/W	0x10	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[02] (page1) (ACCESS[C9,CA]) 0x01					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV02	7:0	R/W	0x20	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[03] (page1) (ACCESS[C9,CA]) 0x02					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV03	7:0	R/W	0x30	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[04] (page1) (ACCESS[C9,CA]) 0x03					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV04	7:0	R/W	0x40	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[05] (page1) (ACCESS[C9,CA]) 0x04					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV05	7:0	R/W	0x50	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[06] (page1) (ACCESS[C9,CA]) 0x05					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV06	7:0	R/W	0x60	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[07] (page1) (ACCESS[C9,CA]) 0x06					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV07	7:0	R/W	0x70	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[08] (page1) (ACCESS[C9,CA]) 0x07					
Name	Bits	R/W	Default	Comments	Config
DEF_CRV08	7:0	R/W	0x80	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]	

Register:: DEF_CRV[09] (page1) (ACCESS[C9,CA]) 0x08				
Name	Bits	R/W	Default	Comments
DEF_CRV09	7:0	R/W	0x90	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[10] (page1) (ACCESS[C9,CA]) 0x09				
Name	Bits	R/W	Default	Comments
DEF_CRV10	7:0	R/W	0xA0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[11] (page1) (ACCESS[C9,CA]) 0x0A				
Name	Bits	R/W	Default	Comments
DEF_CRV11	7:0	R/W	0xB0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[12] (page1) (ACCESS[C9,CA]) 0x0B				
Name	Bits	R/W	Default	Comments
DEF_CRV12	7:0	R/W	0xC0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[13] (page1) (ACCESS[C9,CA]) 0x0C				
Name	Bits	R/W	Default	Comments
DEF_CRV13	7:0	R/W	0xD0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[14] (page1) (ACCESS[C9,CA]) 0x0D				
Name	Bits	R/W	Default	Comments
DEF_CRV14	7:0	R/W	0xE0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[15] (page1) (ACCESS[C9,CA]) 0x0E				
Name	Bits	R/W	Default	Comments
DEF_CRV15	7:0	R/W	0xF0	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1]

Register:: DEF_CRV[16] (page1) (ACCESS[C9,CA]) 0x0F				
Name	Bits	R/W	Default	Comments
DEF_CRV16	7:0	R/W	0x00	Pre-Defined Y-Curve; Keep DEF_CRV[N] ≥ DEF_CRV[N-1] Note : default = 0x00 means 0x100 (256)

When y-curve boundary is changed (DEF_CRV[16] != 0x00), disable histogram noise filter.

Registers below is effective only when auto mode is disable and black/white level expansion is enabled.
When auto mode is enabled (DCC_MODE=0), Y_BL_BIAS and Y_WL_BIAS are read-only.

Register:: Y_BL_BIAS (page1) (ACCESS[C9,CA]) 0x10				
Name	Bits	R/W	Default	Comments
Y_BL_BIAS	7:0	R/W	0x00	Y Offset for Black-Level Expansion (Y_L' = 4*Y_BL_BIAS)

Register:: Y_WL_BIAS (page1) (ACCESS[C9,CA]) 0x11				
Name	Bits	R/W	Default	Comments
Y_WL_BIAS	7:0	R/W	0x00	Y Offset for While-Level Expansion (1023-Y_H' = 4*Y_WL_BIAS)

Load double buffer CRED-00 ~ CRED-11 (page1) after write CRED-11 when DCC enable

Register:: SAT_FACTOR (page1) (ACCESS[C9,CA]) 0x12				
Name	Bits	R/W	Default	Comments
Reserved	7:6	--	--	Reserved
SAT_FACTOR	5:0	R/W	0x00	Saturation Compensation Factor = 0 ~ 32.

Registers below is effective only when auto mode is enabled.
In manual mode (DCC_MODE=1), BLD_VAL will be fixed to 0. It means Y-curve is fully determined by DEF_CUR[01~15]

Register:: BLD_UB (page1) (ACCESS[C9,CA]) 0x13					
Name	Bits	R/W	Default	Comments	Config
BLD_UB	7:0	R/W	0x00	Upper Bound of Blending Factor	

Register:: BLD_LB (page1) (ACCESS[C9,CA]) 0x14					
Name	Bits	R/W	Default	Comments	Config
BLD_LB	7:0	R/W	0x00	Lower Bound of Blending Factor	

Register:: DEV_FACTOR (page1) (ACCESS[C9,CA]) 0x15					
Name	Bits	R/W	Default	Comments	Config
DEV_FACTOR	7:0	R/W	0x00	Deviation Weighting Factor	

Register:: BLD_VAL_SEL (page1) (ACCESS[C9,CA]) 0x16					
Name	Bits	R/W	Default	Comments	Config
WL_RANGE	7:6	R/W	0x00	White-Level Range 00: Yi = 512 (Z8) 01: Yi = 576 (Z9) 10: Yi = 640 (Z10) 11: Yi = 704 (Z11)	
WL_BLD_VAL	5:4	R/W	0x00	White-Level Blending Factor 00: 0 (user-defined curve) 01: R/2 10: R 11: 2R	
BL_RANGE	3:2	R/W	0x00	Black-Level Range 00: Yi = 448 (Z7) 01: Yi = 384 (Z6) 10: Yi = 320 (Z5) 11: Yi = 256 (Z4)	
BL_BLD_VAL	1:0	R/W	0x00	Black-Level Blending Factor 00: 0 (user-defined curve) 01: R/2 10: R 11: 2R	

Register:: BLD_VAL (page1) (ACCESS[C9,CA]) 0x17					
Name	Bits	R/W	Default	Comments	Config
BLD_VAL	7:0	R	--	= Max{ BLD_UB - [(DEV_VAL*DEV_FACTOR)/256], BLD_LB}	

Register:: DEV_VAL_HI (page1) (ACCESS[C9,CA]) 0x18					
Name	Bits	R/W	Default	Comments	Config
DEV_VAL_HI	7:0	R	--	Bit[8:1] of Deviation Value	

Register:: DEV_VAL_LO (page1) (ACCESS[C9,CA]) 0x19					
Name	Bits	R/W	Default	Comments	Config
DEV_VAL_LO	7	R	--	Bit[0] of Deviation Value	
Reserved	6:0	--	--	Reserved	

Register:: SRAM initial value (page2) (ACCESS[C9,CA]) 0x00-0x8F					
Name	Bits	R/W	Default	Comments	Config
SRAM_XX	7:0	W	--	Addr 00: SRAM_00 Addr 01: SRAM_01 Addr 8F : SRAM_8F	

Register::: SRAM_BIST (page3)					(ACCESS[C9,CA]) 0x00
Name	Bits	R/W	Default	Comments	Config
BIST_EN	7	R/W	0	BIST_EN 0: disable 1: enable	
RAM_Mode	6	R/W	0	RAM_Mode 0: dclk domain mode (normal mode, BIST) 1: MCU domain mode (SCG test)	
Reserved	5:2	--	--	Reserved	
BIST_PERIOD	1	R	--	BIST_Period 0: BIST is done 1: BIST is running	
BIST_OK	0	R	--	BIST_OK 0: SRAM fail 1: SRAM ok	

Address:CB~CF reserved

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ICM(Page 7)

Register:: ICM_CONTROL					0xD0
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_acm_enable	7	R/W	0	ICM Enable 0: Disable (Default) 1: Enable	
Reg_rgb2y_mode	6	R/W	0	Y Correction Mode 0: $dY = (8dU+dV)/8$ 1: $dY = (6dU+dV)/8$	
Reg_uv_off_range	5	R/W	0	ICM U/V Delta Range: 0: Original -128~+127 1: Double -256~254	
Reg_cm0_enable	4	R/W	0	CM0 Enable 0: Disable 1: Enable	
Reg_cm1_enable	3	R/W	0	CM1 Enable 0: Disable 1: Enable	
Reg_cm2_enable	2	R/W	0	CM2 Enable 0: Disable 1: Enable	
Reg_cm3_enable	1	R/W	0	CM3 Enable 0: Disable 1: Enable	
Reg_cm4_enable	0	R/W	0	CM4 Enable 0: Disable 1: Enable	

Register:: ICM_SEL					0xD1
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_acm_test_mode	7:5	R/W	0	ICM Test Mode 000: Disable 001: Bypass U, V result 010: Bypass hue/saturation result 011: Bypass dU, dV value 1xx: R,B as LUT input, and bypass LUT output to R/G/B output	
Reg_4x_delta	4	R/W	0	delta U/V range extend 0: Delta U/V x1 (default) 1: Delta U/V x4	
Reg_cm5_enable	3	R/W	0	CM5 Enable 0: Disable 1: Enable	
Reg_cm_select	2:0	R/W	0	CM Select 000: Select Chroma Modifier 0 for Accessing Through Data Port 001: Select Chroma Modifier 1 for Accessing Through Data Port 010: Select Chroma Modifier 2 for Accessing Through Data Port 011: Select Chroma Modifier 3 for Accessing Through Data Port 100: Select Chroma Modifier 4 for Accessing Through Data Port 101: Select Chroma Modifier 5 for Accessing Through Data Port 110~111: Reserved	

Register::ICM_ADDR					0xD2
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_neg_comp_en	7	R/W	0	Negative Compensate Enable	

				0: Disable 1: Enable Negative Compensate is valid only when Max value Compensate is disable (0xD4[0] = 0).	
Icm_addr	6:0	R/W	0	ICM port address	

Register:::ICM_DATA 0xD3					
Name	Bits	Read/ Write	Reset State	Comments	Config
Icm_data	7:0	R/W	0	ICM port data	

ICM_ADDR will be increased automatically after each byte of ICM_DATA has been accessed.

Register::: icm_cmn_mst_hue_HB 0xD3-00					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_mst_hue[11:8]	3:0	R/W	0	High Byte[11:8] of Master Hue for Chroma Modifier N.	

Register::: icm_cmn_mst_hue_LB 0xD3-01					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_cmn_mst_hue[7:0]	7:0	R/W	0	Low Byte[7:0] of Master Hue for Chroma Modifier N.	

Register::: icm_cmn_mst_hue_set 0xD3-02					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_cmn_left_width	7:6	W	0	CM[N].LWID 00: CM[N] left width = 64 01: CM[N] left width = 128 10: CM[N] left width = 256 11: CM[N] left width = 512	
Reg_cmn_left_buf	5:4	W	0	CM[N].LBUF 00: CM[N] left Buffer = 0 01: CM[N] left Buffer = 64 10: CM[N] left Buffer = 128 11: CM[N] left Buffer = 256	
Reg_cmn_right_width	3:2	W	0	CM[N].RWID 00: CM[N] right width = 64 01: CM[N] right width = 128 10: CM[N] right width = 256 11: CM[N] right width = 512	
Reg_cmn_right_buf	1:0	W	0	CM[N].RBUF 00: CM[N] right Buffer = 0 01: CM[N] right Buffer = 64 10: CM[N] right Buffer = 128 11: CM[N] right Buffer = 256	

Only when 0xD4[1] = 0, 0xD3-00~02 will be used.

Register:::U/V_Offset 0xD3-03~5C					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reg_uv_offset	7:0	R/W	0	ICM port data Addr 03: cmn mst U Offset 00, -128~127 Addr 04: cmn mst V Offset 00, -128~127 Addr 05: cmn mst U Offset 01, -128~127 Addr 06: cmn mst V Offset 01, -128~127 Addr 07: cmn mst U Offset 02, -128~127 Addr 08: cmn mst V Offset 02, -128~127	

				<p>Addr 40: cmn rbuf V Offset 06, -128~127 Addr 41: cmn rbuf U Offset 07, -128~127 Addr 42: cmn rbuf V Offset 07, -128~127</p> <p>Addr 43: cmn lbuf U Offset 00, -128~127 Addr 44: cmn lbuf V Offset 00, -128~127 Addr 45: cmn lbuf U Offset 01, -128~127 Addr 46: cmn lbuf V Offset 01, -128~127 Addr 47: cmn lbuf U Offset 02, -128~127 Addr 48: cmn lbuf V Offset 02, -128~127 Addr 49: cmn lbuf U Offset 03, -128~127 Addr 4A: cmn lbuf V Offset 03, -128~127 Addr 4B: cmn lbuf U Offset 04, -128~127 Addr 4C: cmn lbuf V Offset 04, -128~127 Addr 4D: cmn lbuf U Offset 05, -128~127 Addr 4E: cmn lbuf V Offset 05, -128~127 Addr 4F: cmn lbuf U Offset 06, -128~127 Addr 50: cmn lbuf V Offset 06, -128~127 Addr 51: cmn lbuf U Offset 07, -128~127 Addr 52: cmn lbuf V Offset 07, -128~127</p> <p>Only when 0xD4[2] = 1, following registers (0xD3-53~5C) are valid. Each Umax is expressed as 1-bit sign, 9-bits integer & 2-bits fractional (s9.2), ranged from -510 to 510</p> <p>Addr 53[3:0]: cmn mst Umax[11:8] Addr 54[7:0]: cmn mst Umax[7:0]</p> <p>Addr 55[3:0]: cmn rwid Umax[11:8] Addr 56[7:0]: cmn rwid Umax[7:0]</p> <p>Addr 57[3:0]: cmn lwid Umax[11:8] Addr 58[7:0]: cmn lwid Umax[7:0]</p> <p>Addr 59[3:0]: cmn rbuf Umax[11:8] Addr 5A[7:0]: cmn rbuf Umax[7:0]</p> <p>Addr 5B[3:0]: cmn lbuf Umax[11:8] Addr 5C[7:0]: cmn lbuf Umax[7:0]</p>	
--	--	--	--	---	--

Register:: icm_cmn_rbuf_hue					0xD3-5D
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_rbuf_hue[11:8]	3:0	R/W	0	High Byte[11:8] of rbuf Hue for Chroma Modifier N.	

Register:: icm_cmn_rbuf_hue					0xD3-5E
Name	Bits	Read/Write	Reset State	Comments	Config
Reg_cmn_rbuf_hue[7:0]	7:0	R/W	0	Low Byte[7:0] of rbuf Hue for Chroma Modifier N.	

Register:: icm_cmn_rwid_range					0xD3-5F
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_rwid_range[11:8]	3:0	R/W	0	High Byte[11:8] of rwid range for Chroma Modifier N.	

Register:: icm_cmn_rwid_range					0xD3-60
Name	Bits	Read/Write	Reset State	Comments	Config
Reg_cmn_rwid_range [7:0]	7:0	R/W	0	Low Byte[7:0] of rwid range for Chroma Modifier N.	

Register:: icm_cmn_mst_range					0xD3-61
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_mst_range[11:8]	3:0	R/W	0	High Byte[11:8] of mst range for Chroma Modifier N.	

Register:: icm_cmn_msn_range					0xD3-62
Name	Bits	Read/Write	Reset State	Comments	Config
Reg_cmn_mst_range [7:0]	7:0	R/W	0	Low Byte[7:0] of mst range for Chroma Modifier N.	

Register:: icm_cmn_lwid_range					0xD3-63
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_lwid_range[11:8]	3:0	R/W	0	High Byte[11:8] of lwid range for Chroma Modifier N.	

Register:: icm_cmn_lwid_range					0xD3-64
Name	Bits	Read/Write	Reset State	Comments	Config
Reg_cmn_lwid_range [7:0]	7:0	R/W	0	Low Byte[7:0] of lwid range for Chroma Modifier N.	

Register:: icm_cmn_lbuf_range					0xD3-65
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	----	0	Reserved to 0	
Reg_cmn_lbuf_range[11:8]	3:0	R/W	0	High Byte[11:8] of lbuf range for Chroma Modifier N.	

Register:: icm_cmn_lbuf_range					0xD3-66
Name	Bits	Read/Write	Reset State	Comments	Config
Reg_cmn_lbuf_range [7:0]	7:0	R/W	0	Low Byte[7:0] of lbuf range for Chroma Modifier N.	

Only when 0xD4[2] = 1, 0xD3-5D~66 are valid.

Register:: ICM_SEL					0xD4
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:3	----	0	Reserved to 0	
Reg_icm_mode	2	R/W	0	0: Original ICM 1: New ICM	
Reg_icm_buf_uvoffset_reset	1	R/W	0	0: All U/V offset on right/left buffer will be set to 0 1: U/V offset on right/left buffer is used	
Reg_max_comp_en	0	R/W	0	Max value Compensate Enable 0: Disable 1: Enable Once Max value Compensate is Enable, Negative Compensate (0xD2[7]) is invalid. Max value Compensate is Enable has higher priority than Negative Compensate.	

DCR(Page 7)

Register:::DCR Address Port 0xD8					
Name	Bit s	R/W	Default	Comments	Config
DCR_ADDR	7:2	--	0	DCR address	
RESULT_READ	1	R/W	0	0: Disable Read to refresh measure result. 1: Read DCR measure result.	
MEASURE_START	0	R/W	0	0: Finish or disable 1: Start DCR computation.	

Register::: DCR Data Port 0xD9					
Name	Bits	R/W	Default	Comments	Config
DCR_DATA	7:0	R/W	0x00	DCR data	

Register::: DCR_THRESHOLD1 (ACCESS[D8,D9]) 0x00					
Name	Bits	R/W	Default	Comments	Config
THRESHOLD1_VALUE	7:0	R/W	0x08	DCR threshold1. (R+G+B)*0.75	

If we want to set threshold1 = 200. THRESHOLD1_VALUE = 200*0.75 = 150.

Register::: DCR_THRESHOLD2 (ACCESS[D8,D9]) 0x01					
Name	Bits	R/W	Default	Comments	Config
THRESHOLD2_VALUE	7:0	R/W	0x60	DCR threshold2. (threshold2 > threshold1) (R+G+B)*0.75	

If we want to set threshold2 = 200. THRESHOLD2_VALUE = 200*0.75 = 150.

If we expect the target_thd = 10b'R+10'bG+10'bB /3

And in firmware that THD*4 = R+G+B

so that → 3* target_thd = 4* THD , => THD = 3/4 target_thd.

Register:::DCR_ABOVE_TH1_NUM_2 (ACCESS[D8,D9]) 0x02					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_NUM_2	7:0	R	0	Total pixel number above threshold1: bit[23:16]	

Register:::DCR_ABOVE_TH1_NUM_1 (ACCESS[D8,D9]) 0x03					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_NUM_1	7:0	R	0	Total pixel number above threshold1: bit[15:8]	

Register:::DCR_ABOVE_TH1_NUM_0 (ACCESS[D8,D9]) 0x04					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_NUM_0	7:0	R	0	Total pixel number above threshold1: bit[7:0]	

Register:::DCR_ABOVE_TH1_VAL_3 (ACCESS[D8,D9]) 0x05					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_VAL_3	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[31:24]	

Register:::DCR_ABOVE_TH1_VAL_2 (ACCESS[D8,D9]) 0x06					
Name	Bits	R/W	Default	Comments	Config

ABOVE_TH1_VAL_2	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[23:16]	
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Register::DCR ABOVE TH1_VAL_1 (ACCESS[D8,D9]) 0x07					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_VAL_1	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[15:8]	

Register::DCR ABOVE TH1_VAL_0 (ACCESS[D8,D9]) 0x08					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH1_VAL_0	7:0	R	0	Total sum (R+G+B) of pixel value above threshold1: bit[7:0]	

Register::DCR ABOVE TH2_NUM_2 (ACCESS[D8,D9]) 0x09					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_2	7:0	R	0	Total pixel number above threshold2: bit[23:16]	

Register::DCR ABOVE TH2_NUM_1 (ACCESS[D8,D9]) 0x0A					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_1	7:0	R	0	Total pixel number above threshold2: bit[15:8]	

Register::DCR ABOVE TH2_NUM_0 (ACCESS[D8,D9]) 0x0B					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_NUM_0	7:0	R	0	Total pixel number above threshold2: bit[7:0]	

Register::DCR ABOVE TH2_VAL_3 (ACCESS[D8,D9]) 0x0C					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_3	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[31:24]	

Register::DCR ABOVE TH2_VAL_2 (ACCESS[D8,D9]) 0x0D					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_2	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[23:16]	

Register::DCR ABOVE TH2_VAL_1 (ACCESS[D8,D9]) 0x0E					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_1	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[15:8]	

Register::DCR ABOVE TH2_VAL_0 (ACCESS[D8,D9]) 0x0F					
Name	Bits	R/W	Default	Comments	Config
ABOVE_TH2_VAL_0	7:0	R	0	Total sum (R+G+B) of pixel value above threshold2: bit[7:0]	

Register::DCR_HIGH_LV_NUM_R_1 (ACCESS[D8,D9]) 0x10				
Name	Bits	R/W	Default	Comments
HIGH_LV_NUM_R_1	7:0	R	0	Dynamically detect highest level pixel number of red channel. RMAX_NUM[15:8]

Register::DCR_HIGH_LV_NUM_R_0 (ACCESS[D8,D9]) 0x11				
Name	Bits	R/W	Default	Comments
HIGH_LV_NUM_R_0	7:0	R	0	Dynamically detect highest level pixel number of red channel. RMAX_NUM[7:0]

Register::DCR_LOW_LV_NUM_R_1 (ACCESS[D8,D9]) 0x12				
Name	Bits	R/W	Default	Comments
LOW_LV_NUM_R_1	7:0	R	0	Dynamically detect the lowest level pixel number of red channel. RMIN_NUM[15:8]

Register::DCR_LOW_LV_NUM_R_0 (ACCESS[D8,D9]) 0x13				
Name	Bits	R/W	Default	Comments
LOW_LV_NUM_R_0	7:0	R	0	Dynamically detect the lowest level pixel number of red channel. RMIN_NUM[7:0]

Register::DCR_HIGH_LV_VAL_R (ACCESS[D8,D9]) 0x14				
Name	Bits	R/W	Default	Comments
HIGH_LV_VAL_R	7:0	R	0	Dynamically detect highest level value of red channel.

Register::DCR_LOW_LV_VAL_R (ACCESS[D8,D9]) 0x15				
Name	Bits	R/W	Default	Comments
LOW_LV_VAL_R	7:0	R	0	Dynamically detect the lowest level value of red channel.

Register::DCR_HIGH_LV_NUM_G_1 (ACCESS[D8,D9]) 0x16				
Name	Bits	R/W	Default	Comments
HIGH_LV_NUM_G_1	7:0	R	0	Dynamically detect the highest level pixel number of green channel. GMAX_NUM[15:8]

Register::DCR_HIGH_LV_NUM_G_0 (ACCESS[D8,D9]) 0x17				
Name	Bits	R/W	Default	Comments
HIGH_LV_NUM_G_0	7:0	R	0	Dynamically detect the highest level pixel number of green channel. GMAX_NUM[7:0]

Register::DCR_LOW_LV_NUM_G_1 (ACCESS[D8,D9]) 0x18				
Name	Bits	R/W	Default	Comments
LOW_LV_NUM_G_1	7:0	R	0	Dynamically detect the lowest level pixel number of green channel. GMIN_NUM[15:8]

Register::DCR_LOW_LV_NUM_G_0				(ACCESS[D8,D9]) 0x19	
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_G_0	7:0	R	0	Dynamically detect the lowest level pixel number of green channel. GMIN_NUM[7:0]	
Register::DCR_HIGH_LV_VAL_G				(ACCESS[D8,D9]) 0x1A	
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_VAL_G	7:0	R	0	Dynamically detect the highest level value of green channel.	

Register::DCR_LOW_LV_VAL_G				(ACCESS[D8,D9]) 0x1B	
Name	Bits	R/W	Default	Comments	Config
LOW_LV_VAL_G	7:0	R	0	Dynamically detect the lowest level value of green channel.	

Register::DCR_HIGH_LV_NUM_B_1				(ACCESS[D8,D9]) 0x1C	
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_B_1	7:0	R	0	Dynamically detect the highest level pixel number of blue channel. BMAX_NUM[15:8]	

Register::DCR_HIGH_LV_NUM_B_0				(ACCESS[D8,D9]) 0x1D	
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_NUM_B_0	7:0	R	0	Dynamically detect the highest level pixel number of blue channel. BMAX_NUM[7:0]	

Register::DCR_LOW_LV_NUM_B_1				(ACCESS[D8,D9]) 0x1E	
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_B_1	7:0	R	0	Dynamically detect the lowest level pixel number of blue channel. BMIN_NUM[15:8]	

Register::DCR_LOW_LV_NUM_B_0				(ACCESS[D8,D9]) 0x1F	
Name	Bits	R/W	Default	Comments	Config
LOW_LV_NUM_B_0	7:0	R	0	Dynamically detect the lowest level pixel number of blue channel. BMIN_NUM[7:0]	

Register:: DCR_HIGH_LV_VAL_B				(ACCESS[D8,D9]) 0x20	
Name	Bits	R/W	Default	Comments	Config
HIGH_LV_VAL_B	7:0	R	0	Dynamically detect the highest level value of blue channel.	

Register:: DCR_LOW_LV_VAL_B				(ACCESS[D8,D9]) 0x21	
Name	Bits	R/W	Default	Comments	Config
LOW_LV_VAL_B	7:0	R	0	Dynamically detect the lowest level value of blue channel.	

Name	Bits	Read/ Write	Reset State	Comments	Config

Reg_acm_enable	7	R/W	0	ICM Enable 0: Disable (Default) 1: Enable	
Reg_rgb2y_mode	6	R/W	0	Y Correction Mode 0: $dY = (8dU+dV)/8$ 1: $dY = (6dU+dV)/8$	
Reg_uv_off_range	5	R/W	0	ICM U/V Delta Range: 0: Original -128~+127 1: Double -256~254	
Reg_cm0_enable	4	R/W	0	CM0 Enable 0: Disable 1: Enable	
Reg_cm1_enable	3	R/W	0	CM1 Enable 0: Disable 1: Enable	
Reg_cm2_enable	2	R/W	0	CM2 Enable 0: Disable 1: Enable	
Reg_cm3_enable	1	R/W	0	CM3 Enable 0: Disable 1: Enable	
Reg_cm4_enable	0	R/W	0	CM4 Enable 0: Disable 1: Enable	

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CABC Histogram (Page7)

Register::CABC_Ctrl					0xDB		
Name	Bits	R/W	Default	Comments		Config	
Reg_CABC_Test_EN	7:6	R/W	0x00	Tese Mode: 0x01: dvs,dhs,all_den,den,inwin_den,bor_den, all_den_pre6, all_den_prex, frame_start, frame_end, dbuf_trig, 5'h0. dvs_out,dhs_out,all_den_out, gma_den_out,gma_inwin_den_out, gma_bor_den_out, all_den_prex_out,all_den_pre6_out, dither_all_den_pre3, 7'h0. 0x10 : 1'b0, larger_histo_th[14:0], rgb_max[7:0], mux_lhn[3:0],4'h0 0x11 : 1'b0,reg_dcr_read, reg_dcr_read_d2,read_en, reg_popup_r,pop_r,shn_value_wr,reg_popup_w,popup_w, histo_thn_w,histo_thn_wr,den, den_s2, idle_state, lhn_state, shn_state, histo_cnt[8:0]7'h0.			
Reserved	5:4	--	--	Reserved to 0			
DCR_DATA_SRC	3	R/W	0	DCR data from 0: Original DCR (default) 1: The same as CABC			
CABC_EN	2	R/W	0	CABC Histogram Enable 0: Disable 1: Enable			
Reserved	1	R/W	0	Reserved			
CABC/DCR_Crtl	0	R/W	00	CABC / DCR Data Update : 0: CABC / DCR data Update simultaneously 1: CABC / DCR data Update independently			

Register:: CABC Address Port					0xDC	
Name	Bits	R/W	Default	Comments		Config
CABC_ADDR	7:0	R/W	0x00	CABC address		

Register:: CABC Data Port					0xDD	
Name	Bits	R/W	Default	Comments		Config
CABC_DATA	7:0	R/W	0x00	CABC data		

Register:: NOR_FACTOR_H					(ACCESS[DC,DD]) 0x00	
Name	Bits	R/W	Default	Comments		Config
Reserved	7:6	--	--	Reserved to 0		
NOR_FAC_H	5:0	R/W	0x00	Bit[21:16] of Normalized Factor; NF=(255/N)*(2^22)		

Register:: NOR_FACTOR_M					(ACCESS[DC,DD]) 0x01	
Name	Bits	R/W	Default	Comments		Config
NOR_FAC_M	7:0	R/W	0x00	Bit[15:8] of Normalized Factor; NF=(255/N)*(2^22)		

Register:: NOR_FACTOR_L					(ACCESS[DC,DD]) 0x02	
Name	Bits	R/W	Default	Comments		Config
NOR_FAC_L	7:0	R/W	0x00	Bit[7:0] of Normalized Factor; NF=(255/N)*(2^22)		

Register:: S0_VALUE					(ACCESS[DC,DD]) 0x03	
Name	Bits	R/W	Default	Comments		Config
S0_VALUE	7:0	R	--	Normalized Histogram S0 Value		

Register:: S1_VALUE					(ACCESS[DC,DD]) 0x04	
Name	Bits	R/W	Default	Comments		Config
S1_VALUE	7:0	R	--	Normalized Histogram S1 Value		

Register:: S2_VALUE (ACCESS[DC,DD]) 0x05					
Name	Bits	R/W	Default	Comments	Config
S2_VALUE	7:0	R	--	Normalized Histogram S2 Value	

Register:: S3_VALUE (ACCESS[DC,DD]) 0x06					
Name	Bits	R/W	Default	Comments	Config
S3_VALUE	7:0	R	--	Normalized Histogram S3 Value	

Register:: S4_VALUE (ACCESS[DC,DD]) 0x07					
Name	Bits	R/W	Default	Comments	Config
S4_VALUE	7:0	R	--	Normalized Histogram S4 Value	

Register:: S5_VALUE (ACCESS[DC,DD]) 0x08					
Name	Bits	R/W	Default	Comments	Config
S5_VALUE	7:0	R	--	Normalized Histogram S5 Value	

Register:: S6_VALUE (ACCESS[DC,DD]) 0x09					
Name	Bits	R/W	Default	Comments	Config
S6_VALUE	7:0	R	--	Normalized Histogram S6 Value	

Register:: S7_VALUE (ACCESS[DC,DD]) 0x0A					
Name	Bits	R/W	Default	Comments	Config
S7_VALUE	7:0	R	--	Normalized Histogram S7 Value	

Register:: S8_VALUE (ACCESS[DC,DD]) 0x0B					
Name	Bits	R/W	Default	Comments	Config
S8_VALUE	7:0	R	--	Normalized Histogram S8 Value	

Register:: S9_VALUE (ACCESS[DC,DD]) 0x0C					
Name	Bits	R/W	Default	Comments	Config
S9_VALUE	7:0	R	--	Normalized Histogram S9 Value	

Register:: S10_VALUE (ACCESS[DC,DD]) 0x0D					
Name	Bits	R/W	Default	Comments	Config
S10_VALUE	7:0	R	--	Normalized Histogram S10 Value	

Register:: S11_VALUE (ACCESS[DC,DD]) 0x0E					
Name	Bits	R/W	Default	Comments	Config
S11_VALUE	7:0	R	--	Normalized Histogram S11 Value	

Register:: S12_VALUE (ACCESS[DC,DD]) 0x0F					
Name	Bits	R/W	Default	Comments	Config
S12_VALUE	7:0	R	--	Normalized Histogram S12 Value	

Register:: S13_VALUE (ACCESS[DC,DD]) 0x10					
Name	Bits	R/W	Default	Comments	Config
S13_VALUE	7:0	R	--	Normalized Histogram S13 Value	

Register:: S14_VALUE (ACCESS[DC,DD]) 0x11					
Name	Bits	R/W	Default	Comments	Config
S14_VALUE	7:0	R	--	Normalized Histogram S14 Value	

Register:: POPUP_CTRL (ACCESS[DC,DD]) 0x12					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	--	Reserved to 0	
POPUP_BIT	0	R/W	--	Reg[03]~Reg[11] are updated every frame. Once POPUP_BIT is read, the value of Reg[03] ~ Reg[11] will not be updated until	

			Reg[11] is read.	
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DCR and CABC refresh can be controlled by Read_Result bit in DCR or POPUP_CTRL in CABC. By Read_Result, DCR and CABC will refresh when this bit set to 0. By POPUP_CTRL, DCR and CABC will refresh after reading S14 value.

Register:: TH0_VALUE (ACCESS[DC,DD]) 0x20					
Name	Bits	R/W	Default	Comments	Config
TH0_VALUE	7:0	R/W	0x10	Threshold 0 of the histogram	

Register:: TH1_VALUE (ACCESS[DC,DD]) 0x21					
Name	Bits	R/W	Default	Comments	Config
TH1_VALUE	7:0	R/W	0x 20	Threshold 1 of the histogram	

Register:: TH2_VALUE (ACCESS[DC,DD]) 0x22					
Name	Bits	R/W	Default	Comments	Config
TH2_VALUE	7:0	R/W	0x 30	Threshold 2 of the histogram	

Register:: TH3_VALUE (ACCESS[DC,DD]) 0x23					
Name	Bits	R/W	Default	Comments	Config
TH3_VALUE	7:0	R/W	0x 40	Threshold 3 of the histogram	

Register:: TH4_VALUE (ACCESS[DC,DD]) 0x24					
Name	Bits	R/W	Default	Comments	Config
TH4_VALUE	7:0	R/W	0x 50	Threshold 4 of the histogram	

Register:: TH5_VALUE (ACCESS[DC,DD]) 0x25					
Name	Bits	R/W	Default	Comments	Config
TH5_VALUE	7:0	R/W	0x 60	Threshold 5 of the histogram	

Register:: TH6_VALUE (ACCESS[DC,DD]) 0x26					
Name	Bits	R/W	Default	Comments	Config
TH6_VALUE	7:0	R/W	0x 70	Threshold 6 of the histogram	

Register:: TH7_VALUE (ACCESS[DC,DD]) 0x27					
Name	Bits	R/W	Default	Comments	Config
TH7_VALUE	7:0	R/W	0x 80	Threshold 7 of the histogram	

Register:: TH8_VALUE (ACCESS[DC,DD]) 0x28					
Name	Bits	R/W	Default	Comments	Config
TH8_VALUE	7:0	R/W	0x 90	Threshold 8 of the histogram	

Register:: TH9_VALUE (ACCESS[DC,DD]) 0x29					
Name	Bits	R/W	Default	Comments	Config
TH9_VALUE	7:0	R/W	0x A0	Threshold 9 of the histogram	

Register:: TH10_VALUE (ACCESS[DC,DD]) 0x2A					
Name	Bits	R/W	Default	Comments	Config
TH10_VALUE	7:0	R/W	0x B0	Threshold 10 of the histogram	

Register:: TH11_VALUE (ACCESS[DC,DD]) 0x2B					
Name	Bits	R/W	Default	Comments	Config
TH11_VALUE	7:0	R/W	0x C0	Threshold 11 of the histogram	

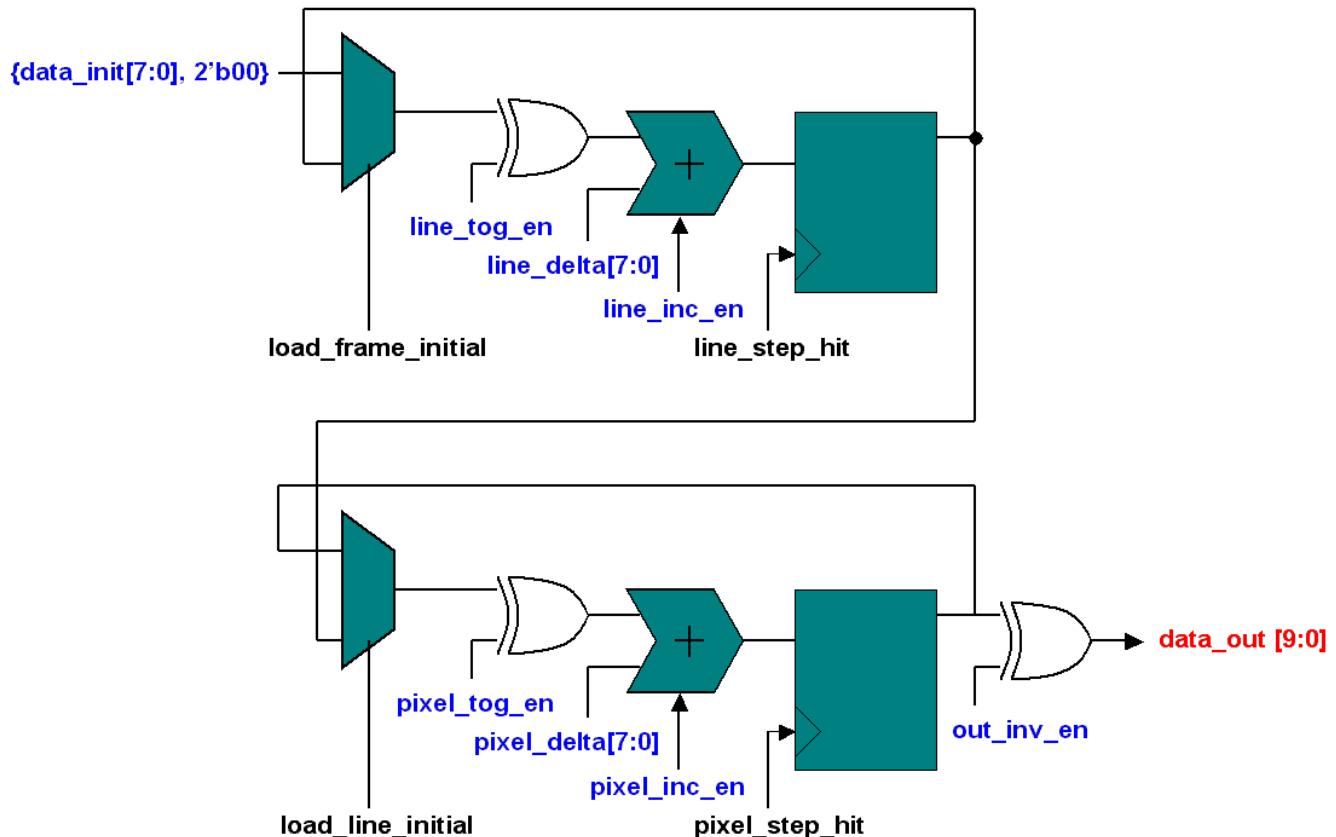
Register:: TH12_VALUE (ACCESS[DC,DD]) 0x2C					
Name	Bits	R/W	Default	Comments	Config
TH12_VALUE	7:0	R/W	0x D0	Threshold 12 of the histogram	

Register:: TH13_VALUE (ACCESS[DC,DD]) 0x2D					
Name	Bits	R/W	Default	Comments	Config
TH13_VALUE	7:0	R/W	0x E0	Threshold 13 of the histogram	

Register:: TH14_VALUE (ACCESS[DC,DD]) 0x2E					
Name	Bits	R/W	Default	Comments	Config
TH14_VALUE	7:0	R/W	0x F0	Threshold 14 of the histogram	

Pattern Generator in D-Domain (Page 7)

RTD2485XD supports programmable patterns, such as gray-level, chessboard, dot-pattern, etc., for display image testing.



Register::DISP_PG_R_CTRL							0xF0
Name	Bits	R/W	Default	Comments			Config
PG_ENABLE	7	R/W	0	Dispaly Pattern Gen. Function Enable			
PG_R_CTRL_DUM	6	R/W	0	Dummy			
PG_ROUT_INV_EN	5	R/W	0	Inverse Data Output			
PG_R_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF			
LINE_R_TOG_EN	3	R/W	0	Data toggled in each line -step			
LINE_R_INC_EN	2	R/W	0	Data increment in each line-step			
PIXEL_R_TOG_EN	1	R/W	0	Data toggled in each pixel-step			
PIXEL_R_INC_EN	0	R/W	0	Data incremented in each pixel-step			

Register::DISP_PG_G_CTRL						0xF1
Name	Bits	R/W	Default	Comments		Config
PG_G_CTRL_DUM	7:6	R/W	0	Dummy		
PG_GOUT_INV_EN	5	R/W	0	Inverse Data Output		
PG_G_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF		
LINE_G_TOG_EN	3	R/W	0	Data toggled in each line -step		
LINE_G_INC_EN	2	R/W	0	Data increment in each line-step		
PIXEL_G_TOG_EN	1	R/W	0	Data toggled in each pixel-step		
PIXEL_G_INC_EN	0	R/W	0	Data incremented in each pixel-step		

Register::DISP_PG_B_CTRL						0xF2
Name	Bits	R/W	Default	Comments		Config
PG_B_CTRL_DUM	7:6	R/W	0	Dummy		
PG_BOUT_INV_EN	5	R/W	0	Inverse Data Output		
PG_B_CLAMP_EN	4	R/W	0	Adder result clamp to 10'h3FFF		
LINE_B_TOG_EN	3	R/W	0	Data toggled in each line -step		
LINE_B_INC_EN	2	R/W	0	Data increment in each line-step		
PIXEL_B_TOG_EN	1	R/W	0	Data toggled in each pixel-step		
PIXEL_B_INC_EN	0	R/W	0	Data incremented in each pixel-step		

Register::DISP_PG_R_Initial						0xF3
Name	Bits	R/W	Default	Comments		Config
PG_R_INIT	7:0	R/W	0	Initial Pattern Value for Red Data [9:2]		

Register::DISP_PG_G_Initial						0xF4
Name	Bits	R/W	Default	Comments		Config
PG_G_INIT	7:0	R/W	0	Initial Pattern Value for Green Data [9:2]		

Register::DISP_PG_B_Initial						0xF5
Name	Bits	R/W	Default	Comments		Config
PG_B_INIT	7:0	R/W	0	Initial Pattern Value for Blue Data [9:2]		

Register::DISP_PG_Pixel_Delta						0xF6
Name	Bits	R/W	Default	Comments		Config
PG_PIXEL_DELTA	7:0	R/W	0	Pixel Delta value for incremental		

Register::DISP_PG_Line_Delta						0xF7
Name	Bits	R/W	Default	Comments		Config

PG_LINE_DELTA	7:0	R/W	0	Line Delta value for incremental	
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Register::DISP_PG_Pixel_Step_MSB					0xF8
Name	Bits	R/W	Default	Comments	Config
PG_PIXEL_STEP_M	7:0	R/W	01h	Pixel Step for toggle/incremental, can not be 0	

Register::DISP_PG_Line_Step_MSB					0xF9
Name	Bits	R/W	Default	Comments	Config
PG_LINE_STEP_M	7:0	R/W	01h	Line Step for toggle/incremental, can not be 0	

Register::DISP_PG Step LSB					0xFA
Name	Bits	R/W	Default	Comments	Config
LINE_STEP_DUM	7:6	R/W	0	Dummy	
PG_LINE_STEP_L	5:4	R/W	0	Decimal part for Line-step	
PIXEL_STEP_DUM	3:2	R/W	0	Dummy	
PG_PIXEL_STEP_L	1:0	R/W	0	Decimal part for Pixel-step	

Ex: If the pattern is 256 gray level in 640 pixels, the wanted pixel_step is $640/256 = 2.5$. Hence,
PG_PIXEL_STEP_M = 2h and **PG_PIXEL_STEP_L = 2'b10**.

({PG_PIXEL_STEP_M, PG_PIXEL_STEP_L} = 2.5).

DVC – Digital Volume Control(Page 8)
Digital Volume Control

Register::DVC_0 0xA0					
Name	Bits	R/W	Default	Comments	Config
DVC_EN	7	R/W	0x0	H/W DVC Enable 0:Disable (gain is directly apply) 1:Enable (delay volume control)	
AUD_CNT_DISABLE	6	R/W	0x0	1:disable the counter (for power saving) 0:normal mode	
reserved	5:4	--	--	reserved	
DVC_DOWN_DB	3:2	R/W	0x3	Active when DVC_DOWN_VA = 0 00: -1dB (gain1=gain1*7/8) 01: -1/2dB (gain1=gain1*15/16) 10: -1/4dB (gain1=gain1*31/32) 11: -1/8dB (gain1=gain1*63/64)	
DVC_UP_DB	1:0	R/W	0x3	Active when DVC_UP_VA = 0 00: +1dB (gain1=gain1*9/8) 01: +1/2dB (gain1=gain1*17/16) 10: +1/4dB (gain1=gain1*33/32) 11: +1/8dB (gain1=gain1*65/64)	

Register:: DVC_1 0xA1					
Name	Bits	R/W	Default	Comments	Config
DVC_DOWN_VA	7:0	R/W	0x0	Delay volume down value	

Register:: DVC_2 0xA2					
Name	Bits	R/W	Default	Comments	Config
DVC_UP_VA	7:0	R/W	0x0	Delay volume up value	

Register::DVC_WINDOW_CONTROL_0 0xA3					
Name	Bits	R/W	Default	Comments	Config
DVC_ZC_WIN[11:8]	7:4	R/W	0x2	DVC_ZC_WIN[11:8] : zero-crossing time-out window size (unit: pcm samples)	
reserved	3:0	--	--	reserved	

Register::DVC_WINDOW_CONTROL_1 0xA4					
Name	Bits	R/W	Default	Comments	Config
DVC_ZC_WIN[7:0]	7:0	R/W	0x52	DVC_ZC_WIN[7:0] : zero-crossing time-out window size (unit: pcm samples)	

Register:: GAIN_0 0xA5					
Name	Bits	R/W	Default	Comments	Config
DVC_GAIN	7:0	R/W	0xFF	DVC GAIN TARGET 0 : gain = 0 1 : gain = 1/256 2: gain = 2/256 ... 254 : gain = 254/256 255: gain = 1	

Register:: GAIN_1 0xA6					
Name	Bits	R/W	Default	Comments	Config

DVC_GAIN_L	7:0	R	0x0	Gain Value in L	
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Register:: GAIN_2					0xA7
Name	Bits	R/W	Default	Comments	Config
DVC_GAIN_R	7:0	R	0x0	Gain Value in R	

Register:: GAIN_DONE					0xA8
Name	Bits	R/W	Default	Comments	Config
DVC_DONE	7	R	0x0	DVC Done signal by L & R. clear by re-set DVC_GAIN	
reserved	6:4	--	--	reserved	
HARD_GAIN	3:0	R/W	0	0000: 0dB 0001: 6dB 0010: 12dB 0011: 18dB 0100: 24dB 0101: -6dB 0110: -12dB 0111: -18dB 1000: -24dB	

PEAK DETECTION

Register:: PEAK_CTRL_0					0xA9
Name	Bits	R/W	Default	Comments	Config
Pdetect_enable	7	R/W	0	Peak detect enable 0: disable 1: enable	
Rev_peak_d3	6:4	R/W	0	Debug mode	
Peak_ovfl_det_l_irq_en	3	R/W	0	Left channel peak overflow detected IRQ enable 0: disable 1: enable	
Peak_ovfl_det_r_irq_en	2	R/W	0	Right channel peak overflow detected IRQ enable 0: disable 1: enable	
Peak_ovfl_det_l	1	R	0	Left channel peak overflow detected	Wclr_out
Peak_ovfl_det_r	0	R	0	Right channel peak overflow detected	Wclr_out

Register:: PEAK_CTRL_1					0xAA
Name	Bits	R/W	Default	Comments	Config
Debounce_cnt_l[7:5]	7:5	R/W	0x1	The de-bouncing threshold to judge if peak volume exceeds the threshold debounce_cnt 000: 2^0 001: 2^1 010: 2^2 111: 2^7	
Rev_peak_d4_4	4	R/W	0	Reserved	
Debounce_cnt_r[3:1]	3:1	R/W	0x1	The de-bouncing threshold to judge if peak volume exceeds the threshold debounce_cnt 000: 2^0 001: 2^1 010: 2^2 111: 2^7	
Rev_peak_d4_0	0	R/W	0	Reserved	

Register:: PEAK_CTRL_L_0	0xAB
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Name	Bits	R/W	Default	Comments	Config
Ovf_th_l[23:16]	7:0	R/W	0x20	the overflow threshold of left channel[23:16]	

Register:: PEAK_CTRL_L_1 0xAC					
Name	Bits	R/W	Default	Comments	Config
Ovf_th_l[15:8]	7:0	R/W	0	the overflow threshold of left channel[15:8]	

Register:: PEAK_CTRL_L_2 0xAD					
Name	Bits	R/W	Default	Comments	Config
Ovf_th_l[7:0]	7:0	R/W	0	the overflow threshold of left channel[7:0]	

Register:: PEAK_CTRL_L_3 0xAE					
Name	Bits	R/W	Default	Comments	Config
Monitor_window_l[15:8]	7:0	R/W	0x1	Monitor period of left channel for peak detection [15:8] Unit: fs	

Register:: PEAK_CTRL_L_4 0xAF					
Name	Bits	R/W	Default	Comments	Config
Monitor_window_l[7:0]	7:0	R/W	0x80	Monitor period of left channel for peak detection [7:0] Unit: fs	

Register:: PEAK_CTRL_R_0 0xB0					
Name	Bits	R/W	Default	Comments	Config
Ovf_th_r[23:16]	7:0	R/W	0x20	the overflow threshold of right channel[23:16]	

Register:: PEAK_CTRL_R_1 0xB1					
Name	Bits	R/W	Default	Comments	Config
Ovf_th_r[15:8]	7:0	R/W	0	the overflow threshold of right channel[15:8]	

Register:: PEAK_CTRL_R_2 0xB2					
Name	Bits	R/W	Default	Comments	Config
Ovf_th_r[7:0]	7:0	R/W	0	the overflow threshold of right channel[7:0]	

Register:: PEAK_CTRL_R_3 0xB3					
Name	Bits	R/W	Default	Comments	Config
Monitor_window_r[15:8]	7:0	R/W	0x1	Monitor period of right channel for peak detection [15:8] Unit: fs	

Register:: PEAK_CTRL_R_4 0xB4					
Name	Bits	R/W	Default	Comments	Config
Monitor_window_r[7:0]	7:0	R/W	0x80	Monitor period of right channel for peak detection [7:0] Unit: fs	

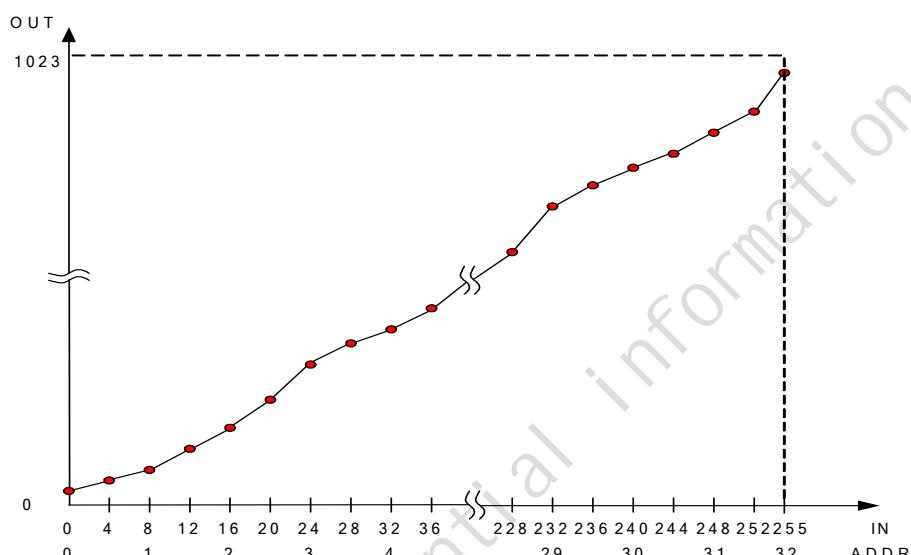
Address:B6~FF reserved

Input Gamma Control (Page 9)
Address: A0 INPUT_GAMMA_PORT

Bit	Mode	Function
7:0	R/W	Access port for input gamma correction table

- The Gamma Table written to this port should follow the sequences as expressed below:

{2'b0, g0[9:4]}, {g0[3:0]}, 2'b0, g16[9:8]}, {g16[7:0]},	<- addr = 0
{2'b0, g32[9:4]}, {g32[3:0]}, 2'b0, g48[9:8]}, {g48[7:0]},	<- addr = 1
...,	
{2'b0, g992[9:4]}, {g992[3:0]}, 2'b0, g1008[9:8]}, {g1008[7:0]},	<- addr = 31
{2'b0, g1023[9:4]}, {g1023[3:0]}, 4'b0}, {8'b0}	<- addr = 32
- There are two thresholds divide Input Gamma Table into three divisions.
- From 0 to threshold 1 is the first division.
- From (threshold 1 + 1) to threshold 2 is the second division.
- Above threshold 2 is the third division


Address: A1 INPUT_GAMMA_CTRL

Default: 00h

Bit	Mode	Function
7	R/W	Enable Access Channels for Input Gamma Correction Coefficient: 0: disable these channels (Default) 1: enable these channels
6	R/W	Input Gamma table enable 0: by pass (Default) 1: enable
5:0	--	Reserved to 0

Address: A2 INPUT_GAMMA_LOW_THRE

Default: 11h

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R/W	Input Gamma low threshold value

Both threshold values are restricted in 0~64

Address: A3 INPUT_GAMMA_HIGH_THRE

Default: 22h

Bit	Mode	Function
7	R/W	Reserved to 0
6:0	R/W	Input Gamma high threshold value

High threshold value has to be greater than low threshold value.
Both threshold values are restricted in 0~64

Address:A4~FF reserved

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Signal Detection (Page A)

Register::: DP_SIG_DET_00						0xA0
Name	Bit	R/W	Default	Description		Config
DP_SIG_DET_LANE3_EN	7	R/W	0	Start the signal detect process (Lane3), write clear. After measured done, hardware auto disable function. 0: Disable 1: Started		
DP_SIG_DET_LANE2_EN	6	R/W	0	Start the signal detect process (Lane2), write clear. After measured done, hardware auto disable function. 0: Disable 1: Started		
DP_SIG_DET_LANE1_EN	5	R/W	0	Start the signal detect process (Lane1), write clear. After measured done, hardware auto disable function. 0: Disable 1: Started		
DP_SIG_DET_LANE0_EN	4	R/W	0	Start the signal detect process (Lane0), write clear. After measured done, hardware auto disable function. 0: Disable 1: Started		
DP_LANE3_VAL	3	R	0	The Lane3 will be valid when Bit Rate Upper Bound > LANE3_COUNT > Bit Rate Lower Bound 0: Not Valid 1: Valid		
DP_LANE2_VAL	2	R	0	The Lane2 will be valid when Bit Rate Upper Bound > LANE2_COUNT > Bit Rate Lower Bound 0: Not Valid 1: Valid		
DP_LANE1_VAL	1	R	0	The Lane1 will be valid when Bit Rate Upper Bound > LANE1_COUNT > Bit Rate Lower Bound 0: Not Valid 1: Valid		
DP_LANE0_VAL	0	R	0	The Lane0 will be valid when Bit Rate Upper Bound > LANE0_COUNT > Bit Rate Lower Bound 0: Not Valid 1: Valid		

* Add: DP_LANEx_VAL Clear Bit to **0xB7 Bit0**

Register::: DP_SIG_DET_01						0xA1
Name	Bit	R/W	Default	Description		Config
EN_SIGDET_LANE3	7	R/W	0	PHY Lane 3 enable signal. 0; disable 1: enable Active when signal detection enabled. Page B en_sigdet = 1		
EN_SIGDET_LANE2	6	R/W	0	PHY Lane 2 enable signal. 0; disable 1: enable Active when signal detection enabled. Page B en_sigdet = 1.		
EN_SIGDET_LANE1	5	R/W	0	PHY Lane 1 enable signal. 0; disable 1: enable Active when signal detection enabled. Page B en_sigdet = 1.		
EN_SIGDET_LANE0	4	R/W	0	PHY Lane 0 enable signal. 0; disable 1: enable Active when signal detection enabled. Page B en_sigdet = 1.		

DP_XTAL_CYCLE	3:2	R/W	0	Select the counter cycles of Xtal 00: 125 01: 250 10: 500 11: 1000.	
DP_VAD_CHK_TIME	1:0	R/W	3	Select valid lane checking times, lane will be valid only if every time is valid. 00: 1 times 01: 2 times 10: 3 times 11: 4 times.	

Register:: DP_SIG_DET_02 0xA2					
Name	Bit	R/W	Default	Description	Config
DP_LANE0_SPD_DET	7:6	R	0	According threshold report lane speed 00: Idle or out of range 01: RBR 10: HBR 11: HBR2	
DP_LANE1_SPD_DET	5:4	R	0	According threshold report lane speed 00: Idle or out of range 01: RBR 10: HBR 11: HBR2	
DP_LANE2_SPD_DET	3:2	R	0	According threshold report lane speed 00: Idle or out of range 01: RBR 10: HBR 11: HBR2	
DP_LANE3_SPD_DET	1:0	R	0	According threshold report lane speed 00: Idle or out of range 01: RBR 10: HBR 11: HBR2	

* Default value setting.

Register:: DP_SIG_DET_03 0xA3					
Name	Bit	R/W	Default	Description	Config
DP_RBR_UP_THD_H	7:0	R/W	0x0C	RBR Upper Bound threshold [15:8]	

Register:: DP_SIG_DET_04 0xA4					
Name	Bit	R/W	Default	Description	Config
DP_RBR_UP_THD_L	7:0	R/W	0xE4	RBR Upper Bound threshold [7:0]	

Register:: DP_SIG_DET_05 0xA5					
Name	Bit	R/W	Default	Description	Config
DP_RBR_LOW_THD_H	7:0	R/W	0x0A	RBR Lower Bound threshold [15:8]	

Register:: DP_SIG_DET_06 0xA6					
Name	Bit	R/W	Default	Description	Config
DP_RBR_LOW_THD_L	7:0	R/W	0x8C	RBR Lower Bound threshold [7:0]	

Register:: DP_SIG_DET_07 0xA7					
Name	Bit	R/W	Default	Description	Config
DP_HBR_UP_THD_H	7:0	R/W	0x15	HBR Upper Bound threshold [15:8]	

Register:: DP_SIG_DET_08 0xA8					
Name	Bit	R/W	Default	Description	Config
DP_HBR_UP_THD_L	7:0	R/W	0x7C	HBR Upper Bound threshold [7:0]	

Register:: DP_SIG_DET_09 0xA9					
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Name	Bit	R/W	Default	Description	Config
DP_HBR_LOW_THD_H	7:0	R/W	0x11	HBR Lower Bound threshold [15:8]	

Register:: DP_SIG_DET_10 0xAA					
Name	Bit	R/W	Default	Description	Config
DP_HBR_LOW_THD_L	7:0	R/W	0x94	HBR Lower Bound threshold [7:0]	

Register:: DP_SIG_DET_11 0xAB					
Name	Bit	R/W	Default	Description	Config
DP_HBR2_UP_THD_H	7:0	R/W	0x2A	HBR2 Upper Bound threshold [15:8]	

Register:: DP_SIG_DET_12 0xAC					
Name	Bit	R/W	Default	Description	Config
DP_HBR2_UP_THD_L	7:0	R/W	0xF8	HBR2 Upper Bound threshold [7:0]	

Register:: DP_SIG_DET_13 0xAD					
Name	Bit	R/W	Default	Description	Config
DP_HBR2_LOW_THD_H	7:0	R/W	0x23	HBR2 Lower Bound threshold [15:8]	

Register:: DP_SIG_DET_14 0xAE					
Name	Bit	R/W	Default	Description	Config
DP_HBR2_LOW_THD_L	7:0	R/W	0x28	HBR2 Lower Bound threshold [7:0]	

* LANEx_COUNT_x clear bit to 0xB7 Bit0

Register:: DP_SIG_DET_15 0xAF					
Name	Bit	R/W	Default	Description	Config
LANE0_COUNT_H	7:0	R	0	Report Lane0 counters[15:8]	

Register:: DP_SIG_DET_16 0xB0					
Name	Bit	R/W	Default	Description	Config
LANE0_COUNT_L	7:0	R	0	Report Lane0 counters[7:0]	

Register:: DP_SIG_DET_17 0xB1					
Name	Bit	R/W	Default	Description	Config
LANE1_COUNT_H	7:0	R	0	Report Lane1 counters[15:8]	

Register:: DP_SIG_DET_18 0xB2					
Name	Bit	R/W	Default	Description	Config
LANE1_COUNT_L	7:0	R	0	Report Lane1 counters[7:0]	

Register:: DP_SIG_DET_19 0xB3					
Name	Bit	R/W	Default	Description	Config
LANE2_COUNT_H	7:0	R	0	Report Lane2 counters[15:8]	

Register:: DP_SIG_DET_20 0xB4					
Name	Bit	R/W	Default	Description	Config
LANE2_COUNT_L	7:0	R	0	Report Lane2 counters[7:0]	

Register:: DP_SIG_DET_21 0xB5					
Name	Bit	R/W	Default	Description	Config
LANE3_COUNT_H	7:0	R	0	Report Lane3 counters[15:8]	

Register:: DP_SIG_DET_22 0xB6					
Name	Bit	R/W	Default	Description	Config
LANE3_COUNT_L	7:0	R	0	Report Lane3 counters[7:0]	

Register:: DP_SIG_DET_23						0xB7
Name	Bit	R/W	Default	Description	Config	
LANE3_NO_CLOCK	7	R	0	No input clock.(Lane 3) 0: Input clock exists. 1: No input clock		
LANE2_NO_CLOCK	6	R	0	No input clock.(Lane 2) 0: Input clock exists. 1: No input clock		
LANE1_NO_CLOCK	5	R	0	No input clock.(Lane 1) 0: Input clock exists. 1: No input clock		
LANE0_NO_CLOCK	4	R	0	No input clock.(Lane 0) 0: Input clock exists. 1: No input clock		
Reserved	3:1	R/W	0	Reserved.		
DETECT_RESET	0	R		Write to clear DP_LANEx_VAL , LANEx_COUNT	Wclr_out	

Register:: DP_SIG_DET_24						0xB8
Name	Bit	R/W	Default	Description	Config	
Reserved	7:0	R/W	0	Reserved.		

Address:B9~FF reserved

GDI PHY (Page B)

Power On Region

PHY CONTROL

Register::SIG_DET 0XA0					
Name	Bits	R/W	Default	Comments	Config
sig_det_rsv	7:4	R/W	0	RESERVED	
rext2vdd	3	R/W	1	1: bandgap external resistor 6.2K connect to VDD 0: connect to GND	
reg_itune_lvds[1:0]	2:1	R/W	01	tuning ibhx20u to LVDS 00:15u 01:20u 10:25u 11:30u Active when LVDS bias current select to GDI.	
en_sigdet	0	R/W	0	1: Enable signal detection 0: Disable signal detection	

Register:: FLD_FSM_0 0XA1					
Name	Bits	R/W	Default	Comments	Config
fld_fsm_rsv	7:6	R/W	0	Reserved	
fld_st_lane1	5:3	R	0	lane1 FLD state	
fld_st_lane0	2:0	R	0	lane0 FLD state	

Register:: FLD_FSM_1 0xA2					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	R/W	0	Reserved	
fld_st_lane3	5:3	R	0	lane3 FLD state	
fld_st_lane2	2:0	R	0	lane2 FLD state	

Register:: Reserved_1 0xA3					
Name	Bits	R/W	Default	Comments	Config
fld_st_rsv	7:0	R/W	0	Reserved	

Register::CDR_2 0XA4					
Name	Bits	R/W	Default	Comments	Config
lpf_cp1p_sel	7	R/W	0	select CDR lpf cp 1pF	
lpf_cs60p_sel	6	R/W	0	select CDR lpf cs 46pF	
lpf_cp05p_sel	5	R/W	0	select CDR lpf cp 0.5pF	
rev_reg[4:3]	4:3	R/W	0	If datarate < 1Gbps, increase LE low frequency boost(for 30M 0.7425G case) 00:6dB@0.7425G 01/10:9dB@0.7425G 11:12dB@0.7425G	
rev_reg [2:1]	2:1	R/W	1	Reserved	
rev_reg [0]	0	R/W	1	[0] Enable background offset calibration DAC: 0:disable 1:enable	

Register::CDR_3 0XA5					
Name	Bits	R/W	Default	Comments	Config
vco_div	7:6	R/W	0	VCO Divider Mcode: 00=VCO/1, 01=VCO/2, 10=VCO/4, 11=VCO/8	
sel_bb	5	R/W	1	0=linear PD 1=Binary PD <1.35G linear PD (no support edge-based adaptation) >1.35G binary PD	

sel_half	4	R/W	1	0=Full rate PD(Linear mode) 1=Half rate PD (BB mode)	
sel_vcmfb	3	R/W	0	Charge pump common mode voltage Setting 0: set charge pump common mode voltage to CPVREF, i.e. 0.55/0.6/0.65/0.5V 1: set charge pump common mode voltage to Vdd/2	
vco_vc_manual	2	R/W	0	0: VCO in CDR loop 1:force VCO control voltage to +/-100mV by vco_vc if cp_en_manual =1'b0	
kvco	1:0	R/W	1	Kvco boost: 00=388MHz/V, 01=526MHz/V, 10=640MHz/V, 11=832MHz/V	

Register::CDR_4					0xA6	
Name	Bits	R/W	Default	Comments	Config	
cp_sel	7:4	R/W	1	Charge pump current 0000: 3.75uA 0001: 7.5uA 0010: 11.25uA 0011: 15uA 0100: 7.5uA 0101: 15uA 0110: 22.5uA 0111: 30uA 1000: 11.25uA 1001: 22.5uA 1010: 33.75uA 1011: 45uA 1100: 15uA 1101: 30uA 1110: 45uA 1111: 60uA		
cpsr	3:1	R/W	1	Loop resister: 100=0.5k 101=1k 000=2k 110=3k 001=4k 010=8k 011=10k 111=12k		
Reserved	0	R/W	0	Reserved		

A5[7:4], A5[1:0], A6, AA[0] enable when AF[6]=1

Register:: CDR_5					0XA7	
Name	Bits	R/W	Default	Comments	Config	
dvco_div	7:6	R	0	DVCO_DIV<1:0>		
dsel_bb	5	R	0	DSEL_BB		
dsel_half	4	R	0	DSEL_HALF		
reg_test	3:1	R/W	4	Analog test selection to SOG 0:ibn_45u 1:ibhn_25u 2:ibx_50u 3:ibhx_50u 4:HV_Z0 5:RX_V12 6:RX_V12 7:RX_G		
en_vco_biasr	0	R/W	0	0: VCO bias large R controlled by FLD 1: VCO bias using large RC(better phase noise).		

Register::CDR_6 0xA8					
Name	Bits	R/W	Default	Comments	Config
data_rdy	7:4	R	0	CDR[3:0] Data Ready of Each Lane 0: unlock, 1:lock	
cdr_6_rsv	3:2	R/W	0	RESERVED	
spd_det	1:0	R	0	DP Rate Detect: 00: low rate(1.62G), 01: high rate(2.7G) 10:3.24Gbps(Useless),11:reserved	

Register::CDR_7 0XA9					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
loop_ok_in_regb	6	R/W	0	1'b0:loop_ok=1 when reg_loop_f_sel=1	
reg_loop_f_sel	5	R/W	0	1'b0:select as RL6049E mode det output	
sel_cktp1	4	R/W	0	sel_cktp1 1'b0=select from FSM(default), 1'b1=select from en_cktp1 (valid only DP mode)	
cdr_7_rsv	3:2	R/W	3	reserved register	
en_cktp1	1	R/W	1	1'b0=disable tp1 input (valid only DP mode and sel_cktp1=1'b1) 1'b1=enable tp1 input (default),	
reg_xtal_sel	0	R/W	1	1'b1=FLD xtal divider select /8	

Register:: CDR_8 0XAA					
Name	Bits	R/W	Default	Comments	Config
bpdgain	7	R/W	1	BPD gain	
sel_cont3	6	R/W	1	1=binary PD UP/DN pulse div3 0=binary PD UP/DN pulse div4	
sel_ibx	5	R/W	0	VCO bias current 0: from ibn(reference to internal resistor), 1: from ibx(reference to external resistor)	
sel_ib90	4:3	R/W	1	90u bias current: 00=80u, 01=90u, 10=100u, 11=110u	
sel_ib25	2:1	R/W	2	25u bias current: 00=15u, 01=20u, 10=25u, 11=30u.	
cpsc	0	R/W	0	Loop capacitor: 0=2p disable, 1=2p enable	

Register:: CDR_9 0XAB					
Name	Bits	R/W	Default	Comments	Config
cdr_9_rsv	7	R/W	0	Reserved	
xtal_en	6	R/W	1	1=crystal input 0=non crystal, (DP,using TP1 as FLD reference clock)	
rxcom_sel	5:4	R/W	1	rx amplifier input common mode voltage: 2'b00=VDD-0.35V , 2'b01=VDD-0.3V (default), 2'b10=VDD-0.25V, 2'b11=VDD-0.2V	
rstb_z0	3	R/W	1	50 Ohm calibration reset signal @ manual mode(0XAB[2])	
z0_manual	2	R/W	0	1: Manual select Z0 calibration reset signal ,from A4[3]rstb_z0 0:reset signal from rxen	

en_wide_temp	1	R/W	0	en_wide_temp: vco' s Vc @FLD 0 : disable vco_vc control . Vc=0 (default) 1 : enable vco vc control. (0XAB[0])	
vco_vc	0	R/W	0	vco control voltage when vco_vc_manual=1'b1 0=-0.1V,1=0.1V	

Register::CDR_A 0XAC					
Name	Bits	R/W	Default	Comments	Config
dp_rate_in	7:6	R/W	0	DP_RATE_MANUAL 00=Reduced Bit Rate (1.62Gbps) 01=High Bit Rate (2.7Gbps) 10=3.24Gbps (Useless) 11=reserved	
dp_rate_manual	5	R/W	0	1=use dp_rate_in to set freq_ld in DP mode 0=use auto detected result from mode_det	
dp_mode	4	R/W	0	0=hmdi mode 1=dp mode	
dp_dm_sel	3	R/W	0	0=dp legency mode 1=dp dual mode enable only if dp_mode=1	
Reserved	2:0	R/W	0	Reserved	

Register::RXMISC_0 0XAD					
Name	Bits	R/W	Default	Comments	Config
cdrcpop_en	7	R/W	0	1=enable CDR charge pump charge sharing OP	
ultralow_rate	6	R/W	0	if input datarate <225M, this bit should be set 1	
sel_csop_in	5	R/W	1	0=CDR CP CSOP input from Rs 1=CDR CP CSOP input from Cs	
cp_adj_en	4	R/W	1	1:enable adjust charge pump current when tracking	
adp_eq_off	3	R/W	0	1:DFE equalizer adaptation disable 0:DFE equalizer adaptation enable Active when auto_mode 0xAF[7] = 1	
adp_time	2:0	R/W	0	adaptive equalizer turn on time delay after CDR close loop	

Register:: RXMISC_1 0XAE					
Name	Bits	R/W	Default	Comments	Config
cpvref_sel	7:6	R/W	0	CDR CP Vref: 00: 0.55V, 01: 0.60V, 10: 0.65V, 11: 0.50V	
rxmisc_54_rsv	5:4	R/W	0	Reserved	
rxmisc_3_rsv	3	R/W	1	Reserved	
rxmisc_21_rsv	2:1	R/W	0	RESERVED	
sel_sync	0	R/W	1	Div5 out phase: 0: clock edge at middle point of data, 1:clock edge align with data edge	

Register::RXMISC_2 0XAF					
Name	Bits	R/W	Default	Comments	Config
auto_mode	7	R/W	1	FLD auto mode: 0=FLD manual mode, 1= FLD auto mode,	
loop_manual	6	R/W	0	Parameter manual set: 0=auto set by mode detect, 1=manual set (divider,PD)	
cp_en_manual	5	R/W	0	Enable only at FLD manual mode(active @AF[7]=0):CP	

				enable (CDR close loop) 0=CP disable(CDR open loop), 1=CP enable CP(CDR close loop)	
adp_en_manual	4	R/W	0	Adaptive Equalizer manual mode enable(active @AF[7]=0): 0: disable 1: enable	
calib_manual	3	R/W	0	data_rdy <= calib_manual when auto_mode=0(active @AF[7]=0):	
calib_time	2:0	R/W	7	data_rdy output delay time(after DFE start work) (active@AF[7] =1)	

Register:: EQ_0 0xB0					
Name	Bits	R/W	Default	Comments	Config
dfe_tap1_en	7	R/W	0	Enable dfe tap1 (summing amplifier)	
dfe_tap2_en	6	R/W	0	Enable dfe tap2(summing amplifier)	
dfe_tap3_en	5	R/W	0	Enable dfe tap3(summing amplifier)	
dfe_tap4_en	4	R/W	0	Enable dfe tap4(summing amplifier)	
dfe_tap_rsv	3	R/W	0	reserved	
lpd_disable_alltap	2	R/W	0	1:Disable all taps when lpd mode 0: not disable	
fast_bias_en	1	R/W	1	1: Fast bias set 0:slow bias set	
band_RST	0	R/W	0	VCO band reset: 0=not reset when FLD detect unlock, 1=reset when FLD detect unlock	

Register:: EQ_1 0xB1					
Name	Bits	R/W	Default	Comments	Config
le_eq_rsv	7:6	R/W	0x00	Reserved	
le_hi_gain_en	5	R/W	0	1:LE high gain mode 0: normal mode	
le_mode_hdmi0_dp1	4	R/W	0	Active when le_hi_gain_mode=1 1:DP 0:HDMI	
le_bias_ehance	3	R/W	1	1:high bit rate 0:low bit rate	
sumamp_bias_ehance	2	R/W	0	1:sumamp bias=125u 0:sumamp bias=100u	
sa_rsel	1	R/W	1	1:low gain/high BW 0: high gain/low BW	
dfe_cmp_hsmode	0	R/W	1	1:high bit rate 0:low bit rate	

Register:: EQ_2 0XB2					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
fore_koffset_en	6	R/W	1	Equalizer foreground offset calibration enable:	

				0: disable 1: enable	
fore_offset_autok	5	R/W	1	Equalizer foreground offset calibration using auto mode: 0: disable 1: enable	
fore_offset_rsv	4:0	R/W	0	Reserved	

Register::Single_End				0xB3	
Name	Bits	R/W	Default	Comments	Config
p0_100k_en	7	R/W	0		
p1_100k_en	6	R/W	0		
p_channel_on	5	R/W	1	switch p channel 50ohm z0 @ used port	
n_channel_on	4	R/W	1	switch n channel 50ohm z0 @ used port	
single_end_rsv	3:0	R/W	0	reserved	

0xB3 Single_End usage:

- [7] p0_100k_en . Port 0 100k
- [6] p1_100k_en . Port 1 100k
- [5] p_channel_on. P switch connected, P z0 en --> valid @ used port
- [4] n_channel_on. N switch connected, N z0 en --> valid @ used port

case 1(Normal)

- [7] p0_100k_en = 1 or 0
- [6] p1_100k_en = 1 or 0
- 50ohm Z0 en
- [5] p_channel_on = 1
- [4] n_channel_on = 1

case 2(Single ended mode for data in P channel)

- [7] p0_100k_en = 1
- [6] p1_100k_en = 1
- 50ohm Z0 en
- [5] p_channel_on = 1
- [4] n_channel_on = 0

case 3(Single ended mode for data in N channel)

- [7] p0_100k_en = 1
- [6] p1_100k_en = 1
- 50ohm Z0 en
- [5] p_channel_on = 0
- [4] n_channel_on = 1

case 4(Power Saving Mode)

- [7] p0_100k_en = 1
- [6] p1_100k_en = 1
- 50ohm Z0 en periodically
- [5] p_channel_on = 1
- [4] n_channel_on = 1

case 5(non HDMI Mode)

- [7] p0_100k_en = 0
- [6] p1_100k_en = 0
- 50ohm Z0 disable
- [5] p_channel_on = 1
- [4] n_channel_on = 1

Register:: Power_0				0XB4	
Name	Bits	R/W	Default	Comments	Config

cmu_en	7:4	R/W	0	CMU_EN[7:0], power control for VCO of lane3..0 0:disable 1:enable	
rx_en	3:0	R/W	0	RX_EN[3:0], power control for Rx channel 3..0, 0:disable 1:enable	

Register:: 2D_switch				0XB5	
Name	Bits	R/W	Default	Comments	Config
z0_tune	7:6	R/W	11	00:43.75 01: 45 10:47.5 11:50 ohm	
freqadd	5	R/W	0	1=VCO frequency shift up	
freqsub	4	R/W	0	1=VCO frequency shift down	
sel_singlecp	3	R/W	0	CDR charge pump single ended	
din_sel	2	R/W	0	0=port 0; 1=port 1 Short P/N at unused port	
z0_autok	1	R/W	1	50 Ohm calibration 0: Register, 1: Auto-Calibration	
rstb_fsm	0	R/W	1	reset mode_det and FLD 0=reset,1=power on	

Register:: Z0_0				0XB6	
Name	Bits	R/W	Default	Comments	Config
p0_z0_en	7:4	R/W	0	0 = disable 50 Ohm on of port0 1 = Z0 turn ON	
z0_adjr	3:0	R/W	8	Manual Control for 50 ohm resistor (both port 0 & port 1)	

Register:: Z0_1				0XB7	
Name	Bits	R/W	Default	Comments	Config
p1_z0_en	7:4	R/W	0	0 = disable 50 Ohm on of port1, 1 = Z0 turn ON	
dfe_rl	3:2	R/W	0		
dfe_rs	1:0	R/W	0		

Register:: Z0_2				0XB8	
Name	Bits	R/W	Default	Comments	Config
dfe_rc_en	7	R/W	1	Resistor process corner 1: dfe_rl dfe_rs from dfe_rc_code 0: (00/01 typical 10: max 11:min)	
dfe_rc_code	6:5	R	0	DFE read back code	
z0_tst	4:0	R	0	50 Ohm termination debug output	

Register:: Reserved_3				0xB9	
Name	Bits	R/W	Default	Comments	Config
offset_adjr3 [4]	7	R/W	1	1: Lane3 foreground calibration input code MSB	
offset_adjr2 [4]	6	R/W	1	1: Lane2 foreground calibration input code MSB	
offset_adjr1 [4]	5	RW	1	1: Lane1 foreground calibration input code MSB	
offset_adjr0 [4]	4	R/W	1	1: Lane0 foreground calibration input code MSB	
offset_adjr_rsv	3:0	R/W	0	Reserved	

Register::EQ_3				0xBA	
Name	Bits	R/W	Default	Comments	Config

offset_tst_lane3[4]	7	R	0	1.. Lane3 foreground calibration MSB	
offset_tst_lane2[4]	6	R	0	1: Lane2 foreground calibration MSB	
offset_tst_lane1[4]	5	R	0	1: Lane1 foreground calibration MSB	
offset_tst_lane0[4]	4	R	0	1: Lane0 foreground calibration MSB	
offset_range	3:2	R/W	1	Offset calibration current range: 2'b00=+/-22.5u, 2'b01=+/-45u, (default) 2'b10=+/-45u, 2'b11=+/-90u,	
bypass_ok	1	R/W	0	bypass calibration ok signal 1'b1=bypass, 1'b0=auto use calibration ok (default)	
rsserved	0	R/W	0	rsserved	

Register:: BandGap 0XBB					
Name	Bits	R/W	Default	Comments	Config
offcal_range	7:6	R/W	1	Offset calibration current range: 2'b00=+/-22.5u, 2'b01=+/-45u, (default) 2'b10=+/-45u, 2'b11=+/-90u,????	
bypass_ok	5	R/W	0	bypass calibration ok signal 1'b1=bypass, 1'b0=auto use calibration ok (default)	
reserved	4:3	R/W	0	reserved	
psm	2	R/W	0	1=CDR in power saving mode,only output ref clock	
reserved	1:0	R/W	0	Reserved	

lane 01 Calibration value

Register:: EQ_4 0xBC					
Name	Bits	R/W	Default	Comments	Config
offset_tst_lane0[3:0]	7:4	R	0	Calibration offset value of lane 0	
offset_tst_lane1[3:0]	3:0	R	0	Calibration offset value of lane 1	

lane 23 Calibration value

Register:: EQ_5 0xBD					
Name	Bits	R/W	Default	Comments	Config
offset_tst_lane2[3:0]	7:4	R	0	Calibration offset value of lane 2	
offset_tst_lane3[3:0]	3:0	R	0	Calibration offset value of lane 3	

Register:: EQ_6 0xBE					
Name	Bits	R/W	Default	Comments	Config
offset_adjr0[3:0]	7:4	R/W	8	OFFSET_ADJR<3:0> of lane0	
offset_adjr1[3:0]	3:0	R/W	8	OFFSET_ADJR<3:0> of lane1	

Register:: EQ_7 0xBF					
Name	Bits	R/W	Default	Comments	Config
offset_adjr2[3:0]	7:4	R/W	8	OFFSET_ADJR<3:0> of lane2	
offset_adjr3[3:0]	3:0	R/W	8	OFFSET_ADJR<3:0> of lane3	

0xC0~0xC7 HDMI counter For Mode Detect (Useless)

Register::TMDS_CONT_0 0XC0					
Name	Bits	R/W	Default	Comments	Config
r_cont_hi[8]	7	R/W	1		
r_cont_mhi[8]	6	R/W	1		
r_cont_mid[8]	5	R/W	0		
r_cont_mlo[8]	4	R/W	0		
r_cont_lo[8]	3	R/W	0		
reserved	2:0	R/W	0		

Register:: TMDS_CONT_1 0XC1					
Name	Bits	R/W	Default	Comments	Config
r_cont_hi[7:0]	7:0	R/W	D9		

Register:: TMDS_CONT_2 0XC2					
Name	Bits	R/W	Default	Comments	Config
r_cont_mhi[7:0]	7:0	R/W	06		

Register:: TMDS_CONT_3 0XC3					
Name	Bits	R/W	Default	Comments	Config
r_cont_mid[7:0]	7:0	R/W	83		

Register:: TMDS_CONT_4 0XC4					
Name	Bits	R/W	Default	Comments	Config
r_cont_mlo[7:0]	7:0	R/W	42		

Register:: TMDS_CONT_5 0XC5					
Name	Bits	R/W	Default	Comments	Config
r_cont_lo[7:0]	7:0	R/W	19		

Register:: TMDS_CONT_6 0XC6					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
r_cont_divider	6:0	R/W	20	Refer to PPT	

Register:: TMDS_CONT_7 0XC7					
Name	Bits	R/W	Default	Comments	Config
r_cont_timer_rsv	7:3	R/W	0	Reserved	
r_cont_timer	2:0	R/W	2	Refer to PPT	

FLDCOUNTER →

$$\frac{\text{Ck_ref}}{\text{Fld_ref_cont}} = \frac{\text{Ck_sys}}{\text{Fld_cdr_cont}}$$

Fld_cdr_cont →
1. HDMI

	Ck_ref	24.3MHz	Bin	Hex
HDMI	Fld_ref_cont0	320	1 01000000	1 40
	Fld_cdr_cont0	320	1 01000000	1 40

2. DP

		Xtal_en=1			
	Ck_ref	24.3MHz	Counter -1	Bin	Hex
5.4Gbps	Fld_ref_cont2	27	26	0 00011010	0 1A
	Fld_cdr_cont2	300	299	1 00101011	1 2D
HBR(2.7Gbps)	Fld_ref_cont1	27	26	0 00011010	0 1A
	Fld_cdr_cont1	300	299	1 00101011	1 2D
RBR(1.62Gbps)	Fld_ref_cont0	45	44	0 00101100	0 2C
	Fld_cdr_cont0	300	299	1 00101011	1 2D

EX :

24.3	=	270
HBR	27	300

;

24.3	=	162
RBR:	45	300

Register:: FLD_CONT_0					0XC8
Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont0[8]	7	R/W	1		
fld_ref_cont0[8]	6	R/W	1		

reserved	5	R/W	0		
fld_cdr_delta	4:0	R/W	5		

Register:: FLD_CONT_1				0XC9	
Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont0[7:0]	7:0	R/W	40		

Register:: FLD_CONT_2				0XCA	
Name	Bits	R/W	Default	Comments	Config
fld_ref_cont0[7:0]	7:0	R/W	40		

Register:: FLD_CONT_3				0xcb	
Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont1[8]	7	R/W	1		
fld_ref_cont1[8]	6	R/W	0		
fld_cdr_cont2[8]	5	R/W	1		
fld_ref_cont2[8]	4	R/W	0		
fld_ref_cont_rsv	3:0	R/W	0	Reserved	

Register:: FLD_CONT_4				0xcc	
Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont1[7:0]	7:0	R/W	2D		

Register:: FLD_CONT_5				0xcd	
Name	Bits	R/W	Default	Comments	Config
fld_ref_cont1[7:0]	7:0	R/W	1A		

Register:: FLD_CONT_6				0xce	
Name	Bits	R/W	Default	Comments	Config
fld_cdr_cont2[7:0]	7:0	R/W	2D		

Register:: FLD_CONT_7				0xcf	
Name	Bits	R/W	Default	Comments	Config
fld_ref_cont2[7:0]	7:0	R/W	1A		

Register:: RXMISC_3				0xd0	
Name	Bits	R/W	Default	Comments	Config
LANE_MUX_SEL	7:0	R/W	E4	select the data mapping between physical lane and MAC lane [7:6]: lane3 data comes from physical lane # 2'b00: physical lane0 2'b01: physical lane1 2'b10: physical lane2 2'b11: physical lane3 (default) [5:4]: lane2 data comes from physical lane # 2'b00: physical lane0 2'b01: physical lane1 2'b10: physical lane2 (default) 2'b11: physical lane3 [3:2]: lane1 data comes from physical lane # 2'b00: physical lane0 2'b01: physical lane1 (default)	

				2'b10: physical lane2 2'b11: physical lane3 [1:0]: lane0 data comes from physical lane # 2'b00: physical lane0 (default) 2'b01: physical lane1 2'b10: physical lane2 2'b11: physical lane3	
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Register:: RXMISC_4				0XD1	
Name	Bits	R/W	Default	Comments	Config
SAMPLE	7:4	R/W	0	SAMPLE edge selector of each lane 0:positive clock edge of DP clock 1:negative clock edge of DP clock (analog / digital phy clk inverse)	
REG_PN_SWAP	3:0	R/W	0	REG_PN_SWAP, swap pn to avoid pn mismatch (digital phy)	

Register:: Reserved_4				0xD2	
Name	Bits	R/W	Default	Comments	Config
dphy_debug_sel	7	R/W	0	D_PHY and D-DFE debug selection: 0: D_PHY 1: D_DFE	
dig_phy1_rsv	6:0	R/W	0	Reserved	

Register:: Reserved_5				0xD3	
Name	Bits	R/W	Default	Comments	Config
dig_phy2_rsv	7:0	R/W	0	Reserved	

Register:: Reserved_6				0xD4	
Name	Bits	R/W	Default	Comments	Config
dig_phy3_rsv	7:0	R/W	0	Reserved	

Register:: Reserved_7				0xD5	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: Reserved_8				0xD6	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: Reserved_9				0xD7	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: VCO_0				0XD8	
Name	Bits	R/W	Default	Comments	Config
dfvco_lane0_rsv	7	R/W	0	Reserved	
dfvco_lane0	6:0	R	0	FLD lane0 VCO auto calibration result	

Register:: VCO_1				0XD9	
Name	Bits	R/W	Default	Comments	Config
dfvco_lane1_rsv	7	R/W	0	Reserved	

dfvco_lane1	6:0	R	0	FLD lane1 VCO auto calibration result	
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Register:: VCO_2					
0XDA					
Name	Bits	R/W	Default	Comments	Config
dfvco_lane2_rsv	7	R/W	0	Reserved	
dfvco_lane2	6:0	R	0	FLD lane2 VCO auto calibration result	

Register:: VCO_3					
0XDB					
Name	Bits	R/W	Default	Comments	Config
dfvco_lane3_rsv	7	R/W	0	Reserved	
dfvco_lane3	6:0	R	0	FLD lane3 VCO auto calibration result	

Register:: VCO_4					
0xDC					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	R/W	0	Reserved	
rfvco_lane0	6:0	R/W	3F	FLD Manual set Lane0 vco band selection=0~127	

Register:: VCO_5					
0xDD					
Name	Bits	R/W	Default	Comments	Config
rfvco_lane1_rsv	7	R/W	0	Reserved	
rfvco_lane1	6:0	R/W	3F	FLD Manual set Lane1 vco band selection=0~127	

Register:: VCO_6					
0xDE					
Name	Bits	R/W	Default	Comments	Config
rfvco_lane2_rsv	7	R/W	0	Reserved	
rfvco_lane2	6:0	R/W	3F	FLD Manual set Lane2 vco band selection=0~127	

Register:: VCO_7					
0xDF					
Name	Bits	R/W	Default	Comments	Config
rfvco_lane3_rsv	7	R/W	0		
rfvco_lane3	6:0	R/W	3F	FLD Manual set Lane3 vco band selection=0~127	

Register:: DIG_00					
0xE0					
Name	Bits	R/W	Default	Comments	Config
CTL_SEL	7	R/W	1	CTL_SEL, select primary control signal 0:from primary input 1:from SI	
SI_X1X2_SEL	6	R/W	1	SI_X1X2_SEL, interface clock rate selector 0:16 bits 1:8 bits	
SI_ENCH_MODE	5	R/W	0	SI_ENCH_MODE, enhanced control mode enable	
SI_HD_DP_SEL	4	R/W	1	SI_HD_DP_SEL, HDMI/DP selector 0: DP, 1: HDMI	
HDMI_X4_SEL	3:0	R/W	0	HDMI_X4_SEL HDMI clock divided by 4 mode	

Register:: DIG_01					
0xE1					
Name	Bits	R/W	Default	Comments	Config
DP_CLK_INV	7:4	R/W	0	DP_CLK_INV, inverse dp_clk clock (digital phy / mac clock inverse)	
DP_CLKX2_INV	3:0	R/W	0	DP_CLKX2_INV, inverse dp_clkx2 clock	

Register:: DIG_02 0xE2					
Name	Bits	R/W	Default	Comments	Config
SCRAMB_DIS	7	R/W	0	SCRAMB_DIS, disable de-scrambling	
COMMA_DIS	6	R/W	0	COMMA_DIS, disable comma detection enable when D10.2 input	
COMSEL	5:3	R/W	0	COMSEL, comma number selector 000: 3 comma 001: 4 comma 010: 6 comma 011: 8 comma 100: 10 comma 101: 12 comma 110: 14 comma 111: 16 comma	
PRBS_REVERSE	2	R/W	0	PRBS_REVERSE, reverse PRBS7 pattern generator	
Reserve_dig_00	1	R/W	0	1: 4 symbol match {SR,BF/3C,BF/3C,SR} →scrambler reset 0 : 3 symbol match → scrambler reset	
RXBIST_CLK	0	R/W	0	RXBIST CLK selector 0: from analog cdr clk 1:form TX clock	

Register:: DIG_03 0xE3					
Name	Bits	R/W	Default	Comments	Config
ERROR_COUNT_CLEAR	7	R/W	0	Error count clear	
RXBIST_SOURCE	6:5	R/W	0	RXBIST_SOURCE, rx bist source selection 00: from PMA(normal function) 01: from comdet input 10: from 10b8b input 11: from de-scrambling input	
RXBIST_DEST	4:3	R/W	0	RXBIST_DEST, rx bist destination selection 00: disable rxbist 01: to comdet output 10: to 10b8b output 11: to de-scrambling output	
PRBS_SEL	2	R/W	0	PRBS_SEL, prbs pattern selection 0: prbs 7 1: prbs31	
dig_03_rsv	1:0	R/W	0	Reserved	

Register:: DIG_04 0xE4					
Name	Bits	R/W	Default	Comments	Config
BIST_SEED	7:0	R/W	0	BIST_SEED, bist seed pattern	

Register:: DIG_05 0xE5					
Name	Bits	R/W	Default	Comments	Config
RX_DEBUG[7]	7	R/W	0	RX digital debug	
RX_DEBUG[6:5]	6:5	R/W	0	Bist lane select 00: lane0 ; 01: lane1; 10: lane2; 11: lane3	
RX_DEBUG[4:0]	4:0	R/W	0		

Register:: DIG_06 0xE6					
Name	Bits	R/W	Default	Comments	Config
BYTE_COUNT_MSB	7:0	R	0	BYTE_COUNT[15:8], received packet number	

Register:: DIG_07					0xE7
Name	Bits	R/W	Default	Comments	Config
BYTE_COUNT_LSB	7:0	R	0	BYTE_COUNT[7:0], received packet number	

Register:: DIG_08					0xE8
Name	Bits	R/W	Default	Comments	Config
RXBIST_ERR_CNT	7:0	R	0	RXBIST_ERR_CNT, received error counter	

Remove 0xE9~0xEF for HDMI Tx Test Chip

Register:: SSCG_DIG					0XE9
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	R/W	0	RESERVED	
ASSR_MODE	0	R/W	1	0: ASSR mode	

Register:: DIG_TX_00					0xEA
Name	Bits	R/W	Default	Comments	Config
dig_tx_00_rsv	7:0	R/W	0	RESERVED	

Register:: DIG_TX_01					0xEB
Name	Bits	R/W	Default	Comments	Config
dig_tx_01_rsv	7:0	R/W	0	Reserved	

Register:: DIG_TX_02					0xEC
Name	Bits	R/W	Default	Comments	Config
dig_tx_02_rsv	7:0	R/W	0	Reserved	

Register:: DIG_TX_03					0xED
Name	Bits	R/W	Default	Comments	Config
dig_tx_03_rsv	7:0	R/W	0	Reserved	

Register:: Reserved_A					0xEE
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register::DIG_TX_04					0xEF
Name	Bits	R/W	Default	Comments	Config
dig_tx_04_rsv	7:0	R/W	0	Reserved	

Register:: AUX_1					0xF0
Name	Bits	R/W	Default	Comments	Config
AUX_VLDO	7:5	R/W	4	Voltage mode LDO output voltage: 000: 300mv 001: 450mv 010: 600mv 011: 750mv 100: 900mv(default) 101: 1050mv 110: 1200mv 111: 1300mv	
AUX_SELVCOM	4	R/W	0	Select RX common mode 's generation : 0:from I*R (50u@3.3V)	

				1:from R array (only 10u@1.2V)	
AUX_ADJR	3:0	R/W	8	AUX 50 ohm resistor hand mode set	

Register:: AUX_2 0xF1					
Name	Bits	R/W	Default	Comments	Config
AUX_AUTO_K	7	R/W	1	AUX 50 ohm calibration enable : 0:disable 1:enable	
AUX_SE_FROM_MP	6	R/W	1	Aux single ended input from Channel P	
AUX_SE_SINGLEEND	5	R/W	0	Enable aux single ended input decode function	
AUX_SEL_THRESHOLD	4:3	R/W	3	AUX channel input threshold selection 00:25mv 01:50mv 10:75mv 11:100mv	
AUX_ENTST	2	R/W	0	Aux debug enable	
EN_AUX_PSM	1	R/W	0	Enable aux power saving mode	Wport Rport
EN_AUX_RX_BIGZ0	0	R/W	0	Enlarge aux rx termination resistance	

Register:: AUX_3 0xF2					
Name	Bits	R/W	Default	Comments	Config
EN_AUX_PSM_BIAS	7	R/W	0	Aux power saving mode's bias come from bandgap	Wport Rport
AUX_TST	6:1	R	0	Aux block debug signal out	
AUX_Z0_OK	0	R	0	Aux Z0 calibration output	

Register:: AUX_4 0xF3					
Name	Bits	R/W	Default	Comments	Config
AUX_REV_7_6	7:6	R/W	3	AUX common mode voltage buffer bias current select 00,250u@1.2V 01,450u@1.2V 10,850u@1.2V 11,1050u@1.2V	Wport Rport
AUX_REV_5_1	5:1	R/W	0	RESERVED	
AUX_REV_0	0	R/W	0	1.Turn off D2 DDA 0.Normal	Wport Rport

Register:: AUX_5 0xF4					
Name	Bits	R/W	Default	Comments	Config
AUX_RSTB	7	R/W	1	Aux rstb , should toggle this bit to enable auto k and other timing sequence.	
DDA_50U_D2	6	R/W	0	Normal Mode: Bias from bandgap 0: old mode (default) 1: new mode. I/2	
DDA_PSM_50U_D2	5	R/W	1	Power Saving Mode: Bias from Constant GM 0: old mode 1: new mode. I/2 (default)	
bg_psm	4	R/W	0	Bandgap power saving mode	Wport Rport
bg_en	3	R/W	1	BG_EN	Wport Rport
bg_db	2:0	R/W	4	3'b000=1.155V, 3'b001=1.167V, 3'b010=1.178V 3'b011=1.19V, 3'b100=1.202V, 3'b101=1.213V 3'b110=1.225V, 3'b111=1.237V,	Wport Rport

Register::: HW_AUTO_PS 0xF5					
Name	Bits	R/W	Default	Comments	Config
FW_DBUF	7	R	0	Double buffer of Page B F1[1], F2[7], F3[7:6][0], F4[4:0], F5[1] setting 1: FW load setting 0: no action	Wclr_out
FW_DBUF_EN	6	R/W	0	1:FW double buffer 0xF5[7] enable 0:Disable	
HW_AUTO_ENTER_PS_AUX_EN	5	R/W	0	HW load Page B F1[1], F2[7], F3[7:6][0], F5[1] setting to enter power saving mode for AUX 1: HW load setting when aux idle 0: Disable	Wport Rport
HW_AUTO_ENTER_PS_BB_EN	4	R/W	0	HW load Page B F4[4:0] setting to enter power saving mode for bandgap 1: HW load setting when aux idle 0: Disable	Wport Rport
HW_AUTO_EXIT_PS_AUX_EN	3	R/W	0	HW reset PageB F1[1], F2[7], F3[7:6][0] and F5[1] to exit power saving mode for AUX 1: HW reset setting when receive aux signal 0: Disable	Wport Rport
HW_AUTO_EXIT_PS_BB_EN	2	R/W	0	HW reset Page B F4[4:0] to exit power saving mode for bandgap 1: HW reset setting when receive aux signal 0: Disable	Wport Rport
SINGLE_END_MODE	1	R/W	0	1: receive single end data (collocate analog) 0: disable	Wport Rport
HW_AUTO_REV	0	R/W	0	Reserved	

Register::: TXBIST_00 0XF6					
Name	Bits	R/W	Default	Comments	Config
target_cont_lo[8]	7	R/W	0	when dp_rate=00 RBR target counter	
target_cont_mlo[8]	6	R/W	0	when tp1 dp_rate=01 HBR target counter	
target_cont_mid[8]	5	R/W	0	when tp1 dp_rate=10 target counter	
target_cont_mhi[8]	4	R/W	0	when tp1 dp_rate=11 reserved	
reserved	3	R/W	0		
same_timer	2:0	R/W	2		

Register::: TXBIST_01 0XF7					
Name	Bits	R/W	Default	Comments	Config
target_cont_lo[7:0]	7:0	R/W	30	when dp_rate=00 RBR target counter	

Register::: TXBIST_02 0XF8					
Name	Bits	R/W	Default	Comments	Config
target_cont_mlo[7:0]	7:0	R/W	50	when tp1 dp_rate=01 HBR target counter	

Register::: TXBIST_03 0XF9					
Name	Bits	R/W	Default	Comments	Config
target_cont_mid[7:0]	7:0	R/W	60	when tp1 dp_rate=10 target counter	

Register:: TXBIST_04				0XFA	
Name	Bits	R/W	Default	Comments	Config
target_cont_mhi[7:0]	7:0	R/W	A0	when tp1 dp_rate=11 reserved	

Register:: TXBIST_05				0xFB	
Name	Bits	R/W	Default	Comments	Config
reserved	7	R/W	0		
div_num_oob	6:0	R/W	10	clock rate divider	

Register:: TXBIST_06				0xFC	
Name	Bits	R/W	Default	Comments	Config
ref_tp1_lane0[9:8]	7:6	R	0	report counter value	
reserved	5:1	R	0		
ref_mode_out[8]	0	R	0	debug port for tp1 detection signal	

Register:: TXBIST_07				0xFD	
Name	Bits	R/W	Default	Comments	Config
ref_tp1_lane0[7:0]	7:0	R	0	report counter value	

Register:: TXBIST_08				0xFE	
Name	Bits	R/W	Default	Comments	Config
ref_mode_out[7:0]	7:0	R	0	debug port for tp1 detection signal	

Register:: RXBIST_0				0xFF	
Name	Bits	R/W	Default	Comments	Config
tp1_det_manual	7	R/W	0	1: tp1 detected 0: no tp1 signal	
tp1_det_manual_sel	6	R/W	0	1: use tp1_det_manual 0: report tp1 by auto fsm (use tp1 detect function)	
reserved	5	R/W	0		
target_cont_delta	4:0	R/W	0	tolerance counter error	

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DisplayPort MAC (Page C)
**MAC CONTROL
GLOBAL CONTROL**

Register:: DP_CTRL 0xA1					
Name	Bits	R/W	Default	Comments	Config
DP_RESET	7	R/W	0	DisplayPort power down and all of DP registers will be cleared to default 0:Normal. 1:Reset. (whole page C registers reset)	Rport wport
DP_POW_DN	6	R/W	1	DisplayPort power down(hardware only) 0: power on. 1: power down.	
HD_DP_SEL	5	R/W	1	HDMI/DisplayPort Selector 0: DisplayPort 1: HDMI	
LANE_NUM	4:3	R/W	0	The number of lanes. 00: reserved 01: 1-lane. 10: 2-lane. 11: 4-lane.	Hw_write
ENHANCE_MD	2	R/W	1	Enhanced mode of control symbols for framing. 0: disable. 1: enable.	Hw_write
CP_TEST_MD	1	R/W	0	CP mode. 0: Nomal. 1: CP.	
PN_SWAP	0	R/W	0	PN Swap 0: no swap. 1: swap.	

Register:: DP_OUTPUT_CTRL 0xA2					
Name	Bits	R/W	Default	Comments	Config
ROUT_EN	7	R/W	0	R output enable. (It will be also disabled when video watch-dog occurred) 0: disable. 1: enable.	Rport wport
GOUT_EN	6	R/W	0	G output enable. (It will be also disabled when video watch-dog occurred) 0: disable. 1: enable.	Rport wport
BOUT_EN	5	R/W	0	B output enable. (It will be also disabled when video watch-dog occurred) 0: disable. 1: enable.	Rport wport
OCLK_EN	4	R/W	0	CLK output enable. (It will be also disabled when video watch-dog occurred) 0: disable. 1: enable.	
PR_RESET	3	R/W	0	Reset pr_unpack block 1:reset 0: normal operation	
AUTO_SET_LANE	2	R	0	Lane-and Enhancement Auto Configuration Hardware automatically write 0xA1[4:2] based on	Wclr_out

				DPCD 0x100 & 0x101.(Write 1 to load.) 0: manual 1: auto load	
AUTO_SET_ENH	1	R	0	<p><u>Bit depth and Component format Auto Configuration</u></p> <p>Hardware automatically write B4-31 based on B4-02. (Write 1 to load.)</p> <p>Enhancement Auto Configuration</p> <p>0: manual 1: auto load</p>	Wclr_out
AUTO_SET_DISP	0	R	0	<p>Display Format Auto Configuration</p> <p>Hardware automatically write pop-up and write B4-3E~B4-4D based on B4-04~B4-15. (Write 1 to load.)</p> <p><u>Bit depth and Component format Auto Configuration</u></p> <p>Hardware automatically write B4-31 based on B4-02. (Write 1 to load.)</p> <p>0: manual 1: auto load</p>	Wclr_out

Register::: DP_OUTPUT_CLK_CTRL 0xA3					
Name	Bits	R/W	Default	Comments	Config
OCLK_INV	7	R/W	0	CLK output inverse. 0: not inverse. 1: inverse.	
Reserved	6	--	0	<p><u>Pixel de repetition auto mode.</u></p> <p>0: manual. 1: auto.</p> <p>Reserved</p>	
AUTO_SET_VTT_E_O	5	R/W	0	Atcive when AUTO_SET_DISP = 1 1: vtotal from stream attribute EVEN 0: vtotal from stream attribute ODD	
DPF_RESET	4	R/W	0	Reset Display Format Block 1: DPF reset 0: normal	
DP_OUTPUT_RSV	3:0	R/W	0	<p><u>Pixel de repetition ratio.</u></p> <p>(manual mode: R/W; auto mode: R-only)</p> <p>0000: no action. 0001: div2. 0010: div3. 0011: div4. 0100: div5. 0101: div6. 0110: div7. 0111: div8. 1000: div9. 1001: div10. other: no action.</p>	

				Reserved	
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Register:: DP_LANE_SWAP 0xA4				
Name	Bits	R/W	Default	Comments
LANE0_SOURCE	7:6	R/W	0	The source selector of lane0. Used for lane swap. 00: lane0. 01: lane1. 10: lane2. 11: lane3.
LANE1_SOURCE	5:4	R/W	1	The source selector of lane1. Used for lane swap. 00: lane0. 01: lane1. 10: lane2. 11: lane3.
LANE2_SOURCE	3:2	R/W	2	The source selector of lane2. Used for lane swap. 00: lane0. 01: lane1. 10: lane2. 11: lane3.
LANE3_SOURCE	1:0	R/W	3	The source selector of lane3. Used for lane swap. 00: lane0. 01: lane1. 10: lane2. 11: lane3.

Notice: All the following lane numbers in this spec are after swapping.

LANE STATUS

//The following byte is read-only.

Register:: DP_LANE_VALID 0xA5				
Name	Bits	R/W	Default	Comments
LANE0_INVALID	7	R/W	1	Lane0 PHY stable or not 1: not ready. 0: ready. (Write 1 to clear)
LANE1_INVALID	6	R/W	1	Lane1 PHY stable or not 1: not ready. 0: ready. (Write 1 to clear)
LANE2_INVALID	5	R/W	1	Lane2 PHY stable or not 1: not ready. 0: ready. (Write 1 to clear)
LANE3_INVALID	4	R/W	1	Lane3 PHY stable or not 1: not ready. 0: ready. (Write 1 to clear)
LANE0_DEC_ERR	3	R/W	0	ANSI 8B/10B decode error. (Read_only) 0: no error. 1: error happened. Write 1 to clear.
LANE1_DEC_ERR	2	R/W	0	ANSI 8B/10B decode error. (Read_only) 0: no error. 1: error happened. Write 1 to clear.
LANE2_DEC_ERR	1	R/W	0	ANSI 8B/10B decode error. (Read_only) 0: no error.

				1: error happened. Write 1 to clear.	
LANE3_DEC_ERR	0	R/W	0	ANSI 8B/10B decode error. (Read_only) 0: no error. 1: error happened. Write 1 to clear.	Rport Wport

Register:: DP_LANE_CDR 0xA6					
Name	Bits	R/W	Default	Comments	Config
LANE0_CDR_NRDY	7	R/W	0	Lane0 PHY CDR lock. 0: locked. 1: non-locked. (Write 1 to clear)	Rport Wport
LANE1_CDR_NRDY	6	R/W	0	Lane1 PHY CDR lock. 0: locked. 1: non-locked. (Write 1 to clear)	Rport Wport
LANE2_CDR_NRDY	5	R/W	0	Lane2 PHY CDR lock. 0: locked. 1: non-locked. (Write 1 to clear)	Rport Wport
LANE3_CDR_NRDY	4	R/W	0	Lane3 PHY CDR lock. 0: locked. 1: non-locked. (Write 1 to clear)	Rport Wport
VFIFO_OVF_UNI	3	R	0	Video FIFO overflows earlier than underflow. 0: not overflow. 1: overflow. Write 1 to clear.	Wclr_out
SFIFO_UDF_UNI	2	R	0	Small FIFO underflows earlier than overflow. 0: not underflow. 1: underflow. Write 1 to clear.	Wclr_out
SP_DET	1:0	R	0	00: 1.62G 01: 2.7G 1X: others	

Register:: MN_CH_SYNC 0xA7					
Name	Bits	R/W	Default	Comments	Config
LANE0_CLK_INV_ST	7	R/W	0	Case1: lane0_clk_inv_auto=0 Lane1 clk inverse or not is controlled by this register. 0: not inverse. 1: inverse. Case2: lane0_clk_inv_auto=1 Reveal Lane0 clk inverse status. (Read only) 0: not inverse. 1: inverse.	Rport Wport
LANE1_CLK_INV_ST	6	R/W	0	Case1: lane1_clk_inv_auto=0 Lane1 clk inverse or not is controlled by this register.	Rport Wport

				0: not inverse. 1: inverse. Case2: lane1_clk_inv_auto=1 Reveal Lane1 clk inverse status. (Read only) 0: not inverse. 1: inverse.	
LANE2_CLK_INV_ST	5	R/W	0	Case1: lane2_clk_inv_auto=0 Lane2 clk inverse or not is controlled by this register. 0: not inverse. 1: inverse. Case2: lane2_clk_inv_auto=1 Reveal Lane2 clk inverse status. (Read only) 0: not inverse. 1: inverse.	Rport Wport
LANE3_CLK_INV_ST	4	R/W	0	Case1: lane3_clk_inv_auto=0 Lane3 clk inverse or not is controlled by this register. 0: not inverse. 1: inverse. Case2: lane3_clk_inv_auto=1 Reveal Lane3 clk inverse status. (Read only) 0: not inverse. 1: inverse.	Rport Wport
LANE0_CLK_INV_AUTO	3	R/W	1	Lane 0 clk inverse auto. 0: not auto. 1: auto.	
LANE1_CLK_INV_AUTO	2	R/W	1	Lane 1 clk inverse auto. 0: not auto. 1: auto.	
LANE2_CLK_INV_AUTO	1	R/W	1	Lane 2 clk inverse auto. 0: not auto. 1: auto.	
LANE3_CLK_INV_AUTO	0	R/W	1	Lane 3 clk inverse auto. 0: not auto. 1: auto.	

Register:: MN_DE_SKEW 0xA8					
Name	Bits	R/W	Default	Comments	Config
DESKEW_MODE	7	R/W	0	0: using BE as deskew control pulse 1: using all control signal to deskew	
PP_RST	6	R/W	1	Reset Possibility Priority counter 0: not reset 1: reset	
PP_AUTO_DIV2	5	R/W	1	Auto divide Possibility Priority counters of all lanes by two when one lane's counter reaches maximum value. 0: disable. 1: enable.	
DESKEW_2LCLK_EN	4	R/W	1	Remove 2 link clock skew inserted between lanes. 0: disable. 1: enable.	
DESKEW_WITH_VALID	3	R/W	0	Only de-skew the valid lanes. 0: disable. 1: enable.	

DESKW_LEVEL	2:0	R/W	0	De-skew level selector. This process is after 2-clk inter-lane de-skew. Purpose is to eliminate the skew caused by poor channel consition or channel_sync. Each layer can solve 2-clk skew. 000: No de-skew. 001: 1-layer. 010: 2-layer. 011: 3-layer. 011: 3-layer. 1xx: 4-layer.	
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Register:: MN_ERRC 0xA9					
Name	Bits	R/W	Default	Comments	Config
VIDEO_ERRC_EN	7	R/W	1	Video error correction. (Use interpolation to replace those pixels with ANSI 8B/10B dec_errs) 0: disable. 1: enable.	
AUDIO_ERRC_EN	6	R/W	1	Audio error correction. (Use interpolation to replace those samples with more than 1 err found from RS_decoder) 0: disable. 1: enable.	
STRM_ATTR_ERRC_EN	5	R/W	1	Main stream attributes error correction. (Filter out those attributes different from previous ones.) 0: disable. 1: enable.	
Reserved	4:3	--	0		
CTRL_ERRC_EN	2	R/W	0	Control symbol error correction 1 : enable 0 : disable	
CTRL_ERRC_WARNING	1	R/W	0	4 lanes : more than 2 lanes has control 2 lanes : just 1 lane has control 1 lane : no warning	Rport Wport
CTRL_ERRC_ERROR	0	R/W	0	4 lanes : just 1 lane has control 2 lanes : no error 1 lane : no error	Rport Wport

Register:: MN_ERRC_CTRL 0xAA					
Name	Bits	R/W	Default	Comments	Config
EN_DET	7	R	0	Enhance Mode Detect (write 1 to clear) 0: not enhance mode 1: enhance mode	Wclr_out
MN_RSV2	6:0	R/W	0	reserved	

CRC

Register:: DP_CRC_CTRL 0xAB					
Name	Bits	R/W	Default	Comments	Config

CRC_START	7	R/W	0	Start CRC calculation on next frame. 0: stop and clear CRC(AC~B1) 1: start.	
CRC_DONE	6	R	0	CRC calcuation finished. 0: not finished. 1: finished.	
CRC_NON_STABLE	5	R	0	Active when CRC_START = 1 0: CRC stable until now 1: CRC is non stable	Wclr_out
CR_CB_EN	4	R/W	0	Change R to CR and B to CB enable 0:origin mode CRC_R = CR0 CR0 CR2 CR2... CRC_B = CB0 CB0 CB2 CB2 1:new mode CRC_R = CR0, CR2 , ... CRC_B = CB0, CB2, ...	
CR_CB_SWITCH	3	R/W	0	Monitor CB CR CRC in 0xBE,0xBF 0 : CB CR CB CR ... 1: CR CB CR CB...	
CRC_RSV	2:0	R/W	0	Reserved.	

Register:: DP_CRC_R_M 0xAC					
Name	Bits	R/W	Default	Comments	Config
CRC_R_M	7:0	R	0	Bit 15~8 of CRC result of R channel.	

Register:: DP_CRC_R_L 0xAD					
Name	Bits	R/W	Default	Comments	Config
CRC_R_L	7:0	R	0	Bit 7~0 of CRC result of R channel.	

Register:: DP_CRC_G_M 0xAE					
Name	Bits	R/W	Default	Comments	Config
CRC_G_M	7:0	R	0	Bit 15~8 of CRC result of G channel.	

Register:: DP_CRC_G_L 0xAF					
Name	Bits	R/W	Default	Comments	Config
CRC_G_L	7:0	R	0	Bit 7~0 of CRC result of G channel.	

Register:: DP_CRC_B_M 0xB0					
Name	Bits	R/W	Default	Comments	Config
CRC_B_M	7:0	R	0	Bit 15~8 of CRC result of B channel.	

Register:: DP_CRC_B_L 0xB1					
Name	Bits	R/W	Default	Comments	Config

CRC_B_L	7:0	R	0	Bit 7~0 of CRC result of B channel.	
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Register:: DP_MEM_BIST 0xB2					
Name	Bits	R/W	Default	Comments	Config
Ln0_valid	7	R	0	Write 1 to clear 1:lnx valid (catch 3BS+1SR without Error) 0:lnx invalid	Wclr_out
Ln1_valid	6	R	0	Write 1 to clear 1:lnx valid (catch 3BS+1SR without Error) 0:lnx invalid	Wclr_out
Ln2_valid	5	R	0	Write 1 to clear 1:lnx valid (catch 3BS+1SR without Error) 0:lnx invalid	Wclr_out
Ln3_valid	4	R	0	Write 1 to clear 1:lnx valid (catch 3BS+1SR without Error) 0:lnx invalid	Wclr_out
abuf_bist_pass	3	R	0	Bist test result	
abuf_bist_start	2	R/W	0	Write '1' to trigger Video FIFO Bist When reading '0', it represents the bist is done.	Wport rport
vfifo_bist_pass	1	R	0	Bist test result	
vfifo_bist_start	0	R/W	0	Write '1' to trigger Video FIFO Bist When reading '0', it represents the bist is done.	Wport rport

B3,B4 is DP accessing port

Register:: DP_ADR 0xB3					
Name	Bits	R/W	Default	Comments	Config
DP_ADR	7:0	R/W	0	DisplayPort accessing port address.	Rport Wport

Register:: DP_DAT 0xB4					
Name	Bits	R/W	Default	Comments	Config
DP_DAT	7:0	R/W	0	DisplayPort accessing port data.	Rport Wport

Register:: DP_DEBUG_SEL0 0xB5					
Name	Bits	R/W	Default	Comments	Config
phy_dbg_en	7	R/W	0	Enable phy test output. 0: test mac 1: test phy	
block_sel	6:4	R/W	0	Debug output selector. 000: pixel regeneration 001: AUX-CH 010: display format 011: channel recovery 100: sclk gen 101: secondary data 110: reserved 111:aux_phy_dig	

dp_test_sel_pr	3:0	R/W	0	Debug output selector of pixel regeneration	
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Register:: DP_DEBUG_SEL1				0xB6	
Name	Bits	R/W	Default	Comments	Config
dp_test_sel_auxch	7:4	R/W	0	Debug output selector of AUX-CH	
dp_test_sel_df	3:0	R/W	0	Debug output selector of display format	

Register:: DP_DEBUG_SEL2					0xB7	
Name	Bits	R/W	Default	Comments	Config	
dp_test_sel_chrc	7:6	R/W	0	Debug output selector of channel recovery.		
dp_test_sel_sec_data	5:3	R/W	0	Debug output selector of sclk gen		
BS_OCR	2	R	0	BS has occur in bs_lane_choose 1 : occur 0 : not occur write 1 to clear	Wclr_out	
BS_LANE_CHOOSE	1:0	R/W	0	0 : lane0 1 : lane1 2 : lane2 3 : lane3		

Register:: DP_INFO_FM_ADR					0xB8	
Name	Bits	R/W	Default	Comments	Config	
HD_DP_DBG_SEL	7	R/W	0	debug signal select from HDMI or DP 1:HDMI 0:DP		
DP_INFO_FM_ADR	6:0	R/W	0	Info-frame memory address. 00'h~58'h		

Register:: DP_INFO_FM_DAT					0xB9	
Name	Bits	R/W	Default	Comments	Config	
DP_INFO_FM_DAT	7:0	R	0	Info-frame memory dat.		

Register:: DP_RSV0						0xBA	
Name	Bits	R/W	Default	Comments	Config		
DP_RSV0	7:0	R/W	0	Bit 7: GPI_RX3P_EN Bit 6: GPI_RX3N_EN Bit 5: GPI_RX2P_EN Bit 4: GPI_RX2N_EN Bit 3: GPI_RX1P_EN Bit 2: GPI_RX1N_EN Bit 1: GPI_RX0P_EN Bit 0: GPI_RX0N_EN Reserved			

Register:: DP_channel_rec						0xBB
Name	Bits	R/W	Default	Comments		Config
DP_CH_RSV	7:6	R/W	0	DP REXT FUNCITON Enable 0:REXT 1:GPI(Used for BIST_EN by POR) Reserved		
INTRA_DESKEW_EN	5	R/W	1	NEW intra lane deskew enable		
reserved	4	--	--	Reserved		
LANE_ALIGN	3	R	0	1:ctrl align 0:ctrl not align		
SYMB_ERR_CNT_TYPE[1:0]	2:1	R/W	00	00:pattern 00 01:pattern 4A 10:pattern B5 11:pattern 4A or B5		
reserved	0	--	0	Reserved		

Register:: DP_SKEW						0xBC
Name	Bits	R/W	Default	Comments		Config
EH_ERRC	7	R/W	0	active when enhance mode = 1 1: error correction enhance mode in HDCP 0: disable		
SKEW_LANE_SEL	6	R/W	0	0: select LANE0 and LANE1 to report SKEW 1: select LANE2 and LANE3 to report SKEW		
L0_L2_SKEW	5:3	R		L0 or L2 Skew that deskew function fix.		
L1_L3_SKEW	2:0	R		L1 or L3 Skew that deskew function fix.		

Register:: DPCD_600_CTRL						0xBD
Name	Bits	R/W	Default	Comments		Config
DP_DPCD_RSV	7:4	R/W	0	Reserved byte		
Wr_600_en	3	R/W	0	Firmware write DPCD 600 [2:0] enable		
Dpcd_600	2:0	R/W	0	Active when wr_600_en = 1		Rport Wport

Register:: CRC_CB_M						0xBE
Name	Bits	R/W	Default	Comments		Config
CRC_CB[15:8]	7:0	R	0	CRC_CB VALUE when 422		

Register:: CRC_CB_L						0xBF
Name	Bits	R/W	Default	Comments		Config
CRC_CB[7:0]	7:0	R	0	CRC_CB VALUE when 422		

AUX_CH

Register::DPCD_CTRL 0xC0						
Name	Bits	R/W	Default	Comments	Config	
AUXCH_DIG_PWDN	7	R/W	1	0: normal run. 1: power down.	Rport Wport	
AUX_DET	6	R	0	Aux ch active detection. Reserved		
DPCD_REG_PWDN	5	R/W	0	0: normal run 1: power down	Rport Wport	
AUX_MAC_CLK_SEL	4	R/W	0	0: from eclk_ng 1: from xclk		
AUX_ERROR_CNT_AUTO	3	R/W	0	0: error count in DPCD 210-217 by firmware 1: by hardware auto		
IIC_NATIVE_INSERT	2	R	0	1 means when IIC transaction is divided into multiple AUX transaction, Native AUX request is inserted.		
AUX_DATA_FIFO_SEL	1	R/W	0	0: Native AUX Fifo 1: IIC Fifo (for uP access DATA FIFO)		
DPCD_ACCESS_PORT_AUTO_INC	0	R/W	1	1: auto increase 0: keep in the same address.		

C1~C4 is DPCD register accessing port

Register::DPCD_ADDR_PORT_H 0xC1						
Name	Bits	R/W	Default	Comments	Config	
RESERVED	7:4	-	0	Reserved		
ADDR_PORT_H	3:0	R/W	0	Address port (Bits19:16) for embedded DPCD access, auto increase after DATA_PORT being accessed.	Rport wport	

Register::DPCD_ADDR_PORT_M 0xC2						
Name	Bits	R/W	Default	Comments	Config	
ADDR_PORT_M	7:0	R/W	0	Address port (Bits15:8) for embedded DPCD access,auto increase after DATA_PORT being accessed.	Rport wport	

Register::DPCD_ADDR_PORT_L 0xC3						
Name	Bits	R/W	Default	Comments	Config	

ADDR_PORT_L	7:0	R/W	0	Address port (Bits7:0) for embedded DPCD access,auto increase after DATA_PORT being accessed.	Rport wport
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Register::DPCD_DATA_PORT 0xC4					
Name	Bits	R/W	Default	Comments	Config
DATA_PORT	7:0	R/W	0	Data port for embedded DPCD access	Rport wport

Register:: AUX_PHY_DIG1 0xC5					
Name	Bits	R/W	Default	Comments	Config
AVE_POS	7:3	R/W	0x18	Average start position (average 8 cycles)	
AUX_CLKSEL	2:1	R/W	0	Active whe C6[7] = 0 00:27Mhz 01:25Mhz 150Mhz 10:24,576Mhz 120Mhz 11,14,318MHz	
AUX_PN_SWAP	0	R/W	0	AUX CHANNEL PN SWAP 0: no swap 1: swap	

Register:: AUX_PHY_DIG2 0xC6					
Name	Bits	R/W	Default	Comments	Config
AUX_CLKSEL_AUTO_EN	7	R/W	1	Used Rx counter value to set the AUX CLK select	
AUX_NEW_MODE	6	R/W	1	1. modify the sync pattern 0. origin mode	
aux_phy_clk200m_en	5	R/W	0	aux phy use 150M clk to sample AUX_D1	
FAKE_LT_EN	4	R/W	0	Fake link training enable Active when D0[2] = 1	
FLT_SWING	3:2	R/W	2	Fake link training swing level 00: level 0 01: level 1 10: level 2 11: level 3	
FLT_PREM	1:0	R/W	1	Fake link training pre-amphasis level 00: level 0 01: level 1 10: level 2 11: level 3	

Register:: AUX_RESERVE2 0xC7					
Name	Bits	R/W	Default	Comments	Config

TP1_OCR	7	R	0	Training pattern 1 has occurred	Wclr_out
TP2_OCR	6	R	0	Training patter 2 has occurred	Wclr_out
TEND_OCR	5	R	0	Training pattern end has occured	Wclr_out
PCHARGE_NUM	4:0	R/W	9	When AUX_RX in precharge state, it will go to Sync0 state when receiving “prechare_num” number of toggle count.	

Register:: AUX_PHY_DIG3				0xC8	
Name	Bits	R/W	Default	Comments	Config
AVE_MAN_EN	7	R/W	0	1.manual mode 0.auto mode	
AVE_NUM	6:0	R/W	D	Average Number	

Register:: AUX_RSV				0xC9	
Name	Bits	R/W	Default	Comments	Config
AUX_RSV	7:0	R/W	0	Reserved byte	

Register:: READ_RESERVE0				0xCA	
Name	Bits	R/W	Default	Comments	Config
read_reserve0	7:0	R	0	Reserved byte	

Register:: READ_RESERVE1				0xCB	
Name	Bits	R/W	Default	Comments	Config
read_reserve1	7:0	R	0	Reserved byte	

Register:: LANE0_OUT				0xCC	
Name	Bits	R/W	Default	Comments	Config
LANE0_DATA	7:0	R	0	Lane0 D10.2 Decode Data	

Register:: LANE1_OUT				0xCD	
Name	Bits	R/W	Default	Comments	Config
LANE1_DATA	7:0	R	0	Lane1 D10.2 Decode Data	

Register:: LANE2_OUT				0xCE	
Name	Bits	R/W	Default	Comments	Config
LANE2_DATA	7:0	R	0	Lane2 D10.2 Decode Data	

Register:: LANE3_OUT				0xCF	
Name	Bits	R/W	Default	Comments	Config

Name	Bits	R/W	Default	Comments	Config
LANE3_DATA	7:0	R	0	Lane3 D10.2 Decode Data	

Register:: AUX_MODE_SET 0xD0					
Name	Bits	R/W	Default	Comments	Config
TIMEOUT_TARGET[3:0]	7:4	R/W	F	LSB of Timeout target value settings (set with 0xF4[4:3])	
ERROR_RST_FSM_EN	3	R/W	0	1: if rx_error, reset AUX FSM (不用驗) 0: disable	
DP_LINK_TRANS_EN	2	R/W	0	Enable Automatically Link Training Process. (set with 0xC6[4])	
DP_AUX_AUTO_EN	1	R/W	1	Native AUX-CH handle selection: 0 : Firmware handle AUX-CH request. 1 : Hardware handle AUX-CH request. If bit1=0 DPCD Read only register can WRITE	
DP_AUX_EN	0	R/W	0	Enable DisplayPort AUX channel	

Register:: DP_IIC_SET 0xD1					
Name	Bits	R/W	Default	Comments	Config
IIC_CK_PRD	7:4	R/W	1	IIC SCL clock frequency settings. SCL Period = 37ns * 16 * (IIC_CK_PRD + 1)	
IGN_RX_ERROR	3	R/W	0	1: ignore rx error 0: use rx_error to gated	
IIC_HALT_MD	2	R/W	0	0: IIC keep going when not finish. 1: IIC IS HALTED AFTER AUX-REPLY AND CONTINUE WHEN RECEIVED A AUX COMMAND	
DP_IICRD_NEW	1	R/W	0	0: Treat 2 nd repeated I2C command with MOT = 0 as 'status update' when the previous I2C read command .was not done. 1: TREAT 2ND REPEATED I2C COMMAND WITH MOT = 0 AS NEW IIC-OVER-AUX COMMAND.	
DP_MCUIIC_EN	0	R/W	0	Enable auto IIC mapping onto aux channel 1: MCU handle case 0: Auto	

Register:: AUX_RX_CMD 0xD2					
Name	Bits	R/W	Default	Comments	Config
RX_CMD	7:4	R	0	Aux Channel Received Command Tx Request Command (Read) When bit 3=1(Native AUX_CH transaction) Bit 2:0=Request type 000=Write 001=Read When bit 3=0(I2C transaction) Bit 2=MOT(Middle-of-Transaction) Bit1:0=I2C_Command 00=Write	

				01=Read 10=Write Status Request 11=Reserved	
RX_ADDR_H	3:0	R	0	Aux Channel Received Address (High Byte)	

Register:: AUX_RX_ADDR_M 0xD3					
Name	Bits	R/W	Default	Comments	Config
RX_ADDR_M	7:0	R	0	Aux Channel Received Address (Middle Byte)	

Register:: AUX_RX_ADDR_L 0xD4					
Name	Bits	R/W	Default	Comments	Config
RX_ADDR_L	7:0	R	0	Aux Channel Received Address (Low Byte)	

Register:: AUX_RXLEN 0xD5					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:4	--	0	Reserved	
RX_LEN	3:0	R	0	Aux Channel Received Length when read Aux ACK Length settings when write (not IIC automatic mode , namely MCU IIC mode)	

Register:: AUX_RX_Data 0xD6					
Name	Bits	R/W	Default	Comments	Config
AUX_RXDATA	7:0	R	0	Aux Channel Received Data Port	

Register:: AUX_TX_CMD 0xD7					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:4	--	0	Reserved	
TX_CMD	3:0	R/W	0	Aux Channel Transmitted Data Length Setting. Writing this address will trigger Aux-CH reply Rx Reply Command (Write) Bit3:2=I2C-over-AUX Reply field 00=I2C ACK 01=I2C NACK 10=I2C DEFER 11=Reserved Bit1:0=Native AUX CH Reply field 00=AUX_ACK 01=NACK 10=DEFER 11=Reserved	Wport Rport

Register:: AUX_TX_LEN					0xD8
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:4	--	0	Reserved	
TX_LEN	3:0	R/W	0	Aux Tx Length settings. (Tx_Request)	Rport Wport

Register:: AUX_TX_Data					0xD9
Name	Bits	R/W	Default	Comments	Config
AUX_TXDATA	7:0	W	0	Aux Channel Transmitted Data Setting	Wport

Register:: AUX_FIFO_RST					0xDA
Name	Bits	R/W	Default	Comments	Config
AUX_FIFO_RSV	7:6	R/W	0	Reserved	
DPCD20X_AUTO_CLR_EN	5	R/W	0	1: When Tx write TP1, auto clear DPCD 0x00202, 0x00203, 0x00204[0]. Auto clear DPCD 0x00206, 0x00207 when fake link training enabled. 0: Disable	
IIC_SLAVE_ADD_INT	4	R	0	IIC slave address int Write 1 to clear	Wclr_out
SCL_RATE_CHG	3	R/W	0	Due to the aux mac domain clk change 0: if aux mac clk use eclk_ng 1: if aux mac clk use xclk	
WRHDCP_INT_E_N	2	R/W	0	DP Source write DPCD 68xxx interrupt enable	
WRHDCP_INT	1	R/W	0	DP Source has written DPCD 68xxx(for HDCP) address Write 1 to clear	Rport Wport
AUX_FIFO_RST	0	R/W	0	Write '1' to clear AUX Data FIFO pointer.	Rport wport

Register:: AUX_Status					0xDB
Name	Bits	R/W	Default	Comments	Config
AUX_SDM_EN	7	R/W	0	apply AUX SDM to avoid clk drift when sync_end 1: enable 0: disable	
SYNC_CNT_MODE	6	R/W	1	1: rounding 0: truncate	
AUXNACKM	5	R/W	1	When write Read Only DPCD 1: reply NACK only 0: reply NACK+M	
AUXNOREPLY	4	R/W	1	When Aux Error, '1' : sink will no reply '0' : sink will reply defer	

RCV_AUX_ERROR	3	R	0	Error Occur when Aux-CH Receive the host command. Write AUX_RX_INT bit '0' to clear.	
DP_FIFO_FULL	2	R	0	16-bytes Data FIFO is full	
DP_FIFO_EMPTY	1	R	0	16-bytes Data FIFO is empty	
DP_ADDR_ONLY	0	R	0	1: Aux Channel Address-only transaction	

Register::: AUX_IRQ_STATUS					0xDC
Name	Bits	R/W	Default	Comments	Config
AUX_PHY_INT_EN	7	R/W	0	AUX PHY INTERRUPT ENABLE	
AUX_PHY_INT	6	R/W	0	when aux phy found aux signal toggle =>interrupt write 1 to clear	Rport Wport
WR0T_INT_EN	5	R/W	0	Write other address (reference to DD) interrupt enable	
WR0T_INT	4	R/W	0	Write other address (reference to DD) interrupt Write 1 to clear	Rport Wport
TIMEOUT_EN	3	R/W	0	Enable Aux-CH timeout as an interrupt source	
AUX_RX_EN	2	R/W	0	Enable Receiving AUX-CH as an interrupt source	
TIMEOUT_INT	1	R/W	0	Timeout and auto reply. Write 1 to clear.	Rport Wport
AUX_RX_INT	0	R/W	0	Receive AUX Channel Command, Clear when writing '1'. (When DP_AUX_AUTO_EN = 1, assert when reserved DPCD registers is encounterd. When DP_AUX_AUTO_EN = 0, assert regardless of the DPCD registers.	Rport Wport

Register::: AUX_DPCD_IRQ					0xDD
Name	Bits	R/W	Default	Comments	Config
WR102_INT	7	R/W	0	DP Source has written DPCD 00102 address Write 1 to clear	Rport Wport
WR100_101_INT	6	R/W	0	DP Source has written DPCD 00100 and 00101 address Write 1 to clear	Rport Wport
WR103_108_INT	5	R/W	0	DP Source has written DPCD 00103 to 00108 address Write 1 to clear	Rport

						Wport
WR201_INT	4	R/W	0	DP Source has written DPCD 00201 IRQ field. Write 1 to clear	Rport Wport	
WR260_261_INT	3	R/W	0	DP Source has written DPCD 00260 to 00261 address for TEST EDID CHECKSUM Write 1 to clear	Rport Wport	
WR270_INT	2	R/W	0	DP Source has written DPCD 00270 address to test CRC Write 1 to clear	Rport Wport	
WR300_302_INT	1	R/W	0	DP Source has written DPCD 00300 to 00302 address Write 1 to clear	Rport Wport	
WR600_INT	0	R/W	0	DP Source has written DPCD 00403 to 00600 address for power saving purpose. Write 1 to clear	Rport Wport	

Register::AUX_DPCD_IRQ_EN					0xDE	
Name	Bits	R/W	Default	Comments	Config	
WR102_INT_EN	7	R/W	1	WR102_INT enable		
WR100_101_INT_EN	6	R/W	0	WR100_101_INT enable		
WR103_108_INT_EN	5	R/W	0	WR103_108_INT enable		
WR201_INT_EN	4	R/W	0	WR201_INT enable		
WR260_261_INT_EN	3	R/W	0	WR260_261_INT enable		
WR270_INT_EN	2	R/W	0	WR270_INT enable		
WR300_302_INT_EN	1	R/W	0	WR300_302_INT enable		
WR600_INT_EN	0	R/W	1	WR600_INT enable		

Register:: AUX_IIC_MASTER_CTRL					0xDF	
Name	Bits	R/W	Default	Comments	Config	
LEN_UPDATE_CHECK_EN	7	R/W	0	set 1: Enable length update check when IIC read. Reply IIC_NACK AUX_ACK to Source Device if mismatch. Set 0: Disable		

WRLEN_CHECK_EN	6	R/W	0	set 1: Check received data number and its length when IIC write. Reply AUX_NACK to Source Device if mismatch Set 0: Disable	
IIC_IDLE_TIMOUT_EN	5	R/W	0	set 1: Enable IIC idle timeout counter set 0: Disable	
IIC_IDLE_TIMOUT_SET	4:0	R/W	0	Timeout target value settings Timeout period: (reg_iic_idle_timeout_set[4:0]+1)*4.85ms	

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DP_HDCP1.4 (Page C)

Register:: DP_HDCP_CONTROL					0xE0	
Name	Bits	R/W	Default	Comments		Config
HDCP_EN	7	R/W	1	HDCP FUNCTION ENABLE		
ENC_DIS_REF_BS	6	R/W	0	During Encryption, when receiving BS(not SR) , ‘1’ : disable the encryption ‘0’ : not disable the encryption.		
LRK_MODE	5	R/W	0	Active when line enc_dis_ref_bs = 0. ‘1’ : Line rekey only when receiving CPBS ‘0’ : Line rekey when receiving CPBS or BS		
HDCP_2LANE_SWAP	4	R/W	0	Swap the cipher output during 2 lane.		
HDCP_1LANE_SWAP	3	R/W	0	Swap the cipher output during 1 lane.		
NOT_DECRY_OUT_EN	2	R/W	0	‘1’ : not decrypt out (manual, even when encryption). ‘0’: auto decrypt out		
RE_AUTH_KM	1	R/W	0	‘1’ : manual clear the authkm flag to 0. ‘0’ : authkm clear to 0 only when receiving authst.		
KEY_DL_EN	0	R/W	0	Device Key Access Port download enable High : enable Low : disable, this would reset the address of Device Key Access Port to 0.		

Register:: DP_HDCP_KEY_DOWNLOAD_PORT					0xE1	
Name	Bits	R/W	Default	Comments		Config
KEY_DL_PORT	7:0	R/W	0	When enable device key accessing 40x56 table, the 56-bit key table will be transferred to 64-bit pseudo data with 7 th , 15 th , 23rd, 31st, 39 th , 47 th , 55 th bits inserted. The inserted data are ‘0’. And the write sequence is: {D0-Byte0, D0-Byte1, D0-Byte2, D0-Byte3, D0-Byte4, D0-Byte5, D0-Byte6, D0-Byte7}, {D1-Byte0, D1-Byte1, 1-Byte2, D1-Byte3, D1-Byte4, D1-Byte5, D1-Byte6, D1-Byte7}, Accessing this port must be coded/decoded by REALTEK protection code.		

Register:: DP_HDCP_KEY_OUTPUT					0xE2	
Name	Bits	R/W	Default	Comments		Config
KEY_OUT	7:0	R	0	Active when key_dl_en = 1		

Register::HDCP_IRQ					0xE3	
Name	Bits	R/W	Default	Comments		Config
IRQ_BY_LIF_EN	7	R/W	0	Link integrity failure IRQ enable. ‘1’: When IRQ assert, firmware can manually set the		

				bit3(Link_integrity_failure) when bit5(lif_manual_mode == 1). '0' : IRQ not enable	
IRQ_BY_R0_EN	6	R/W	0	R0_available IRQ enable. '1' : When IRQ assert, firmware can manually set the bit2(R0_available) when bit4(r0_manual_mode == 1) . '0' : IRQ not enable	
CP_IRQ_AUTO_SET	5	R/W	0	'1' : auto set when r0_available '0': disable	
R0_MANUAL_MODE	4	R/W	0	'1':r0_available is control by firmware '0':control by digital circuit	
HDCP_IRQ_RSV0	3	R/W	0	Reserved.	
R0_AVAILABLE	2	R/W	0	Active when r0_manual_mode == 1	
hdcp_reset	1	R/W	0	0: normal 1 : reset hdcp block	
HDCP_IRQ_RSV1	0	R/W	0	Reserved.	

Register::HDCP_INTGT_VRF 0xE4					
Name	Bits	R/W	Default	Comments	Config
INTGT_VRF_EN	7	R/W	0	Link integrity enable, '1': Enable '0' : Disable	
MISMATCH_PAT_NUM	6:4	R/W	3	Programmable mismatched pattern number in one frame. 000: Not defined. 001:1 pattern ... 111:7 patterns	
MISMATCH_FRAME_NUM	3:2	R/W	1	Programmable mismatched frame number 00:1 frame 01:2 frames 10:3 frames 11:4 frames	
INTGT_VRF_FAILURE	1	R	0	'1': failure '0' : OK	Rport Wport
km_clk_sel	0	R/W	1	Clock Selection for KM Calculation 0: Choose crystal clock 1: Choose EMCU non-stop clock	

Register::HDCP_INTGT_VRF_PAT_MSB 0xE5					
Name	Bits	R/W	Default	Comments	Config
INTGT_VRF_PAT_MSB	7:0	R/W	53	Setting of integrity pattern (bit15:8)	

Register::HDCP_INTGT_VRF_PAT_LSB 0xE6					
Name	Bits	R/W	Default	Comments	Config
INTGT_VRF_PAT_LSB	7:0	R/W	1F	Setting of integrity pattern (bit7:0)	

Register::HDCP_INTGT_VRF_ANS_MSB 0xE7					
Name	Bits	R/W	Default	Comments	Config

INTGT_VRF_ANS_MSB	7:0	R	--	Real calculation result of integrity pattern (bit15:8)	
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Register::HDCP_INTGT_VRF_ANS_LSB				0xE8	
Name	Bits	R/W	Default	Comments	Config
INTGT_VRF_ANS_LSB	7:0	R	--	Real calculation result of integrity pattern (bit7:0)	

Register:: DP_HDCP_BIST				0xE9	
Name	Bits	R/W	Default	Comments	Config
HDCP_BIST_R_RSV	7:3	R	0	Reserved	
HDCP_BIST_MODE	2	R/W	0	BIST ENABLE.	
HDCP_BIST_DONE	1	R	0	BIST IS DONE.	
HDCP_BIST_FAIL_0	0	R	0	Active when BIST_DONE = 1. '1':BIST Fail. '0':BIST success.	

Register::HDCP_DEBUG				0xEA	
Name	Bits	R/W	Default	Comments	Config
AUTHDONE	7	R		After receiving aksv, auth start	
ENC_ENABLE	6	R		Km add is done.-After receiving CPSR	
AUTHKM	5	R		Km is calculated.	
DP_HDCP_TST_EN	4	R/W	0	1:hdcp test mode enable 0:disable	
DP_HDCP_TST_MODE	3:2	R/W	0	Tst mode select	
RI_EN	1	R/W	0	Read RI enable ◦ RI is always change ◦ Turn Off and then turn on this bit could hold RI value each time.	
HDCP_DEB_R_RSV	0	R	0	Reserved	

Register::RI_BYTE_MSB				0xEB	
Name	Bits	R/W	Default	Comments	Config
RI[15:8]	7:0	R		Ri MSB	

Register::RI_BYTE_LSB				0xEC	
Name	Bits	R/W	Default	Comments	Config
RI[7:0]	7:0	R		Ri LSB	

Register::KM_BYTE_6				0xED	
Name	Bits	R/W	Default	Comments	Config
KM[55:48]	7:0	R		Km[55:48] value.	

Register::KM_BYTE_5				0xEE	
Name	Bits	R/W	Default	Comments	Config
KM[47:40]	7:0	R		Km[47:40] value.	

Register::KM_BYTE_4					0xEF
Name	Bits	R/W	Default	Comments	Config
KM[39:32]	7:0	R		Km[39:32] value.	

Register::KM_BYTE_3					0xF0
Name	Bits	R/W	Default	Comments	Config
KM[31:24]	7:0	R		Km[31:24] value.	

Register::KM_BYTE_2					0xF1
Name	Bits	R/W	Default	Comments	Config
KM[23:16]	7:0	R		Km[23:16] value.	

Register::KM_BYTE_1					0xF2
Name	Bits	R/W	Default	Comments	Config
KM[15:8]	7:0	R		Km[15:8] value.	

Register::KM_BYTE_0					0xF3
Name	Bits	R/W	Default	Comments	Config
KM[7:0]	7:0	R		Km[7:0] value.	

Register:: AUX_TX_TIMER					0xF4
Name	Bits	R/W	Default	Comments	Config
AUX_D1	7	R	0	AUX D1 value (used in FT)	
AUX_D2	6	R	0	AUX D2 value (used in FT)	
AUX_TIMER_EN	5	R/W	0	1:Use aux_tx_timer to delay the ACK Timer 0:No use this timer	
TIMEOUT_TARGET[5:4]	4:3	R/W	3	MSB of Timeout target value settings (set with 0xD0[7:4])	
IIC_ACK_TIMER_EN	2	R/W	0	1:Use aux_tx_timer to delay the IIC ACK Timer 0:No use this timer	
AUX_TX_RSV	1:0	R/W	0	Reserved	

Register:: AUX_ERROR_HANDLE					0xF5
Name	Bits	R/W	Default	Comments	Config
AUX_ERROR_RSV	7	R/W	0	reserved	
AUX_D2_EN	6	R/W	0	Use ~AUX_D2_EN as DATA	
EHANDLE_EN	5	R/W	1	Enable : DATA -> END when encounter IDLE	
SYNC1_WO_IDLE	4	R/W	1	Sync1 State keep when encounter IDLE	
EHANDLE_MAN_DIS	3	R/W	0	Manchester error check (LL) Disable	
EHANDLE_STOP_DIS	2	R/W	0	Stop pattern Error Handle Disable	
EHANDLE_SYNCEND_DIS	1	R/W	0	Sync_end pattern Error Handle Disable	
EHANDLE_8X_dis	0	R/W	0	Byte boundary check Error Handle Disale.	

Register:: AUX_ERROR_HANDLE2 0xF6					
Name	Bits	R/W	Default	Comments	Config
Auxch_st	7:5	R	0	Record auxch mac state machine state If this state is 001, you can change the aux phy clk from power saving mode 000:idle state 001:receive standby state 010:transmit standby state	
lclk_sel	4	R/W	0	If HDCP handshake occur before link training, we can change the link clk to xtal clk to calculate R0 first 0 : link clk 1 : xclk	
MAN_ERROR	3	R	0	Manchester error (write 1 to clear)	Wclr_out
STOP_ERROR	2	R	0	Stop pattern error(write 1 to clear)	Wclr_out
SYNCEND_ERROR	1	R	0	Sync end pattern error(write 1 to clear)	Wclr_out
DATA_8X_ERROR	0	R	0	Data not 8x error(write 1 to clear)	Wclr_out

Register:: ERR_CNT 0xF7					
Name	Bits	R/W	Default	Comments	Config
ERR_CNT_IRQ	7	R	0	Error counter >= { ERR_CNT_THRESHOLD, 9'h1FF }. Write 1 clear. It's better to turn off sym_err_cnt_en first, or you can't clear this bit.	Wclr_out
ERR_CNT_IRQ_EN	6	R/W	0	IRQ enable	
ERR_CNT_THRESHOLD	5:0	R/W	30	{ ERR_CNT_THRESHOLD, 9'h1FF }	

HW auto exit power saving mode AUX

Register:: MSA 0xF8					
Name	Bits	R/W	Default	Comments	Config
LANE_NUM_MEA_EN	7	R/W	0	Enable lane num measure	
MSA_DONE	6	R	0	Lane num measure done.	
MSA_LENGTH	5:0	R	3F	Lane 0 MSA Length, Valid when bit6 asserted. 36: 1 lane 18: 2 lane	

				9 : 4 lane	
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Register::: MCUIIC 0xF9					
Name	Bits	R/W	Default	Comments	Config
MCUIIC_RSV	7:4	R/W	0	reserved	
MCUIIC_NEW	3	R/W	0	For MCU HANDLE mode should set this bit	
DP_ADDR_ONLY_MCUIIC	2	R	0	ADDRESS ONLY FLAG	
ADDR_ONLY_NEW	1	R/W	0	Intel Aux IIC protocol not meet IIC Spec	
Reserved	0	--	0	reserved	

Register::: AUX_RXST 0xFA					
Name	Bits	R/W	Default	Comments	Config
AUX_RXST_R_RSV	7:5	R	0	Reserved byte	
Aux_rxst_int_en	4	R/W	0	Normal Aux Rx state interrupt enable	
Aux_rxst_int_st	3:1	R/W	0	Normal Aux_rxst_int flag is trigger by encounter what state 001:sync0 state 010:sync1 state 011:data state 100:end state 101:precharge state	
Aux_rxst_int	0	R	0	Normal Aux Rx state interrupt flag	Wclr_out

Register::: IIC_SLAVE_ADD 0xFB					
Name	Bits	R/W	Default	Comments	Config
IIC_SLAVE_ADDRESS	7:1	R/W	0x37	IIC slave address	
IIC_SLAVE_ADD_INT_EN	0	R/W	0	IIC slave address int enable	

Register::: W_RESERVE0 0xFC					
Name	Bits	R/W	Default	Comments	Config
W_RESERVE0	7:0	R/W	0	Reserved byte	

Register::: W_RESERVE1 0xFD					
Name	Bits	R/W	Default	Comments	Config

W_RESERVE1	7:0	R/W	0	Reserved byte	
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Register:: W_RESERVE2 0xFE					
Name	Bits	R/W	Default	Comments	Config
W_RESERVE2	7:0	R/W	0	Reserved byte	

DISPLAYPORT ACCESSING PORT (START)

MAIN STREAM ATTRIBUTES

Register:: MN_STRM_ATTR_CTRL 0x00					
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_POPUP	7	R	0	Popup the main stream attributes. (Byte 0x03~0x12) 0: no action. 1: pop-up.	Wclr_out
MN_VIDEO_POPUP	6	R	0	Popup the Mvid/Nvid. (Byte 0x13~0x18) 0: no action. 1: pop-up.	Wclr_out
MN_AUDIO_POPUP	5	R	0	Popup the Maud/Naud. (Byte 0x19~0x1E) 0: no action. 1: pop-up.	Wclr_out
AUDIO_CH_ST_POPUP	4	R	0	Popup the audio channel status. (Byte 0x1F~0x23) 0: no action. 1: pop-up.	Wclr_out
AUTO_CLR_MN_EN	3	R/W	1	Auto clear Mvid/Nvid, Maud/Naud when main-stream attribute changed. 0: disable. 1: enable.	
POPUP_RESET	2	R	0	write to clear strm_attr, mn video, mn_audio popup value	Wclr_out
STEREO_VIDEO_ATTR	1:0	R	0	Stereo video attribute. 00 : No stereo video transported 01 : For progressive video, the next frame is RIGHT eye For interlaced video, TOP field is RIGHT eye and BOTTOM field is LEFT eye 10 : RESERVED and must not be used 11 : For progressive video, the next frame is LEFT eye For interlaced video, TOP field is LEFT eye and BOTTOM field is RIGHT eye (Need not popup, it's real time flag)	

Register:: DP_VBID 0x01					
Name	Bits	R/W	Default	Comments	Config

AUD_CH_CNT	7:5	R	0	Audio channel count. (Audio stream header byte3) Actual channel count -1.	
AMUTE	4	R	0	The VB-ID[4] information. 0: normal. 1: audio mute.	
NO_VIDEO	3	R	0	The VB-ID[3] information. 0: normal. 1: no video stream.	
INTERLACE_MD	2	R	0	The VB-ID[2] information. 0: progressive mode. 1: interlaced mode.	
FIELD	1	R	0	The VB-ID[1] information. (Valid when interlace_md == 1'b1) 0: even field. 1: odd field.	
VBLK	0	R	0	The VB-ID[0] information 0: not vertical blanking. 1: vertical blanking.	

Register:: MN_STRM_ATTR_MISC 0x02					
Name	Bits	R/W	Default	Comments	Config
COLOR_BIT_WIDTH	7:5	R	0	The main-stream attribute "Misc". Bit depth per color 000: 6-bit. 001: 8-bit. 010: 10-bit. 011: 12-bit. 100: 16-bit. Other: reserved.	
YCC_COL	4	R	0	Colorimetry. 0: ITU-R BT601-5 1: ITU-R BT709-5	
DYN_RANGE	3	R	0	Dynamic range. 0: VESA 1: CEA	
COMP_FORMAT	2:1	R	0	Component format. 00: RGB 01: YCbCr422 10: YcbCr444 Other: reserved.	
SYNC_CLK_EN	0	R	0	Synchronous Clock. 0: asynchronous. 1: synchronous.	

Register:: MN_STRM_ATTR_MISC1 0x03					
Name	Bits	R/W	Default	Comments	Config
Interlace_en	7	R/W	0	Enable interlace mode 1: address 36~3B will be active 0: just 39~3B is active	
Interlace_auto	6	R/W	0	0: reference to VB_ID[1] 1: reference by bs counter by hardware	

Interlace_detect	5	R	0	Hardware detect interlace or not Write 1 to clear	Wclr_out
Fie_inv	4	R/W	0	Active when bit 6 =1, inverse the inner field.	
Field_force_toggle	3	R/W	0	Force field to toggle	
MEASURE_INTERLACE_SEL	2:1	R/W	0	For measure vblk length 00: origin 01: top_field(odd) 10: bottom_field(even).	
VTT_EVEN	0	R	0	Interlaced vertical total even. 0: odd. 1: even.	

The following main-stream attributes bytes have to be popuped.

Register:: MN_STRM_ATTR_HTT_M					0x04
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HTT_M	7:0	R	0	Bit15~8 of the main-stream attribute “Htotal”.	

Register:: MN_STRM_ATTR_HTT_L					0x05
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HTT_L	7:0	R	0	Bit7~0 of the main-stream attribute “Htotal”.	

Register:: MN_STRM_ATTR_HST_M					0x06
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HST_M	7:0	R	0	Bit15~8 of the main-stream attribute “Hstart”.	

Register:: MN_STRM_ATTR_HST_L					0x07
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HST_L	7:0	R	0	Bit7~0 of the main-stream attribute “Hstart”.	

Register:: MN_STRM_ATTR_HWD_M					0x08
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HWD_M	7:0	R	0	Bit15~8 of the main-stream attribute “Hwidth”.	

Register:: MN_STRM_ATTR_HWD_L					0x09
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HWD_L	7:0	R	0	Bit7~0 of the main-stream attribute “Hwidth”.	

Register:: MN_STRM_ATTR_HSW_M					0x0A
Name	Bits	R/W	Default	Comments	Config
STRM_ATTR_HSP	7	R	0	The main-stream attribute “HSP”.	

STRM_ATTR_HSW_M	6:0	R	0	Bit14~8 of the main-stream attribute “HSW”.	
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Register:: MN_STRM_ATTR_HSW_L 0x0B				
Name	Bits	R/W	Default	Comments
STRM_ATTR_HSW_L	7:0	R	0	Bit7~0 of the main-stream attribute “HSW”.

Register:: MN_STRM_ATTR_VTTE_M 0x0C				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VTTE_M	7:0	R	0	Bit15~8 of the main-stream attribute “Vtotal” when even field(VB-ID[2]==1 & VB-ID[1]==0).

Register:: MN_STRM_ATTR_VTTE_L 0x0D				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VTTE_L	7:0	R	0	Bit7~0 of the main-stream attribute “Vtotal” when even field(VB-ID[2]==1 & VB-ID[1]==0).

Register:: MN_STRM_ATTR_VTTO_M 0x0E				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VTTO_M	7:0	R	0	Bit15~8 of the main-stream attribute “Vtotal” of odd field(VB-ID[2]==1 & VB-ID[1]==1).

Register:: MN_STRM_ATTR_VTTO_L 0x0F				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VTTO_L	7:0	R	0	Bit7~0 of the main-stream attribute “Vtotal” of odd field(VB-ID[2]==1 & VB-ID[1]==1).

Register:: MN_STRM_ATTR_VST_M 0x10				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VST_M	7:0	R	0	Bit15~8 of the main-stream attribute “Vstart”.

Register:: MN_STRM_ATTR_VST_L 0x11				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VST_L	7:0	R	0	Bit7~0 of the main-stream attribute “Vstart”.

Register:: MN_STRM_ATTR_VHT_M 0x12				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VHT_M	7:0	R	0	Bit15~8 of the main-stream attribute “Vheight”.

Register:: MN_STRM_ATTR_VHT_L 0x13				
Name	Bits	R/W	Default	Comments

STRM_ATTR_VHT_L	7:0	R	0	Bit7~0 of the main-stream attribute “Vheight”.	
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Register:: MN_STRM_ATTR_VSW_M 0x14				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VSP	7	R	0	The main-stream attribute “VSP”.
STRM_ATTR_VSW_M	6:0	R	0	Bit14~8 of the main-stream attribute “VSW”.

Register:: MN_STRM_ATTR_VSW_L 0x15				
Name	Bits	R/W	Default	Comments
STRM_ATTR_VSW_L	7:0	R	0	Bit7~0 of the main-stream attribute “VSW”.

Mvid/Nvid

Register:: MN_M_VID_H 0x16				
Name	Bits	R/W	Default	Comments
M_VID_H	7:0	R	0	Bit23~16 of “Mvid”

Register:: MN_M_VID_M 0x17				
Name	Bits	R/W	Default	Comments
M_VID_M	7:0	R	0	Bit15~8 of “Mvid”

Register:: MN_M_VID_L 0x18				
Name	Bits	R/W	Default	Comments
M_VID_L	7:0	R	0	Bit7~0 of “Mvid”

Register:: MN_N_VID_H 0x19				
Name	Bits	R/W	Default	Comments
N_VID_H	7:0	R	0	Bit23~16 of “Nvid”

Register:: MN_N_VID_M 0x1A				
Name	Bits	R/W	Default	Comments
N_VID_M	7:0	R	0	Bit15~8 of “Nvid”

Register:: MN_N_VID_L 0x1B				
Name	Bits	R/W	Default	Comments
N_VID_L	7:0	R	0	Bit7~0 of “Nvid”

Register:: MN_AVERAGE 0x1C					
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	--	0	Reserved.	
MN_TO_NCTS	5	R/W	1	To sclkg block 0: from origin mn 1: from mn after average	
MN_AVE_DONE	4	R	0	MN average done , then you can read M_VID and N_VID	
MN_AVE_RECAL	3	R	0	Write 1 to re-calculate MN average value. (at the same time user should set the [2:0] value)	Wclr_out
MN_AVE_NUM	2:0	R/W	0	000:average 1 (no average) 001:average 2 010:average 4 011:average 8 100:average 16 else:average 1(no average)	

Maud/Naud

Register:: MN_M_AUD_H 0x1D					
Name	Bits	R/W	Default	Comments	Config
M_AUD_H	7:0	R	0	Bit23~16 of “Maud”	
Register:: MN_M_AUD_M 0x1E					
Name	Bits	R/W	Default	Comments	Config
M_AUD_M	7:0	R	0	Bit15~8 of “Maud”	

Register:: MN_M_AUD_L 0x1F					
Name	Bits	R/W	Default	Comments	Config
M_AUD_L	7:0	R	0	Bit7~0 of “Maud”	

Register:: MN_N_AUD_H 0x20					
Name	Bits	R/W	Default	Comments	Config
N_AUD_H	7:0	R	0	Bit23~16 of “Naud”	

Register:: MN_N_AUD_M 0x21					
Name	Bits	R/W	Default	Comments	Config
N_AUD_M	7:0	R	0	Bit15~8 of “Naud”	

Register:: MN_N_AUD_L 0x22					
Name	Bits	R/W	Default	Comments	Config

N_AUD_L	7:0	R	0	Bit7~0 of “Naud”	
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Register:: DP_AUD_CH_STATUS0 0x23					
Name	Bits	R/W	Default	Comments	Config
AUD_CH_STATUS0	7:0	R	0	Bit7~0 of “channel status”	

Register:: DP_AUD_CH_STATUS1 0x24					
Name	Bits	R/W	Default	Comments	Config
AUD_CH_STATUS1	7:0	R	0	Bit15~8 of “channel status”	

Register:: DP_AUD_CH_STATUS2 0x25					
Name	Bits	R/W	Default	Comments	Config
AUD_CH_STATUS2	7:0	R	0	Bit23~16 of “channel status”	

Register:: DP_AUD_CH_STATUS3 0x26					
Name	Bits	R/W	Default	Comments	Config
AUD_CH_STATUS3	7:0	R	0	Bit31~24 of “channel status”	

Register:: DP_AUD_CH_STATUS4 0x27					
Name	Bits	R/W	Default	Comments	Config
AUD_CH_STATUS4	7:0	R	0	Bit39~32 of “channel status”	

0x28~0x2F are reserved.

VIDEO FIFO

The following byte is read-only.

Register:: MN_VFIFO_STATUS 0x30					
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	--			
vfifo_full	5	R	0	Video FIFO full. 0: not full. 1: full. Write 1 to clear.	Wclr_out
vfifo_empty	4	R	0	Video FIFO empty. 0: not empty. 1: empty. Write 1 to clear.	Wclr_out
vfifo_ovf	3	R	0	Video FIFO overflow. 0: not overflow. 1: overflow. Write 1 to clear.	Wclr_out
vfifo_udf	2	R	0	Video FIFO underflow. 0: not underflow.	Wclr_out

				1: underflow. Write 1 to clear.	
sfifo_empty	1	R	0	Small FIFO empty. 0: not empty. 1: empty. Write 1 to clear.	Wclr_out
sfifo_udf	0	R	0	Small FIFO underflow. 0: not underflow. 1: underflow. Write 1 to clear.	Wclr_out

Register:: MN_PIX_REG_CTRL 0x31					
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	--	0	Reserved.	
Component_format	4:3	R/W	0	00 = RGB 01 = YcbCr422 10 = YcbCr444 11 = Reserved	HW_write
colorbit	2:0	R/W	1	Bit depth per color/component 000 = 6bits 001 = 8 bits 010 = 10 bits 011 = 12 bits 100 = 16 bits 101, 110, 111 = Reserved	HW_write

Register:: MAX_VFIFO_WL_CLR 0x32					
Name	Bits	R/W	Default	Comments	Config
VFIFO_RSV	7:1	R/W	0	Reserved.	
max_vf_wl_clr	0	W	0	Write '1' to reset max video fifo water level record.	RPORT WPOR

Register:: MAX_VFIFO_WL 0x33					
Name	Bits	R/W	Default	Comments	Config
max_vf_water_level	7:0	R/W	0	Max Video Water Level Index (Note: To avoid asynchronous problem, reading this address will latch the current value and the previous value will be read)	RPORT WPOR

Register:: VFIFO_WL 0x34					
Name	Bits	R/W	Default	Comments	Config
vf_water_level	7:0	R/W	0	Current Video Water Level Index (Note: To avoid asynchronous problem, reading this address will latch the current value and the	RPORT WPOR

				previous value will be read)	
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DISPLAY FORMAT

Register:: MN_DPF_CTRL 0x35					
Name	Bits	R/W	Default	Comments	Config
DISP_EN	7	R/W	0	Start to generate display format 0: disable. 1: enable.	
DISP_DBUF	6	R	0	Double buffer of the display format. FW has to write this bit after write all the following display format settings.	Wclr_out
DISP_HSVS_FORMAT	5	R/W	1	Display format selector. (Method of generation of HS/VS) 0: full last line. 1: frame-sync.	
DISP_DE_FORMAT	4	R/W	0	Display format selector. (Method of generation of DE) 0: normal. 1: digital mode.	
VS_BS_OR_BE	3	R/W	0	The source of virtual VS. 0: BS 1: BE	
DE_BS_OR_BE	2	R/W	0	The triggering source of DE in digital mode. 0: BS 1: BE	
FIELD_INV	1	R/W	0	Enable field_out inverse. 0: not inverse. 1: inverse.	
LASTLINE4_EN	0	R/W	1	Active in frame-sync mode 1:last line pixel is time of 4 0: normal operation	

Register:: MN_EVBLK2VS_H 0x36					
Name	Bits	R/W	Default	Comments	Config
EVBLK2VS_H	7:0	R/W	0	Bit23~16 of the counts between even field BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_EVBLK2VS_M 0x37					
Name	Bits	R/W	Default	Comments	Config
EVBLK2VS_M	7:0	R/W	2F	Bit15~8 of the counts between even field vertical BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_EVBLK2VS_L 0x38					
Name	Bits	R/W	Default	Comments	Config
EVBLK2VS_L	7:0	R/W	3E	Bit7~0 of the counts between even field vertical BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_OVBLK2VS_H 0x39					
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Name	Bits	R/W	Default	Comments	Config
OVBLK2VS_H	7:0	R/W	0	Bit23~16 of the counts between odd field BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_OVBLK2VS_M 0x3A					
Name	Bits	R/W	Default	Comments	Config
OVBLK2VS_M	7:0	R/W	2F	Bit15~8 of the counts between odd field vertical BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_OVBLK2VS_I 0x3B					
Name	Bits	R/W	Default	Comments	Config
OVBLK2VS_L	7:0	R/W	3E	Bit7~0 of the counts between odd field vertical BS/BE and virtual VS. (Counted by link clock)	

Register:: MN_HBLK2DE_M 0x3C					
Name	Bits	R/W	Default	Comments	Config
reserved	7	--	--	reserved	
HBLK2DE_M	6:0	R/W	0	Bit14~8 of the counts between horizontal BS/BE and DE. This is valid only when digital mode. (Counted by link clock)	

Register:: MN_HBLK2DE_I 0x3D					
Name	Bits	R/W	Default	Comments	Config
HBLK2DE_L	7:0	R/W	0	Bit7~0 of the counts between horizontal BS/BE and DE. This is valid only when digital mode. (Counted by link clock)	

Register:: MN_DPF_HTT_M 0x3E					
Name	Bits	R/W	Default	Comments	Config
DPF_HTT_M	7:0	R/W	07	Bit15~8 of the display format “Htotal”. 1792	HW_write

Register:: MN_DPF_HTT_L 0x3F					
Name	Bits	R/W	Default	Comments	Config
DPF_HTT_L	7:0	R/W	0	Bit7~0 of the display format “Htotal”. 1792	HW_write

Register:: MN_DPF_HST_M 0x40					
Name	Bits	R/W	Default	Comments	Config
DPF_HST_M	7:0	R/W	01	Bit15~8 of the display format “Hstart”. 356	HW_write

Register:: MN_DPF_HST_L 0x41					
Name	Bits	R/W	Default	Comments	Config
DPF_HST_L	7:0	R/W	64	Bit7~0 of the display format “Hstart”. 356	HW_write

Register:: MN_DPF_HWD_M 0x42					
Name	Bits	R/W	Default	Comments	Config
DPF_HWD_M	7:0	R/W	05	Bit15~8 of the display format “Hwidth”. 1366	HW_write

Register:: MN_DPF_HWD_L 0x43					
Name	Bits	R/W	Default	Comments	Config
DPF_HWD_L	7:0	R/W	56	Bit7~0 of the display format “Hwidth”. 1366	HW_write

Register:: MN_DPF_HSW_M 0x44					
Name	Bits	R/W	Default	Comments	Config
DPF_HSP	7	R/W	0	The display format “HSP”.	
DPF_HSW_M	6:0	R/W	0	Bit14~8 of the display format “HSW”. 143	HW_write

Register:: MN_DPF_HSW_L 0x45					
Name	Bits	R/W	Default	Comments	Config
DPF_HSW_L	7:0	R/W	8F	Bit7~0 of the display format “HSW”. 143	HW_write

Register:: MN_DPF_VTT_M 0x46					
Name	Bits	R/W	Default	Comments	Config
DPF_VTT_M	7:0	R/W	03	Bit15~8 of the display format “Vtotal”. 798	HW_write

Register:: MN_DPF_VTT_L 0x47					
Name	Bits	R/W	Default	Comments	Config
DPF_VTT_L	7:0	R/W	1E	Bit7~0 of the display format “Vtotal”. 798	HW_write

Register:: MN_DPF_VST_M 0x48					
Name	Bits	R/W	Default	Comments	Config
DPF_VST_M	7:0	R/W	0	Bit15~8 of the display format “Vstart”. 27	HW_write

Register:: MN_DPF_VST_L 0x49					
Name	Bits	R/W	Default	Comments	Config
DPF_VST_L	7:0	R/W	1B	Bit7~0 of the display format “Vstart”. 27	HW_write

Register:: MN_DPF_VHT_M 0x4A					
Name	Bits	R/W	Default	Comments	Config

DPF_VHT_M	7:0	R/W	03	Bit15~8 of the display format “Vheight”. 768	HW_write
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Register:: MN_DPF_VHT_L 0x4B					
Name	Bits	R/W	Default	Comments	Config
DPF_VHT_L	7:0	R/W	0	Bit7~0 of the display format “Vheight”. 768	HW_write

Register:: MN_DPF_VSW_M 0x4C					
Name	Bits	R/W	Default	Comments	Config
DPF_VSP	7	R/W	0	The display format “VSP”.	
DPF_VSW_M	6:0	R/W	0	Bit14~8 of the display format “VSW”. 3	HW_write

Register:: MN_DPF_VSW_L 0x4D					
Name	Bits	R/W	Default	Comments	Config
DPF_VSW_L	7:0	R/W	03	Bit7~0 of the display format “VSW”. 3	HW_write

Register:: MN_DPF_FREERUN 0x4E					
Name	Bits	R/W	Default	Comments	Config
FREERUN_EN	7	R/W	0	Active when display enable 1: bit[6]will Active 0: bit[6]will useless	
VSYNC_FREERUN	6	R	0	Active in full last line mode Write 1 to clear 1:free run 0:normal mode	Wclr_out
BE_HIT_VBID0	5	R	0	BE hit vbid[0] write 1 to clear	Wclr_out
SAFEMD_EN	4	R/W	0	DP fail safe mode(1:1 display) Used in frame sync mode is better or you will enlarge the VTOTAL (if using in full last line mode,should off/on the disp_en) 0: Normal display 1: 1:1 display	
SAFEMD_SWAP	3	R/W	0	Swap the Display timing 1:swap 0:no swap	
reserved	2:0	--	0	Reserved.	

0x4F is reserved.

STREAM CLOCK REGENERATOR

Register:: MN_SCLKG_CTRL 0x50					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_IN_SEL	7	R/W	1	PLL input clock selector. 0: crystal clk.	Rport Wport

				1: link clk.	
SCLKG_OCLK_SEL	6:5	R/W	0	Output clock selector (Before div. S) 00: PLL output. 01: crystal clk. 1x: link clk.	Rport Wport
SCLKG_DBUF	4	R	0	Double buffer of all stream clk setting. 0: no action. 1: write current data to HW.	Wclr_out
SCLKG_PLL_N	3:0	R/W	3	N code of PLL 0000: div2. 1111: div 17 If “sclkg_pllbpn” = 1'b1, no div, else, div number is decided by these four bits.	Rport Wport

Register:: MN_SCLKG_DIVM 0x51					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_M	7:0	R/W	04	M code of PLL 00'h: div 2. ff'h: div 257.	Rport Wport

Register:: MN_SCLKG_DIVS 0x52					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_DIV2_EN	7	R/W	0	Divide the clock (after div. S) by 2. (Used in interlaced mode) 0: disable. 1: enable.	Rport Wport
SCLKG_PLL_DIVS	6:0	R/W	1	Divide the oclk by 2*S. 00'h: no div. 01'h: div 2. 7f'h: div 254	Rport Wport

Register:: MN_SCLKG_OFFSETS_H 0x53					
Name	Bits	R/W	Default	Comments	Config
SCLKG_LD_D_CODE	7	R	0	Load offset value. 0: disable 1: enable	Wclr_out
SCLKG_PS_OLD	6	R/W	0	Phase Swallow Tracking old mode enable 0:new mode (sum_r=P+sum_c+sum_r[12:0]) 1:old mode when sum_r<0 (sum_r=P+sum_c-(2^13-sum_r[12:0]))	
SCLKG_MN_BL_EN	5	R/W	0	MN value block enable 0:disable 1:enable	
SCLKG_MN_BT	4:3	R/W	0	Strength of blocking MN input. (Active when bit5 is '1') 00: 1/2 01: 1/3 10: 1/5 11: 1/8	
SCLKG_PLL_OFFSETS_H	2:0	R/W	0	Bit18~16 of offset value. (This is 2's complement.) 1bit causes 1/8*2^-18 frequency offset.	

Register:: MN_SCLKG_OFFSET_M 0x54					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_OFFSET_M	7:0	R/W	0	Bit15~8 of offset value. (This is 2's complement.) 1bit causes 1/8*2^-18 frequency offset.	

Register:: MN_SCLKG_OFFSET_L 0x55					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_OFFSET_L	7:0	R/W	0	Bit7~0 of offset value. (This is 2's complement.) 1bit causes 1/8*2^-18 frequency offset.	

Register:: MN_SCLKG_TRK_CTRL 0x56					
Name	Bits	R/W	Default	Comments	Config
SCLKG_MN_EN	7	R/W	0	Enable M/N tracking 0: disable. 1: enable.	Rport Wport
SCLKG_VS_EN	6	R/W	0	Enable VS tracking 0: disable. 1: enable.	Rport Wport
SCLKG_VS_STEP_EN	5	R/W	0	VS tracking mode selector. 0: Normal. 1: Step (The step size is equal to I code in this mode.)	
SCLKG_VS_PER2_EN	4	R/W	0	Enable VS tracking every two VS. 0: every VS. 1: every 2 VS	
RESERVED	3:2	--	0	Reserved.	
SCLKG_PLL_IN_DIV_SEL	1:0	R/W	3	PLL input: 0: div 1 1: div 2 2: div 4 3: div 8	Rport Wport

Register:: MN_SCLKG_TRK_MN_I_H 0x57					
Name	Bits	R/W	Default	Comments	Config
SCLKG_RSV0	7:3	R/W	0	Reserved.	
SCLKG_MN_I_H	2:0	R/W	0	Bit18~16 of the M/N tracking I code	

Register:: MN_SCLKG_TRK_MN_I_M 0x58					
Name	Bits	R/W	Default	Comments	Config
SCLKG_MN_I_M	7:0	R/W	0	Bit15~8 of the M/N tracking I code	

Register:: MN_SCLKG_TRK_MN_I_L 0x59					
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Name	Bits	R/W	Default	Comments	Config
SCLKG_MN_I_L	7:0	R/W	0	Bit7~0 of the M/N tracking I code	

Register:: MN_SCLKG_TRK_MN_P_H 0x5A					
Name	Bits	R/W	Default	Comments	Config
SCLKG_RSV1	7:3	R/W	0	Reserved.	
SCLKG_MN_P_H	2:0	R/W	0	Bit18~16 of the M/N tracking P code	

Register:: MN_SCLKG_TRK_MN_P_M 0x5B					
Name	Bits	R/W	Default	Comments	Config
SCLKG_MN_P_M	7:0	R/W	0	Bit15~8 of the M/N tracking P code	

Register:: MN_SCLKG_TRK_MN_P_L 0x5C					
Name	Bits	R/W	Default	Comments	Config
SCLKG_MN_P_L	7:0	R/W	0	Bit7~0 of the M/N tracking P code	

Register:: MN_SCLKG_TRK_MN_PE 0x5D					
Name	Bits	R/W	Default	Comments	Config
SCLKG_RSV2	7:5	R/W	0	Reserved.	
SCLKG_MN_PE	4:0	R/W	0	Phase error equals how many numbers of dds clock. (Max==1F'h) (Read- only) Write 1F'h to clear.	Rport Wport

Register:: MN_SCLKG_TRK_MN_NLOCK 0x5E					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:6	--	0	Reserved.	
SCLKG_MN_NLOCK	5	R/W	0	The flag of the PE larger than the Phase error threshold, (This bit is Read only) 0: locked. 1: nonlocked. (Write 1 to clear)	Rport Wport
SCLKG_MN_NLOCK_THR	4:0	R/W	0	Phase error threshold of M/N tracking non-lock. (Max ==1F'h)	

If “the phase error of M/N tracking” is greater than “sclk_mn_nlock_thr”, “mn_nlock” would be automatically assigned to 1 until FW clear it.

Register:: MN_SCLKG_TRK_VS_I_H 0x5F					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:3	--	0	Reserved.	
SCLKG_VS_I_H	2:0	R/W	0	Bit18~16 of the VS tracking I code	

Register:: MN_SCLKG_TRK_VS_I_M 0x60					
Name	Bits	R/W	Default	Comments	Config
SCLKG_VS_I_M	7:0	R/W	0	Bit15~8 of the VS tracking I code	

Register:: MN_SCLKG_TRK_VS_I_L 0x61					
Name	Bits	R/W	Default	Comments	Config
SCLKG_VS_I_L	7:0	R/W	0	Bit7~0 of the VS tracking I code	

Register:: MN_SCLKG_TRK_VS_P_H 0x62					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:3	--	0	Reserved.	
SCLKG_VS_P_H	2:0	R/W	0	Bit18~16 of the VS tracking P code	

Register:: MN_SCLKG_TRK_VS_P_M 0x63					
Name	Bits	R/W	Default	Comments	Config
SCLKG_VS_P_M	7:0	R/W	0	Bit15~8 of the VS tracking P code	

Register:: MN_SCLKG_TRK_VS_P_L 0x64					
Name	Bits	R/W	Default	Comments	Config
SCLKG_VS_P_L	7:0	R/W	0	Bit7~0 of the VS tracking P code	

Register:: MN_SCLKG_TRK_VS_PE 0x65					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:5	--	0	Reserved.	
SCLKG_VS_PE	4:0	R/W	0	Phase error equals how many numbers of dds clock. (Max==1F'h) (Read- only) Write 1F'h to clear.	Rport Wport

Register:: MN_SCLKG_TRK_VS_NLOCK 0x66					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:6	--	0	Reserved.	
SCLKG_VS_NLOCK	5	R/W	0	The flag of the PE larger than the Phase error threshold, (This bit is Read only) 0: locked. 1: nonlocked. (Write 1 to clear)	Rport Wport
SCLKG_VS_NLOCK_THR	4:0	R/W	0	Phase error threshold of VS tracking non-lock. (Max ==1F'h)	

If “the phase error of VS tracking” is greater than “sclkgs_vs_nlock_thr”, “vs_nlock” would be

automatically assigned to 1 until FW clear it.

Register:: MN_SCLKG_SDM_CTRL 0x67					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:6	--	0	Reserved.	
SDM_OV_UD	5	R/W	0	Flag of sum_r of SDM overflow /underflow (Read only) 0: no overflow, no underflow. 1: overflow or underflow happened. (Write 1 to clear)	Rport Wport
SDM_EN	4	R/W	0	Enable SDM (phase swallow) 0: disable. 1: enable.	
RESERVED	3:0	--	0	Reserved.	

Register:: MN_SCLKG_SDM_TEST 0x68					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:6	--	0	Reserved.	
SDM_TST_EN	5	R/W	0	Enable test mode. 0: normal run 1: test mode.	
SDM_TST_PH_UP	4	R/W	0	Phase swallow direction in test mode. 0: phase down. (faster) 1: phase up. (slower)	
SDM_TST_AMP	3:0	R/W	0	Phase Swallow Cycle. Any bit is set to 1 for swallow, 0 for hold.	

Register:: MN_SCLKG_SDM_SUMC_H 0x69					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:4	--	0	Reserved.	
SCLKG_SDM_SUMC_H	3:0	R	0	Bir18~16 of SUM_C in SDM	

Register:: MN_SCLKG_SDM_SUMC_M 0x6A					
Name	Bits	R/W	Default	Comments	Config
SCLKG_SDM_SUMC_M	7:0	R	0	Bir15~8 of SUM_C in SDM	

Register:: MN_SCLKG_SDM_SUMC_L 0x6B					
Name	Bits	R/W	Default	Comments	Config
SCLKG_SDM_SUMC_L	7:0	R	0	Bir7~0 of SUM_C in SDM	

SDRRS MODE (for changing frame rate)

Register:: MN_SCLKG_INTERRUPT					0x6E
Name	Bits	R/W	Default	Comments	Config
SCLKG_N_INT_TH	7:6	R/W	2	Ratio of Ncode compare to previous N code threshold => if over this threshold, assert interrupt 00: 1/2 01: 1/4 10: 1/8 11: 1/16	
SCLKG_N_INT	5	R/W	0	Over-ratio N code interrupt Write 1 to clear	Rport Wport
SCLKG_N_INT_EN	4	R/W	0	Over-ratio N code interrupt enable	
SCLKG_M_INT_TH	3:2	R/W	2	M code (as above) 00: 1/2 01: 1/4 10: 1/8 11: 1/16	
SCLKG_M_INT	1	R/W	0	Over-ratio M code interrupt Write 1 to clear	Rport Wport
SCLKG_M_INT_EN	0	R/W	0	Over-ratio M code interrupt enable	

Register:: SDRRS_MODE					0x6F
Name	Bits	R/W	Default	Comments	Config
SDDRS_CHG_MN_EN	7	R/W	0	When changing MN in sDDRS mode, MN is keep until TCON finish the last 2 line, then update the newest MN. 0 : disable 1 : enable	
SCLKG_RSV3	6:0	R/W	0	Reserved	

Register:: MN_SCLKG_PLL_PWR					
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_PWDN	7	R/W	1	SCLKG PLLPWDN 0: power up 1: power down	
SCLKG_PLL_FREEZE	6	R/W	0	SCLKG PLLFREEZE 0: normal 1: freeze	
SCLKG_PLL_CALBP	5	R/W	0	SCLKGPLL bypass calibration(active high)	
SCLKG_PLL_CALSW	4	R/W	0	calibration validated (go high after power on 1200us)	
SCLKG_PLL_CALLCH	3	R/W	0	latch calibration (go high after power on 1100us)	
SCLKG_PLL_CMPEN	2	R/W	0	cmp enable (go high after power on 1000us)	
SCLKG_PLL_O	1:0	R/W	1	SCLKGPLLO div 2^(SCLKGPLLO)	Rport Wport

Register:: MN_SCLKG_PLL_CHP					0x71
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_RS	7:5	R/W	3	SCLKG PLL Loop Filter Resister Control RS: 000:16K 001:18K 010:20K 011:22K 100: 24K 101: 26K 110:28K 111:30K	
SCLKG_PLL_CS	4:3	R/W	2	SCLKG PLL Loop Filter Capacitor Control CS= 00:18p, 01:20p, 10:24p, 11:28p	
SCLKG_PLL_IP	2:0	R/W	0	SCLKG PLL Charge Pump Current Control Icp=(2.5uA+2.5uA*bit[0]+5uA*bit[1]+10uA*bit[2]) Keep DPM/Icp constant=10.67	

Register:: MN_SCLKG_PLL_WD					0x72
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_STATUS	7	R	0	SCLKGSTATUS	Wclr_out
SCLKG_PLL_WDRST	6	R/W	0	SCLKGWDRST	
SCLKG_PLL_WDSET	5	R/W	0	SCLKGWDSET	
SCLKG_PLL_VCOMD	4:3	R/W	2	SCLKG PLL VCO Default mode 00: VCO slowest, 11: VCO fastest	
SCLKG_PLL_RESERVE	2	R/W	1	SCLKGPLLRESERVE, phase swallow circuit clock select 0:fvco,default is 1 1:fps	
SCLKG_PLL_STOP	1	R/W	1	SCLKGSTOP	
SCLKG_PLL_CP	0	R/W	0	CP Control 0:CP=1.77pF 1:CP=2.1pF	

Register:: MN_SCLKG_PLL_INSEL					0x73
Name	Bits	R/W	Default	Comments	Config
SCLKG_PLL_VO2	7	R	0	SCLKG PLL CAL OUT2	
SCLKG_PLL_VO1	6	R	0	SCLKG PLL CAL OUT1	
SCLKG_PLL_CAL	5:4	R	0	SCLKG PLL calibrated VCO code	
SCLKG_RESERVED	3	R/W	0	Reserved.	
SCLKG_PLL_BPN	2	R/W	0	SCLKG PLLBPN 0:divider PLL N code enable 1:divider PLL N code disable (N=1)	Rport Wport
SCLKG_PLL_RESERVED1	1	R/W	0	SCLKG PLL RESERVE1	
SCLKG_PLL_VCORSTB	0	R/W	0	RESET VCO (active high)	

Register:: MN_SCLKG_PLL_STOP 0x74					
Name	Bits	R/W	Default	Comments	Config
DPLL_STOP125	7	R/W	1	DPLL 12.5% SSC Frequency Tuning 1:Enable 0:Disable	
DPLL_STOP250	6	R/W	1	DPLL 25% SSC Frequency Tuning 1:Enable 0:Disable	
RESERVED	5:0	--	0	Reserved.	

如果是 YCbCr 要填對應的黑色, RGB 就全部都 0, DE 之外的都是這個值

Register:: MN_DPF_BG_RED_M 0x75					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_RED_M	7:0	R/W	0	Back ground color of Red[15:8]	

Register:: MN_DPF_BG_RED_L 0x76					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_RED_L	7:0	R/W	0	Back ground color of Red[7:0]	

Register:: MN_DPF_BG_GRN_M 0x77					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_GRN_M	7:0	R/W	0	Back ground color of Green[15:8]	

Register:: MN_DPF_BG_GRN_L 0x78					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_GRN_L	7:0	R/W	0	Back ground color of Green [7:0]	

Register:: MN_DPF_BG_BLU_M 0x79					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_BLU_M	7:0	R/W	0	Back ground color of Blue[15:8]	

Register:: MN_DPF_BG_BLU_L 0x7A					
Name	Bits	R/W	Default	Comments	Config
DPF_BG_BLU_L	7:0	R/W	0	Back ground color of Blue[7:0]	

0x7B~0x7F are reserved.

REED-SOLOMON DECODER

Register:: MN_RS_DEC_CTRL 0x80					
Name	Bits	R/W	Default	Comments	Config
RS_DEC_EN	7	R/W	0	Reed-Solomon decoder enable 0: disable. 1: enable.	
RS_DEC_ERR2_PROC	6	R/W	0	Drop out those packets with more than one error except for audio packet. This is valid only when enabling rs_dec_en. 0: keep those packets. 1: drop out those packets.	

CODE_NB_SWAP	5	R/W	0	nb0 <-> nb1, nb2 <-> nb3, ..., p0 <->p1 0: not swap 1: swap	
CODE_REVERSE	4	R/W	0	nb0, nb1, nb2, ..., p0, p1 <-> p1, p0, nb7, ..., nb1, nb0. 0: not revert. 1: reset.	
RS_ERR1	3	R/W	0	One error has been found in RS decoder. Write 1 to clear. (read-only)	Rport Wport
RS_ERR2	2	R/W	0	One error has been found in RS decoder. Write 1 to clear. (read-only)	Rport Wport
RESERVED	1:0	--	0	Reserved.	

Register::: RS_DEC_ERR_HANDLE 0x81					
Name	Bits	R/W	Default	Comments	Config
RS_RSV0	7:4	R/W	0	reserved	
DP_LYO1_MOD_EN	3	R/W	0	Force to write any data into FIFO even as the data is with 2-nibble RS code Error	
SP_CNT_MOD_EN	2	R/W	0	Reset RS FSM status in the beginning of every Seceondary Data Packet	
RS_ERR2_ENH_MODE	1	R/W	0	Force the rest data as being with 2-nibble RS code Error once 1-nibble RS code error has been occurred	
RS_ERR2_MODE	0	R/W	0	Force the rest data as being with 2-nibble RS code Error once 2-nibble RS code error has been occurred	

0x82~0x83 are reserved.

MN VALUE INTERRUPT → TCON 在用的

Register::: MN_SCLKG_INTERRUPT1 0x84					
Name	Bits	R/W	Default	Comments	Config
IRQ_BY_REG_EN	7	R/W	0	0: irq by ratio value in 6E 1: irq by register value	
M THR[22:16]	6:0	R/W	0	Assert irq if M value is changing over this threshold M THR[22:16]	

Register::: MN_SCLKG_INTERRUPT2 0x85					
Name	Bits	R/W	Default	Comments	Config
M THR[15:8]	7:0	R/W	8	M THR[15:8]	

Register::: MN_SCLKG_INTERRUPT3 0x86					
Name	Bits	R/W	Default	Comments	Config
M THR[7:0]	7:0	R/W	71	M THR[7:0]	

Register::: MN_SCLKG_INTERRUPT4 0x87					
Name	Bits	R/W	Default	Comments	Config
IRQ_N_BY_REG_EN	7	R/W	0	0: irq by ratio value in 6E 1: irq by register value	
N THR[22:16]	6:0	R/W	0	Assert irq if M value is changing over this threshold N THR[22:16]	

Register:: MN_SCLKG_INTERRUPT5 0x88					
Name	Bits	R/W	Default	Comments	Config
N THR[15:8]	7:0	R/W	8	N THR[15:8]	

Register:: MN_SCLKG_INTERRUPT6 0x89					
Name	Bits	R/W	Default	Comments	Config
N THR[7:0]	7:0	R/W	71	N THR[7:0]	

AUDIO BUFFER

Register:: DP_AUD_CTRL 0x90					
Name	Bits	R/W	Default	Comments	Config
ABUF_EN	7	R/W	0	Enable audio buffer 0: disable. 1: enable.	
AUD_CH_ST_REG	6	R/W	0	Regenerate channel status rather than from FIFO. 0: disable. 1: enable.	
ATYPE_SRC	5	R/W	0	The source to determine the audio coding type. 0: channel status. 1: valid bit.	
ATYPE	4	R	0	Audio coding type 0: LPCM 1: non-PCM.	
DP_ATYPE	3:0	R	0	Audio coding type 0000:60958 -like other: reserved	

The following byte is read-only.

Register:: DP_AUD_ID 0x91					
Name	Bits	R/W	Default	Comments	Config
AUD_PKT_ID	7:0	R/W	0	Choose those packet with this IP to play.	

Register:: DP_AUD_BUF_STATUS 0x92					
Name	Bits	R/W	Default	Comments	Config
AUD_BUF_FULL	7	R/W	0	Audio buffer full. 0: not full. 1: full. Write 1 to clear.	Rport Wport
AUD_BUF_EMPTY	6	R/W	0	Audio buffer empty. 0: not empty. 1: empty. Write 1 to clear.	Rport Wport
AUD_BUF_OVFL	5	R/W	0	Audio buffer overflow. 0: not overflow. 1: overflow. Write 1 to clear.	Rport Wport
AUD_BUF_UDFL	4	R/W	0	Audio buffer underflow. 0: not underflow. 1: underflow. Write 1 to clear.	Rport Wport

aud_new_mode	3	R/W	1	for fix some bugs	
Sec_data_reset	2	R/W	0	Reset sec data block	
RESERVED	1:0	--	0	Reserved.	

The following byte is read-only.

Register:: DP_AUD_BUFWL					0x93
Name	Bits	R/W	Default	Comments	Config
AUD_BUFWL_MAX	7:4	R/W	0	Max buffer depth. Value: 0'h~F'h Write 0'h to clear.	Rport Wport
AUD_BUFWL_MIN	3:0	R/W	0	Min buffer depth. Value 0'h~F'h. Write F'h to clear.	Rport Wport

Register:: DP_BCH_CNT					0x94
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	--	--		
Dp_bch_cnt	4:0	R	0	DP bch cnt read flag	

0x95~0x9F are reserved.

MEASUREMENT

Register:: MN_MEAS_CTRL					0xA0
Name	Bits	R/W	Default	Comments	Config
MEAS_EN	7	R/W	0	Measurement enable 0: disable. 1: enable.	
MEAS_DONE	6	R	0	Measurement finished. 0: not finished. 1: finished.	
MEAS_POPUP	5	R	0	Pop up measure result.	Wclr_out
RESERVED	4	--	0	Reserved.	
V_BS2BS_LENGTH_H	3:0	R	0	Bit19~16 of the length between 2 vertical BS. (Counted by crystal clock)	

Register:: MN_MEAS_VLN_M					0xA1
Name	Bits	R/W	Default	Comments	Config
V_BS2BS_LENGTH_M	7:0	R	0	Bit15~8 of the length between 2 vertical BS. (Counted by crystal clock)	

Register:: MN_MEAS_VLN_L					0xA2
Name	Bits	R/W	Default	Comments	Config
V_BS2BS_LENGTH_L	7:0	R	0	Bit7~0 of the length between 2 vertical BS. (Counted by crystal clock)	

Register:: MN_MEAS_HLN_M 0xA3					
Name	Bits	R/W	Default	Comments	Config
H_BS2BS_LENGTH_M	7:0	R	0	Bit15~8 of the length between 2 horizontal BS. (Counted by crystal clock)	

Register:: MN_MEAS_HLN_L 0xA4					
Name	Bits	R/W	Default	Comments	Config
H_BS2BS_LENGTH_L	7:0	R	0	Bit7~0 of the length between 2 horizontal BS. (Counted by crystal clock)	

Register:: MN_MEAS_VBLN_M 0xA5					
Name	Bits	R/W	Default	Comments	Config
VBLK_LENGTH_M	7:0	R	0	Bit15~8 of the length during vertical blanking period. (Counted by crystal clock)	

Register:: MN_MEAS_VBLN_S 0xA6					
Name	Bits	R/W	Default	Comments	Config
VBLK_LENGTH_L	7:0	R	0	Bit7~0 of the length during vertical blanking period. (Counted by crystal clock)	

Register:: MN_MEAS_HBLN_M 0xA7					
Name	Bits	R/W	Default	Comments	Config
HBLK_LENGTH_M	7:0	R	0	Bit15~8 of the length during horizontal blanking period. (Counted by crystal clock)	

Register:: MN_MEAS_HBLN_L 0xA8					
Name	Bits	R/W	Default	Comments	Config
HBLK_LENGTH_L	7:0	R	0	Bit7~0 of the length during horizontal blanking period. (Counted by crystal clock)	

Register:: MN_MEAS_DE_BP 0xA9					
Name	Bits	R/W	Default	Comments	Config
DPF_BP[19:16]	7:4	R	0	[19:16] Vsync Back Port	
DPF_DE[19:16]	3:0	R	0	[19:16] Data Enable (excluding hblank inside the DE)	

Register:: MN_MEAS_BP_MSB 0xAA					
Name	Bits	R/W	Default	Comments	Config
DPF_BP[15:8]	7:0	R	0	[15:8] Vsync Back Port	

Register:: MN_MEAS_BP_LSB 0xAB					
Name	Bits	R/W	Default	Comments	Config

DPF_BP[7:0]	7:0	R	0	[7:0] Vsync Back Port	
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Register:: MN_MEAS_DE_MSB 0xAC					
Name	Bits	R/W	Default	Comments	Config
DPF_DE[15:8]	7:0	R	0	[15:8] Data Enable (including hblank inside the DE)	

Register:: MN_MEAS_DE_LSB 0xAD					
Name	Bits	R/W	Default	Comments	Config
DPF_DE[7:0]	7:0	R	0	[7:0] Data Enable (including hblank inside the DE)	

Register:: VHEIGHT_MSB 0xAE					
Name	Bits	R/W	Default	Comments	Config
reserved	7:4	--			
VHEIGHT[11:8]	3:0	R	0	Vheight [11:8]	

Register:: VHEIGHT_LSB 0xAF					
Name	Bits	R/W	Default	Comments	Config
VHEIGHT[7:0]	7:0	R	0	Vheight [7:0]	

ERROR COUNTER

Register:: DP_ERR_CNT_CTRL 0xB0					
Name	Bits	R/W	Default	Comments	Config
ERR_CNT_EN	7	R/W	0	Start error count. 0: stop. 1: start.	
ERR_CNT_LANE_SEL	6:5	R/W	0	Lane selector. 00: Lane 0. 00: Lane 1. 00: Lane 2. 00: Lane 3.	
ERR_CNT_SOURCE	4:2	R/W	0	Error count source. 000: Symbol error count. 001: ANSI 8B/10B decode error 010: ANSI 8B/10B disparity error 011: Both ANSI 8B/10B decode error & disparity error. 1xx: PRBS7 bit error	
ERR_CLR_SEL	1:0	R/W	0	00 :select DPCD 210 212 214 216 to clear 01: select DPCD 211 213 215 217 to clear 10: or both from 00 and 01	

Register:: DP_ERR_CNT_RESULT_M 0xB1					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7	--	0	Reserved.	
ERR_CNT_RESULT_M	6:0	R	0	Bit14~8 of error count.	

Register:: DP_ERR_CNT_RESULT_L 0xB2					
Name	Bits	R/W	Default	Comments	Config
ERR_CNT_RESULT_L	7:0	R	0	Bit7~0 of error count.	

Register:: DP_EQ_CRC_CTRL 0xB3					
Name	Bits	R/W	Default	Comments	Config
EQ_CRC_EN	7	R/W	0	EQ training CRC enable 0: disable. 1: enable.	
EQ_CRC_LANE_SEL	6:5	R/W	0	Lane selector. 00: lane0. 01: lane1. 10: lane2. 11: lane3.	
RESERVED	4	--	0	Reserved.	
LANE0_EQ_CRC_NOK	3	R/W	0	EQ CRC not OK. 0: OK. 1: not OK	Rport Wport
LANE1_EQ_CRC_NOK	2	R/W	0	EQ CRC not OK. 0: OK. 1: not OK	Rport Wport
LANE2_EQ_CRC_NOK	1	R/W	0	EQ CRC not OK. 0: OK. 1: not OK	Rport Wport
LANE3_EQ_CRC_NOK	0	R/W	0	EQ CRC not OK. 0: OK. 1: not OK	Rport Wport

Register:: DP_EQ_CRC_ANS 0xB4					
Name	Bits	R/W	Default	Comments	Config
EQ_CRC_ANS	7:0	R/W	F9	Correct CRC answer. (When calculated CRC non-equal to this value, crc_nok will go high.)	

Register:: DP_EQ_CRC 0xB5					
Name	Bits	R/W	Default	Comments	Config
EQ_CRC_OUT	7:0	R	0	Calculated CRC of the certain lane specified by “eq_crc_lane_sel”.	

0xB6~0xBF are reserved.

INFO-FRAME MEMORY

Register:: DP_INFO_FM_RSV0				0xC0	
Name	Bits	R/W	Default	Comments	Config
DP_INFO_FM_RSV0	7:0	R/W	0	Packet type of RSV0.	

Register:: DP_INFO_FM_RSV1				0xC1	
Name	Bits	R/W	Default	Comments	Config
DP_INFO_FM_RSV1	7:0	R/W	0	Packet type of RSV1.	

Register:: DP_PORT_RSV0				0xC2	
Name	Bits	R/W	Default	Comments	Config
IIC_DEB_NUM	7:4	R/W	F	IIC debounce stage number	
IIC_SCL_DEB_EN	3	R/W	0	IIC SCL from pad debounce enable.	
IIC_SDA_DEB_EN	2	R/W	0	IIC SDAL from pad debounce enable.	
DP_PORT_RSV0	1:0	R/W	0	Info frame memory address. 00'h~58'h Reserved byte	

Register:: DP_PORT_RSV1				0xC3	
Name	Bits	R/W	Default	Comments	Config
DP_PORT_RSV1	7:0	R/W	0	Info frame memory dat. Reserved byte	

Address mapping of info-frame memory.

Info-frame Type	Storage Bytes	Address
AVI	13	00'h~0C'h
AUDIO	10	0D'h~16'h
MPEG	10	17'h~20'h
RSV0	28	21'h~3C'h
RSV1	28	3D'h~58'h

WATCH-DOG

//The following byte is read-only.

Register:: DP_GLB_STATUS				0xC4	
Name	Bits	R/W	Default	Comments	Config
VBID4_CHG	7	R/W	0	VB-ID[4] has been changed. (Audio mute status) 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VBID3_CHG	6	R/W	0	VB-ID[3] has been changed. (No video stream) 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VBID2_CHG	5	R/W	0	VB-ID[2] has been changed. (Interlaced-mode) 0: not changed.	Rport Wport

				1: changed. Write 1 to clear.	
STRM_ATTR_CHG	4	R/W	0	Main Stream Attributes have been changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
AUD_CH_CNT_CHG	3	R/W	0	Audio channel count has been changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
ATYPE_CHG	2	R/W	0	Audio coding type has been changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
RESERVED	1:0	--	0	Reserved.	

InfoFrame	Bit	Description
AVI	0	Y0Y1C0C1EC0EC1EC2change
	1	A0,R0,R1,R2,R3, M0,M1 change
	2	S0,S1 any bit change
	3	PR0 ~ PR6 change
	4	ITC
	5	Q1Q0
	6	SC1,SC0 change
	7	B0,B1
AUD	8	Top bar, bottom bar, left bar , right bar change
	9	CA0~CA7 change
MPEG	10	LSV0~LSV3 DM_INH any bit change change
	11	MB#3~MB#0 change
	12	FR0 change MF1,MF0 change

Register:: DP_INFO_VAR_EN_M 0xC5					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:5	--	0	Reserved.	
VAR MPG FR EN	4	R/W	0	Enable variation monitor of MPEG FR0 / MF. 0: disable. 1: enable.	
VAR MPG MB EN	3	R/W	0	Enable variation monitor of MPEG MB0~3. 0: disable. 1: enable.	
VAR AUD LSV EN	2	R/W	0	Enable variation monitor of AUD LSV0~3 / DM_INH. 0: disable. 1: enable.	
VAR AUD CA EN	1	R/W	0	Enable variation monitor of AUD CA. 0: disable. 1: enable.	
VAR AVI BAR EN	0	R/W	0	Enable variation monitor of AVI bar. 0: disable. 1: enable.	

Register:: DP_INFO_VAR_EN_L 0xC6					
Name	Bits	R/W	Default	Comments	Config
VAR AVI B EN	7	R/W	0	Enable monitoring variation of AVI B0~1. 0: disable.	

				1: enable.	
VAR_AVI_SC_EN	6	R/W	0	Enable monitoring variation of AVI SC0~1. 0: disable. 1: enable.	
VAR_AVI_Q_EN	5	R/W	0	Enable monitoring variation of AVI Q0~1. 0: disable. 1: enable.	
VAR_AVI_ITC_EN	4	R/W	0	Enable monitoring variation of AVI ITC. 0: disable. 1: enable.	
VAR_AVI_PR_EN	3	R/W	0	Enable monitoring variation of AVI PR0~3. 0: disable. 1: enable.	
VAR_AVI_S_EN	2	R/W	0	Enable monitoring variation of AVI S0~3. 0: disable. 1: enable.	
VAR_AVI_A_EN	1	R/W	0	Enable monitoring variation of AVI A0, R0~3, M0~1. 0: disable. 1: enable.	
VAR_AVI_Y_EN	0	R/W	0	Enable monitoring variation of AVI Y0~1, C0~1, EC0~2. 0: disable. 1: enable.	

//The following byte is read-only.

Register:: DP_INFO_VAR_ST_M 0xC7					
Name	Bits	R/W	Default	Comments	Config
RESERVED	7:5	--	0	Reserved.	
VAR MPG FR	4	R/W	0	MPEG FR0 / MF changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR MPG MB	3	R/W	0	MPEG MB0~3 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR AUD LSV	2	R/W	0	AUD LSV0~3 / DM_INH changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR AUD CA	1	R/W	0	AUD CA changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR AVI BAR	0	R/W	0	AVI bar changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport

//The following byte is read-only.

Register:: DP_INFO_VAR_ST_L 0xC8					
Name	Bits	R/W	Default	Comments	Config
VAR AVI B	7	R/W	0	AVI B0~1 changed. 0: not changed.	Rport Wport

				1: changed. Write 1 to clear.	
VAR_AVI_SC	6	R/W	0	AVI SC0~1 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_Q	5	R/W	0	AVI Q0~1 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_ITC	4	R/W	0	AVI ITC changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_PR	3	R/W	0	AVI PR0~3 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_S	2	R/W	0	AVI S0~3 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_A	1	R/W	0	AVI A0, R0~3, M0~1 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport
VAR_AVI_Y	0	R/W	0	AVI Y0~1, C0~1, EC0~2 changed. 0: not changed. 1: changed. Write 1 to clear.	Rport Wport

Register::: DP_AVWD_CTRL				0xC9	
Name	Bits	R/W	Default	Comments	Config
RESERVED	7	--	0	Reserved.	
VWD_BY MPG_EN	6	R/W	0	Video watch-dog for any change of MPEG info that is monitored. 0: disable. 1: enable.	
VWD_BY AUD_EN	5	R/W	0	Video watch-dog for any change of AUD info that is monitored. 0: disable. 1: enable.	
VWD_BY AVI_EN	4	R/W	0	Video watch-dog for any change of AVI info that is monitored. 0: disable. 1: enable.	
RESERVED	3	--	0	Reserved.	
AWD_BY MPG_EN	2	R/W	0	Audio watch-dog for any change of MPEG info that is monitored. 0: disable. 1: enable.	
AWD_BY AUD_EN	1	R/W	0	Audio watch-dog for any change of AUD info that is monitored. 0: disable. 1: enable.	
AWD_BY AVI_EN	0	R/W	0	Audio watch-dog for any change of AVI info that is monitored.	

				0: disable. 1: enable.	
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Video watch dog is controlled by PageC A2[7:5], clear watch dog flag must turn off watch dog first.

Register:: DP_VWD_CTRL					0xCA
Name	Bits	R/W	Default	Comments	Config
VWD_BY_MN_NLOCK_EN	7	R/W	0	Video watch dog for M/N nonlock 0: disable. 1: enable.	
VWD_BY_VS_NLOCK_EN	6	R/W	0	Video watch dog for VS nonlock 0: disable. 1: enable.	
VWD_BY_VFIFO_OVF_EN	5	R/W	0	Video watch dog for Video FIFO overflow. 0: disable. 1: enable.	
VWD_BY_VFIFO_UDF_EN	4	R/W	0	Video watch dog for Video FIFO underflow. 0: disable. 1: enable.	
VWD_BY_STRM_ATTR_CHG_EN	3	R/W	0	Video watch dog for any change of Main-stream attributes. 0: disable. 1: enable.	
VWD_BY_INVALID_EN	2	R/W	0	Video watch dog for any invalidity from PHY. Video watch dog for any lane decode error. 0: disable. 1: enable.	
VWD_BY_VBID3_EN	1	R/W	0	Video watch dog for any change of VB-ID[3] 0: disable. 1: enable.	
VWD_BY_VBID2_EN	0	R/W	0	Video watch dog for any change of VB-ID[2] 0: disable. 1: enable.	

Audio watch dog is controlled by Page2 CA-30[4]

Register:: DP_AWD_CTRL					0xCB
Name	Bits	R/W	Default	Comments	Config
AWD_BY_ABUF_OVF_EN	7	R/W	0	Audio watch dog for audio buffer overflow 0: disable. 1: enable.	
AWD_BY_ABUF_UDF_EN	6	R/W	0	Audio watch dog for audio buffer underflow 0: disable. 1: enable.	
AWD_BY_STRM_ATTR_CHG_EN	5	R/W	0	Audio watch dog for any change of Main-stream attributes. 0: disable. 1: enable.	
AWD_BY_INVALID_EN	4	R/W	0	Audio watch dog for any invalidity from PHY. Audio watch dog for any lane decode error. 0: disable. 1: enable.	

AWD_BY_VBID4_EN	3	R/W	0	Audio watch dog for any VB-ID[4] going high. 0: disable. 1: enable.	
AWD_BY_VBID3_EN	2	R/W	0	Audio watch dog for any VB-ID[3] going high. 0: disable. 1: enable.	
AWD_BY_VBID2_EN	1	R/W	0	Audio watch dog for any VB-ID[2] going high. 0: disable. 1: enable.	
AWD_BY_ATYPE_EN	0	R/W	0	Audio watch dog for audio coding type change. 0: disable. 1: enable.	

INTERRUPT

Register::: DP_IRQ_CTRL0 0xCC					
Name	Bits	R/W	Default	Comments	Config
IRQ	7	R/W	0	IRQ happened. (Read-only) 0: no irq. 1: irq happened. Write 1 to clear.	Rport Wport
IRQ_BY MPG_EN	6	R/W	0	IRQ for any change of MPEG info that is monitored. 0: disable. 1: enable.	
IRQ_BY AUD_EN	5	R/W	0	IRQ for any change of AUD info that is monitored. 0: disable. 1: enable.	
IRQ_BY AVI_EN	4	R/W	0	IRQ for any change of AVI info that is monitored. 0: disable. 1: enable.	
IRQ_BY MN_NLOCK_EN	3	R/W	0	IRQ for M/N nonlock 0: disable. 1: enable.	
IRQ_BY VS_NLOCK_EN	2	R/W	0	IRQ for VS nonlock 0: disable. 1: enable.	
IRQ_BY VFIFO_OVF_EN	1	R/W	0	IRQ for Video FIFO overflow. 0: disable. 1: enable.	
IRQ_BY VFIFO_UDF_EN	0	R/W	0	IRQ for Video FIFO underflow. 0: disable. 1: enable.	

Register::: DP_IRQ_CTRL1 0xCD					
Name	Bits	R/W	Default	Comments	Config
IRQ_BY STRM_ATTR_CHG_EN	7	R/W	0	IRQ for any change of Main-stream attributes. 0: disable. 1: enable.	
IRQ_BY INVALID_EN	6	R/W	0	IRQ for any invalidity from PHY. IRQ for any lane decode error. 0: disable. 1: enable.	

IRQ_BY_VBID4_EN	5	R/W	0	IRQ for any change of VB-ID[4]. 0: disable. 1: enable.	
IRQ_BY_VBID3_EN	4	R/W	0	IRQ for any change of VB-ID[3]. 0: disable. 1: enable.	
IRQ_BY_VBID2_EN	3	R/W	0	IRQ for any change of VB-ID[2]. 0: disable. 1: enable.	
IRQ_BY_ABUF_OVF_EN	2	R/W	0	IRQ for audio buffer overflow. 0: disable. 1: enable.	
IRQ_BY_ABUF_UDF_EN	1	R/W	0	IRQ for audio buffer underflow. 0: disable. 1: enable.	
IRQ_BY_ATYPE_EN	0	R/W	0	IRQ for audio coding tpye change. 0: disable. 1: enable.	

Address 0xB3 DP port end

RESERVED BITS

Register::: REV_PORT_0 0xD0					
Name	Bits	R/W	Default	Comments	Config
REV_P0	7:0	R/W	0	Reserved R/W	

Register::: REV_PORT_1 0xD1					
Name	Bits	R/W	Default	Comments	Config
REV_P1	7:0	R/W	FF	Reserved R/W	

Register::: REV_PORT_2 0xD2					
Name	Bits	R/W	Default	Comments	Config
REV_P2	7:0	R/W	0	Reserved R/W	

Register::: REV_PORT_3 0xD3					
Name	Bits	R/W	Default	Comments	Config
REV_P3	7:0	R/W	FF	Reserved R/W	

Register::: REV_PORT_4 0xD4					
Name	Bits	R/W	Default	Comments	Config
REV_P4	7:0	R/W	0	Reserved R/W	

Register::: REV_PORT_5 0xD5					
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Name	Bits	R/W	Default	Comments	Config
REV_P5	7:0	R/W	FF	Reserved R/W	

DISPLAYPORT ACCESSING PORT (END)

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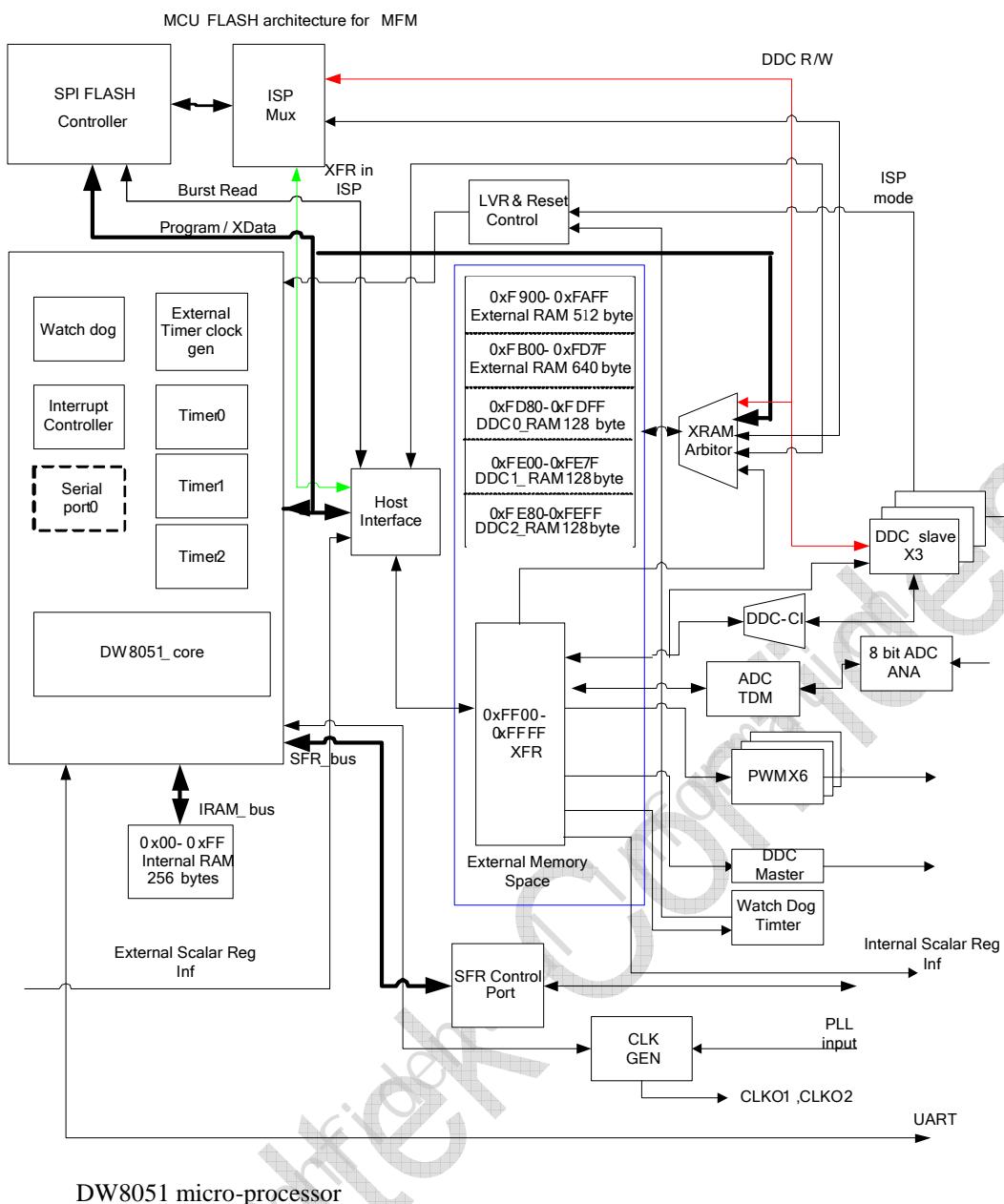
MCU register 1(page D)

Embedded MCU Function

Designware DW8051 of Synopsys is integrated into this chip and is compatible with other industry 8051 series. A lot of peripherals are integrated and accessed by XFR (eXternal Function Register). When embedded MCU is used, scalar-related registers are access via XFR, too. The program code is stored in external serial FLASH. If the external MCU is used, the integrated peripherals can be accessed via special page in scalar's register map.

Features

- 8051 core, CPU operating frequency up to 50MHz
- 256-byte IRAM, 1.5K byte shared XRAM
- external serial FLASH, support GPIO bank switching for 128K byte and up to 16M bytes for XFR bank switching
- Compliant with VESA DDC1/2B/2Bi/CI
- Embedded triple ports DDC RAM(0~768 bytes shared with XRAM)
- Six channels of PWM DAC
- Watchdog timer with programmable interval
- Three 16-bit counters/timers (T0, T1, and ET2)
- Programmable frequency clock output, 2 clock output ports
- One full-duplex serial port
- Six interrupt sources with 2 external interrupts
- Four channels of 8-bit ADC
- Hardware ISP, no boot code required
- Built-in Low voltage reset circuit



The DW8051 is compatible with industry standard 803x/805x and provides the following design features and enhancements to the standard 8051 microcontroller:

High speed architecture

Compared to standard 8051, the DW8051 processor core provides increased performance by executing instructions in a 4-clock bus cycle, as opposed to the 12-clock bus cycle in the standard 8051. The shortened bus timing improves the instruction execution rate for most instructions by a factor of three over the standard 8051 architectures. The average speed improvement for the entire instruction set is approximately 2.5X.

Stretch Memory Cycles

The stretch memory cycle feature enables application software to adjust the speed of data memory access. The DW8051 can execute the MOVX instruction in as little as 2 instruction cycles. However, it is sometimes desirable to stretch this value; for example, to access slow memory or slow memory-mapped peripherals such as UARTs or LCDs.

The three LSBs of the Clock Control Register (at SFR location 8Eh) control the stretch value. You can use stretch values between zero and seven. A stretch value of zero adds zero instruction cycles, resulting in MOVX instructions executing in two instruction cycles. A stretch value of seven adds seven instruction cycles, resulting in MOVX instructions executing in nine instruction cycles. The stretch value can be changed dynamically under program control.

By default, the stretch value resets to one (three cycle MOVX). For full-speed data memory access, the software must set the stretch value to zero. The stretch value affects only data memory access. The only way to reduce the speed of program memory (ROM) access is to use a slower clock.

Dual Data Pointers

The DW8051 employs dual data pointers to accelerate data memory block moves. The standard 8051 data pointer (DPTR) is a 16-bit value used to address external data RAM or peripherals. The DW8051 maintains the standard data pointer as DPTR0 at SFR locations 82h and 83h. It is not necessary to modify code to use DPTR0.

The DW8051 adds a second data pointer (DPTR1) at SFR locations 84h and 85h. The SEL bit in the DPTR Select register, DPS (SFR 86h), selects the active pointer. When SEL = 0, instructions that use the DPTR will use DPL0 and DPH0. When SEL = 1, instructions that use the DPTR will use DPL1 and DPH1. SEL is the bit 0 of SFR location 86h. No other bits of SFR location 86h are used.

All DPTR-related instructions use the currently selected data pointer. To switch the active pointer, toggle the SEL bit. The fastest way to do so is to use the increment instruction (INC DPS). This requires only one instruction to switch from a source address to a destination address, saving application code from having to save source and destination addresses when doing a block move.

Using dual data pointers provides significantly increased efficiency when moving large blocks of data.

Timer Rate Control

One important difference exists between the DW8051 and 80C32 regarding timers. The original 80C32 used a 12 clock per cycle scheme for timers and consequently for some serial baud rates(depending on the mode). The DW8051 architecture normally runs using 4 clocks per cycle. However, in the area of timers, it will default to a 12 clock per cycle scheme on a reset. This allows existing code with real-time dependencies such as baud rates to operate properly. If an application needs higher speed timers or serial baud rates, the timers can be set to run at the 4 clock rate. The Clock Control register (CKCON – 8Eh) determines these timer speeds. When the relevant CKCON bit is a logic 1, the device uses 4 clocks per cycle to generate timer speeds. When the control bit is set to a zero, the device uses 12 clocks for timer speeds. The reset condition is a 0. CKCON.5 selects the speed of Timer 2. CKCON.4 selects Timer 1 and CKCON.3 selects Timer zero. Note that unless a user desires very fast timing, it is unnecessary to alter these bits. Note that the timer controls are independent.

RESET

There are five reset sources.

- RST pin
The external reset is high active and its pulse width must be larger than 8 clock cycles. The RST pin can reset the DW8051
- Low voltage reset(LVR) and power on reset(POR)
- Software can use SOF_RST register to reset whole chip

- Watchdog can reset DW8051
- When entering ISP mode, DW8051 will enter reset state. When exiting ISP mode, DW8051 will also assert a reset, too.

Special Function Registers

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP									81h
DPL0									82h
DPH0									83h
DPL1									84h
DPH1									85h
DPS	0	0	0	0	0	0	SEL		86h
PCON	SMOD 0		1	1	GF1	GF0	STOP	IDLE	87h
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	88h
TMOD	GATE	C/T	M1	M0	GATE	C/T	M1	M0	89h
TL0									8Ah
TL1									8Bh
TH0									8Ch
TH1									8Dh
CKCON			T2M	T1M	T0M	MD2	MD1	MD0	8Eh
SPC_FNC	0	0	0	0	0	0	WRS		8Fh
P1_W	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	90h
MPAGE									92h
P1_R	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	93h
SCON0	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	98h
SBUF0									99h
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	A0h
IE	EA	0	ET2	ES0	ET1	EX1	ET0	EX0	A8h
P3_W	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B0h
P3_R	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	B3h
IP	1	0	PT2	PS0	PT1	PX1	PT0	PX0	B8h
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/ RL2	C8h
RCAP2L									CAh
RCAP2H									CBh
TL2									CCh
TH2									CDh
PSW	CY	AC	F0	RS1	RS0	OV	F1	P	D0h
ACC									E0h
B									F0h

SFR reset value

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Addr
SP	0	0	0	0	0	1	1	1	81h
DPL0	0	0	0	0	0	0	0	0	82h
DPH0	0	0	0	0	0	0	0	0	83h
DPL1	0	0	0	0	0	0	0	0	84h
DPH1	0	0	0	0	0	0	0	0	85h
DPS	0	0	0	0	0	0	0	0	86h
PCON	0	0	1	1	0	0	0	0	87h
TCON	0	0	0	0	0	0	0	0	88h
TMOD	0	0	0	0	0	0	0	0	89h
TL0	0	0	0	0	0	0	0	0	8Ah
TL1	0	0	0	0	0	0	0	0	8Bh
TH0	0	0	0	0	0	0	0	0	8Ch
TH1	0	0	0	0	0	0	0	0	8Dh
CKCON	0	0	0	0	0	0	0	1	8Eh
SPC_FNC	0	0	0	0	0	0	0	0	8Fh
P1_W	1	1	1	1	1	1	1	1	90h
MPAGE	0	0	0	0	0	0	0	0	92h
SCON0	0	0	0	0	0	0	0	0	98h
SBUF0	0	0	0	0	0	0	0	0	99h
P2	0	0	0	0	0	0	0	0	A0h
IE	0	0	0	0	0	0	0	0	A8h
P3_W	1	1	1	1	1	1	1	1	B0h
IP	1	0	0	0	0	0	0	0	B8h
T2CON	0	0	0	0	0	0	0	0	C8h
RCAP2L	0	0	0	0	0	0	0	0	CAh
RCAP2H	0	0	0	0	0	0	0	0	CBh
TL2	0	0	0	0	0	0	0	0	CCh
TH2	0	0	0	0	0	0	0	0	CDh
PSW	0	0	0	0	0	0	0	0	D0h
ACC	0	0	0	0	0	0	0	0	E0h
B	0	0	0	0	0	0	0	0	F0h

DW8051 user-modifiable parameters

ram_256	1
timer2	1
rom_addr_size	0
Serial	1
extd_intr	0

REG_XFR_WRAPPER is the eXternal Function Register defined in 0xFF00 ~ 0xFFFF in DW8051's XDATA memory space. There are three possible input sources for REG_XFR_WRAPPER. In embedded MCU mode, DW8051 has the power of control.

	PAGE D						PAGE E						PAGE F			
	A	B	C	D	E	F	A	B	C	D	E	F	A	B	C	D
0xFFXX	0X	1X	2X	3X	4X	5X	6X	7X	8X	9X	AX	BX	CX	DX	EX	FX
X0	IRQ	ADC	ADC_DDC	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	SPI-FLASH	PWM	GPIO	WD	GPIO	GPIO	GPIO	SPI_WP
X1	IRQ	ADC	ADC_DDC	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	SPI-FLASH	PWM	GPIO		GPIO	GPIO	GPIO	
X2	VS IRQ	ADC	VSYNC_Sel	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	SPI-FLASH	PWM	GPIO		GPIO	GPIO	SFR	PWM_I2C
X3	OSD turbo	ADC	DDC-CI	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	I2C	PWM	GPIO		GPIO	GPIO	SFR	SCA
X4	OSD turbo	ADC	DDC-CI	DDC-CI	PWM	PWM	SPI-FLASH	SPI-FLASH	I2C	PWM	GPIO		GPIO	GPIO	EDID_I_RQ	SCA
X5	OSD turbo	ADC	DDC-CI	DDC-CI	PWM	I2C	SPI-FLASH	SPI-FLASH	I2C	PWM	Flash		GPIO	GPIO	EDID_I_RQ	SCA
X6	OSD turbo	ADC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	SPI-FLASH	I2C	PWM	Flash		GPIO	GPIO	GPIO	SCA
X7	OSD turbo	ADC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	I2C	PWM	Flash		GPIO	GPIO		SCA
X8	ADC	OSD turbo	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	I2C	PWM	Flash		GPIO	GPIO		SCA
X9	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	Flash		GPIO	GPIO	Dummy	SCA
XA	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	WD		GPIO	GPIO	WD	SCA
XB	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	WD		GPIO	GPIO	WD	SCA
XC	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	PWM	WD		GPIO	GPIO	ISP	Bank-Switch
XD	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash	WD		GPIO	GPIO	ISP	Bank-Switch
XE	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash	WD		GPIO	GPIO	ISP	Bank-Switch
XF	ADC	ADC_DDC	DDC-CI	PWM	PWM	I2C	SPI-FLASH	GPIO	GPIO	Flash	WD		GPIO	GPIO	ISP	Bank-Switch



0xFF00	(Page D) 0xA0	0xFF10	(Page D) 0xB0	0xFF20	(Page D) 0xC0	0xFF30	(Page D) 0xD0	0xFF40	(Page D) 0xE0	0xFF50	(Page D) 0xF0
0xFF01	(Page D) 0xA1	0xFF11	(Page D) 0xB1	0xFF21	(Page D) 0xC1	0xFF31	(Page D) 0xD1	0xFF41	(Page D) 0xE1	0xFF51	(Page D) 0xF1
0xFF02	(Page D) 0xA2	0xFF12	(Page D) 0xB2	0xFF22	(Page D) 0xC2	0xFF32	(Page D) 0xD2	0xFF42	(Page D) 0xE2	0xFF52	(Page D) 0xF2
0xFF03	(Page D) 0xA3	0xFF13	(Page D) 0xB3	0xFF23	(Page D) 0xC3	0xFF33	(Page D) 0xD3	0xFF43	(Page D) 0xE3	0xFF53	(Page D) 0xF3
0xFF04	(Page D) 0xA4	0xFF14	(Page D) 0xB4	0xFF24	(Page D) 0xC4	0xFF34	(Page D) 0xD4	0xFF44	(Page D) 0xE4	0xFF54	(Page D) 0xF4
0xFF05	(Page D) 0xA5	0xFF15	(Page D) 0xB5	0xFF25	(Page D) 0xC5	0xFF35	(Page D) 0xD5	0xFF45	(Page D) 0xE5	0xFF55	(Page D) 0xF5
0xFF06	(Page D) 0xA6	0xFF16	(Page D) 0xB6	0xFF26	(Page D) 0xC6	0xFF36	(Page D) 0xD6	0xFF46	(Page D) 0xE6	0xFF56	(Page D) 0xF6
0xFF07	(Page D) 0xA7	0xFF17	(Page D) 0xB7	0xFF27	(Page D) 0xC7	0xFF37	(Page D) 0xD7	0xFF47	(Page D) 0xE7	0xFF57	(Page D) 0xF7
0xFF08	(Page D) 0xA8	0xFF18	(Page D) 0xB8	0xFF28	(Page D) 0xC8	0xFF38	(Page D) 0xD8	0xFF48	(Page D) 0xE8	0xFF58	(Page D) 0xF8
0xFF09	(Page D) 0xA9	0xFF19	(Page D) 0xB9	0xFF29	(Page D) 0xC9	0xFF39	(Page D) 0xD9	0xFF49	(Page D) 0xE9	0xFF59	(Page D) 0xF9
0xFF0A	(Page D) 0xAA	0xFF1A	(Page D) 0xBA	0xFF2A	(Page D) 0xCA	0xFF3A	(Page D) 0xDA	0xFF4A	(Page D) 0xEA	0xFF5A	(Page D) 0xFA
0xFF0B	(Page D) 0xAB	0xFF2B	(Page D) 0xBB	0xFF2B	(Page D) 0xCE	0xFF3B	(Page D) 0xDB	0xFF4B	(Page D) 0xEB	0xFF5B	(Page D) 0xFB
0xFF0C	(Page D) 0xAC	0xFF1C	(Page D) 0xBC	0xFF2C	(Page D) 0xCC	0xFF3C	(Page D) 0xDC	0xFF4C	(Page D) 0xEC	0xFF5C	(Page D) 0xFC
0xFF0D	(Page D) 0xAD	0xFF1D	(Page D) 0xBD	0xFF2D	(Page D) 0xCD	0xFF3D	(Page D) 0xDD	0xFF4D	(Page D) 0xED	0xFF5D	(Page D) 0xFD
0xFF0E	(Page D) 0xAE	0xFF1E	(Page D) 0xBE	0xFF2E	(Page D) 0xCE	0xFF3E	(Page D) 0xDE	0xFF4E	(Page D) 0xEE	0xFF5E	(Page D) 0xFE
0xFF0F	(Page D) 0xAF	0xFF1F	(Page D) 0xBF	0xFF2F	(Page D) 0xCF	0xFF3F	(Page D) 0xDF	0xFF4F	(Page D) 0xEF	0xFF5F	(Page D) 0xFF

0xFF60	(Page E) 0xA0	0xFF70	(Page E) 0xB0	0xFF80	(Page E) 0xC0	0xFF90	(Page E) 0xD0	0xFFA0	(Page E) 0xE0	0xFFB0	(Page E) 0xF0
0xFF61	(Page E) 0xA1	0xFF71	(Page E) 0xB1	0xFF81	(Page E) 0xC1	0xFF91	(Page E) 0xD1	0xFFA1	(Page E) 0xE1	0xFFB1	(Page E) 0xF1
0xFF62	(Page E) 0xA2	0xFF72	(Page E) 0xB2	0xFF82	(Page E) 0xC2	0xFF92	(Page E) 0xD2	0xFFA2	(Page E) 0xE2	0xFFB2	(Page E) 0xF2
0xFF63	(Page E) 0xA3	0xFF73	(Page E) 0xB3	0xFF83	(Page E) 0xC3	0xFF93	(Page E) 0xD3	0xFFA3	(Page E) 0xE3	0xFFB3	(Page E) 0xF3
0xFF64	(Page E) 0xA4	0xFF74	(Page E) 0xB4	0xFF84	(Page E) 0xC4	0xFF94	(Page E) 0xD4	0xFFA4	(Page E) 0xE4	0xFFB4	(Page E) 0xF4
0xFF65	(Page E) 0xA5	0xFF75	(Page E) 0xB5	0xFF85	(Page E) 0xC5	0xFF95	(Page E) 0xD5	0xFFA5	(Page E) 0xE5	0xFFB5	(Page E) 0xF5
0xFF66	(Page E) 0xA6	0xFF76	(Page E) 0xB6	0xFF86	(Page E) 0xC6	0xFF96	(Page E) 0xD6	0xFFA6	(Page E) 0xE6	0xFFB6	(Page E) 0xF6
0xFF67	(Page E) 0xA7	0xFF77	(Page E) 0xB7	0xFF87	(Page E) 0xC7	0xFF97	(Page E) 0xD7	0xFFA7	(Page E) 0xE7	0xFFB7	(Page E) 0xF7
0xFF68	(Page E) 0xA8	0xFF78	(Page E) 0xB8	0xFF88	(Page E) 0xC8	0xFF98	(Page E) 0xD8	0xFFA8	(Page E) 0xE8	0xFFB8	(Page E) 0xF8
0xFF69	(Page E) 0xA9	0xFF79	(Page E) 0xB9	0xFF89	(Page E) 0xC9	0xFF99	(Page E) 0xD9	0xFFA9	(Page E) 0xE9	0xFFB9	(Page E) 0xF9
0xFF6A	(Page E) 0xAA	0xFF7A	(Page E) 0xBA	0xFF8A	(Page E) 0xCA	0xFF9A	(Page E) 0xDA	0xFFAA	(Page E) 0xEA	0xFFBA	(Page E) 0xFA
0xFF6B	(Page E) 0xAB	0xFF7B	(Page E) 0xBB	0xFF8B	(Page E) 0xCB	0xFF9B	(Page E) 0xDB	0xFFAB	(Page E) 0xEB	0xFFBB	(Page E) 0xFB
0xFF6C	(Page E) 0xAC	0xFF7C	(Page E) 0xBC	0xFF8C	(Page E) 0xCC	0xFF9C	(Page E) 0xDC	0xFFAC	(Page E) 0xEC	0xFFBC	(Page E) 0xFC
0xFF6D	(Page E) 0xAD	0xFF7D	(Page E) 0xBD	0xFF8D	(Page E) 0xCD	0xFF9D	(Page E) 0xDD	0xFFAD	(Page E) 0xED	0xFFBD	(Page E) 0xFD
0xFF6E	(Page E) 0xAE	0xFF7E	(Page E) 0xBE	0xFF8E	(Page E) 0xCE	0xFF9E	(Page E) 0xDE	0xFFAE	(Page E) 0xEE	0xFFBE	(Page E) 0xFE
0xFF6F	(Page E) 0xAF	0xFF7F	(Page E) 0xBF	0xFF8F	(Page E) 0xCF	0xFF9F	(Page E) 0xDF	0xFFAF	(Page E) 0xEF	0xFFBF	(Page E) 0xFF

0xFFC0	(Page F) 0xA0	0xFFD0	(Page F) 0xB0	0xFFE0	(Page F) 0xC0	0xFFFF0	(Page F) 0xD0				
0xFFC1	(Page F) 0xA1	0xFFD1	(Page F) 0xB1	0xFFE1	(Page F) 0xC1	0xFFFF1	(Page F) 0xD1				
0xFFC2	(Page F) 0xA2	0xFFD2	(Page F) 0xB2	0xFFE2	(Page F) 0xC2	0xFFFF2	(Page F) 0xD2				
0xFFC3	(Page F) 0xA3	0xFFD3	(Page F) 0xB3	0xFFE3	(Page F) 0xC3	0xFFFF3	(Page F) 0xD3				
0xFFC4	(Page F) 0xA4	0xFFD4	(Page F) 0xB4	0xFFE4	(Page F) 0xC4	0xFFFF4	(Page F) 0xD4				
0xFFC5	(Page F) 0xA5	0xFFD5	(Page F) 0xB5	0xFFE5	(Page F) 0xC5	0xFFFF5	(Page F) 0xD5				
0xFFC6	(Page F) 0xA6	0xFFD6	(Page F) 0xB6	0xFFE6	(Page F) 0xC6	0xFFFF6	(Page F) 0xD6				
0xFFC7	(Page F) 0xA7	0xFFD7	(Page F) 0xB7	0xFFE7	(Page F) 0xC7	0xFFFF7	(Page F) 0xD7				
0xFFC8	(Page F) 0xA8	0xFFD8	(Page F) 0xB8	0xFFE8	(Page F) 0xC8	0xFFFF8	(Page F) 0xD8				
0xFFC9	(Page F) 0xA9	0xFFD9	(Page F) 0xB9	0xFFE9	(Page F) 0xC9	0xFFFF9	(Page F) 0xD9				
0xFFCA	(Page F) 0xAA	0xFFDA	(Page F) 0xBA	0xFFEA	(Page F) 0xCA	0xFFFFA	(Page F) 0xDA				
0xFFCB	(Page F) 0xAB	0xFFDB	(Page F) 0xBB	0xFFEB	(Page F) 0xCB	0xFFFFB	(Page F) 0=DB				
0xFFCC	(Page F) 0xAC	0xFFDC	(Page F) 0xBC	0xFFEC	(Page F) 0xCC	0xFFFFC	(Page F) 0xDC				
0xFFCD	(Page F) 0xAD	0xFFDD	(Page F) 0xBD	0xFFED	(Page F) 0xCD	0xFFFFD	(Page F) 0xDD				
0xFFCE	(Page F) 0xAF	0xFFDE	(Page F) 0xBE	0xFFEE	(Page F) 0xCF	0xFFFFE	(Page F) 0xDE				
0xFFCF	(Page F) 0xAF	0xFFDF	(Page F) 0xBF	0xFFEF	(Page F) 0xCF	0xFFFFF	(Page F) 0xDF				

In external MCU mode, external host interface has the privilege to access REG_XFR_WRAPPER. The total 256 addresses are separated into 3 pages. 0xFF00 ~ 0xFF5F is Page D, 0xFF60 ~0xFFBF is Page E and 0xFFC0 ~ 0xFFFF is Page F. External host control signals are passed to scalar register interface. Host interface must integrate the output of scalar interface and REG_XFR_WRAPPER depends on page selection.

When ISP is activated, REG_XFR_WRAPPER is accessed by ISP interface, it has the highest priority. DW8051 and external host is selected by power-on-latch signal, ext_host_sel.

Interrupt Control

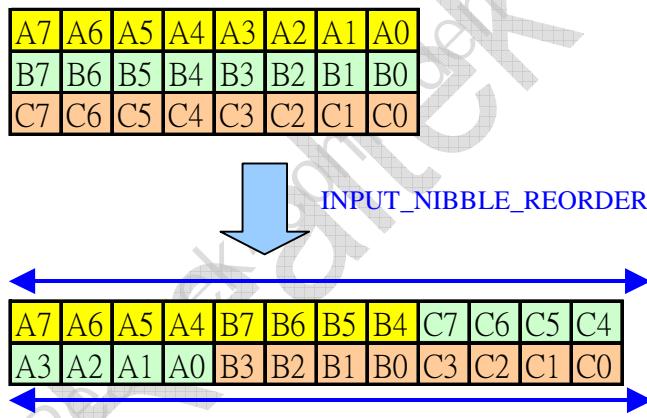
Register::IRQ_Status 0xFF00					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	--	--	Reserved	
M2PLL_IRQ_EVENT	6	R/W	0	M2PLL-abnormal Event Status 1. Select M2PLL as clock source, but M2PLL power down, power saving or output disable, clear this bit to disable the interrupt	Rport Wport
Reserved	5	R/W	0	Reserved	Rport Wport
SCA_IRQ_EVENT	4	R/W	0	Scalar-related Event Status 1. IF Scalar integrated IRQ event occurred since the last status cleared	Rport Wport
I2CM_IRQ_EVENT	3	R/W	0	I2C module Event Status 1. IF I2C module IRQ event occurred since the last status cleared	Rport Wport
ADC_IRQ_EVENT	2	R/W	0	ADC Event Status 1: If the ADC IRQ event occurred since the last status cleared	Rport Wport
WDT_IRQ_EVENT	1	R/W	0	WDT_IRQ event status 1: If the WDT_IRQ event occurred since the last status cleared	Rport Wport
DDC_IRQ_EVENT	0	R/W	0	DDC Event Status 1: If the DDC IRQ event occurred since the last status cleared	Rport Wport

Register::IRQ_Priority 0xFF01					
Name	Bits	R/W	Default	Comments	Config
Reserved	7	--	--	Reserved	
M2PLL_IRQ_PRI	6	R/W	0	M2PLL-abnormal IRQ Priority 0: Connected to int0 1: Connected to int1	
Reserved	5	R/W	0	Reserved	
SCA_IRQ_PRI	4	R/W	0	Scalar integrated IRQ Priority 0: Connected to int0 1: Connected to int1	
I2CM_IRQ_PRI	3	R/W	0	I2C module IRQ Priority 0: Connected to int0 1: Connected to int1	
ADC_IRQ_PRI	2	R/W	0	ADC IRQ Priority 0: Connected to int0 1: Connected to int1	
WDT_IRQ_PRI	1	R/W	0	WDT IRQ Priority 0: Connected to int0 1: Connected to int1	

DDC_IRQ_PRI	0	R/W	0	DDC IRQ Priority 0: Connected to int0 1: Connected to int1	
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Register::: VSYNC_IRQREV_DUMMY1 0xFF02					
Name	Bits	R/W	Default	Comments	Config
VS1_IRQ_PRI	7	R/W	1	VS1 IRQ Priority 0: Connected to int0 1: Connected to int1	
VS0_IRQ_PRI	6	R/W	0	VS0 IRQ Priority 0: Connected to int0 1: Connected to int1	
VS1_IRQ_EVENT	5	R/W	0	VS1 Event Status, write 0 to clear	
VS0_IRQ_EVENT	4	R/W	0	VS0 Event Status, , write 0 to clear	
VS1_INT_EN	3	R/W	0	VS1 Interrupt enable 0: disable 1 :enable	
VS1_trigger_type	2	R/W	0	VS1 trigger type 0: posedge trigger 1: bypass mode (level trigger)	
VS0_INT_EN	1	R/W	0	VS0 Interrupt enable 0: disable 1: enable	
VS0_trigger_type	0	R/W	0	VS0 trigger type 0: posedge trigger 1: bypass mode (level trigger)	

OSD reorder



Register:::Triple_Bytes_Operation 0xFF03					
Name	Bits	R/W	Default	Comments	Config
GLOBAL_NIBBLE_REORDER_EN	7	R/W	0	1: The input bit sequence of three bytes, A[7:0], B[7:0] C[7:0] will be reordered to A[7:4], B[7:4], C[7:4], A[3:0], B[3:0], C[3:0] before any operation and change back to input sequence at the end 0: No modification	
INPUT_NIBBLE_REORDER_EN	6	R/W	1	1: The input bit sequence of three bytes,	

				A[7:0], B[7:0], C[7:0] will be reordered to {A[7:4], B[7:4], C[7:4]}, {A[3:0], B[3:0], C[3:0]} before any operation 0: No modification	
OUTPUT_NIBBLE_REORDER_EN	5	R/W	0	1: The output bit sequence of three bytes, A[7:4], B[7:4], C[7:4], A[3:0], B[3:0], C[3:0] will be reordered to A[7:0], B[7:0], C[7:0] before output 0: No modification	
TBO_dummy	4	R/W	0	Dummy Bit	
FIRST_BYTE_SHIFT_DIRECTION	3	R/W	1	1: LEFT SHIFT 0: RIGHT SHIFT	
LEFT_BYTE_SHIFT_DIRECTION	2	R/W	0	1: LEFT SHIFT 0: RIGHT SHIFT	
RESTART_FROM_LAST	1	R/W	0	1: Restart from last three bytes (auto_clear)	rport WPORT
RESTART_FROM_FIRST	0	R/W	0	1: Restart from input first bytes (auto_clear)	RPORT WPORT

Register::Shift_Bits_Number 0xFF04					
Name	Bits	R/W	Default	Comments	Config
FIRST_BITS_SHIFT	7:4	R/W	0	The left/right bit shift times.	
SECOND_BITS_SHIFT	3:0	R/W	0	The left/right bit shift times.	

Register::Byte_Address 0xFF05					
Name	Bits	R/W	Default	Comments	Config
THIRD_BITS_SHIFT	7:4	R/W	0	The left/right bit shift times.	
LEFT_BITS_SHIFT	3:0	R/W	0	The left/right bit shift times.	

Register::Input_Triple_Bytes 0xFF06					
Name	Bits	R/W	Default	Comments	Config
INPUT_OP_BYTES	7:0	R/W	0	Three bytes input by sequence here.	Rport Wport

Register::Result_Triple_Bytes 0xFF07					
Name	Bits	R/W	Default	Comments	Config
OUTPUT_OP_BYTES	7:0	R/W	0	Output bytes input by sequence here.	RPORT WPORT

Register::Byte_Address 0xFF18					
Name	Bits	R/W	Default	Comments	Config
ALL_ADDR_RST	7	R/W	0	1: Write 1 to reset input/result triple bytes address to 0	RPORT WPORT
Reserved	6:3	R/W	--	Reserved	
INPUT_OUTPUT_CONTROL	2	R/W	0	1: Write BYTE_ADDR to control address of result triple bytes 0: Write BYTE_ADDR to control address of input triple bytes	Rport Wport
BYTE_ADDR	1:0	R/W	0	Byte Address for Current Input or Result bytes	Rport Wport

ADC

A/D Converter

RTD2485XD has embedded 4 channels of analog-to-digital converter by A_circuit. The ADCs_ACKT convert analog input voltage on the four A/D input pins to four 8-bit digital data stored in XFRs (FF09 ~ FF0C) sequentially.

The ADC conversion range is from GND to VDD and the conversion is linear and monotonic with no missing codes. To start A/D conversion, set STRT_ADCx = 1 and the conversion will be completed in less than 12us for 4 channels.

ADC_Ackt block diagram (for Key Sensing, D-connector)

Register::ADC_Acontrol 0xFF08					
Name	Bits	R/W	Default	Comments	Config
STRT_ADC_ACKT	7	R/W	0	Write 1 to start the A/D conversion. Auto clear when A/D Conversion has been completed. 0:A/D Conversion has been completed 1:A/D Conversion is not completed yet	Rport Wport
ADC_ATEST	6	R/W	0	0: Normal operation 1: ADC test mode	
Reserved	5:3	R/W	0	Reserved	
ADC_A_BIAS_ADJ	2:1	R/W	1	ADC bias current adjust 00: 5u 01: 20u 10: 10u 11: 30u	
ADC_A_CK_SEL	0	R/W	0	Inverse ADC input clock pos/neg 0: pos 1: neg	

Register::ADC_A0_convert_result 0xFF09					
Name	Bits	R/W	Default	Comments	Config
ADC_A0_DATA	7:0	R	FF	Converted data of ADC_A0	

Register::ADC_A1_convert_result 0xFF0A					
Name	Bits	R/W	Default	Comments	Config
ADC_A1_DATA	7:0	R	FF	Converted data of ADC_A1	

Register::ADC_A2_convert_result 0xFF0B					
Name	Bits	R/W	Default	Comments	Config
ADC_A2_DATA	7:0	R	FF	Converted data of ADC_A2	

Register::ADC_A3_convert_result 0xFF0C					
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Name	Bits	R/W	Default	Comments	Config
ADC_A3_DATA	7:0	R	FF	Converted data of ADC_A3	

Register:::ADC_CLK_DIV					0xFF0D
Name	Bits	R/W	Default	Comments	Config
ADC_CLK_SEL	7	R/W	0	ADC clk from 0: Xtal/IOSC 1: M2PLL	
ADC_CLK_DIV	6:0	R/W	0x04	ADC clk divider 0x00 is DIV1, 0x01 is DIV1, 0x02 is DIV2 and so on. ADC clk target is 3Mhz.	

Register::: Auto_Mode_Ctrl01						0xFF0E
Name	Bits	R/W	Default	Comments	Config	
ADC_INT_flag	7	R/W	0	Interrupt flag Write "1" to clear	Rport Wport	
Reserved	6:3	R/W	0	Reserved		
ADC_Auto_Mode_EN	2	R/W	0	0: Disable 1: Enable auto mode		
ADC_EN_DEBU	1	R/W	1	0: disable de-bounce 1: enable de-bounce. meas 3 times (based on waiting time)		
ADC_INT_EN	0	R/W	0	(L_Threshold < Meas < H_Threshold), Meas_Cnt +1, Meas_Cnt > debounce times, into ISR 0: disable INT 1: enable INT		

Register:::ADC0_THRESHOLD_H						0xFF0F
Name	Bits	R/W	Default	Comments	Config	
ADC0_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode		

Register:::ADC0_THRESHOLD_L						0xFF10
Name	Bits	R/W	Default	Comments	Config	
ADC0_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode		

Register:::ADC1_THRESHOLD_H						0xFF11
Name	Bits	R/W	Default	Comments	Config	
ADC1_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode		

Register:::ADC1_THRESHOLD_L						0xFF12
Name	Bits	R/W	Default	Comments	Config	
ADC1_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode		

Register:::ADC2_THRESHOLD_H						0xFF13
Name	Bits	R/W	Default	Comments	Config	
ADC2_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode		

Register:::ADC2_THRESHOLD_L						0xFF14
Name	Bits	R/W	Default	Comments	Config	
ADC2_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode		

Register::ADC3_THRESHOLD_H 0xFF15					
Name	Bits	R/W	Default	Comments	Config
ADC3_HI_THRESHOLD	7:0	R/W	00	High threshold value for auto mode	

Register::ADC3_THRESHOLD_L 0xFF16					
Name	Bits	R/W	Default	Comments	Config
ADC3_LO_THRESHOLD	7:0	R/W	00	Low threshold value for auto mode	

Register::CTRL0_WAIT_TIME_VALUE 0xFF17					
Name	Bits	R/W	Default	Comments	Config
ADC_Wait_Value	7:0	R/W	0x01	Wait time= wait_value * 1.3ms (0.75Khz), 1.3ms < wait time < 340ms	

DDC

RTD2485XD has three DDC ports. The MCU can access the following three DDC interface:

- DDC_RAM1 (FD80~FDFF) through pin ASDL and ASDA by ADC DDC channel.
- DDC_RAM2 (FE00~FE7F) through pin DSDL and DSDA by DVI DDC channel.
- DDC_RAM3 (FE80~FEFF) through pin HSDL and HSDA by HDMI DDC channel.

Besides, the DDC_RAM1, DDC_RAM2, DDC_RAM3 can be assigned from 128 to 256bytes. The actual sizes of each DDC_RAM are determined by the combination of ADDCRAM_ST, DDDCRAM_ST, and HDDCRAM_ST. The DDC RAMs are shared with MCU's XSRAM, configuration must be take care for reserving XSRAM for programming. For example, Set ADDCRAM_ST = 0x2, DDDCRAM_ST = 0x3, HDDCRAM_ST = 0x2 and disable , DVI DDC. The XSRAM for MCU is 512 bytes and ADC DDC/HDMI DDC is used with 256 bytes.

The DDC of RTD2485XD is compliant with VESA DDC standard. All DDC slaves are in DDC1 mode after reset. When a high to low transition is detected on ASCL/DSCL/HSCL pin, the DDC slave will enter DDC2 transition mode. The DDC slave can revert to DDC1 mode if the SCL signal keeps unchanged for 128 VSYNC periods in DDC2 transition mode and RVT_A_DDC1_EN / RVT_D_DDC1_EN / RVT_H_DDC1_EN = 1. In DDC2 transition mode, the DDC slave will lock in DDC2 mode if a valid control byte is received. Furthermore, user can force the DDC slave to operate DDC2 mode by setting A_DDC2 / D_DDC2/ H_DDC2 = 1.

Register:: ADC_SEGMENT_ADDRESS 0xFF19					
Name	Bits	R/W	Default	Comments	Config
ADC_SEG_ADDR	7:1	R/W	0x30	ADC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: ADC_SEGMENT_DATA 0xFF1A					
Name	Bits	R/W	Default	Comments	Config
ADC_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, ADC_SEGMENT_ADDRESS, in ADC DDC	Rport Wport

Register::ADC_DDC_enable 0xFF1B					
Name	Bits	R/W	Default	Comments	Config
A_DDC_ADDR	7:5	R/W	0	ADC DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is "A")	
A_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce clock (after clock divider) 1: De-bounce reference clock	
A_DDC_W_STA	3	R/W	0	ADC DDC Write Status (for external DDC access only) It is cleared after write. (No matter what the data are)	Rport wport
A_DDCRAM_W_EN	2	R/W	0	ADC DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable	
A_DBN_EN	1	R/W	1	ADC DDC De-bounce Enable 0: Disable 1: Enable (with crystal/4)	
A_DDC_EN	0	R/W	0	ADC DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable	

Register::ADC_DDC_control_1 0xFF1C					
Name	Bits	R/W	Default	Comments	Config

A_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock	
A_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage	
A_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1. Serial flash clock (M2PLL / Flash_DIV)	
A_DDC2	2	R/W	0	Force to ADC DDC to DDC2 mode 0: Normal operation 1: DDC2 is active	
RST_A_DDC	1	R/W	0	Reset ADC DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport wport
RVT_A_DDC1_EN	0	R/W	0	ADC DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::ADC_DDC_control_2					0xFF1D	
Name	Bits	R/W	Default	Comments	Config	
A SEG WR EN	7	R/W	0	Enable interrupt of ADC segment address write 0: Disable 1: Enable		
Reserved	6:5	--	--	Reserved		
ADC_DDCCI_EN	4	R/W	1	ADC DDC-CI Channel Enable Switch 0: Disable 1: Enable		
ADC_DDCISP_EN	3	R/W	1	ADC DDC ISP Channel Enable Switch 0: Disable 1: Enable If all of DDC ISP Channel are disable, ADC DDC ISP Channel will be enable.		
ADC_DDCSEG_EN	2	R/W	1	ADC DDC Segment Channel Enable Switch 0: Disable 1: Enable		
A SEG WR	1	R/W	0	ADC DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write		Wport Rport
A_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL		

Register::DVI_DDC_enable					0xFF1E	
Name	Bits	R/W	Default	Comments	Config	
D_DDC_ADDR	7:5	R/W	0	DVI DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is "A")		
D_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce clock (after clock divider) 1: De-bounce reference clock		

D_DDC_W_STA	3	R/W	0	DVI DDC External Write Status (for external DDC access only) It is cleared after write.	Wport rport
D_DDCRAM_W_EN	2	R/W	0	DVI DDC External Write Enable (for external DDC access only) 0: Disable 1: Enable	
D_DBN_EN	1	R/W	1	DVI DDC Debounce Enable 0: Disable 1: Enable (with crystal/4)	
D_DDC_EN	0	R/W	0	DVI DDC Channel Enable Switch 0: MCU access Enable 1: External DDC access Enable	

Register::DVI_DDC_control_1					0xFF1F
Name	Bits	R/W	Default	Comments	Config
D_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock	
D_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage	
D_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1: Serial flash clock (M2PLL / Flash_DIV)	
D_DDC2	2	R/W	0	Force to DVI DDC to DDC2 mode 0: Normal operation 1: DDC2 is active	
RST_D_DDC	1	R/W	0	Reset DVI DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport wport
RVT_D_DDC1_EN	0	R/W	0	DVI DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::DVI_DDC_control_2					0xFF20
Name	Bits	R/W	Default	Comments	Config
D_SEG_WR_EN	7	R/W	0	Enable interrupt of DVI segment address write 0: Disable 1: Enable	
Reserved	6:5	--	--	Reserved	
DVI_DDCCI_EN	4	R/W	1	DVI DDC-CI Channel Enable Switch 0: Disable 1: Enable	
DVI_DDCISP_EN	3	R/W	1	DVI DDC ISP Channel Enable Switch 0: Disable 1: Enable	
DVI_DDCSEG_EN	2	R/W	1	DVI DDC Segment Channel Enable Switch 0: Disable 1: Enable	

D_SEG_WR	1	R/W	0	DVI DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write	Wport Rport
D_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL	

Register::DDCARAM_partition 0xFF21					
Name	Bits	R/W	Default	Comments	Config
ISP_DDC2B_SWITCH	7	R/W	0	0 : Not Allow DDC2B access in ISP Mode , ddc can program 1 : Allow DDC2B access in ISP Mode , but can not program	
FORCE_DDCRAM_ST	6	R/W	0	Force ADC/DVI/HDMI DDC RAM Start Address to be 0xFD00 1: enable 0: disable (RAM start address decided by bit[5:4], bit[3:2], bit[1:0])	
ADDCRAM_ST	5:4	R/W	0x3	ADDC RAM Start Address is 0xFC00 + ADDCRAM_ST*0x80, ADDCRAM SIZE = DDDCRAM_ST – ADDCRAM_ST	
DDDCRAM_ST	3:2	R/W	0x3	DDDC RAM Start Address is 0xFC80 + DDDCRAM_ST*0x80, DDDCRAM SIZE = HDDCRAM_ST – DDDCRAM_ST	
HDDCRAM_ST	1:0	R/W	0x3	HDDC RAM Start Address is 0xFD00 + ADDCRAM_ST*0x80, HDDCRAM SIZE = 0xFF00 – HDDCRAM_ST	

XRAM Arbitor	Byte	Start	End	
External RAM	1152	0xF900	0xFD7F	xData
DDC0_RAM	128	0xFD80	0xFFFF	VGA
DDC1_RAM	128	0xFE00	0xFE7F	DVI_1
DDC2_RAM	128	0xFE80	0xFEFF	DVI_2
External RAM	896	0xF900	0xFC7F	xData
DDC0_RAM	128	0xFC80	0xFCFF	VGA
DDC1_RAM	256	0xFD00	0xFFFF	HDMI_1
DDC2_RAM	256	0xFE00	0xFEFF	HDMI_2

Register::VSYNC_Sel 0xFF22					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:4	-			
VS_CON0	3:2	R/W	0	00: VSYNC0 signal is connected to ADC DDC 01: VSYNC0 signal is connected to DVI DDC 1x: VSYNC0 signal is connected to HDMI DDC	
VS_CON1	1:0	R/W	0	00: VSYNC1 signal is connected to ADC DDC 01: VSYNC1 signal is connected to DVI DDC 1x: VSYNC1 signal is connected to HDMI DDC	

DDC-CI

Register:::IIC_set_slave					0xFF23
Name	Bits	R/W	Default	Comments	Config
IIC_ADDR	7:1	R/W	37	IIC Slave Address to decode	
CH_SEL	0	R/W	0	Channel Select, overridden by HCH_SEL(0xFF2B[0]) = 1 0: from ADC DDC 1: from DVI DDC (In auto switch mode, this bit will be set by hardware, and thus read only)	Rport Wport

pin121 / pin122 → DDCSCL3 / DDCSDA3, (HDMI DDC) → **0xFF2B** Bit 0 Enable
 pin123/ pin124 → DDCSCL2 / DDCSDA2, (DVI DDC), → **0xFF23** Bit 0 Enable

Register:::IIC_sub_in					0xFF24
Name	Bits	R/W	Default	Comments	Config
IIC_SUB_ADDR	7:0	R	00	IIC Sub-Address Received	

Register:::IIC_data_in					0xFF25
Name	Bits	R/W	Default	Comments	Config
IIC_D_IN	7:0	R	00	IIC data received. 16-bytes depth read in buffer mode	RPORT

Register:::IIC_data_out					0xFF26
Name	Bits	R/W	Default	Comments	Config
IIC_D_OUT	7:0	W	00	IIC data to be transmitted	Rport Wport

Register:::IIC_status					0xFF27
Name	Bits	R/W	Default	Comments	Config
A_WR_I	7	R/W	0	If ADC DDC detects a STOP condition in write mode, this bit is set to "1". Write 0 to clear.	Rport Wport
D_WR_I	6	R/W	0	If DVI DDC detects a STOP condition in write mode, this bit is set to "1". Write 0 to clear.	Rport Wport
DDC_128VS0_I	5	R/W	0	In DDC2 Transition mode, SCL idle for 128 VSYNC. Write 0 to clear.	Rport Wport
STOP_I	4	R/W	0	If IIC detects a STOP condition(slave address must match), this bit is set to "1". Write 0 to clear.	Rport Wport
D_OUT_I	3	R	0	If IIC_DATA_OUT loaded to serial-out-byte, this bit is set to "1". Write IIC_data_out (FF26) to clear.	
D_IN_I	2	R	0	If IIC_DATA_IN latched, this bit is set to "1". Read IIC_data_in (FF25) to clear.	
SUB_I	1	R/W	0	If IIC_SUB latched, this bit is set to "1" Write 0 to clear.	Rport Wport
SLV_I	0	R/W	0	If IIC_SLAVE latched, this bit is set to "1" Write 0 to clear.	Rport Wport

Register::IIC_IRQ_control					0xFF28
Name	Bits	R/W	Default	Comments	Config
AWI_EN	7	R/W	0	0: Disable the A_WR_I signal as an interrupt source 1: Enable the A_WR_I signal as an interrupt source	
DWI_EN	6	R/W	0	0: Disable the D_WR_I signal as an interrupt source 1: Enable the D_WR_I signal as an interrupt source	
DDC_128VSI0_EN	5	R/W	0	0: Disable the 128VSO_I signal as an interrupt source 1: Enable the 128VSO_I signal as an interrupt source	
STOPI_EN	4	R/W	0	0: Disable the STOP_I signal as an interrupt source 1: Enable the STOP_I signal as an interrupt source	
DOI_EN	3	R/W	0	0: Disable the D_OUT_I signal as an interrupt source 1: Enable the D_OUT_I signal as an interrupt source	
DII_EN	2	R/W	0	0: Disable the D_IN_I signal as an interrupt source 1: Enable the D_IN_I signal as an interrupt source	
SUBI_EN	1	R/W	0	0: Disable the SUB_I signal as an interrupt source 1: Enable the SUB_I signal as an interrupt source	
SLVI_EN	0	R/W	0	0: Disable the SLV_I signal as an interrupt source 1: Enable the SLV_I signal as an interrupt source	

Register::IIC_status2					0xFF29
Name	Bits	R/W	Default	Comments	Config
IIC_FORCE_SCL_L	7	R/W	0	Force SCL = 0 when one of the following tow case happen: 1. IIC_BUF_FULL = 1 in write mode 2. IIC_BUF_EMPTY = 1 in read mode	
FORCE_NACK	6	R/W	0	Force IIC return NACK when one of the following tow case happen: IIC_BUF_FULL = 1 in write mode	
IIC_BUF_OV	5	R/W	0	IIC_DATA_BUFFER Overflow. Write '0' to clear	Rport Wport
IIC_BUF_UN	4	R/W	0	IIC_DATA_BUFFER Underflow. Write '0' to clear	Rport Wport
DDC_128VS1_I Not Used	3	R/W	0	In DDC2 Transition mode, SCL idle for 128 VSYNC. Write 0 to clear. Write '0' to clear Not Used	Rport Wport
IIC_BUF_FULL	2	R	0	IIC_DATA_BUFFER Full If IIC_DATA buffer is full, this bit is set to "1". (On-line monitor) The IIC_DATA buffer Full status will be on-line-monitor the condition, once it becomes full, it kept high, if it is not-full, then it goes low.	
IIC_BUF_EMPTY	1	R	0	IIC_DATA_BUFFER Empty If IIC_DATA buffer is empty, this bit is set to "1". (On-line monitor) The IIC_DATA buffer Empty status will be on-line-monitor the condition, once it becomes empty, it kept high, if it is not-empty, then it goes low.	
H_WR_I	0	R/W	0	If HDMI DDC detects a STOP condition in write mode, this bit is set to "1". Write 0 to clear.	Rport Wport

Register::IIC_IRQ_control2					0xFF2A
Name	Bits	R/W	Default	Comments	Config
AUTO_RST_BUF	7	R/W	0	Auto reset IIC_DATA Buffer	

				0: disable 1: enable In host (pc) write enable, when IIC write (No START after IIC_SUB), reset IIC_DATA buffer.	
RST_DATA_BUF	6	R/W	0	Reset IIC_DATA buffer 0: Finish 1: Reset	Wport Rport
DATA_BUF_WEN	5	R/W	0	IIC_DATA buffer write enable 0: host (pc) write enable 1: slave (mcu) write enable Both PC and MCU can read IIC_DATA buffer, but only one can write IIC_DATA buffer.	
DDC_CH_Auto_Switch_En	4	R/W	0	DDCCI Channel Auto Switch Enable 0: Manual Mode Switch 1: Auto Switch (In Auto Mode, DDC will auto switch to the only one active channel when the other two channel are non active) (Auto Reset Buffer when channel switch at auto mode)	
DDC_128VSI1_EN Not Used	3	R/W	0	0: Disable the 128VS1_I signal as an interrupt source 1: Enable the 128VS_I signal as an interrupt source Not Used	
DDC_BUF_FULL_EN	2	R/W	0	0: Disable the DDC_DATA_BUFFER Full signal as an interrupt source 1: Enable the DDC_DATA_BUFFER Full signal as an interrupt source	
DDC_BUF_EMPTY_EN	1	R/W	0	0: Disable the DDC_DATA_BUFFER Empty signal as an interrupt source 1: Enable the DDC_DATA_BUFFER Empty signal as an interrupt source	
HWI_EN	0	R/W	0	0: Disable the H_WR_I signal as an interrupt source 1: Enable the H_WR_I signal as an interrupt source	

Register::IIC_channel_control					0xFF2B
Name	Bits	R/W	Default	Comments	Config
CH_Switch_Auto_Rst_en	7	R/W	0	In Auto Switch Mode, Auto Reset Buffer when channel switch happen 0: Disable 1: Enable	
Force_Null_Msg_out	6	R/W	0	Force DDCCI output Null Message(even when ddcci buffer not empty) 0: stop output null message 1: start output null message	
Null_Msg_En	5	R/W	0	Null Message Enable 0: disable 1: enable	
Null_Msg_Rst_Buf_en	4	R/W	0	0:Disable Auto Reset Buffer When Null Message 1:Enable Auto Reset Buffer When Null Message	
IIC_BUF_OV_EN	3	R/W	0	0: Disable the IIC_DATA_BUFFER overflow signal as an interrupt source 1: Enable the IIC_DATA_BUFFER overflow signal as an interrupt source	
IIC_BUF_UN_EN	2	R/W	0	0: Disable the IIC_DATA_BUFFER underflow signal as an interrupt source 1: Enable the IIC_DATA_BUFFER underflow signal as an interrupt source	
RLS_SCL_SU	1	R/W	0	Set IIC data Setup Time When holding SCL low 0: Use Delay Chain (~5ns) 1: Use Crystal Clock to increase data setup time relative to SCL clock line	
HCH_SEL	0	R/W	0	Channel Select of DDC-CI 1: from HDMI DDC 0: controlled by CH_SEL	Wport Rport

			(In auto switch mode, this bit will be set by hardware, and thus read only)	
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pin121 / pin122 → DDCSCL3 / DDCSDA3, (HDMI DDC) → **0xFF2B** Bit 0 Enable
 pin123/ pin124 → DDCSCL2 / DDCSDA2, (DVI DDC), → **0xFF23** Bit 0 Enable

Register::HDMI_DDC_enable 0xFF2C					
Name	Bits	R/W	Default	Comments	Config
H_DDC_ADDR	7:5	R/W	0	HDMI DDC Channel Address Least Significant 3 Bits (The default DDC channel address MSB 4 Bits is “A”)	
H_SCL_DBN_SEL	4	R/W	0	SCL Debounce Clock Selection 0: De-bounce reference clock 1: De-bounce clock (after clock divider)	
H_DDC_W_STA	3	R/W	0	HDMI DDC Write Status (for external DDC access only) It is cleared after write.	Rport Wport
H_DDCCRAM_W_EN	2	R/W	0	HDMI DDC SRAM Write Enable (for external DDC access only) 0: Disable 1: Enable	
H_DBN_EN	1	R/W	1	HDMI DDC De-bounce Enable 0: Disable 1: Enable (with crystal/4)	
H_DDC_EN	0	R/W	0	HDMI DDC Channel Enable Bit 0: MCU access Enable 1: DDC channel Enable	

Register::HDMI_DDC_control_1 0xFF2D					
Name	Bits	R/W	Default	Comments	Config
H_DBN_CLK_SEL	7:6	R/W	0	De-bounce clock divider 00: 1/1 reference clock 01: 1/2 reference clock 1X: 1/4 reference clock	
H_STOP_DBN_SEL	5:4	R/W	3	De-bounce sda stage 00: no latch stage 01: latch one stage 10: latch two stage 11: latch three stage	
H_SYS_CK_SEL	3	R/W	0	De-bounce reference clock 0: crystal clock 1: Serial flash clock (M2PLL / Flash_DIV)	
H_DDC2	2	R/W	0	Force to HDMI DDC to DDC2 mode 0: Normal operation 1: DDC2 is active	
RST_H_DDC	1	R/W	0	Reset HDMI DDC circuit 0: Normal operation 1: reset (auto cleared)	Rport Wport
RVT_H_DDC1_EN	0	R/W	0	HDMI DDC revert to DDC1 enable(SCL idle for 128 VSYNC) 0: Disable 1: Enable	

Register::HDMI_DDC_control_2					0xFF2E
Name	Bits	R/W	Default	Comments	Config
H_SEG_WR_EN	7	R/W	0	Enable interrupt of HDMI segment address write 0: Disable 1: Enable	
Dummy_3	6:5	R/W	0		
HDMI_DDCCI_EN	4	R/W	1	HDMI DDC-CI Channel Enable Switch 0: Disable 1: Enable	
HDMI_DDCISP_EN	3	R/W	1	HDMI DDC ISP Channel Enable Switch 0: Disable 1: Enable	
HDMI_DDCSEG_EN	2	R/W	1	HDMI DDC Segment Channel Enable Switch 0: Disable 1: Enable	
H_SEG_WR	1	R/W	0	HDMI DDC Segment Write Status 0: no external write after clear 1: new external write after clear It is cleared after write	Wport Rport
H_FORCE_SCL_L	0	R/W	0	Force external SCL bus low 1: Driving SCL = 0 after external SCL = 0 0: Release SCL	

The access ports below are used for external host interface only.

Register::ADC_DDC_INDEX					0XFF2F
Name	Bits	R/W	Default	Comments	Config
A_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::ADC_DDC_ACCESS_PORT					0XFF30
Name	Bits	R/W	Default	Comments	Config
A_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register::DVI_DDC_INDEX					0XFF31
Name	Bits	R/W	Default	Comments	Config
D_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::DVI_DDC_ACCESS_PORT					0XFF32
Name	Bits	R/W	Default	Comments	Config
D_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register::HDMI_DDC_INDEX					0XFF33
Name	Bits	R/W	Default	Comments	Config
H_DDC_INDEX	7:0	R/W	0	DDC SRAM Read/Write Index Register [7:0]	Rport Wport

Register::HDMI_DDC_ACCESS_PORT					0XFF34
Name	Bits	R/W	Default	Comments	Config
H_DDC_ACCESS_PORT	7:0	R/W	0	DDC SRAM Read/Write Port	Rport Wport

Register:: DDCCI_REMAIN_DATA					0xFF35
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	Reserved	
DDCCI_REMAIN_LEN	5:0	R	0	DDCCI Remaining data length (= write_pointer – read_pointer)	

Register:: DVI_SEGMENT_ADDRESS					0xFF36
Name	Bits	R/W	Default	Comments	Config
DVI_SEG_ADDR	7:1	R/W	0x30	DVI DDC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: DVI_SEGMENT_DATA					0xFF37
Name	Bits	R/W	Default	Comments	Config
DVI_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, DVI_SEGMENT_ADDRESS, in DVI DDC	Rport Wport

Register:: HDMI_SEGMENT_ADDRESS					0xFF38
Name	Bits	R/W	Default	Comments	Config
HDMI_SEG_ADDR	7:1	R/W	0x30	HDMI DDC slave address for segment control	
Reserved	0	--	--	Reserved	

Register:: HDMI_SEGMENT_DATA					0xFF39
Name	Bits	R/W	Default	Comments	Config
HDMI_SEG_DATA	7:0	R/W	0x00	Data Access for Slave ID, HDMI_SEGMENT_ADDRESS, in HDMI DDC	Rport Wport

Register:: DDCCI_Null_Byte1					0xFFB1
Name	Bits	R/W	Default	Comments	Config
DDCCI_Null_Byte1	7:0	R/W	0x6E	When DDC is not selected as active DDCCI channel, or buffer empty, DDC will feedback null bytes.	

Register:: DDCCI_Null_Byte2					0xFFB2
Name	Bits	R/W	Default	Comments	Config
DDCCI_Null_Byte2	7:0	R/W	0x80	When DDC is not selected as active DDCCI channel, or buffer empty, DDC will feedback null bytes.	

Register:: DDCCI_Null_Byte3					0xFFB3
Name	Bits	R/W	Default	Comments	Config
DDCCI_Null_Byte3	7:0	R/W	0xBE	When DDC is not selected as active DDCCI channel, or buffer empty, DDC will feedback null bytes.	

PWM

RTD2485XD supports 6 channels of PWM DAC. The resolution of each PWM is 12-bit. PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5 are connected to DA0, DA1, DA2, DA3, DA4 and DA5 respectively. The figure below represents the PWM clock generator. Based on the clock, we make up the PWM waveform which frequency is 1/4096 of the PWM clock.

The PWM duty registers have 12-bit resolution. These registers have double buffer mechanism. When write the MSB bit, the 12-bit data will be loaded.

The PWM frequency is :

$$F_{PWM} = f_{clk} / 2^M / (N+1) / DUT$$

Where each variables are controlled by:

M: PWMx_M

N: PWMxH_N * 256 + PWMxL_N

DUT: (PWMx_DUT_8B == 1)? 256 : 4096

The 12bit duty PWM frequency range is :

fclk=14.3M, fpwm = 3.5KHz ~ 0.1Hz

fclk=27M, fpwm = 6.6KHz ~ 0.2Hz

fclk=243M, fpwm = 60KHz ~ 1.8Hz

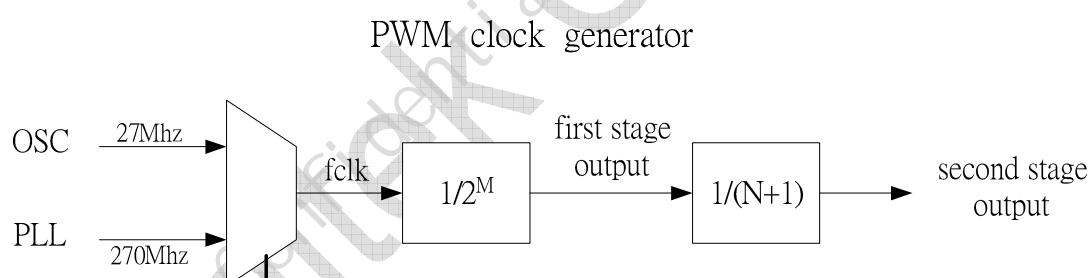
The 8bit duty PWM frequency range is :

fclk=14.3M, fpwm = 56KHz ~ 1.6Hz

fclk=27M, fpwm = 105.6KHz ~ 3.2Hz

fclk=243M, fpwm = 960KHz ~ 28.8Hz

fclk=270M, fpwm = 1056KHz ~ 32Hz



Register:::PWM_CK_SEL					0xFF3A
Name	Bits	R/W	Default	Comments	Config
PWM_CK_SEL_DUMMY	7:6	R/W	0	dummy	
PWM5_CK_SEL	5	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	
PWM4_CK_SEL	4	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	

PWM3_CK_SEL	3	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	
PWM2_CK_SEL	2	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	
PWM1_CK_SEL	1	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	
PWM0_CK_SEL	0	R/W	0	PWMx clock generator input source 0: Crystal 1: PLL output (When PWM5_CK_SEL_HS = 0)	

Register:::PWM03_M 0xFF3B					
Name	Bits	R/W	Default	Comments	Config
PWM3_M	7:6	R/W	0	PWMx clock first stage divider	
PWM2_M	5:4	R/W	0	PWMx clock first stage divider	
PWM1_M	3:2	R/W	0	PWMx clock first stage divider	
PWM0_M	1:0	R/W	0	PWMx clock first stage divider	

Register:::PWM45_M 0xFF3C					
Name	Bits	R/W	Default	Comments	Config
PWM_M_DUMMY	7	R/W	0	dummy	
PWM_REF_SEL	6:4	R/W	0	PWM Reference Source Select 0: PWM0 1: PWM1 2: PWM2 3: PWM3 4: PWM4 5: PWM5 6/7: No use	
PWM5_M	3:2	R/W	0	PWMx clock first stage divider	
PWM4_M	1:0	R/W	0	PWMx clock first stage divider	

Register:::PWM01_N_MSB 0xFF3D					
Name	Bits	R/W	Default	Comments	Config
PWM1H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM0H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register:::PWM0_N_LSB 0xFF3E					
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Name	Bits	R/W	Default	Comments	Config
PWM0L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM1_N_LSB 0xFF3F					
Name	Bits	R/W	Default	Comments	Config
PWM1L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM23_N_MSB 0xFF40					
Name	Bits	R/W	Default	Comments	Config
PWM3H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM2H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register::PWM2_N_LSB 0xFF41					
Name	Bits	R/W	Default	Comments	Config
PWM2L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM3_N_LSB 0xFF42					
Name	Bits	R/W	Default	Comments	Config
PWM3L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM45_N_MSB 0xFF43					
Name	Bits	R/W	Default	Comments	Config
PWM4H_N	7:4	R/W	0	PWMx clock Second stage divider MSB[11:8]	
PWM5H_N	3:0	R/W	0	PWMx clock Second stage divider MSB[11:8]	

Register::PWM4_N_LSB 0xFF44					
Name	Bits	R/W	Default	Comments	Config
PWM4L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWM5_N_LSB 0xFF45					
Name	Bits	R/W	Default	Comments	Config
PWM5L_N	7:0	R/W	0	PWMx clock Second stage divider LSB[7:0]	

Register::PWML 0xFF46					
Name	Bits	R/W	Default	Comments	Config
PWM_W_DB_WR	7	R/W	0	Write 1 to Set PWM_Width if PWM_W_DB_EN = 1'b1. Auto-Clear after PWM_Width was loaded	Rport Wport
PWM_W_DB_MODE	6	R/W	0	PWM Width Setting Double-Buffer Mode 0: Setting active after PWM_W_DB_WR = 1 1: Setting active after PWM_W_DB_WR = 1 & DVS.	
PWM5L	5	R/W	0	0: enable Active H 1: enable Active L	
PWM4L	4	R/W	0	0: enable Active H 1: enable Active L	

PWM3L	3	R/W	0	0: enable Active H 1: enable Active L	
PWM2L	2	R/W	0	0: enable Active H 1: enable Active L	
PWM1L	1	R/W	0	0: enable Active H 1: enable Active L	
PWM0L	0	R/W	0	0: enable Active H 1: enable Active L	

Register:::PWM_VS_CTRL 0xFF47					
Name	Bits	R/W	Default	Comments	Config
PWM_VS_CTRL_DUM	7:6	R/W	0	dummy	
PWM5_VS_RST_EN	5	R/W	0	0: Disable 1: Enable PWM5 reset by DVS	
PWM4_VS_RST_EN	4	R/W	0	0: Disable 1: Enable PWM4 reset by DVS	
PWM3_VS_RST_EN	3	R/W	0	0: Disable 1: Enable PWM3 reset by DVS	
PWM2_VS_RST_EN	2	R/W	0	0: Disable 1: Enable PWM2 reset by DVS	
PWM1_VS_RST_EN	1	R/W	0	0: Disable 1: Enable PWM1 reset by DVS	
PWM0_VS_RST_EN	0	R/W	0	0: Disable 1: Enable PWM0 reset by DVS	

Register:::PWM_EN 0xFF48					
Name	Bits	R/W	Default	Comments	Config
PWM_W_DB_EN	7	R/W	0	0: PWM Width set when write MSB 1: PWM Width setting double-buffered enable	
PWM_WIDTH_SEL	6	R/W	0	0: PWMxL_DUT is active 1: PWMxL_DUT is inactive, forced to 4'h0 internally	
PWM5_EN	5	R/W	0	0: PWM output disable 1: PWM output enable	
PWM4_EN	4	R/W	0	0: PWM output disable 1: PWM output enable	
PWM3_EN	3	R/W	0	0: PWM output disable 1: PWM output enable	
PWM2_EN	2	R/W	0	0: PWM output disable 1: PWM output enable	
PWM1_EN	1	R/W	0	0: PWM output disable 1: PWM output enable	
PWM0_EN	0	R/W	0	0: PWM output disable 1: PWM output enable	

Register:::PWM_CK 0xFF49					
Name	Bits	R/W	Default	Comments	Config
PWM5_REF_CTRL_EN	7	R/W	0	0: PWM5 normal ouput 1: PWM reference gated by PWM5 output	
PWM4_REF_CTRL_EN	6	R/W	0	0: PWM4 normal ouput 1: PWM reference gated by PWM4 output	
PWM5_CK	5	R/W	0	0: Select first stage	

				output 1: Select second stage output	
PWM4_CK	4	R/W	0	0: Select first stage output 1: Select second stage output	
PWM3_CK	3	R/W	0	0: Select first stage output 1: Select second stage output	
PWM2_CK	2	R/W	0	0: Select first stage output 1: Select second stage output	
PWM1_CK	1	R/W	0	0: Select first stage output 1: Select second stage output	
PWM0_CK	0	R/W	0	0: Select first stage output 1: Select second stage output	

Register:::PWM0H_DUT					0xFF4A
Name	Bits	R/W	Default	Comments	Config
PWM0H_DUT	7:0	R/W	0	PWM0[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:::PWM1H_DUT					0xFF4B
Name	Bits	R/W	Default	Comments	Config
PWM1H_DUT	7:0	R/W	0	PWM1[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:::PWM01L_DUT					0xFF4C
Name	Bits	R/W	Default	Comments	Config
PWM1L_DUT	7:4	R/W	0	PWM1[3:0] duty width	Rport Wport
PWM0L_DUT	3:0	R/W	0	PWM0[3:0] duty width	Rport Wport

Register:::PWM2H_DUT					0xFF4D
Name	Bits	R/W	Default	Comments	Config
PWM2H_DUT	7:0	R/W	0	PWM2[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:::PWM3H_DUT					0xFF4E
Name	Bits	R/W	Default	Comments	Config
PWM3H_DUT	7:0	R/W	0	PWM3[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data	Rport Wport

			will be loaded.	
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Register:::PWM23L_DUT					0xFF4F
Name	Bits	R/W	Default	Comments	Config
PWM3L_DUT	7:4	R/W	0	PWM3[3:0] duty width	Rport Wport
PWM2L_DUT	3:0	R/W	0	PWM2[3:0] duty width	Rport Wport

Register:::PWM4H_DUT					0xFF50
Name	Bits	R/W	Default	Comments	Config
PWM4H_DUT	7:0	R/W	0	PWM4[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:::PWM5H_DUT					0xFF51
Name	Bits	R/W	Default	Comments	Config
PWM5H_DUT	7:0	R/W	0	PWM5[11:4] duty width When write the MSB bit (PWM_W_DB_EN=0) , the 12-bit data will be loaded.	Rport Wport

Register:::PWM45L_DUT					0xFF52
Name	Bits	R/W	Default	Comments	Config
PWM5L_DUT	7:4	R/W	0	PWM5[3:0] duty width	Rport Wport
PWM4L_DUT	3:0	R/W	0	PWM4[3:0] duty width	Rport Wport

Register::: PWM_DUT_TYPE					0xFF53
Name	Bits	R/W	Default	Comments	Config
PWM3_REF_CTRL_EN	7	R/W	0	0: PWM3 normal output 1: PWM reference gated by PWM3 output	
PWM2_REF_CTRL_EN	6	R/W	0	0: PWM2 normal output 1: PWM reference gated by PWM2 output	
PWM5_DUT_8B	5	R/W	0	PWM5 duty width type When PWM5_DUT_8B =1, only PWM5H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM4_DUT_8B	4	R/W	0	PWM4 duty width type When PWM4_DUT_8B =1, only PWM4H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM3_DUT_8B	3	R/W	0	PWM3 duty width type When PWM3_DUT_8B =1, only PWM3H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM2_DUT_8B	2	R/W	0	PWM2 duty width type When PWM2_DUT_8B =1, only PWM2H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
PWM1_DUT_8B	1	R/W	0	PWM1 duty width type When PWM1_DUT_8B =1, only PWM1H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	

PWM0_DUT_8B	0	R/W	0	PWM0 duty width type When PWM0_DUT_8B =1, only PWM0H_DUT is used as 8bit-resolution duty, and increase the PWM frequency x 16	
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Register::PWM_CNT_MODE					0xFF54
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	Reserved	
PWM5_CNT_MODE	5	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM4_CNT_MODE	4	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM3_CNT_MODE	3	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM2_CNT_MODE	2	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM1_CNT_MODE	1	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	
PWM0_CNT_MODE	0	R/W	0	0: duty mode 1: high/total counter mode. The total level count is {PWMxH_TOTALCNT, PWMxL_TOTALCNT}, high level count is {PWMxH_DUT, PWMxL_DUT}, and limited H/L transition number by PWMx_CYCLE_MAX	

I2C Control Module

RTD2485XD provides one I2C master interface only.

Master

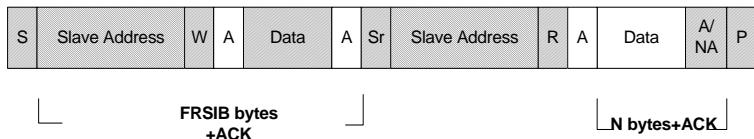
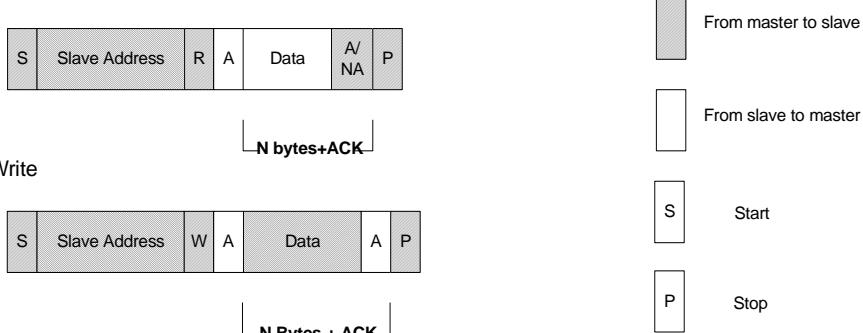
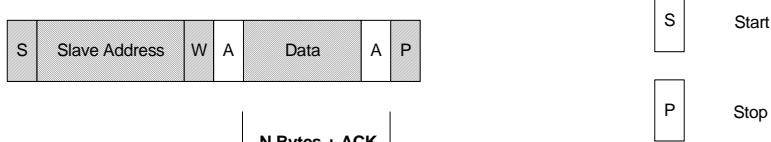
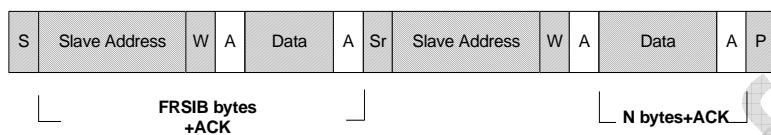
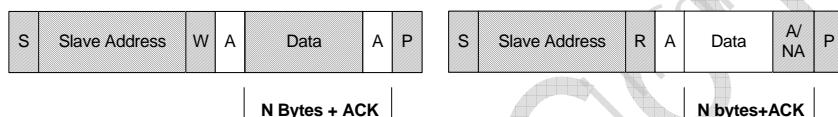
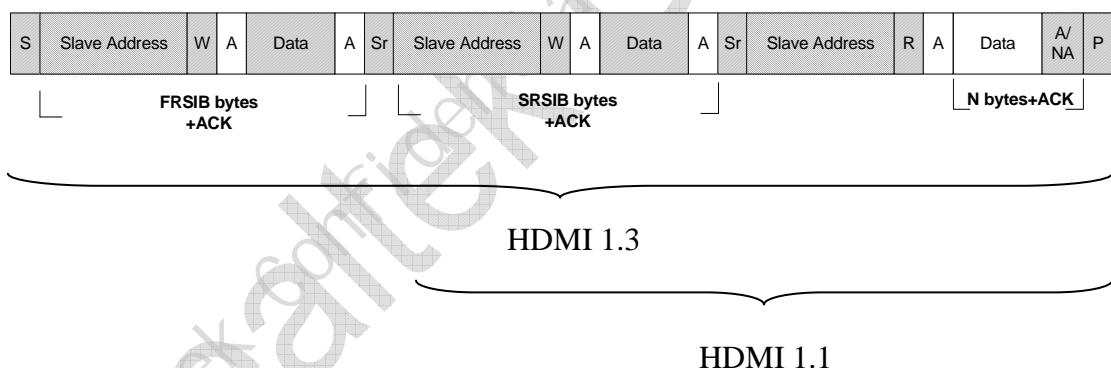
In the Random read operation, the slave address and data are clocked in and acknowledged by the slave. The master will generate another start condition. In Current address read operation, the internal data word address counter maintains the data word address accessed during the last read or write operation,

incremented by one. The data word address stays valid between operations as long as the power is maintained. A Write operation requires data words following the slave address word and acknowledgment. The master terminates the write sequence with a stop condition. In Write with restart operation, master will generate another start condition after transmitting the slave address and data. If slave needs stop condition between data and restart command (Sr) in the Random read operation, software can transmit the Current address read operation following A Write operation. The maximum value of data FIFO (N) is 24. The slave address byte will be written into FIFO register together with data. Software must write the eighth bit of slave address byte to decide the access is read or write.

NOTE:

- (a) RTD2485XD supports master and function
- (b) RTD2485XD doesn't support arbitration mechanism while one system exists over 2 masters
- (c) FIFO can't support R/W at the same time. It means that you can't transmit data successively while the byte counts over 24, since MCU have to refresh the FIFO data for the next transmit
- (d) Master supports the function that slave can hold SCL to zero after ACK when slave can't give master data that master wanted.

Signal Name	Type	Function	Note
SCL	O		
SDA	I/O		

Random Read

Current Address Read

Write

Write with restart

Write + Current Address Read

Read with two restart


So we can identify whether HDMI 1.1 or 1.3 by receiving the first 2 ACK from slaves

Register:: I2CM_CR0					0xFF55
Name	Bits	R/W	Default	Comments	Config
I2CM_SW_RSTN	7	R/W	0	IIC master software reset 0: Reset, Blocking I2CM module 1: Enable I2CM module	

CS	6	R/W	0	Command Start 0 = Stop, after completing whole transaction, it returns to zero 1 = Start	wport rport
RWL	5:1	R/W	0	Read/Write data Length for related commands. Not includes slave address byte in FIFO register. When access, controller will parse the byte followed last start (or Sr) byte to know the command type. 0x00 = 1 bytes 0x17 = 24 bytes	
TORE	0	R/W	1	TOR enable If TOR is desired, I2C rate must be constrained form 25kb/s~400kb/s. This constraint is due to the time-out register bit.	

Register:: I2CM_CR1					0xFF56
Name	Bits	R/W	Default	Comments	Config
TOR	7:0	R/W	0x3A	Time-out register Time-out = TOR x 2 x ((FD10+1)/input clock) (For receive/transmit one bit) If time-out occur, it will trigger Transaction Error Interrupt Flag Note: time-out must > (1 SCL low period + repeat start setup time)	

Register:: I2CM_CR2					0xFF57
Name	Bits	R/W	Default	Comments	Config
reserved	7	-	0	Reserved to 0	
BURST	6	R/W	0	Burst mode enabled to write over 24 bytes to slave devices. While burst is enabled, whole I2C will be halted to let MCU write another more bytes to FIFO. After the job done, we have to set I2CM_SR to be high to continue the I2C write job	
SBAIFD	5	R/W	0	Second byte ACK in FRSIB data (for identifying HDMI 1.3 needed) SBAIFD indicates that whether master checks ACK from slave or not after emitting second data in FRSIB data. 0: To check 1: Not check	
FBAIFD	4	R/W	0	First byte ACK in FRSIB data (for identifying HDMI 1.3 needed) FBAIFD indicates that whether master checks ACK from slave or not after emitting first data in FRSIB data. 0: To check 1: Not check	
SRSIB	3:2	R/W	0	Second repeat start interval byte (For HDMI need) After transmitting SRSIB bytes that, include slave address & data bytes, follow the first repeat start command, the master will produce second repeat start command. The slave address or device address byte is included in this interval. Default interval is one byte. 0 = 1 bytes; 1=2 byte etc. Note: The eighth bit of slave address or device address byte followed by second repeat start command must be Read.	
FRSIB	1:0	R/W	0	First repeat start interval byte (For HDMI need) After transmitting FRSIB bytes that, include slave address & data bytes, follow the original start command, the master will produce first repeat start command. The original slave address or device address byte is included in this interval. Default interval is one byte. 0 = 1 bytes; 1=2 bytes, etc.	

Register:: I2CM_CR3					0xFF58
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	-	0	Reserved to 0	
RSC	4:3	R/W	0	Repeat start count 00: No repeat start 01: one repeat start 10: two repeat start 11: forbidden	
TEIE	2	R/W	0	Transaction Error Interrupt Enable	
MRCIE	1	R/W	0	Master Receive complete Interrupt Enable	
MTCIE	0	R/W	0	This Interrupt enable bit serve two conditions, one is “Master Transmit complete Interrupt Enable in single mode” and the other is “Master Transmit partial Done Interrupt Enable in burst mode”	

Register:: I2CM_STR0					0xFF59
Name	Bits	R/W	Default	Comments	Config
reserved	7	-	0	Reserved to 0	
I2CMD	6:4	R/W	0	I2C master debounce 0: sample rate=(input clk / (FD10+1)) 1: sample rate=(input clk / (FD10+1)) / 2 : 7: sample rate= (input clk / (FD10+1)) / 8	
FTPC	3:0	R/W	0x3	Fall time period count If the value of (Bus clock/FD10) does not approximate 10Mhz, FTPC can make sure that fall time of SCL is more than 300ns.	

Register:: I2CM_STR1					0xFF5A
Name	Bits	R/W	Default	Comments	Config
STA_SUGPIO_C	7:0	R/W	0x09	STA setup time period count In repeat start, the setup time of SCL must match the I2C spec.	

Register:: I2CM_STR2					0xFF5B
Name	Bits	R/W	Default	Comments	Config
SHPC	7:0	R/W	0x09	SCL high period counter (SCL High period=100ns*SHPC) SHPC must include rising time in the I2C spec.	

Register:: I2CM_STR3					0xFF5C
Name	Bits	R/W	Default	Comments	Config
SLPC	7:0	R/W	0x10	SCL low period counter (SCL low period=100ns*SLPC) SLPC must include falling time in the I2C spec.	

Register:: I2CM_SR					0xFF5D
Name	Bits	R/W	Default	Comments	Config
reserved	7:5	-	0	Reserved to 0	
BSA	4	R/W	0	Send again Control bit in burst mode 1: Send 0: Not action Write “1” to clear	wport rport
BMPIF	3	R/W	0	Burst Mode Pending Interrupt Flag While setting as burst mode and I2C master transmit data in TDD, this flag is asserted.	wport rport

				Write “1” to clear	
TEIF	2	R/W	0	Transaction Error Interrupt Flag When master transmit/receive fault or time-out occurrence, I2C controller will lift the flag up and return to bus idle. Write “1” to clear	wport rport
MRCIF	1	R/W	0	Master Receive complete Interrupt flag Write “1” to clear	wport rport
MTCIF	0	R/W	0	This Interrupt enable bit serves two conditions, one is “Master Transmit complete Interrupt Enable in single mode” and the other is “Master Transmit partial Done Interrupt Enable in burst mode” Write “1” to clear	wport rport

Register:: I2CM_TD					0xFF5E
Name	Bits	R/W	Default	Comments	Config
TDD	7:0	R/W	0	Target Device Data to receive or transmit	wport rport

Register:: I2CM_CCR					0xFF5F
Name	Bits	R/W	Default	Comments	Config
reserved	7:6	-	0	Reserved to 0	
FD10	5:0	R/W	0x01	Frequency 10M Divisor 0 are forbidden 10M=input clock/(FD10+1) When power on, software must write FD10 to let I2C controller generate ~10 Mhz clock.	

MCU Register2(Page E) SPI-FLASH
Common Instruction Register

Register::common_inst_en					0xFF60	
Name	Bits	R/W	Default	Comments	Config	
com_inst	7:5	R/W	0x0	000: no operation 001 : write 010 : Read 011 : write after WREN 100 : write after EWSR 101 : Erase		
write_num	4:3	R/W	0x0	Common instruction write number		
rd_num	2:1	R/W	0x0	Common instruction read number		
com_inst_en	0	R/W	0x0	Common instruction enable (auto clear when finish)		Wport Rport

Register::common_op_code					0xFF61	
Name	Bits	R/W	Default	Comments	Config	
com_op	7:0	R/W	0x0	Common instruction op code		

Register::wren_op_code					0xFF62	
Name	Bits	R/W	Default	Comments	Config	
wren_op	7:0	R/W	0x06	Write enable op code		

Register::ewsr_op_code					0xFF63	
Name	Bits	R/W	Default	Comments	Config	
ewsr_op	7:0	R/W	0x50	Enable write register op code		

Register::Flash_prog_ISP0					0xFF64	
Name	Bits	R/W	Default	Comments	Config	
prog_h	7:0	R/W	0x00	Flash program/write/dummy/read CRC high byte[23:16]		Wport Rport

Register::Flash_prog_ISP1					0xFF65	
Name	Bits	R/W	Default	Comments	Config	
prog_m	7:0	R/W	0x00	Flash program/write/dummy/read CRC middle byte[15:8]		Wport Rport

Register::Flash_prog_ISP2					0xFF66	
Name	Bits	R/W	Default	Comments	Config	
prog_l	7:0	R/W	0x00	Flash program/write/dummy/read CRC low byte[7:0]		Wport Rport

Register::common_inst_read_port0					0xFF67	
Name	Bits	R/W	Default	Comments	Config	
com_rd_h	7:0	R	0x00	Common instruction read high byte[23:16]		

Register::common_inst_read_port1					0xFF68
Name	Bits	R/W	Default	Comments	Config
com_rd_m	7:0	R	0x00	Common instruction read middle byte[15:8]	

Register::common_inst_read_port2					0xFF69
Name	Bits	R/W	Default	Comments	Config
com_rd_l	7:0	R	0x00	Common instruction read low byte[7:0]	

Common Instruction Usage :

1. Set common instruction type.
2. Set common instruction OP code.
3. Set write number (0 ~ 3).
4. Set read number if common instruction type is read.
5. Write data to **Flash_prog_write_dum_readCRC_ISP** if write number > 0 .
6. Execution common instruction enable.
7. Polling common instruction enable in ISP mode → If it is finished and the instruction is read, read the Data in **common_inst_read_port** .
8. It would auto clear in normal mode. Then read the Data in **common_inst_read_port** if the instruction type is read.

Common Instruction Setting Example :

Write function

	com_op	write_num=0			rd_num =0		
WREN	06h	X	X	X	X	X	X
WRDI	04h	X	X	X	X	X	X
EWSR	50h	X	X	X	X	X	X
DP	B9h	X	X	X	X	X	X
RDP	ABh	X	X	X	X	X	X

Read function

write_num =0 , rd_num=3

	com_op	rd_num setting					
RDID	9Fh	ID23-ID16	ID15-ID8	ID7-ID0			
JEDEC ID READ*1	9Fh	ID2	ID1	Device ID			

write_num=0, rd_num=1

RDCR	A1h	RD_CR					
RDSR	05h	RD_SR					

write_num=3, rd_num=1 or 2

RES	ABh	DUMMY	DUMMY	DUMMY	Electronic Signature		
REMS	90h	DUMMY	DUMMY	00h	ID	Device ID	

Write after WREN function

	com_op	write_num=1	rd_num=0				
WRSR	01h	WR_SR					

Write after WRSR function

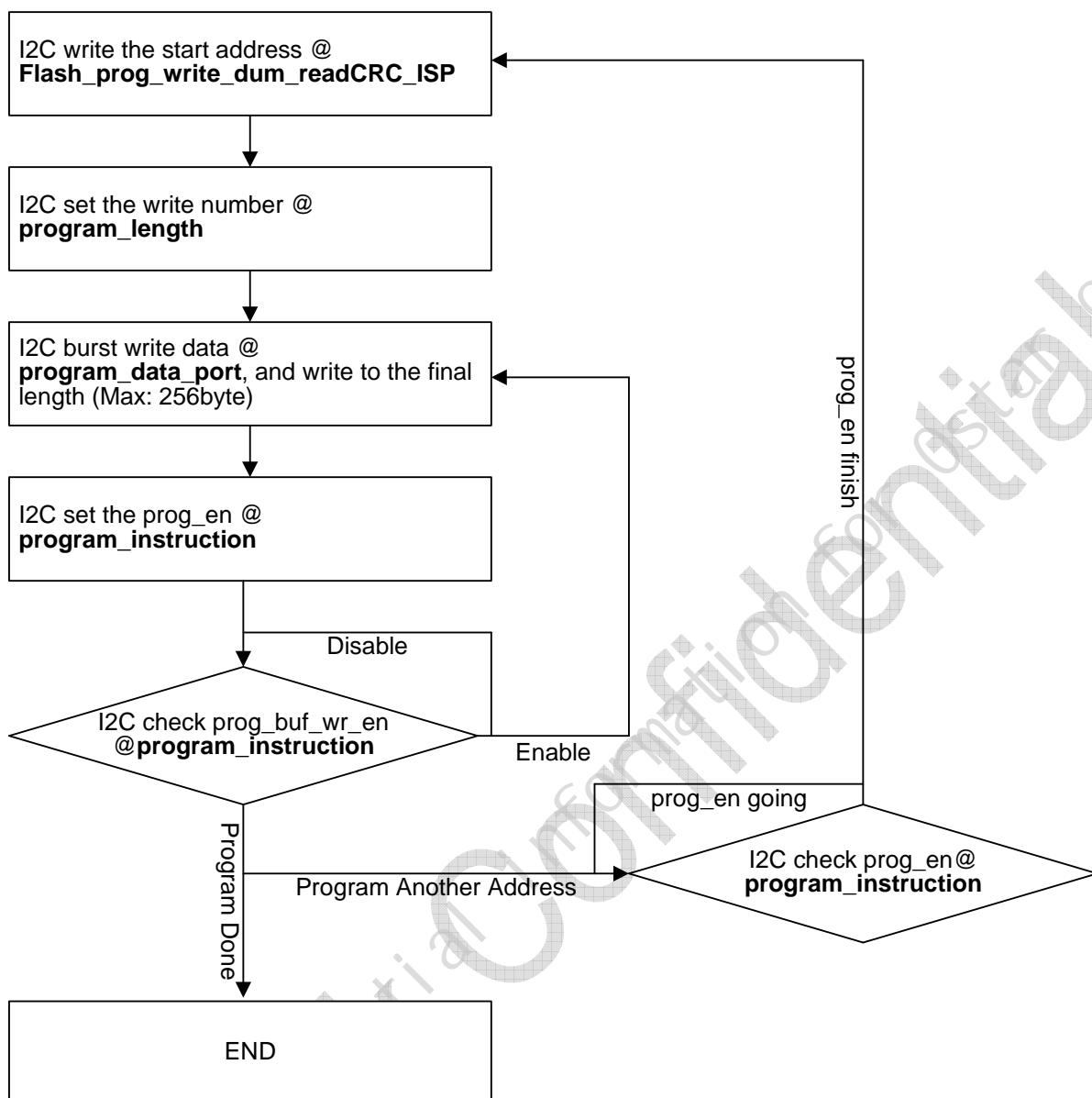
	com_op	write_num=1	rd_num=0				
WRCR	F1h	WR_CR					

Erase function

	com_op	write_num = 0 or 3			rd_num=0		
SECTOR_ER (4k byte)	20h	AD1	AD2	AD3			
BLOCK_ER (64k byte)	D8h	AD1	AD2	AD3			
Page Erase	DBh	AD1	AD2	AD3			
CHIP_ER	C7h						

Program/Read/ISP/CRC Register

ISP Protocol of Program Data :



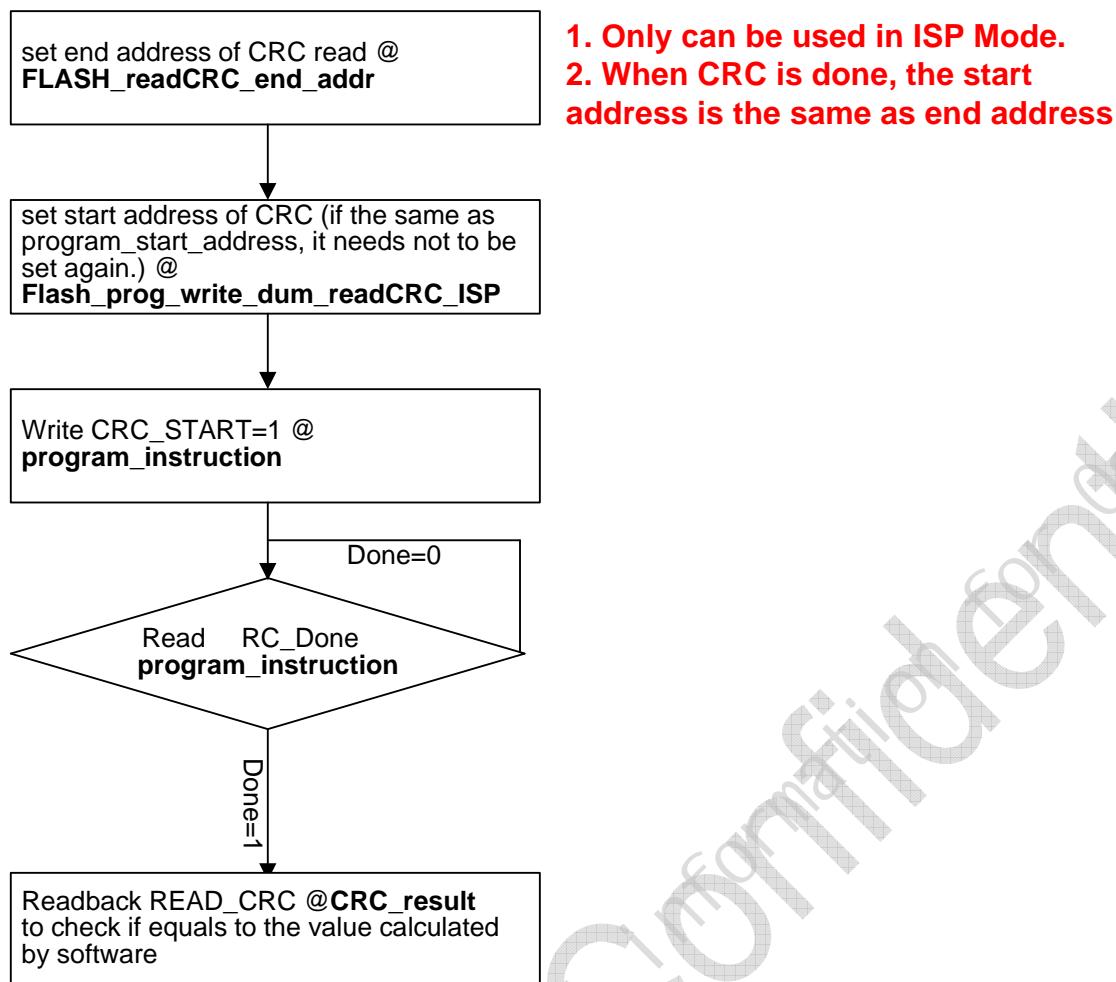
In SPI Mode

1. We use two 256 bytes buffer for Program.
2. We write buffer by DDC Channel.
3. We auto switch two buffer during program.
→ If `prog_buf_wr_en = 1`, you can keep write data to buffer.

In Normal mode

1. We use one 256 bytes buffer for Program.
2. We write buffer by uP.
3. We only use one buffer during program.
→ We can program Max. 256 bytes one time.

Protocol of CRC of read Data :



Register::read_op_code					0xFF6A
Name	Bits	R/W	Default	Comments	Config
read_op	7:0	R/W	0x03	Read command op code	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Register::fast_read_op_code					0xFF6B
Name	Bits	R/W	Default	Comments	Config
Fast_read_op	7:0	R/W	0x0B	Fast read command op code Include Fast dual read op code & fast read dual input output op code	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Register::read_instruction					0xFF6C
Name	Bits	R/W	Default	Comments	Config
read_mode	7:6	R/W	0x0	00: normal read 01: fast read 10: fast dual data read 11: fast dual input and dual output	Wen_out
latch_so_rise	5	R/W	0x0	0: latch Flash SO Data in rising edge 1: latch Flash SO Data in falling edge	Wen_out
drive_si_fall	4	R/W	0x0	0: Output Flash SI Data in falling edge 1: Output Flash SI Data in rising edge	Wen_out

si_dly_sel	3:2	R/W	0x0	00: 0ns 10: 4ns 11: 6ns	01: 2ns 11: 6ns	Wen_out
Reserved	1:0	R/W	0x0	00: 0ns 01: Reserved 10: Reserved 11: Reserved		Wen_out

Note: 1. Normally, SPI Flash drive data in falling edge and sample data in rising edge !!!

2. It would force flash controller to idle state when write this byte.

Register::program_op_code				0xFF6D		
Name	Bits	R/W	Default	Comments	Config	
prog_op	7:0	R/W	0xff	Program command op code		

Register::read_status_register_op_code				0xFF6E		
Name	Bits	R/W	Default	Comments	Config	
rdsr_op	7:0	R/W	0x05	Read status register register command op code		

Register::program_instruction				0xFF6F		
Name	Bits	R/W	Default	Comments	Config	
isp_en	7	R/W	0x0	Enable ISP program : all registers except this register can't write/read when ISP_ENABLE=0 0: disable 1: enable (gating 8051 clock)	Rport Wport	
prog_mode	6	R/W	0x0	0: normal mode (other select reference 0xFF6F[3]) 1: AAI mode		
prog_en	5	R/W	0x0	0: finish 1: program on-going (write 1 to start, auto clear when finish)	Rport Wport	
prog_buf_wr_en	4	R	0x1	0: can't write data to sram 1: can write data to sram		
Prog_normal_mode	3	R/W	0x0	Program normal mode select 0: page program (1byte OP code + 3byte address + N byte data) 1: single byte program , hardware implement single byte write (1Byte OP + 3Byte Addr + Data0, 1Byte OP + 3Byte Addr + Data1, ...)		
crc_start	2	R/W	0x0	When write one, read data from PROG_ST_ADDR to PROG_END_ADDR. And at the same time the CRC is calculated by IC automatically. This bit will be auto cleared when crc_done is 1.(Can be trigger in ISP Mode only)	Rport Wport	
crc_done	1	R	0x1	It will show 1 when CRC is done, and will return to 0 when CRC_START is set.		
rst_flash_ctrl	0	R/W	0x0	0: disable 1: software reset flash controller	Rport Wport	

No Use Parser::program_data_port				0xFF70		
Name	Bits	R/W	Default	Comments	Config	

prog_port	7:0	W		Program write data port to SRAM	
-----------	-----	---	--	---------------------------------	--

Name	Bits	R/W	Default	Comments	Config
prog_length	7:0	R/W	0xFF	Program write number	

Name	Bits	R/W	Default	Comments	Config
rdcrc_end_addr_h	7:0	R/W	0x00	Read CRC end address high byte [23:16]	

Name	Bits	R/W	Default	Comments	Config
rdcrc_end_addr_m	7:0	R/W	0x00	Read CRC end address middle byte [15:8]	

Name	Bits	R/W	Default	Comments	Config
rdcrc_end_addr_l	7:0	R/W	0x00	Read CRC end address low byte [7:0]	

Name	Bits	R/W	Default	Comments	Config
crc_result	7:0	R	-	CRC value of data between PROG_ST_ADDR and RDCRC_END_ADDR	

Flash timing Register

Name	Bits	R/W	Default	Comments	Config
cen_high_num	7:4	R/W	0x9	Chip enable high number[3:0] (based on flash clock) Cycle : 1 ~ 16 (0x0 ~ 0xF)	Wen_out
cen_setup_num	3:2	R/W	0x0	Chip enable setup number (based on flash clock) Cycle : 0.5 ~ 3.5 Cycle : 1 ~ 4 (if drive_si_fall)	Wen_out
cen_hold_num	1:0	R/W	0x0	Chip enable hold number (based on flash clock) Cycle : 1 ~ 4 Cycle : 0.5 ~ 3.5 (if drive_si_fall)	Wen_out

Note : 1 It would force flash controller to idle state when write this byte.

Name	Bits	R/W	Default	Comments	Config
AAI_Mode_Byt_Num	7:0	R/W	0x1	SST flash, AAI mode, transfer number 0x00: transfer 1 byte 0x01: transfer 1byte 0x02: transfer 2bytes and so on	

Name	Bits	R/W	Default	Comments	Config
ISP_CMD_INSERT	7:0	R/W	0x1		

Reserved	7	R/W	0	Reserved	
Force_CE_low	6	R/W	0	0: Normal 1: Force CE low between Common instructions (Only effective in burst write from XRAM, between common write/read instructions)	
ISP_CMD_WAIT_RESO_M0	5:4	R/W	0	cmd wait time resolution, m0 divider divide value = 2^{m0} 00: divide 1 01: divide 2 10: divide 4 11: divide 8	
ISP_CMD_WAIT_RESO_M1	3:1	R/W	0	cmd wait time resolution, m1 divider divide value = 2^{m1}	
ISP_CMD_INSERT_EN	0	R/W	0	Enable insert CMD before isp program 0: disable 1: enable	

Register:::ISP_CMD_LENGTH				0xFF82	
Name	Bits	R/W	Default	Comments	Config
ISP_CMD_LENGTH	7:0	R/W	0xFF	Total max length of ISP CMD: 0x00: length=1 0x01: length=2 ... 0xFF: length=256	

ISP Command Format:

`cmd_length(=1+n1) + cmd_wait_length + cmd_opcode + n1 byte data`

`cmd_length(=1+n2) + cmd_wait_length + cmd_opcode + n2 byte data`

...

`cmd_length=0 (end)`

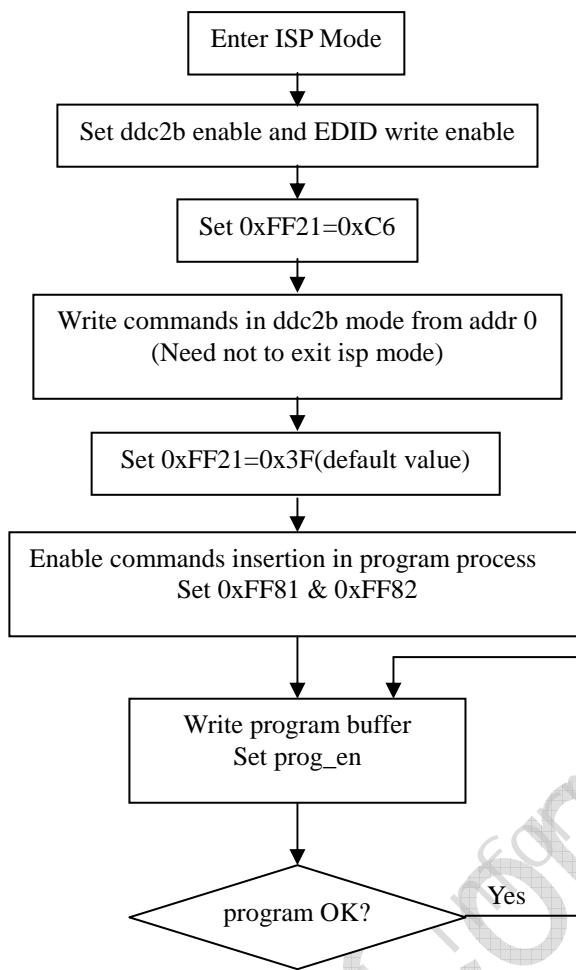
wait time = $\text{cmd_wait_length} * 2^{m1} * 2^{m0} * (\text{flash_clk period})$

wait time is inserted after current command execution

Example:

- 01 00 06 → opcode=0x06, no data, no wait time
- 02 80 01 7C → opcode=0x01, data=0x7C, wait time= $128 * 2^{m1} * 2^{m0} * (\text{flash_clk period})$
- 01 00 C3 → opcode=0xC3, no data, no wait time
- 01 00 A5 → opcode=0xA5, no data, no wait time
- 01 00 C3 → opcode=0xC3, no data, no wait time
- 01 00 A5 → opcode=0xA5, no data, no wait time
- 01 00 06 → opcode=0x06, no data, no wait time
- 02 FF 01 00 → opcode=0x01, data=0x00, wait time= $255 * 2^{m1} * 2^{m0} * (\text{flash_clk period})$
- 00 → end

To execute the above 8 commands, you need to write 27 bytes to RAM at one time.



ISP command insertion program flow (e.g. for MXIC new flash)

Register: PWM_CK_SEL_HS					0xFF99
Name	Bits	R/W	Default	Comments	Config
PWM1_REF_CTRL_EN	7	R/W	0	0: PWM1 normal output 1: PWM reference gated by PWM1 output	
PWM0_REF_CTRL_EN	6	R/W	0	0: PWM0 normal output 1: PWM reference gated by PWM0 output	
PWM5_CK_SEL_HS	5	R/W	0	PWMx clock generator input source 0: reference PWM5_CK_SEL 1: using DHS as reference clock The total level count is {PWM5H_TOTALCNT, PWM5L_TOTALCNT}, high level count is {PWM5H_DUT, PWM5L_DUT}, and limited H/L transition number by PWM5_CYCLE_MAX	
PWM4_CK_SEL_HS	4	R/W	0	PWMx clock generator input source 0: reference PWM4_CK_SEL 1: using DHS as reference clock The total level count is {PWM4H_TOTALCNT, PWM4L_TOTALCNT}, high level count is {PWM4H_DUT, PWM4L_DUT}, and limited H/L transition number by PWM4_CYCLE_MAX	

PWM3_CK_SEL_HS	3	R/W	0	PWMx clock generator input source 0: reference PWM3_CK_SEL 1: using DHS as reference clock The total level count is {PWM3H_TOTALCNT, PWM3L_TOTALCNT}, high level count is {PWM3H_DUT, PWM3L_DUT}, and H/L transition number is limited by PWM3_CYCLE_MAX	
PWM2_CK_SEL_HS	2	R/W	0	PWMx clock generator input source 0: reference PWM2_CK_SEL 1: using DHS as reference clock The total level count is {PWM2H_TOTALCNT, PWM2L_TOTALCNT}, high level count is {PWM2H_DUT, PWM2L_DUT}, and H/L transition number is limited by PWM2_CYCLE_MAX	
PWM1_CK_SEL_HS	1	R/W	0	PWMx clock generator input source 0: reference PWM1_CK_SEL 1: using DHS as reference clock The total level count is {PWM1H_TOTALCNT, PWM1L_TOTALCNT}, high level count is {PWM1H_DUT, PWM1L_DUT}, and H/L transition number is limited by PWM1_CYCLE_MAX	
PWM0_CK_SEL_HS	0	R/W	0	PWMx clock generator input source 0: reference PWM0_CK_SEL 1: using DHS as reference clock The total level count is {PWM0H_TOTALCNT, PWM0L_TOTALCNT}, high level count is {PWM0H_DUT, PWM0L_DUT}, and H/L transition number is limited by PWM0_CYCLE_MAX	

100Mhz SPI Flash Calibration

Register::SPI_CAL_Ctrl				0xFF9D	
Name	Bits	R/W	Default	Comments	Config
DLY_CAL_START	7	R/W	0	Write 1 to start SPI calibration. Auto clear when SPI calibration has been completed.	Rport Wport
DLY_CAL_CHECK	6	R/W	1	0: Not check delay out-of-range 1: Check delay out-of-range (> T/2)	
CAL_CLK_DIV	5:4	R/W	0x2	SPI-FLASH clock divider, its clock source is selected by MCU_CLK_SEL, active when DLY_CAL_START 0: divide 1 1: divide 2 2: divide 3 3: divide 4	
DLY_SEL	3:0	R/W	0	Delay selection: (DLY_HI_THR + DLY_LO_THR)/2 reference cali result 0xFF9E 0000: 0.0ns 0001: 0.5ns 0010: 1.0ns 0011: 1.5ns 0100: 2.0ns ... 1111: 7.5ns	

Register::SPI_CAL_Result				0xFF9E	
Name	Bits	R/W	Default	Comments	Config
DLY_HI_THR	7:4	R	0	Calibration pass high threshold	
DLY_LO_THR	3:0	R	0	Calibration pass low threshold	

Register:::SPI_CAL_Data_00
0xFF9F

Name	Bits	R/W	Default	Comments	Config
CAL_DATA0	7:0	R/W	0	Calibration golden data0	

Register:::SPI_CAL_Data_01
0xFFA5

Name	Bits	R/W	Default	Comments	Config
CAL_DATA1	7:0	R/W	0	Calibration golden data1	

Register:::SPI_CAL_Data_02
0xFFA6

Name	Bits	R/W	Default	Comments	Config
CAL_DATA2	7:0	R/W	0	Calibration golden data2	

Register:::SPI_CAL_ADR_H
0xFFA7

Name	Bits	R/W	Default	Comments	Config
CAL_ADR_H	7:0	R/W	0	Calibration flash start address[23:16]	

Register:::SPI_CAL_ADR_M
0xFFA8

Name	Bits	R/W	Default	Comments	Config
CAL_ADR_M	7:0	R/W	0	Calibration flash start address[15:8]	

Register:::SPI_CAL_ADR_L
0xFFA9

Name	Bits	R/W	Default	Comments	Config
CAL_ADR_L	7:0	R/W	0	Calibration flash start address[7:0]	

MCU Register2 (Page E) PWM

Register::PWM01_TOTALCNT_MSB 0xFF90					
Name	Bits	R/W	Default	Comments	Config
PWM1H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]	wport rport
PWM0H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]	wport rport

Register::PWM0_TOTALCNT_LSB 0xFF91					
Name	Bits	R/W	Default	Comments	Config
PWM0L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM1_TOTALCNT_LSB 0xFF92					
Name	Bits	R/W	Default	Comments	Config
PWM1L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM23_TOTALCNT_MSB 0xFF93					
Name	Bits	R/W	Default	Comments	Config
PWM3H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]	wport rport
PWM2H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]	wport rport

Register::PWM2_TOTALCNT_LSB 0xFF94					
Name	Bits	R/W	Default	Comments	Config
PWM2L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM3_TOTALCNT_LSB 0xFF95					
Name	Bits	R/W	Default	Comments	Config
PWM3L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM45_TOTALCNT_MSB 0xFF96					
Name	Bits	R/W	Default	Comments	Config
PWM5H_TOTALCNT	7:4	R/W	0	PWMx , total level count MSB[11:8]	wport rport
PWM4H_TOTALCNT	3:0	R/W	0	PWMx , total level count MSB[11:8]	wport rport

Register::PWM4_TOTALCNT_LSB 0xFF97					
Name	Bits	R/W	Default	Comments	Config
PWM4L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM5_TOTALCNT_LSB 0xFF98					
Name	Bits	R/W	Default	Comments	Config
PWM5L_TOTALCNT	7:0	R/W	0	PWMx , total level count LSB[7:0]	wport rport

Register::PWM_CK_SEL_HS 0xFF99					
Name	Bits	R/W	Default	Comments	Config
PWM_CK_SEL_HS_DUMMY	7:6	R/W	0	Dummy	
PWM5_CK_SEL_HS	5	R/W	0	PWMx clock generator input source 0: reference PWM5_CK_SEL 1: using DHS as reference clock The total level count is {PWM5H_TOTALCNT, PWM5L_TOTALCNT}, high level count is {PWM5H_DUT, PWM5L_DUT}, and limited H/L transition number by PWM5_CYCLE_MAX	

PWM4_CK_SEL_HS	4	R/W	0	PWMx clock generator input source 0: reference PWM4_CK_SEL 1: using DHS as reference clock The total level count is {PWM4H_TOTALCNT, PWM4L_TOTALCNT }, high level count is {PWM4H_DUT, PWM4L_DUT}, and limited H/L transition number by PWM4_CYCLE_MAX	
PWM3_CK_SEL_HS	3	R/W	0	PWMx clock generator input source 0: reference PWM3_CK_SEL 1: using DHS as reference clock The total level count is {PWM3H_TOTALCNT, PWM3L_TOTALCNT }, high level count is {PWM3H_DUT, PWM3L_DUT}, and H/L transition number is limited by PWM3_CYCLE_MAX	
PWM2_CK_SEL_HS	2	R/W	0	PWMx clock generator input source 0: reference PWM2_CK_SEL 1: using DHS as reference clock The total level count is {PWM2H_TOTALCNT, PWM2L_TOTALCNT }, high level count is {PWM2H_DUT, PWM2L_DUT}, and H/L transition number is limited by PWM2_CYCLE_MAX	
PWM1_CK_SEL_HS	1	R/W	0	PWMx clock generator input source 0: reference PWM1_CK_SEL 1: using DHS as reference clock The total level count is {PWM1H_TOTALCNT, PWM1L_TOTALCNT }, high level count is {PWM1H_DUT, PWM1L_DUT}, and H/L transition number is limited by PWM1_CYCLE_MAX	
PWM0_CK_SEL_HS	0	R/W	0	PWMx clock generator input source 0: reference PWM0_CK_SEL 1: using DHS as reference clock The total level count is {PWM0H_TOTALCNT, PWM0L_TOTALCNT }, high level count is {PWM0H_DUT, PWM0L_DUT}, and H/L transition number is limited by PWM0_CYCLE_MAX	

Register:::PWM01_CYCLE_MAX 0xFF9A					
Name	Bits	R/W	Default	Comments	Config
PWM0_CYCLE_MAX	7:4	R/W	0	PWM0 maximum H/L cycle count Output PWM0 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	
PWM1_CYCLE_MAX	3:0	R/W	0	PWM1 maximum H/L cycle count Output PWM1 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	

Register:::PWM23_CYCLE_MAX 0xFF9B					
Name	Bits	R/W	Default	Comments	Config
PWM2_CYCLE_MAX	7:4	R/W	0	PWM2 maximum H/L cycle count Output PWM2 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	
PWM3_CYCLE_MAX	3:0	R/W	0	PWM3 maximum H/L cycle count Output PWM3 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	

Register:::PWM45_CYCLE_MAX					0xFF9C
Name	Bits	R/W	Default	Comments	Config
PWM4_CYCLE_MAX	7:4	R/W	0	PWM4 maximum H/L cycle count Output PWM4 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	
PWM5_CYCLE_MAX	3:0	R/W	0	PWM5 maximum H/L cycle count Output PWM5 clock cycle number between two DVS. When set to 0, there is no limitation. This setting can only make effect by using DHS as reference clock	

MCU register 3 (page F)
GPIO Control

Register::PortD7_pin_reg						0xFF77
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PD7	0	R/W	1	Input/output value of PD.7		Rport wport

Register::PortD6_pin_reg						0xFF78
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PD6	0	R/W	1	Input/output value of PD.6		Rport wport

Register::PortD5_pin_reg						0xFF79
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PD5	0	R/W	1	Input/output value of PD.5		Rport wport

Register::PortD4_pin_reg						0xFF7A
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PD4	0	R/W	1	Input/output value of PD.4		Rport wport

Register::PortD3_pin_reg						0xFF7B
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PD3	0	R/W	1	Input/output value of PD.3		Rport wport

Register::PortD2_pin_reg						0xFF7C
Name	Bits	R/W	Default	Comments		Config

Reserved	7:1	--	0	Reserved	
PD2	0	R/W	1	Input/output value of PD.2	Rport wport

Register::PortD1_pin_reg					0xFF7D
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PD1	0	R/W	1	Input/output value of PD.1	Rport wport

Register::PortD0_pin_reg					0xFF7E
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PD0	0	R/W	1	Input/output value of PD.0	Rport wport

Register::PortB7_pin_reg					0xFF7F
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB7	0	R/W	1	Input/output value of PB.7	Rport wport

Register::PortB6_pin_reg					0xFF89
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB6	0	R/W	1	Input/output value of PB.6	Rport wport

Register::PortB5_pin_reg					0xFF8A
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB5	0	R/W	1	Input/output value of PB.5	Rport wport

Register::PortB4_pin_reg					0xFF8B
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Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB4	0	R/W	1	Input/output value of PB.4	Rport wport

Register::PortB3_pin_reg 0xFF8C					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB3	0	R/W	1	Input/output value of PB.3	Rport wport

Register::PortB2_pin_reg 0xFF8D					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB2	0	R/W	1	Input/output value of PB.2	Rport wport

Register::PortB1_pin_reg 0xFF8E					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB1	0	R/W	1	Input/output value of PB.1	Rport wport

Register::PortB0_pin_reg 0xFF8F					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PB0	0	R/W	1	Input/output value of PB.0	Rport wport

Register::PortC3_pin_reg 0xFFA0					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PC3	0	R/W	1	Input/output value of PC.3	Rport wport

Register::PortC2_pin_reg						0xFFA1
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PC2	0	R/W	1	Input/output value of PC.2		Rport wport

Register::PortC1_pin_reg						0xFFA2
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PC1	0	R/W	1	Input/output value of PC.1		Rport wport

Register::PortC0_pin_reg						0xFFA3
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PC0	0	R/W	1	Input/output value of PC.0		Rport wport

Register::PortC4_pin_reg						0xFFA4
Name	Bits	R/W	Default	Comments		Config
Reserved	7:1	--	0	Reserved		
PC4	0	R/W	1	Input/output value of PC.4		Rport wport

Register::Port_read_control						0xFFC0
Name	Bits	R/W	Default	Comments		Config
PA_pin_reg_n	7	R/W	0	Source selection for PA read back 0: register 1: bus value		
P9_pin_reg_n	6	R/W	0	Source selection for P9 read back 0: register 1: bus value		
P8_pin_reg_n	5	R/W	0	Source selection for P8 read back 0: register 1: bus value		
P7_pin_reg_n	4	R/W	0	Source selection for P7 read back 0: register 1: bus value		
P6_pin_reg_n	3	R/W	0	Source selection for P6 read back 0: register		

				1: bus value Source selection for P5 read back 0: register 1: bus value	
P5_pin_reg_n	2	R/W	0	Source selection for P3 read back* 0: register 1: bus value	
P3_pin_reg_n	1	R/W	0	Source selection for P1 read back* 0: register 1: bus value	

*: only effect in external MCU control, embedded MCU will control the source by assembly code.

Register::Port52_pin_reg					0xFFC1
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P52	0	R/W	1	Input/output value of P5.2	Rport wport

Register::Port53_pin_reg					0xFFC2
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P53	0	R/W	1	Input/output value of P5.3	Rport wport

Register::Port54_pin_reg					0xFFC3
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P54	0	R/W	1	Input/output value of P5.4	Rport wport

Register::Port55_pin_reg					0xFFC4
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P55	0	R/W	1	Input/output value of P5.5	Rport wport

Register::Port56_pin_reg					0xFFC5
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	

P56	0	R/W	1	Input/output value of P5.6	Rport wport
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Register::Port57_pin_reg					0xFFC6
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P57	0	R/W	1	Input/output value of P5.7	Rport wport

Register::Port60_pin_reg					0xFFC7
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P60	0	R/W	1	Input/output value of P6.0	Rport wport

Register::Port61_pin_reg					0xFFC8
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P61	0	R/W	1	Input/output value of P6.1	Rport wport

Register::Port62_pin_reg					0xFFC9
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P62	0	R/W	1	Input/output value of P6.2	Rport wport

Register::Port63_pin_reg					0xFFCA
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P63	0	R/W	1	Input/output value of P6.3	Rport wport

Register::Port64_pin_reg					0xFFCB
Name	Bits	R/W	Default	Comments	Config

Reserved	7:1	--	0	Reserved	
P64	0	R/W	1	Input/output value of P6.4	Rport wport

Register::Port65_pin_reg					0xFFCC
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P65	0	R/W	1	Input/output value of P6.5	Rport wport

Register::Port66_pin_reg					0xFFCD
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P66	0	R/W	1	Input/output value of P6.6	Rport wport

Register::Port67_pin_reg					0xFFCE
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P67	0	R/W	1	Input/output value of P6.7	Rport wport

Register::Port70_pin_reg					0xFFCF
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P70	0	R/W	1	Input/output value of P7.0	Rport wport

Register::Port71_pin_reg					0XFFD0
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P71	0	R/W	1	Input/output value of P7.1	Rport wport

Register::Port72_pin_reg					0xFFD1
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Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P72	0	R/W	1	Input/output value of P7.2	Rport wport

Register::Port73_pin_reg				0xFFD2	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P73	0	R/W	1	Input/output value of P7.3	Rport wport

Register::Port74_pin_reg				0xFFD3	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P74	0	R/W	1	Input/output value of P7.4	Rport wport

Register::Port75_pin_reg				0xFFD4	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P75	0	R/W	1	Input/output value of P7.5	Rport wport

Register::Port76_pin_reg				0xFFD5	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P76	0	R/W	1	Input/output value of P7.6	Rport wport

Register::Port80_pin_reg				0xFFD6	
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P80	0	R/W	1	Input/output value of P8.0	Rport wport

Register::Port81_pin_reg				0xFFD7	

Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P81	0	R/W	1	Input/output value of P8.1	Rport wport

Register::Port90_pin_reg					0xFFD8
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P90	0	R/W	1	Input/output value of P9.0	Rport wport

Register::Port91_pin_reg					0xFFD9
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P91	0	R/W	1	Input/output value of P9.1	Rport wport

Register::Port92_pin_reg					0xFFDA
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P92	0	R/W	1	Input/output value of P9.2	Rport wport

Register::Port93_pin_reg					0xFFDB
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P93	0	R/W	1	Input/output value of P9.3	Rport wport

Register::Port94_pin_reg					0xFFDC
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
P94	0	R/W	1	Input/output value of P9.4	Rport wport

Register::Porta0_pin_reg					0xFFDD
Name	Bits	R/W	Default	Comments	Config

Reserved	7:1	--	0	Reserved	
PA0	0	R/W	1	Input/output value of PA.0	Rport wport

Register::Porta1_pin_reg					0xFFDE
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA1	0	R/W	1	Input/output value of PA.1	Rport wport

Register::Porta2_pin_reg					0xFFDF
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA2	0	R/W	1	Input/output value of PA.2	Rport wport

Register::Porta3_pin_reg					0xFFE0
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA3	0	R/W	1	Input/output value of PA.3	Rport wport

Register::Porta4_pin_reg					0xFFE1
Name	Bits	R/W	Default	Comments	Config
Reserved	7:1	--	0	Reserved	
PA4	0	R/W	1	Input/output value of PA.4	Rport wport

SFR Access

When embedded MCU is selected, the P1, P3 GPIO is controlled by SFR. Both of the port groups must be access by below registers when using external MCU. Below registers are useless when embedded MCU is adopted.

Register::Port1_pin_reg					0xFFE2
Name	Bits	R/W	Default	Comments	Config

P1	7:0	R/W	0xFF	Input/output value of P1 In 8051 mode, register is READ only In ISP mode, register can be READ and WRITE.	Rport Wport
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Register::Port3_pin_reg					0xFFE3
Name	Bits	R/W	Default	Comments	Config
P3	7:0	R/W	0xFF	Input/output value of P3 In 8051 mode, register is READ only In ISP mode, register can be READ and WRITE.	Rport Wport

Register:: DVI_EDID_IRQ					0xFFE4
Name	Bits	R/W	Default	Comments	Config
REV_DUMMY_FFE4	7:6	R/W	1	Dummy 0: Enable SOD Access Xram 1 : Disable SOD Access Xram	
SOD_ACCESS_DISABLE	7				
REV_DUMMY_FFE4	6	R/W	0	Dummy	
DVI_FORCE_NACK	5	R/W	0	In DDC2B Mode, force DVI SDA no output 0:disable 1:enable	
DVI_FORCE_ACK_ZERO	4	R/W	0	In DDC2B Mode, force DVI SDA Output 0 (ACK) 0:disable 1:enable	
DVI_SCL_IRQ_EN	3	R/W	0	DVI SCL Toggle IRQ enable 0:disable 1:enable	
DVI_SCL_IRQ_STATUS	2	R/W	0	DVI SCL Toggle status , write 1 to clear 0: no scl toggle after clear 1: new scl toggle after clear	Rport Wport
DVI_EDIDRD_IRQ_EN	1	R/W	0	DVI EDID READ IRQ enable 0:disable 1:enable	
DVI_EDIDRD_STATUS	0	R/W	0	DVI EDID READ STATUS , write 1 to clear 0: no edid read after clear 1: new edid read after clear	Rport Wport

Register:: HDMI_EDID_IRQ					0xFFE5
Name	Bits	R/W	Default	Comments	Config
EDID_PRE_READ_EN	7	R/W	0	Pre-Read EDID Enable 0: Disable 1: Enable (This bit is for 3 DDC speed-up, Pre-Read happens at sub-address set or inc) SCL max speed: 3.5M (when XRAM works at 7M)	
REV_DUMMY_FFE5	6	R/W	0	Dummy	
HDMI_FORCE_NACK	5	R/W	0	In DDC2B Mode, force HDMI SDA output 1(NACK) 0:disable 1:enable	
HDMI_FORCE_ACK_ZERO	4	R/W	0	In DDC2B Mode force HDMI SDA Output 0 (ACK) 0:disable 1:enable	
HDMI_SCL_IRQ_EN	3	R/W	0	HDMI SCL Toggle IRQ enable 0:disable 1:enable	

HDMI_SCL_IRQ_STATUS	2	R/W	0	HDMI SCL Toggle status , wite 1 to clear 0: no scl toggle after clear 1: new scl toggle after clear	Rport Wport
HDMI_EDIDRD_IRQ_EN	1	R/W	0	HDMI EDID READ IRQ enable 0:disable 1:enable	
HDMI_EDIDRD_STATUS	0	R/W	0	HDMI EDID READ STATUS , wite 1 to clear 0: no edid read after clear 1: new edid read after clear	Rport Wport

Register::Port_read_control_2					0xFFE6
Name	Bits	R/W	Default	Comments	Config
PC_pin_reg_n	7	R/W	0	Source selection for PC read back 0: register 1: bus value	
PB_pin_reg_n	6	R/W	0	Source selection for PB read back 0: register 1: bus value	
PD_pin_reg_n	5	R/W	0	Source selection for PD read back 0: register 1: bus value	
Reserved	4:0	--	0	Reserved	

Register:: VGA_EDID_IRQ					0xFFE7
Name	Bits	R/W	Default	Comments	Config
REV_DUMMY_FFE7	7:6	R/W	0	Dummy	
VGA_FORCE_NACK	5	R/W	0	In DDC2B Mode, force VGA SDA output 1(NACK) 0:disable 1:enable	
VGA_FORCE_ACK_ZERO	4	R/W	0	In DDC2B Mode force VGA SDA Output 0 (ACK) 0:disable 1:enable	
VGA_SCL_IRQ_EN	3	R/W	0	VGA SCL Toggle IRQ enable 0:disable 1:enable	
VGA_SCL_IRQ_STATUS	2	R/W	0	VGA SCL Toggle status , wite 1 to clear 0: no scl toggle after clear 1: new scl toggle after clear	Rport Wport
VGA_EDIDRD_IRQ_EN	1	R/W	0	VGA EDID READ IRQ enable 0:disable 1:enable	
VGA_EDIDRD_STATUS	0	R/W	0	VGA EDID READ STATUS , wite 1 to clear 0: no edid read after clear 1: new edid read after clear	Rport Wport

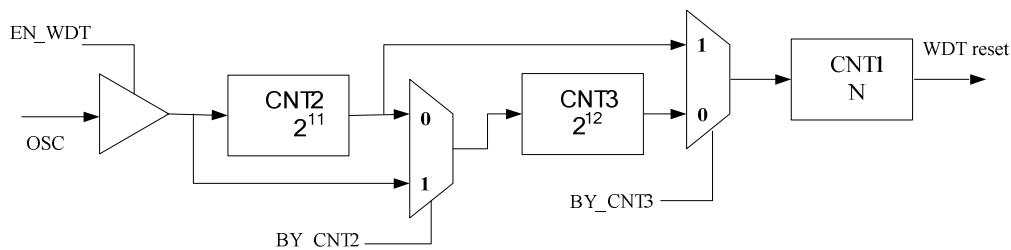
Register:: REV_DUMMY4					0xFFE9
Name	Bits	R/W	Default	Comments	Config
REV_DUMMY4	7:2	R/W	00	Dummy4	REV_DUMMY4
Disable RDSR CE	1	R/W	0	0: Enable RDSR CE 1: Disable RDSR CE	

Disable WREN CE	0	R/W	0	0: Enable WREN CE 1: Disable WREN CE	
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Watchdog Timer

The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is about 0.44 sec to 3.5 sec(assume crystal is 14.3MHz) and can be programmed via register CNT1.

Watchdog timer can be configured to generate an IRQ periodically, when watchdog timer count value increases to the threshold value, and if user do not clear the watchdog timer counters, watchdog timer will overflow to generate reset signal.



Register::WATCHDOG_timer					0xFFEA	
Name	Bits	R/W	Default	Comments	Config	
WDT_EN	7	R/W	1	0: Disable watchdog timer 1: Enable watchdog timer		
CLR_WDT	6	W	0	0: No effect 1: Clear all counters of watchdog and latch the value in counter to 0xFFAA~0xFFAD	Rport Wport	
SF_HLT_WDT_EN	5	R/W	0	1: Stop watchdog counter by SPI-FLASH access		
BW_HLT_WDT_EN	4	R/W	0	1: Stop watchdog counter by scalar burst write action		
Reserved	3	--	--	Reserved		
CNT1	2:0	R/W	0	The number N of counter1 000~111: 1~8		

- When ISP mode is enabled, watchdog will be disabled by hardware.

Register::WDT_test					0xFFEB	
Name	Bits	R/W	Default	Comments	Config	
WDT_Overflow_Flag	7	R/W	0	when watchdog timer counter counts to threshold value, this bit will be set to 1. Write 1 to clear	Rport Wport	
Reserved	6:5	-	0	Reserved		
WDT_TIMER_MODE	4	R/W	0	0: Normal mode 1: Timer mode		
Latch_WDT_CNT_Start	3	W	0	0: Finished 1: Start to latch watchdog timer counter	Rport Wport	
Enable_WDT_IRQ	2	R/W	0	0: Disable watchdog timer counter generate IRQ 1: Enable watchdog timer counter generate IRQ this bit decides to generate an IRQ ,when watchdog timer count value increases to the threshold value.		
BY_CNT2	1	R/W	0	Signal bypass counter2* 0: signal pass through counter2 1: bypass		
BY_CNT3	0	R/W	0	Signal bypass counter3* 0: signal pass through counter3 1: bypass		

*When BY_CNT2 and BY_CNT3 are all assigned one (bypass), watchdog will be counted by CNT3

Register::WATCHDOG_CNT2_Value					0xFFAA	
Name	Bits	R/W	Default	Comments	Config	
WDT_CNT2_L_value	7:0	R	0	value of watchdog timer CNT2[7:0]		

Register:: WATCHDOG_CNT23_Value					0xFFAB
Name	Bits	R/W	Default	Comments	Config
WDT_CNT3_L_value	7:3	R	0	Value of watchdog timer CNT3[4:0]	
WDT_CNT2_H_value	2:0	R	0	Value of watchdog timer CNT2[10:8]	

Register:: WATCHDOG_CNT3_Value					0xFFAC
Name	Bits	R/W	Default	Comments	Config
Reserved	7	-	0	Reserved	
WDT_CNT3_H_value	6:0	R	0	Value of watchdog timer CNT3[11:5]	

Register:: WATCHDOG_CNT1_Value					0xFFAD
Name	Bits	R/W	Default	Comments	Config
Reserved	7:3	-	0	Reserved	
WDT_CNT1_value	2:0	R	0	Value of watchdog timer CNT1[2:0]	

Write FW code to calculate counter value for an example

Eg.

```
DWORD dCounterValue;
dCounterValue = (DWORD) (0xFFAD << 23) | (0xFFAC << 16) | (0xFFAB << 8) | (0xFFAA);
```

Register::WATCHDOG_timer_threshold					0xFFAE
Name	Bits	R/W	Default	Comments	Config
WDT_CNT_threshold_L_value	7:0	R/W	0	threshold value TRH[7:0]. if watchdog timer counter matches threshold value, WDT_Overflow_Flag will be set to 1, and can generate an IRQ if Enable_WDT_IRQ set to 1. If BY_CNT3 = 1 & BY_CNT2 = 0 TRH [7:0] = CNT2[7:0] Else TRH [7:0] = CNT3[7:0]	

Register::WATCHDOG_timer_threshold_mask					0xFFAF
Name	Bits	R/W	Default	Comments	Config
WDT_CNT_threshold_L_mask	7:0	R/W	0	Mask value to threshold value, some bits of threshold value will be ignored. 1: mask. 0: no mask.	

Register::WATCHDOG_timer_H_threshold_mask					0xFFB0
Name	Bits	R/W	Default	Comments	Config
WDT_CNT_threshold_H_mask	7:4	R/W	0	Mask value to threshold value, some bits of threshold value will be ignored. 1: mask. 0: no mask.	
WDT_CNT_threshold_H_value	3:0	R/W	0	threshold value TRH[11:8]. if watchdog timer counter matches threshold value, WDT_Overflow_Flag will be set to 1, and can generate an IRQ if Enable_WDT_IRQ set to 1.	

				If BY_CNT3 = 1 & BY_CNT2 = 0 TRH [11:8] = CNT2[10:8] Else TRH [11:8] = CNT3[11:8]	
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In System Programming

User can program the external serial FLASH by internal hardware without removing serial FLASH from the system. RTD2485XD utilizes DDC channel (ADC/DVI/HDMI DDC) to communicate with IIC host for ISP function. The ISP protocol is mainly compatible with DDC protocol. However, one significant difference is that the LSB of 7-bit ISP address is the address auto increase bit. Thus, we can improve the flash program speed.

Register::ISP_slave_address 0xFFEC					
Name	Bits	R/W	Default	Comments	Config
ISP_ADDR	7:2	R/W	25	ISP slave address	
ISP_ADDR_INC_A	1	R	0	Received LSB of ISP slave address of ADC DDC channel 0: address is nonincrease 1: address is auto-increase	
ISP_ADDR_INC_D	0	R	0	Received LSB of ISP slave address of DVI DDC channel 0: address is nonincrease 1: address is auto-increase	

Register::MCU_control 0xFFED					
Name	Bits	R/W	Default	Comments	Config
PORT_PIN_REG	7	R/W	1	port_pin_reg_n enable 0: port_pin_reg_n signal is disabled 1: port_pin_reg_n signal is enabled	
ISP_ADDR_INC_H	6	R	0	Received LSB of ISP slave address of HDMI DDC channel 0: address is nonincrease 1: address is auto-increase	
FLASH_CLK_DIV	5:2	R/W	2	SPI-FLASH clock divider, its clock source is selected by MCU_CLK_SEL, default is MCU_CLK_SEL/2	
MCU_CLK_SEL	1	R/W	0	CPU clock source select 0: CPU clock is from Crystal divided by DIV 1: CPU clock is from PLL divided by DIV	
CKOUT_SEL	0	R/W	0	CLKO select 0: Select Crystal output 1: Select Mcu clk output	

Register::MCU_clock_control 0xFFEE					
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Name	Bits	R/W	Default	Comments	Config
ISP_MODE	7	R/W	0	ISP Mode Select 0: Normal ISP mode, I2C protocol (Device_ID, address, Data...) 1: AIO Block Write mode I2C protocol (Device_ID, addr, Length, Data...)	Rport Wport
MCU_PERI_NON_STOP	6	R/W	0	1: keep mcu peripheral running whiel mcu stopped by spi flash access 0: peripheral will be stopped with mcu*.	
MCU_CLK_DIV	5:2	R/W	1	MCU clock is FLASH clock/MCU_CLK_DIV.	
SOF_RST	1	R/W	0	Software reset mcu 0: No effect 1: reset RTD2485XD Scaler IC chip	Rport Wport
SCA_HRST	0	R/W	0	Hardware reset for Scalar 0: No effect 1: reset SCALAR module	

*note: this register bit[6] only has effect on peripheral built in SFR, which are timer 0, 1, 2 and serial port 1.

Register::RAM_test 0xFFEF					
Name	Bits	R/W	Default	Comments	Config
MCU_TSTCLK_SEL	7	R/W	0	1: MCU clock is from external pin 0: MCU clock is from crystal/PLL divided by DIV (0xFFED[1])	
SOD_DATA_LOCATION	6:5	R/W	3	Decide sod data wr/rd start location 0: Not used 1: F900 2: FA00 3: F900 SOD Xram space will map to this addr	
Test_mode	4	R/W	0	When test_mode of scalar is enabled for embedded mcu output, the bus is decided by following settins. 0: 10'h0, flash_mcu_clk_gated, bist_clk2pad, xram_clk2pad, 1'b0, shift_in_clk2pad, eclk_ng2pad, eclk_n2pad, eclk2pad, ad8_ckout, ad8_ckini, ad8_dout_s[7:0], ad8_div_clk2pad, fclk2pad 1: 5'h0, fc_addr[23:0], fc_rd_n	
EXT_RAM_BIST	3	R/W	0	Start BIST function for MCU external RAM (512 bytes) 0: finished and clear 1: start	Rport Wport
EXT_RAM_STA	2	R	0	Test result about MCU external RAM 0: fail 1: ok	
INT_RAM_BIST	1	R/W	0	Start BIST function for MCU internal RAM (256 bytes) 0: finished and clear 1: start	Rport Wport
INT_RAM_STA	0	R	0	Test result about MCU internal RAM 0: fail 1: ok	

mode = 0	mode = 1
0	0
0	0
0	0
0	0
0	0
0	fc_addr[23]
0	fc_addr[22]
0	fc_addr[21]
0	fc_addr[20]
0	fc_addr[19]
flash_mcu_clk_gated	fc_addr[18]
bist_clk2pad	fc_addr[17]
xram_clk2pad	fc_addr[16]
0	fc_addr[15]
shift_in_clk2pad	fc_addr[14]
eclk_ng2pad	fc_addr[13]
eclk_n2pad	fc_addr[12]
eclk2pad	fc_addr[11]
ad8_ckout	fc_addr[10]
ad8_ckini	fc_addr[9]
ad8_dout_s [7]	fc_addr[8]
ad8_dout_s [6]	fc_addr[7]
ad8_dout_s [5]	fc_addr[6]
ad8_dout_s [4]	fc_addr[5]
ad8_dout_s [3]	fc_addr[4]
ad8_dout_s [2]	fc_addr[3]
ad8_dout_s [1]	fc_addr[2]
ad8_dout_s [0]	fc_addr[1]
ad8_div_clk2pad	fc_addr[0]
fclk2pad	fc_rd_n

Xdata-SPI-FLASH Write Protect

Register:: Xdata_SPI_FLASH_Write_Protect					0xFFFF
Name	Bits	R/W	Default	Comments	Config
Reserved	7:5	R/W	0	Reserved	
Serial_stop_en	4	R/W	0	Stop 8051 serial 0: run 1: stop	
Timer2_stop_en	3	R/W	0	Stop 8051 timer2 0: run 1: stop	

IdleMode_Stop8051_en	2	R/W	0	Stop 8051 clock in idle mode 0: disable 1: enable	
Timer01_stop_en	1	R/W	0	Stop 8051 timer0 and timer1 0: run 1: stop	
XDATA_Flash_En	0	R/W	0	0: Enable xData write to Flash Function (Default) 1: Disable xData write to Flash Function	

Register:: Reserved 0xFFFF1					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:0	R/W	0	Reserved	

Register:: PWM_I2C_CLOCK_STOP 0xFFFF2					
Name	Bits	R/W	Default	Comments	Config
I2C_CKXTAL_STOP	7	R/W	0	I2c crystal clock stop control 0: run 1: stop	
PWM_CKXTAL_STOP	6	R/W	0	PWM crystal clock stop control 0: run 1: stop	
PWM5_OUTCLK_STOP	5	R/W	0	PWM5 output clock stop control 0: run 1: stop	
PWM4_OUTCLK_STOP	4	R/W	0	PWM4 output clock stop control 0: run 1: stop	
PWM3_OUTCLK_STOP	3	R/W	0	PWM3 output clock stop control 0: run 1: stop	
PWM2_OUTCLK_STOP	2	R/W	0	PWM2 output clock stop control 0: run 1: stop	
PWM1_OUTCLK_STOP	1	R/W	0	PWM1 output clock stop control 0: run 1: stop	
PWM0_OUTCLK_STOP	0	R/W	0	PWM0 output clock stop control 0: run 1: stop	

Scalar Interface

Scalar Interface Related Register

External host interface is selected by power-on latch. The internal XFR access will be auto-switched to external host interface by power-on latch, too.

Scalar's register map must reserve addresses for mapping necessary XFR when using external host interface.

Register:: SCA_INF_CONTROL 0xFFFF3					
Name	Bits	R/W	Default	Comments	Config
REG_READ_EN	7	R	0	Enable Read Action of Scalar Interface	

REG_WRITE_EN	6	R	0	Enable Write Action of Scalar Interface	
ADDR_NON_INC	5	R/W	0	1: turn-off address auto inc	
REG_BURCMD_WR	4	R/W	0	Enable burst write function, mcu will halt till action done or an interrupt triggered. *	Rport Wport
REG_BURDAT_WR	3	R/W	0	Enable burst write data to HOST_ADDR, mcu will halt till action done or an interrupt triggered *	Rport Wport
BURST_CMD_ERR	2	R	0	Burst write command error, value of SCA_INF_BWR_COUNT mismatch the length in content	
DIS_INT_RLS	1	R/W	0	1: disable the function of releasing mcu by interrupt	
PAGE_ADDR_MAP	0	R/W	0	0: Using normal XFR address to access all XFR 1: Using external page address for XFR. XFR can only be accessed by SCA_INF_ADDR, SCA_INF_DATA	

*: MCU will be released when interrupt is triggered. The bit value will maintain 1 before the operation is done. Rewriting this bit to 1 to continue the burst cmd/data write mode.

Register:: SCA_INF_ADDR 0xFFFF4					
Name	Bits	R/W	Default	Comments	Config
HOST_ADDR	7:0	R/W	0x00	Host Interface Access Address	Rport Wport

Register:: SCA_INF_DATA 0xFFFF5					
Name	Bits	R/W	Default	Comments	Config
HOST_DATA	7:0	R/W	0x00	Host Interface Access Data In/Out Continuously R/W with/without address auto-increment depends on ADDR_NON_INC	Rport Wport

Register:: SCA_INF_BWR_ADRH 0xFFFF6					
Name	Bits	R/W	Default	Comments	Config
BWR_ADRH	7:0	R/W	0x00	Burst Write Command Start Address [23:16]	Rport Wport

Register:: SCA_INF_BWR_ADRM 0xFFFF7					
Name	Bits	R/W	Default	Comments	Config
BWR_ADRM	7:0	R/W	0x00	Burst Write Command Start Address [15:8]	Rport Wport

Register:: SCA_INF_BWR_ADRL 0xFFFF8					
Name	Bits	R/W	Default	Comments	Config
BWR_ADRL	7:0	R/W	0x00	Burst Write Command Start Address [7:0]	Rport Wport

Register:: SCA_INF_BWR_COUNT_H 0xFFFF9					
Name	Bits	R/W	Default	Comments	Config
BWR_BYTE_COUNT_H	7:0	R/W	0x00	Burst Write Command Data Length. Left byte count when interrupt is asserted	Rport Wport

Register:: SCA_INF_BWR_COUNT_L 0xFFFFA					
Name	Bits	R/W	Default	Comments	Config
BWR_BYTE_COUNT_L	7:0	R/W	0x00	Burst Write Command Data Length, left byte count when interrupt is asserted	Rport Wport

Register:: SCA_INF_PERIOD 0xFFFFB					
Name	Bits	R/W	Default	Comments	Config
SCA_INF_PERIOD	7:0	R/W	0x02	Interval Between Two Command TI = SYS_PERIOD * 2 * BWR_PERIOD, it will halt mcu extra time TI in normal access and maintain the interval TI between two access in burst write	

			mode.
--	--	--	-------

*For 50MHz system clock, BWR_PERIOD can be delayed to 10.2us > 10us for special requirement of OSD register

Table Format for register burst write command format

```
BYTE code tFONT_GLOBAL[] = {
Length_A, AUTOINC_A, ADDR_A, DATA_A0, DATA_A1.....,
Length_B, AUTOINC_B, ADDR_B, DATA_B0, DATA_B1.....,
.....
-END
0x4 , 0x0, 0xA0, 01
0x6, 0x0, 0x90, 0x01, 0x02, 0x03
.....
0x0
}
```

note: AUTOINC = 0 means enable address auto-increment

Example for firmware reference:

1. OSD font table

```
// set initial address of data = 0x102030
BWR_ADRH = 0x10
BWR_ADRM = 0x20
BWR_ADRL = 0x30
// set data byte count = 0x0890
BWR_BYTE_COUNT_H = 0x08
BWR_BYTE_COUNT_L = 0x90
// set scalar's target register address = 0x58
SCA_INF_ADDR = 0x58
// enable burst data write
SCA_INF_CONTROL[3] = 1'b1
```

2. Command table

```
// set initial address of data = 0x102030
BWR_ADRH = 0x10
BWR_ADRM = 0x20
BWR_ADRL = 0x30
// set data byte count = 0x0890
BWR_BYTE_COUNT_H = 0x08
BWR_BYTE_COUNT_L = 0x90
// enable burst command write
SCA_INF_CONTROL[4] = 1'b1
```

3. Burst Write from XRAM

```
BWR_ADRH = 0x03
BWR_ADRM = 0xF9
BWR_ADRL = 0x00
Burst_Data_source_sel = Burst_Data_source_sel | 0x02 // Burst write from XRAM
// set data byte count = 0x0890
BWR_BYTE_COUNT_H = 0x08
BWR_BYTE_COUNT_L = 0x90
// enable burst command write
SCA_INF_CONTROL[1] = 1'b1 // Disable releasing mcu by interrupt
SCA_INF_CONTROL[0] = 1'b1 // Access XFR by SCA_INF_ADDR, SCA_INF_DATA
SCA_INF_CONTROL[4] = 1'b1
SCA_INF_ADDR = 0x 9F
SCA_INF_DATA = 0x 0F
SCA_INF_ADDR = 0x D3
SCA_INF_DATA = 0x 00 // Clear 0x FFF3[0], Access XFR by XFR address
```

Table Format for A25L020A close software WP command format

BYTE code t A25L020A _CloseWP[] = {

Length_A, AUTOINC_A, ADDR_A, DATA_A0, DATA_A1.....,

Length_B, AUTOINC_B, ADDR_B, DATA_B0, DATA_B1.....,

.....

_END

0x4, 0x01, 0x9F, 0x0E // Enter Page E

0x4, 0x01, 0xA0, 0x20 // 0x FF60 = 0x20

0x4, 0x01, 0xA1, 0x06 // 0x FF61 = 0x06

0x4, 0x01, 0xA0, 0x21 // 0x FF60 = 0x21

0x4, 0x01, 0xA0, 0x38 // 0x FF60 = 0x38

0x4, 0x01, 0xA1, 0x90 // 0x FF61 = 0x90

0x4, 0x00, 0xA4, 0x00, 0x28, 0x00 // 0x FF64 = 0x00, 0x FF65 = 0x28, 0x FF66 = 0x00

0x4, 0x01, 0xA0, 0x39 // 0x FF60 = 0x39

0x4, 0x01, 0xA0, 0x38 // 0x FF60 = 0x38

0x4, 0x01, 0xA1, 0x90 // 0x FF61 = 0x3B

0x4, 0x00, 0xA4, 0x00, 0x28, 0x40 // 0x FF64 = 0x00, 0x FF65 = 0x28, 0x FF66 = 0x40

0x4, 0x01, 0xA0, 0x39 // 0x FF60 = 0x39

0x0

}

note: AUTOINC = 0 means enable address auto-increment

Bank Switch

Due to only one external SPI-FLASH is used for embedded MCU, it is necessary to allocate the non-volatile memory for both program code and external data (XDATA). In default, the 0x0 ~ 0xFFFF is used for program code, and the 0x10000 ~ 0x1FFFF is used for external data. When 64K-byte FLASH is used, there is no space in FLASH reserved for XDATA. XRAM and XFR are still accessible. More than 64K-byte FLASH can be used by designer's plan. GPIO mode for bank switch is used for 128K-byte FLASH and up to 256x64K bytes FLASH is supported by XFR mode. Both of them are supported by KeilC. The start bank of XDATA is defined by XDATA_BSTART. XRAM is allocated to 0xFB00 – 0xFEFF of XDATA's Bank0. Besides, except XFR address 0xFFFFE and 0xFFFF, XFR and XRAM can be chosen if occupy only one bank of XDATA. Designer can set program address to include the whole FLASH address space without using the range reserved for XDATA to avoid partitioning the boundary in

the power of 2. The following table is an example. Program is designed to use only 0x00000 – 0x4FFF, but declare a 0x00000 – 0x7FFFF address space. Bank 5 ~ Bank 7 of program code will be empty and not programmed into FLASH. XDATA is allocated in 0x50000 – 0x7FFFF via setting of XFR.

SPI FLASH Address	Program Address	Xdata	XRAM	XFR
00000-0FFFF	Bank0, 0000-FFFF			
10000-1FFFF	Bank1, 0000-FFFF			
20000-2FFFF	Bank2, 0000-FFFF			
30000-3FFFF	Bank3, 0000-FFFF			
40000-4FFFF	Bank4, 0000-FFFF			
50000-5FFFF	Bank5, 0000-FFFF	Bank0, 0000-FFFF	F900 - FEFF	FF00-FFFF
60000-6FFFF	Bank6, 0000-FFFF	Bank1, 0000-FFFF		FF00-FFFF
70000-7FFFF	Bank7, 0000-FFFF	Bank2, 0001-FFFF		FF00-FFFF

Register::Bank_swich_control 0xFFFFC					
Name	Bits	R/W	Default	Comments	Config
Reserved	7:6	--	0	Reserved	
Burst_Data_source_sel	5	R/W	0	0: Burst data from Ext flash 1: Burst data from Int Xram	
Scalar_Addr_Remapping	4	R/W	0	Scalar Addresss remapping to Xdata, (0x00_00 ~ 0x10_FF) 0: Disable 1: Enable	
GLOBAL_XFR	3	R/W	1	1: XFR will occupy the address space of all XDATA banks. 0: only 0xFFFF will occupy the address of all XDATA banks.	
GLOBAL_XRAM	2	R/W	0	1: XRAM will occupy the address space of all XDATA banks. 0: XRAM only occupy XDATA bank 0	
SW_MODE	1	R/W	0	0: using P3.5 as A16 1: using Pbank_switch (0xFFFF)	
BANK_EN	0	R/W	0	1: Enable Bank Switching Function for program address space 0: Disable Bank Switching, program memory space is 64K byte and GLOBAL_XFR, GLOBAL_XRAM, XDATA_BSTART, XDATA_BSEL still can be used to control XDATA memory space.	

Register::XDATA_bank_start 0xFFFFD					
Name	Bits	R/W	Default	Comments	Config
XDATA_BSTART	7:0	R/W	0xff	The start bank number for XDATA access.	

Register::XDATA_bank_sel 0xFFFFE					
Name	Bits	R/W	Default	Comments	Config

XDATA_BSEL	7:0	R/W	0	First bank number for XDATA access.	
------------	-----	-----	---	-------------------------------------	--

Register::Pbank_switch					0xFFFF
Name	Bits	R/W	Default	Comments	Config
PBANK_SEL	7:0	R/W	0	Bank number for program code access.	

Pin Share Register (page 10)

GPIO Pin List

GPIO Pin List	Name	GPI	GPO <push-pull>	GPO <Open-Drain>	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register	MCU Control
31	PD.7	Y	Y	Y	Y			Page10 , 0xA0	0xFF77
32	PD.6	Y	Y	Y	Y			Page10 , 0xA1	0xFF78
33	PD.5	Y	Y	Y	Y			Page10 , 0xA2	0xFF79
34	PD.4	Y	Y	Y	Y			Page10 , 0xA3	0xFF7A
35	PD.3	Y	Y	Y	Y			Page10 , 0xA4	0xFF7B
36	PD.2	Y	Y	Y	Y			Page10 , 0xA5	0xFF7C
37	PD.1	Y	Y	Y	Y			Page10 , 0xA6	0xFF7D
39	PD.0	Y	Y	Y			Y	Page10 , 0xA7	0xFF7E
40	PC.4	Y	Y	Y			Y	Page10 , 0xA8	0xFFA4
41	PB.7	Y	Y	Y			Y	Page10 , 0xA9	0xFF7F
42	PB.6	Y	Y	Y	Y			Page10 , 0xAA	0xFF89
43	PB.5	Y	Y	Y	Y			Page10 , 0xAB	0xFF8A
44	PB4	Y	Y	Y	Y			Page10 , 0xAC	0xFF8B
45	PB.3	Y	Y	Y	Y			Page10 , 0xAD	0xFF8C
46	PB.2	Y	Y	Y	Y			Page10 , 0xAE	0xFF8D
47	PB.1	Y	Y	Y	Y			Page10 , 0xAF	0xFF8E
48	PB.0	Y	Y	Y	Y			Page10 , 0xB0	0xFF8F
50	P6.0	Y	Y	Y		Y		Page10 , 0xB1	0xFFC7
51	P6.1	Y	Y	Y		Y		Page10 , 0xB2	0xFFC8
52	P6.2	Y	Y	Y		Y		Page10 , 0xD0	0xFFC9
53	P6.3	Y	Y	Y		Y		Page10 , 0xD1	0xFFCA
54	P6.4	Y	Y	Y			Y	Page10 , 0xD2	0xFFCB
55	P6.5	Y	Y	Y			Y	Page10 , 0xD3	0xFFCC
56	P6.6	Y	Y	Y			Y	Page10 , 0xD4	0xFFCD
57	P6.7	Y	Y	Y			Y	Page10 , 0xD5	0xFFCE
58	P3.0	Y	Y	Y			Y	Page10 , 0xD6	SFR Access
59	P3.1	Y	Y	Y			Y	Page10 , 0xD7	SFR Access
63	PC.3	Y	Y	Y			Y	Page10 , 0xD8	0xFFA0
64	P1.0	Y	Y	Y			Y	Page10 , 0xD9	SFR Access
65	P1.1	Y	Y	Y			Y	Page10 , 0xDA	SFR Access
66	P1.2	Y	Y	Y			Y	Page10 , 0xDB	SFR Access
67	P1.3	Y	Y	Y			Y	Page10 , 0xDC	SFR Access
68	P1.4	Y	Y	Y			Y	Page10 , 0xDD	SFR Access
69	P1.5	Y	Y	Y			Y	Page10 , 0xDE	SFR Access
70	P1.6	Y	Y	Y			Y	Page10 , 0xDF	SFR Access
71	P1.7	Y	Y	Y			Y	Page10 , 0xE0	SFR Access
72	PC.2	Y	Y	Y			Y	Page10 , 0xE1	0xFFA1
74	P9.0	Y	Y	Y	Y			Page10 , 0xE2	0xFFD8
75	P9.1	Y	Y	Y	Y			Page10 , 0xE2	0xFFD9
76	P9.2	Y	Y	Y	Y			Page10 , 0xE2	0xFFDA
77	P9.3	Y	Y	Y	Y			Page10 , 0xE2	0xFFDB
78	P9.4	Y	Y	Y	Y			Page10 , 0xE2	0xFFDC
79	PA.0	Y	Y	Y	Y			Page10 , 0xE2	0xFFDD
80	PA.1	Y	Y	Y	Y			Page10 , 0xE2	0xFFDE
81	PA.2	Y	Y	Y	Y			Page10 , 0xE2	0xFFDF
82	PA.3	Y	Y	Y	Y			Page10 , 0xE2	0FFE0
83	PA.4	Y	Y	Y	Y			Page10 , 0xE2	0FFE1

Note: Pin 74~Pin 83 (GPI,GPO,GPIO) can not work when power saving & power Down.

Please don't use Pin 74~Pin 83 for power status detect function.

(Power Saving CR[01] Bit1 Enable, Power Down CR[01] Bit2 Enable)



GPIO Pin List	Name	GPI	GPO <push-pull>	GPO <Open-Drain>	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register	MCU Control
96	P5.2	Y	Y	Y	Y			Page10 , 0xE4	0xFFC1
97	P5.3	Y	Y	Y	Y			Page10 , 0xE5	0xFFC2
98	P5.4	Y	Y	Y	Y			Page10 , 0xE6	0xFFC3
99	P5.5	Y	Y	Y	Y			Page10 , 0xE7	0xFFC4
100	P5.6	Y	Y	Y			Y	Page10 , 0xE8	0xFFC5
101	P5.7	Y	Y	Y			Y	Page10 , 0xE9	0xFFC6
102	P7.6	Y	Y	Y			Y	Page10 , 0xEA	0xFFD5
103	P7.5	Y	Y	Y			Y	Page10 , 0xEB	0xFFD4
104	P7.4	Y	Y	Y			Y	Page10 , 0xEC	0xFFD3
105	P8.0	Y	Y	Y			Y	Page10 , 0xED	0xFFD6
108	P8.1	Y	Y	Y			Y	Page10 , 0xEE	0xFFD7
109	P3.2	Y	Y	Y			Y	Page10 , 0xEF	SFR Access
110	P3.3	Y	Y	Y			Y	Page10 , 0xF0	SFR Access
111	P3.4	Y	Y	Y			Y	Page10 , 0xF1	SFR Access
112	P3.5	Y	Y	Y			Y	Page10 , 0xF2	SFR Access
113	P3.6	Y	Y	Y			Y	Page10 , 0xF3	SFR Access
114	P3.7	Y	Y	Y			Y	Page10 , 0xF4	SFR Access
119	PC.1	N	Y	Y			Y	Page10 , 0xF5	0xFFA2
121	P7.3	Y	Y	Y			Y	Page10 , 0xF6	0xFFD2
122	P7.2	Y	Y	Y			Y	Page10 , 0xF7	0xFFD1
123	P7.1	Y	Y	Y			Y	Page10 , 0xF8	0xFFD0
124	P7.0	Y	Y	Y			Y	Page10 , 0xF9	0xFFCF
126	PC.0	Y	Y	Y		Y		Page10 , 0xFA	0xFFA3

PWM Pin List

GPIO Pin List	Name	(Push-pull)	PWM (Open-drain)	3.3V Tolerance	5V Tolerance	5V Tolerance (When Power Off)	Pin Share Register
39	PWM0	Y	Y			Y	Page10 , 0xA7
44	PWM5	Y	Y	Y			Page10 , 0xAC
48	PWM0	Y	Y	Y			Page10 , 0xB0
54	PWM4	Y	Y			Y	Page10 , 0xD2
55	PWM1	Y	Y			Y	Page10 , 0xD3
55	PWM5	Y	Y			Y	Page10 , 0xD3
63	PWM2	Y	Y			Y	Page10 , 0xD8
64	PWM0	Y	Y			Y	Page10 , 0xD9
64	PWM3	Y	Y			Y	Page10 , 0xD9
65	PWM1	Y	Y			Y	Page10 , 0xDA
68	PWM0	Y	Y			Y	Page10 , 0xDD
69	PWM2	Y	Y			Y	Page10 , 0xDE
70	PWM4	Y	Y			Y	Page10 , 0xDF
71	PWM1	Y	Y			Y	Page10 , 0xE0
71	PWM5	Y	Y			Y	Page10 , 0xE0
72	PWM3	Y	Y			Y	Page10 , 0xE1
96	PWM0	Y	Y	Y			Page10 , 0xE4
97	PWM1	Y	Y	Y			Page10 , 0xE5
98	PWM2	Y	Y	Y			Page10 , 0xE6
99	PWM3	Y	Y	Y			Page10 , 0xE7
100	PWM4	Y	Y			Y	Page10 , 0xE8
101	PWM5	Y	Y			Y	Page10 , 0xE9
102	PWM0	Y	Y			Y	Page10 , 0xEA
103	PWM1	Y	Y			Y	Page10 , 0xEB
109	PWM2	Y	Y			Y	Page10 , 0xE8
114	PWM1	Y	Y			Y	Page10 , 0xED
119	PWM4	Y	Y			Y	Page10 , 0xEF
119	PWM5	Y	Y			Y	Page10 , 0xEF
126	PWM0	Y	Y	Y			Page10 , 0xFA
126	PWM1	Y	Y	Y			Page10 , 0xFA

TCON Pin List

Pin 31	TCON[6]			
Pin 32	TCON[7]			
Pin 33	TCON[8]			
Pin 34	TCON[9]			
Pin 35	TCON[0]			
Pin 36	TCON[10]			
Pin 37	TCON[4]			
Pin 39	TCON[14]			
Pin 41	TCON[5]			
Pin 55	TCON[0]	TCON[5]		
Pin 56	TCON[1]	TCON[4]		
Pin 57	TCON[9]	TCON[11]		
Pin 58	TCON[7]	TCON[10]		
Pin 59	TCON[3]	TCON[5]		
Pin 63	TCON[1]	TCON[8]	TCON[16]	
Pin 64	TCON[0]	TCON[6]	TCON[7]	TCON[15]
Pin 65	TCON[1]	TCON[7]		
Pin 66	TCON[2]	TCON[4]		
Pin 67	TCON[5]	TCON[9]	TCON[12]	
Pin 68	TCON[3]	TCON[13]	TCON[14]	TCON[15]
Pin 69	TCON[3]	TCON[7]		
Pin 70	TCON[9]	TCON[11]		
Pin 71	TCON[8]	TCON[10]		
Pin 72	TCON[6]	TCON[12]		
Pin 97	TCON[S0]			
Pin 98	TCON[13]	TCON[15]		
Pin 99	TCON[0]	TCON[6]	TCON[11]	
Pin 100	TCON[3]	TCON[12]	TCON[S1]	
Pin 101	TCON[14]			
Pin 102	TCON[10]			
Pin 103	TCON[8]			
Pin 104	TCON[5]			
Pin 105	TCON[6]	TCON[9]		
Pin 108	TCON[7]			
Pin 109	TCON[3]			
Pin 110	TCON[2]	TCON[6]	TCON[7]	
Pin 111	TCON[4]	TCON[7]		
Pin 112	TCON[5]	TCON[9]		
Pin 113	TCON[1]	TCON[11]		
Pin 114	TCON[0]	TCON[13]		
Pin 126	TCON[14]			

Test Pin List

GPIO Pin List	Name	Test Pin 0	Test Pin 1	Test Pin 2	Test Pin 3
31	PD.7	Y	Y		
32	PD.6	Y	Y		
33	PD.5	Y	Y		
34	PD.4	Y	Y		
35	PD.3	Y	Y		
36	PD.2	Y	Y		
37	PD.1	Y	Y		
39	PD.0	Y	Y		
40	PC.4	Y	Y		
41	PB.7	Y	Y		
42	PB.6	Y	Y		
43	PB.5	Y	Y		
44	PB4	Y	Y		
45	PB.3	Y	Y		

GPIO Pin List	Name	Test Pin 0	Test Pin 1	Test Pin 2	Test Pin 3
46	PB.2	Y	Y		
47	PB.1	Y	Y		
48	PB.0	Y	Y		
50	P6.0	Y	Y		
51	P6.1	Y	Y		
52	P6.2	Y	Y		
53	P6.3	Y	Y		
54	P6.4	Y	Y		
55	P6.5	Y	Y		
56	P6.6	Y	Y		
57	P6.7	Y	Y		
58	P3.0	Y	Y		
59	P3.1	Y	Y		
63	PC.3	Y	Y		
64	P1.0	Y	Y		
65	P1.1	Y	Y		
66	P1.2	Y	Y		
67	P1.3	Y	Y		
68	P1.4	Y	Y		
69	P1.5	Y	Y		
70	P1.6	Y	Y		
71	P1.7	Y	Y		
72	PC.2	Y	Y		
96	P5.2			Y	Y
97	P5.3			Y	Y
98	P5.4			Y	Y
99	P5.5			Y	Y
100	P5.6			Y	Y
101	P5.7			Y	Y
102	P7.6			Y	Y
103	P7.5			Y	Y
104	P7.4			Y	Y
105	P8.0			Y	Y
108	P8.1			Y	Y
109	P3.2			Y	Y
110	P3.3			Y	Y
111	P3.4			Y	Y
112	P3.5			Y	Y
113	P3.6			Y	Y
114	P3.7			Y	Y
119	PC.1			Y	Y
121	P7.3			Y	Y
122	P7.2			Y	Y
123	P7.1			Y	Y
124	P7.0			Y	Y
126	PC.0			Y	Y

Note: Test Pins are effective only when Test Function 8E-0E[7] = 1
 (force output selected testout signal)

Register: PIN_SHARE_CTRL00 0xA0					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD7	2:0	R/W	0x00	Pin31 000: PDD7i <I> <default> 001: PDD7o <O> <push-pull> 010: PDD7o <O> <open-drain> 011: TCON[6] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL01 0xA1					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD6	2:0	R/W	0x00	Pin32 000: PDD6i <I> <default> 001: PDD6o <O> <push-pull> 010: PDD6o <O> <open-drain> 011: TCON[7] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL02 0xA2					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD5	2:0	R/W	0x00	Pin33 000: PDD5i <I> <default> 001: PDD5o <O> <push-pull> 010: PDD5o <O> <open-drain> 011: TCON[8]<O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL03 0xA3					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD4	2:0	R/W	0x00	Pin34 000: PDD4i <I> <default> 001: PDD4o <O> <push-pull> 010: PDD4o <O> <open-drain> 011: TCON[9] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL04 0xA4					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD3	2:0	R/W	0x00	Pin35 000: PDD3i <I> <default> 001: PDD3o <O> <push-pull> 010: PDD3o <O> <open-drain> 011: TCON[0] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL05 0xA5					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PDD2	2:0	R/W	0x00	Pin36 000: PDD2i <I> <default> 001: PDD2o <O> <push-pull> 010: PDD2o <O> <open-drain> 011: TCON[10] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL06 0xA6					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PDD1	3:0	R/W	0x00	Pin37 0000: PDD1i <I> <default> 0001: PDD1o <O> <push-pull> 0010: PDD1o <O> <open-drain> 0011: TCON[4] <O> 0100: FIELD <O> 0101: L_R <O> 0110: TEST_PIN0 <O> 0111: TEST_PIN1 <O> 1000 DUMMY <O> Effective only if Page10 0xB9[6]=1	

Register: PIN_SHARE_CTRL07 0xA7					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PDD0	3:0	R/W	0x00	Pin39 0000: PDD0i <I> <default> 0001: PDD0o <O> <push-pull> 0010: PDD0o <O> <open-drain> 0011: TCON[14] <O> 0011: PWM0 <O> <push-pull> 0100: PWM0 <O> <open-drain> 0101: TCON[14] <O> 0110: TEST_PIN0 <O>	

				0111: TEST_PIN1 <O> 1000: DUMMY <O> Effective only if Page10 0xB9[6]=1	
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Register: PIN_SHARE_CTRL08 0xA8					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PCD0	2:0	R/W	0x00	Pin40 000: PCD4i <I> <default> 001: PCD4o <O> <push-pull> 010: PCD4o <O> <open-drain> 011: VCLK <I> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O>	

Register: PIN_SHARE_CTRL09 0xA9					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PBD7	2:0	R/W	0x00	Pin41 (PAD_V8_7) 000: PBD7i <I> <default> 001: PBD7o <O> <open-drain> 010: PBD7o <O> <push-pull> 001: PBD7o <O> <push-pull> 010: PBD7o <O> <open-drain> 011: TCON[5] <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL0A 0xAA					
Name	Bits	Read/ Write	Reset State	Comments	Config
PBD5_6	7:6	R/W	0x00	Pin42 (PAD_V8_6) 00: normal output(refer 0xAA[2:0]) <default> 01: IICSCL <IO> <open-drain> 10: IICSCL_AUX <IO> <open-drain> Pin43 (PAD_V8_5) 00: normal output (refer 0xAB[2:0]) <default> 01: IICSDA <IO> <open-drain> 10: IICSDA_AUX <IO> <open-drain> IIC_AUX effective only if Page10 0xBD[1] = 1	
Reserved	5:3	R/W	0x00	Reserved	
PBD6	2:0	R/W	0x00	Pin42 (PAD_V8_6) 000: PBD6i <I> <default> 001: PBD6o <O> <open-drain> 010: PBD6o <O> <push-pull> 001: PBD6o <O> <push-pull> 010: PBD6o <O> <open-drain> 011: TEST_PIN0 <O> 100: TEST_PIN1 <O> 101: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL0B 0xAB					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PBD5	2:0	R/W	0x00	Pin43 (PAD_V8_5) 000: PBD5i <I> <default> 001: PBD5o <O> <open drain> 010: PBD5o <O> <push pull> 001: PBD5o <O> <push-pull> 010: PBD5o <O> <open-drain> 011: TEST_PIN0 <O> 100: TEST_PIN1 <O> 101: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL0C 0xAC					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PBD4	3:0	R/W	0x00	Pin44 (PAD_V8_4) 0000: PBD4i <I> <default> 001: PBD4o <O> <open drain> 010: PBD4o <O> <push pull> 0001: PBD4o <O> <push-pull> 0010: PBD4o <O> <open-drain> 0011: WS <O> 0100: SPDIF3 <O> 0101: PWM5 <O> <push-pull> 0110: PWM5 <O> <open-drain> 0111: TEST_PIN0 <O> 1000: TEST_PIN1 <O> 1001: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL0D 0xAD					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PBD3	2:0	R/W	0x00	Pin45 (PAD_V8_3) 000: PBD3i <I> <default> 001: PBD3o <O> <open drain> 010: PBD3o <O> <push pull> 001: PBD3o <O> <push-pull> 010: PBD3o <O> <open-drain> 011: SCK <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL0E 0xAE					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
PBD2	2:0	R/W	0x00	Pin46 (PAD_V8_2)	

				000: PBD2i <I> <default> 001: PBD2o <O> <open drain> 010: PBD2o <O> <push pull> 001: PBD2o <O> <push-pull> 010: PBD2o <O> <open-drain> 011: MCK <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	
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Register: PIN_SHARE_CTRL0F 0xAF					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PBD1	3:1	R/W	0x00	Pin47 (PAD_V8_1) 000: PBD1i <I> <default> 001: PBD1o <O> <open drain> 010: PBD1o <O> <push pull> 001: PBD1o <O> <push-pull> 010: PBD1o <O> <open-drain> 011: SD0 <O> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	
PIN58_59	0	R/W	0	PIN58_59_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	

Register: PIN_SHARE_CTRL10 0xB0					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PBD0	3:0	R/W	0x00	Pin48 (PAD_V8_0) 0000: PBD0i <I> <default> 001: PBD0o <O> <open drain> 010: PBD0o <O> <push pull> 0001: PBD0o <O> <push-pull> 0010: PBD0o <O> <open-drain> 0011: PWM0 <O> <push-pull> 0100: PWM0 <O> <open-drain> 0101: TEST_PIN0 <O> 0110: TEST_PIN1 <O> 0111: DUMMY <O> Effective only if CR1F[5:4]=2'b10 Page10 0xB9[5:4]=2'b10	

Register: PIN_SHARE_CTRL11 0xB1					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
P6D0	2:0	R/W	0x00	Pin50 (PAD_ADCA0) 000: P6D0i <I> <default> 001: P6D0o <O> <open drain>	

				010: P6D0o <O> <push-pull> 001: P6D0o <O> <push-pull> 010: P6D0o <O> <open-drain> 011: ADCA0(8Bit) <I> 100: Reserved 101: VCLK <I> 100: VCLK <I> 101: TEST_PIN0 <O> 110: TEST_PIN1 <O> 111: DUMMY <O>	
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Register: PIN_SHARE_CTRL12 0xB2					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:5	R/W	0x00	Reserved	
P6D1	4:2	R/W	0x00	Pin51 (PAD_ADCA1) 000: P6D1i <I> <default> 001: P6D1o <O> <open-drain> 010: P6D1o <O> <push-pull> 001: P6D1o <O> <push-pull> 010: P6D1o <O> <open-drain> 011: ADCA1(8Bit) <I> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O>	
PIN121_122	1	R/W	0	PIN121_122_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	
PIN123_124	0	R/W	0	PIN123_124_Low_Leak 0: normal mode (47K pull up with 4.3~4.4v pin level) 1: low leak mode with duty penalty. (47K pull up with over 4.5v pin level)	

Register: PIN_DRIVING_CTRL1 0xB3					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN50_53	7	R/W	0	Driving Current Control – Pin50~53 0: Low 1: High	
PIN54_57	6	R/W	0	Driving Current Control – Pin54~57 0: Low 1: High	
PIN58_59	5	R/W	0	Driving Current Control – Pin58~59 0: Low (8mA) 1: High (12mA)	
PIN63_64	4	R/W	0	Driving Current Control – Pin64~67 0: Low 1: High	
Reserved	3:0	R/W	0x00	Reserved	

Register: PIN_DRIVING_CTRL2 0xB4					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN39_40	7	R/W	0	Driving Current Control – Pin39~40 0: Low 1: High	
PIN41_48	6	R/W	0	Driving Current Control – Pin41~48	

				0: Low 1: High	
PIN110_114	5	R/W	0	Driving Current Control– Pin110~114 0: Low 1: High	
PIN115	4	R/W	0	SPI_SCLK, Driving Current Control – Pin115 0: High (4mA) 1: Low (2mA)	
PIN121_124	3	R/W	0	Driving Current Control– Pin121~124-119-126 0: Low (8mA at pin121-124) 1: High (12mA at pin121-124)	
Pin96_109 Pin100_109	2	R/W	0	Driving Current Control – Pin96~109 Pin100~109 0: Low (4mA) 1: High (8mA)	
Pin74_83	1	R/W	0	Driving Current Control – Pin74~83、Pin86~95 Pin86~99 Active when CR_0x8C_00[1:0] select to TTL Not effective when LVDS or mLVDs 0: Low (4mA x1) 1: High (8mA x2)	
Pin65_72	0	R/W	0	Driving Current Control – Pin65~72 0: Low (4mA) 1: High (8mA)	

Register: PIN_PULLUP_CTRL3 0xB5					
Name	Bits	Read/ Write	Reset State	Comments	Config
PIN50_53	7	R/W	0	Pull Up Control – Pin50~53 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN54_57	6	R/W	0	Pull Up Control – Pin54~57 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN58_59	5	R/W	0	Pull Up Control – Pin58~59 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN64_126	4	R/W	0	Pull Up Control – Pin63~64~119~126 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN110_114	3	R/W	0	Pull Up Control – Pin110~114 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN121_124	2	R/W	0	Pull Up Control – Pin121~124 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN41_48 Reserved	4	R/W	0	Pull Up Control06 – Pin41~48 0: Disable 1: Enable (active only in GPI or open drain case) Reserved	
PIN39_40	0	R/W	0	Pull Up Control – Pin39~40 0: Disable 1: Enable (active only in GPI or open-drain case)	

Register: PIN_PULLUP_CTRL6 0xB6					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7	R/W	0	Reserved	

PIN37	6	R/W	0	Pull Up Control– Pin37 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN36	5	R/W	0	Pull Up Control – Pin36 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN35	4	R/W	0	Pull Up Control– Pin35 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN34	3	R/W	0	Pull Up Control– Pin34 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN33	2	R/W	0	Pull Up Control – Pin33 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN32	1	R/W	0	Pull Up Control – Pin32 0: Disable 1: Enable (active only in GPI or open-drain case)	
PIN31	0	R/W	0	Pull Up Control – Pin31 0: Disable 1: Enable (active only in GPI or open-drain case)	

0xB7~0xB8 reserved

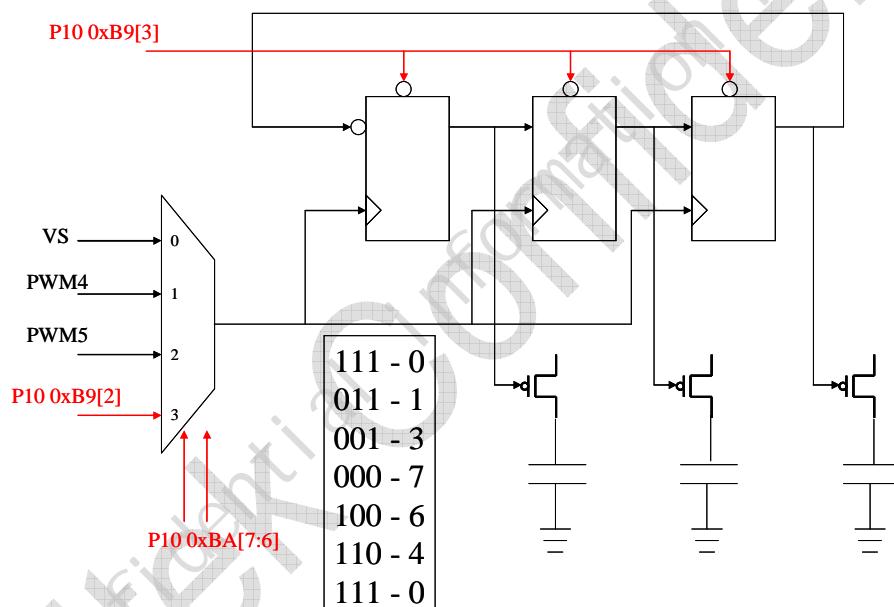
Register: PIN_SHARE_CTRL16 PIN_DRIVING_CTRL3 0xB9					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN116_118	7	R/W	0	Driving Current Control – Pin116~118 0: High (4mA) 1: Low (2mA)	
Reserved	6	R/W	0	Reserved	
P41_48_SEL	5:4	R/W	0x00	Pin41~48 function selection 00: Reserved 01: AUDIO 10: Normal function, refer to Pin Share Part	
Xtal_SPREAD_EN	3	R/W	0	Xtal Spread Spectrum Enable 0: Disable, reset capacitor select 1: Enable	
Xtal_SPREAD_MANUAL_SWITCH	2	R/W	0	Xtal Spread Spectrum Source Manual Switch 0: No Change 1: Switch to different frequency User must set “0: No Change” before “1: Switch to different frequency” (Only take effect when Page 10 CRCA[7:6] 0xBA[7:6] = 2'b11)	
Reserved	1:0	R/W	0x00	Reserved	

Register: DVI_CTRL_OUT_SEL PIN_TYPE_CONFIG0 0xBA					
Name	Bits	Read/Write	Reset State	Comments	Config
Xtal_SPREAD_SOURCE_SEL	7:6	R/W	0x00	Xtal Spread Spectrum Source Select 00: Reference to VS 01: Reference to PWM4 10: Reference to PWM5 11: Adjust by FW (reference to Page 10 CRB9[2])	
PCD3	5	R/W	0	DVI CTRL OUT1 (Pin63) output enable 0: Disable (ref. original Pin63 pin share)	

				1: Enable	
P7D5	4	R/W	0	DVI CTRL OUT2 (Pin103) output enable 0: Disable (ref. original Pin103 pin share) 1: Enable	
DVI_CTRL_OUT1	3:2	R/W	0x00	DVI CTRL OUT1 select 00:CTRL0, 01:CTRL1, 10:CTRL2, 11:CTRL3	
DVI_CTRL_OUT2	1:0	R/W	0x00	DVI CTRL OUT2 select 00:CTRL0, 01:CTRL1, 10:CTRL2, 11:CTRL3	

CRBA[7:6] is used to choose switch reference source, the default capacitor setting is 111(minimum offset). Once VS / PWM signal latched, capacitor will change (111→011→001....,000 is maximum offset).

In manual switch mode, user set CRB9[2] will change the capacitor only one time. If user want to change capacitor again, must set “0: No Change” and then set “1: Switch to different frequency”.



Register: PIN_PULLUP_CTRL4 0xBB					
Name	Bits	Read/Write	Reset State	Comments	Config
PIN102_103	7	R/W	0	Pull Down Control – Pin102~103 0: Disable 1: Enable	
PIN100_101	6	R/W	0	Pull Up Control – Pin100~101 0: Disable 1: Enable	
PIN98_99 Reserved	5	R/W	0	Pull Down Control – Pin98~99 0: Disable 1: Enable Reserved	
PIN96_97 Reserved	4	R/W	0	Pull Up Control – Pin96~97 0: Disable 1: Enable Reserved	

PIN71_72	3	R/W	0	Pull Down Control– Pin71~72 0: Disable 1: Enable	
PIN69_70	2	R/W	0	Pull Up Control – Pin69~70 0: Disable 1: Enable	
PIN67_68	1	R/W	0	Pull Down Control – Pin67~68 0: Disable 1: Enable	
PIN65_66	0	R/W	0	Pull Up Control – Pin65~66 0: Disable 1: Enable	

Register: PIN_PULLUP_CTRL5 0xBC					
Name	Bits	Read/Write	Reset State	Comments	Config
DDC1_SCHMITT_EN	7	R/W	1	DDC1 (pin58,pin59) schmitt trigger enable 0: Disable 1: Enable	
DDC2_SCHMITT_EN	6	R/W	1	DDC2 (pin123,pin124) schmitt trigger enable 0: Disable 1: Enable	
DDC3_SCHMITT_EN	5	R/W	1	DDC3 (pin121,pin122) schmitt trigger enable 0: Disable 1: Enable	
PIN116_117_118	4	R/W	0	Slew Rate Control – Pin116_117_118 0:Fast 1:Slow	
PIN115	3	R/W	0	Slew Rate Control – SPI_SCLK 0: Fast 1; Slow	
Pin116_117_PU	2	R/W	1	Pull Up for Pin 116 & 117 0: Disable 1: Enable	
PIN108_109	1	R/W	0	Pull Down Control – Pin108~109 0: Disable 1: Enable	
PIN104_105	0	R/W	0	Pull Up Control – Pin104~105 0: Disable 1: Enable	

Register: IICAUX_DDC2P_CTRL0 0xBD					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	R/W	0	Reserved	
IIC_AUX_EN	1	R/W	0	Switch IIC_AUX to Pinshare 0: Disable <default> 1: Enable	
DDC2P_EN	0	R/W	0	Switch DDC2P for Pinshare 0: Disable <default> 1: Enable	

Register: PIN_SCHMITT_CTRL0 0xBE					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	R/W	0	Reserved	
IIC_SCHMITT_1	3	R/W	0	IIC SCHMITT trigger for pin56 , pin57	

				0: disable 1: enable	
IIC_SCHMITT_2	2	R/W	0	IIC SCHMITT trigger for pin66 , pin67 0: disable 1: enable	
IIC_SCHMITT_3	1	R/W	0	IIC SCHMITT trigger for pin69 , pin70 0: disable 1: enable	
IIC_SCHMITT_4	0	R/W	0	IIC SCHMITT trigger for pin103 , pin104 0: disable 1: enable	

0xBF reserved

SDRAM control

Register: PIN_SHARE_SDRAM_CTRL0 0xC0					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	reserved to 0	
SDRAM_en	2	R/W	0	SDRAM enable 0: no SDRAM <default> 1: MCM SDRAM	
SDRAM_size	1:0	R/W	0x3	SDRAM size 00: 1Mx16 SDRAM 01: 1Mx32 SDRAM 10: Reserved 11: 2Mx32 SDRAM <default>	

Register: PIN_SHARE_SDRAM_CTRL1 0xC1					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	reserved to 0	
DQM3	3	R/W	0	SDR DQM3 (UDQM) – Data Input/Output Mask 0: non-active 1: active	
DQM2	2	R/W	0	SDR DQM2 (LDQM) – Data Input/Output Mask 0: non-active 1: active	
DQM1	1	R/W	0	SDR DQM1 – Data Input/Output Mask 0: non-active 1: active	
DQM0	0	R/W	0	SDR DQM0 – Data Input/Output Mask 0: non-active 1: active	

Register: PIN_DRIVING_SDRAM_CTRL2 0xC2					
Name	Bits	Read/ Write	Reset State	Comments	Config
E2CTRL13_7	7	R/W	0	Schmitt Trigger Control – SDR CLK 0: On 1: Off	
E2CTRL13_6	6	R/W	0	Slew Rate Control – SDR CLK 0: Fast 1: Slow	
E2CTRL13_5	5	R/W	0	Driving Current Control – SDR CLK	

				0: Low 1: High	
E2CTRL13_4	4	R/W	0	reserved to 0	
E2CTRL13_3	3	R/W	0	Schmitt Trigger Control – SDR Control 0: On 1: Off	
E2CTRL13_2	2	R/W	0	Slew Rate Control – SDR Control 0: Fast 1: Slow	
E2CTRL13_1	1	R/W	0	Driving Current Control – SDR Control 0: Low 1: High	
E2CTRL13_0	0	R/W	0	reserved to 0	

Register: PIN_DRIVING_SDRAM_CTRL3 0xC3					
Name	Bits	Read/ Write	Reset State	Comments	Config
E2CTRL14_7	7	R/W	0	Schmitt Trigger Control – DQ31~24 (DQ8~11) 0: On 1: Off	
E2CTRL14_6	6	R/W	0	Slew Rate Control – DQ31~24 (DQ8~11) 0: Fast 1: Slow	
E2CTRL14_5	5	R/W	0	Driving Current Control – DQ31~24 (DQ8~11) 0: Low 1: High	
E2CTRL14_4	4	R/W	0	reserved to 0	
E2CTRL14_3	3	R/W	0	Schmitt Trigger Control – DQ23~16 (DQ4~7) 0: On 1: Off	
E2CTRL14_2	2	R/W	0	Slew Rate Control – DQ23~16 (DQ4~7) 0: Fast 1: Slow	
E2CTRL14_1	1	R/W	0	Driving Current Control – DQ23~16 (DQ4~7) 0: Low 1: High	
E2CTRL14_0	0	R/W	0	reserved to 0	

Register: PIN_DRIVING_SDRAM_CTRL4 0xC4					
Name	Bits	Read/ Write	Reset State	Comments	Config
E2CTRL15_7	7	R/W	0	Schmitt Trigger Control – DQ15~8 (DQ12~15) 0: On 1: Off	
E2CTRL15_6	6	R/W	0	Slew Rate Control – DQ15~8 (DQ12~15) 0: Fast 1: Slow	
E2CTRL15_5	5	R/W	0	Driving Current Control – DQ15~8 (DQ12~15) 0: Low 1: High	
E2CTRL15_4	4	R/W	0	reserved to 0	
E2CTRL15_3	3	R/W	0	Schmitt Trigger Control – DQ7~0 (DQ0~3) 0: On 1: Off	
E2CTRL15_2	2	R/W	0	Slew Rate Control – DQ7~0 (DQ0~3) 0: Fast 1: Slow	
E2CTRL15_1	1	R/W	0	Driving Current Control – DQ7~0 (DQ0~3)	

				0: Low 1: High	
E2CTRL15_0	0	R/W	0	reserved to 0	

Register: PIN_DRIVING_SDRAM_CTRL5 0xC5					
Name	Bits	Read/ Write	Reset State	Comments	Config
E2CTRL16_7	7	R/W	0	Schmitt Trigger Control – SDR Address 0: On 1: Off	
E2CTRL16_6	6	R/W	0	Slew Rate Control – SDR Address 0: Fast 1: Slow	
E2CTRL16_5	5	R/W	0	Driving Current Control – SDR Address 0: Low 1: High	
E2CTRL16_4	4	R/W	0	reserved to 0	
E2CTRL16_3	3	R/W	0	Schmitt Trigger Control – SDR DQM 0: On 1: Off	
E2CTRL16_2	2	R/W	0	Slew Rate Control – SDR DQM 0: Fast 1: Slow	
E2CTRL16_1	1	R/W	0	Driving Current Control – SDR DQM 0: Low 1: High	
E2CTRL16_0	0	R/W	0	reserved to 0	

0xC6~0xCF reserved

Register: PIN_SHARE_CTRL13 0xD0					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
P6D2	2:0	R/W	0x00	Pin52 (PAD_ADCA2) 000: P6D2i <I> <default> 001: P6D2o <O> <open-drain> 010: P6D2o <O> <push-pull> 001: P6D2o <O> <push-pull> 010: P6D2o <O> <open-drain> 011: ADCA2(8Bit) <I> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O> 110: DUMMY <O>	

Register: PIN_SHARE_CTRL14 0xD1					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
P6D3	2:0	R/W	0x00	Pin53 (PAD_ADCA3) 000: P6D3i <I> <default> 001: P6D3o <O> <open-drain> 010: P6D3o <O> <push-pull> 001: P6D3o <O> <push-pull> 010: P6D3o <O> <open-drain> 011: ADCA3(8Bit) <I> 100: TEST_PIN0 <O> 101: TEST_PIN1 <O>	

			110: DUMMY <O>	
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Register: PIN_SHARE_CTRL15 0xD2					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
P6D4	2:0	R/W	0x00	Pin54 (PAD_ADCA4) 000: P6D4i <I> <default> 001: P6D4o <O> <open-drain> 010: P6D4o <O> <push-pull> 011: PWM4 <O> <open-drain> 001: P6D4o <O> <push-pull> 010: P6D4o <O> <open-drain> 011: PWM4 <O> <push-pull> 100: PWM4 <O> <open-drain> 101: TEST_PIN0 <O> 110: TEST_PIN1 <O> 111: DUMMY <O>	

Register: PIN_SHARE_CTRL16 0xD3					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P6D5	3:0	R/W	0x00	Pin55 (PAD_ADCB0) 0000: P6D5i <I> <default> 0001: P6D5o <O> <open-drain> 0010: P6D5o <O> <push-pull> 0011: PWM1 <O> <open-drain> 0100: PWM1 <O> <push-pull> 0101: PWM5 <O> <push-pull> 0110: TCON[0] <O> 0111: TCON[5] <O> 0001: P6D5o <O> <push-pull> 0010: P6D5o <O> <open-drain> 0011: PWM1 <O> <push-pull> 0100: PWM1 <O> <open-drain> 0101: PWM5 <O> <push-pull> 0110: PWM5 <O> <open-drain> 0111: TCON[0] <O> 1000: TCON[5] <O> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O>	

Register: PIN_SHARE_CTRL17 0xD4					
Name	Bits	Read/ Write	Reset State	Comments	Config
P6D6_7	7:6	R/W	0x00	Pin56 (PAD_ADCB1) 00: normal output(refer 0xD4[2:0]) <default> 01: IICSCL <IO> <open-drain> 10: IICSCL_AUX <IO> <open-drain> Pin57 (PAD_ADCB2) 00: normal output(refer 0xD5[2:0]) <default> 01: IICSDA <IO> <open-drain> 10: IICSDA_AUX <IO> <open-drain> IIC_AUX effective only if Page10 0xBD[1] = 1	
Reserved	5:3	R/W	0x00	Reserved	
P6D6	2:0	R/W	0x00	Pin56 (PAD_ADCB1)	

				000: P6D6i <I> <default> 001: P6D6o <O> < push-pull> 010: P6D6o <O> <open-drain > 011: Reserved 100: TCON[1] <O> 101: TCON[4] <O> 011: TCON[1] <O> 100: TCON[4] <O> 101: TEST_PIN0 <O> 110: TEST_PIN1 <O> 111: DUMMY <O>	
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Register: PIN_SHARE_CTRL18 0xD5					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
P6D7	2:0	R/W	0x00	Pin57 (PAD_ADCB2) 000: P6D7i <I> <default> 001: P6D7o <O> < push-pull> 010: P6D7o <O> <open-drain > 011: Reserved 100: TCON[9] <O> 101: TCON[11] <O> 011: TCON[9] <O> 100: TCON[11] <O> 101: TEST_PIN0 <O> 110: TEST_PIN1 <O> 111: DUMMY <O>	

Register:: PIN_SHARE_CTRL19 0xD6					
Name	Bits	Read/ Write	Reset State	Comments	Config
DDC1	7	R/W	0	Pin58 (PAD_DDCSCL1) 0: DDCSCL1 <IO> <open-drain> <default> 1: normal output(refer 0xD6[4:1]) Pin59 (PAD_DDCSDA1) 0: DDCSDA1 <IO> <open-drain> <default> 1: normal output(refer 0xD7[3:0])	
Reserved	6:5	R/W	0x00	Reserved	
DDCSCL1	4:1	R/W	0x00	Pin58 0000: P3D0i <I> 0001: P3D0o <O> <open drain> 010: P3D0o <O> <push pull> 0001: P3D0o <O> <push-pull> 0010: P3D0o <O> <open-drain> 0011: Reserved 0100: TCON[7] <O> 0101: TCON[10] <O> 0110: TEST_PIN0 <O> 0111: TEST_PIN1 <O> 1000: DUMMY <O>	
USB_DDC1_EN	0	R/W	0	When (Page 10 , 0xA2 0xD6[0] = 1) && (pin55 = 1), disable ddc function of pin58, 59 and swap to pin52, 53.	

Register:: PIN_SHARE_CTRL1A 0xD7					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	

DDCSDA1	3:0	R/W	0x00	Pin59 0000: P3D1i <I> 0001: P3D1o <O> <open drain> 0110: P3D1o <O> <push-pull> 0001: P3D1o <O> <push-pull> 0010: P3D1o <O> <open-drain> 0011: Reserved 0100: TCON[3] <O> 0101: TCON[5] <O> 0110: TEST_PIN0 <O> 0111: TEST_PIN1 <O> 1000: DUMMY <O>	
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Register: PIN_SHARE_CTRL1B 0xD8					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PCD3	3:0	R/W	0x00	Pin63 (PAD_GPIO63) 0000: PCD3i <I> <default> 0001: PCD3o <O> <open drain> 0010: PCD3o <O> <push-pull> 0001: PCD3o <O> <push-pull> 0010: PCD3o <O> <open-drain> 0011: PWM2 <O> <push-pull> 0100: TCON[1] <O> 0101: TCON[8] <O> 0110: PWM2 <O> <open drain> 0111: INT0 <I> 0100: PWM2 <O> <open-drain> 0101: TCON[1] <O> 0110: TCON[8] <O> 0111: TCON[16] <O> 1000: INT0 <I> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O> Effective only if Page 10 0xBA[5] = 0	

Register: PIN_SHARE_CTRL1C 0xD9					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:5	R/W	0x00	Reserved	
P1D0	4:0	R/W	0x00	Pin64 (PAD_TCON0) 00000: P1D0i <I> <default> 00001: P1D0o <O> <open drain> 0010: P1D0o <O> <push-pull> 0011: T2 <I> 0100: SD0 <O> 0101: SPDIF0 <O> 0110: TCON[0] <O> 0111: PWM0 <O> <push-pull> 1000: TCON[7] <O> 1001: PWM0 <O> <open drain> 1010: INT1 <I> 1011: TCON[6] <O> 1100: PWM3 <O> <push-pull> 1101: PWM3 <O> <open drain> 00001: P1D0o <O> <push-pull>	

				00010: P1D0o <O> <open-drain> 00011: PWM0 <O> <push-pull> 00100: PWM0 <O> <open-drain> 00101: PWM3 <O> <push-pull> 00110: PWM3 <O> <open-drain> 00111: TCON[0] <O> 01000: TCON[6] <O> 01001: TCON[7] <O> 01010: TCON[15] <O> 01011: SD0 <O> 01100: SPDIF0 <O> 01101: T2 <I> 01110: INT1 <I> 01111: TEST_PIN0 <O> 10000: TEST_PIN1 <O> 10001: DUMMY <O>	
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Register: PIN_SHARE_CTRL1D 0xDA					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P1D1	3:0	R/W	0x00	Pin65 (PAD_TCON1) 0000: P1D1i <I> 0001: P1D1o <O> <push-pull> 0010: PWM1 <O> <push-pull> 0011: T2EX <I> 0100: TCON[1] <O> 0101: TCON[7] <O> 0110: WS <O> 0111: PWM1 <O> <open-drain> 0010: P1D1o <O> <open-drain> 0011: PWM1 <O> <push-pull> 0100: PWM1 <O> <open-drain> 0101: TCON[1] <O> 0110: TCON[7] <O> 0111: T2EX <I> 1000: WS <O> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O>	

Register: PIN_SHARE_CTRL1E 0xDB					
Name	Bits	Read/ Write	Reset State	Comments	Config
P1D2_3	7	R/W	0	Pin66 (PAD_TCON2) 0: normal output(refer 0xDB[3:0]) <default> 1: DDCSCL2P <IO> <open-drain> Pin67 (PAD_TCON5) 0: normal output(refer 0xDC[3:0]) <default> 1: DDCSDA2P <IO> <open-drain> DDC2P effective only if Page10 0xBD[0] = 1	
Reserved	6:4	R/W	0x00	Reserved	
P1D2	3:0	R/W	0x00	Pin66 (PAD_TCON2) 0000: P1D2i <I> 0001: P1D2o <O> <push-pull> 0010: P1D2o <O> <open-drain> 0011: CLKO <O> 0100: SCK <O> 0101: TCON[2] <O>	

				0110: TCON[4] <O> 0111: TCON[16] <O> 1000: TEST_PIN0 <O> 1001: TEST_PIN1 <O> 1010: DUMMY <O>	
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Register: PIN_SHARE_CTRL1F 0xDC					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P1D3	3:0	R/W	0x00	Pin67 (PAD_TCON5) 0000: P1D3i <I> 0001: P1D3o <O> <push-pull> 0010: P1D3o <O> <open-drain> 0011: MCK <O> 0100: TCON[5] <O> 0101: TCON[9] <O> 0110: TCON[12] <O> 0111: TEST_PIN0 <O> 1000: TEST_PIN1 <O> 1001: DUMMY <O>	

Register: PIN_SHARE_CTRL20 0xDD					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P1D4	3:0	R/W	0x00	Pin68 (PAD_TCON13) 0000: P1D4i <I> 0001: P1D4o <O> <push-pull> 0010: P1D4o <O> <open-drain> 0011: SD0 <O> 100: TCON[3] <O> 101: TCON[13] <O> 0100: PWM0 <O> <push-pull> 0101: PWM0 <O> <open-drain> 0110: SPDIF0 <O> 0111: TCON[14] <O> 1000: TCON[15] <O> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O>	

Register: PIN_SHARE_CTRL21 0xDE					
Name	Bits	Read/ Write	Reset State	Comments	Config
P1D5_6	7:6	R/W	0	Pin69 (PAD_TCON3) 00: normal output(refer 0xDE[3:0]) <default> 01: IICCSCL <IO> <open-drain> 10: DDCSCL2P <IO> <open-drain> Pin70 (PAD_TCON9) 00: normal output(refer 0xDF[3:0]) <default> 01: IICSDA <IO> <open-drain> 10: DDCSDA2P <IO> <open-drain> DDC2P effective only if Page10 0xBD[0] = 1	
Reserved	5:4	R/W	0x00	Reserved	
P1D5	3:0	R/W	0x00	Pin69 (PAD_TCON3) 0000: P1D5i <I> 0001: P1D5o <O> <push-pull>	

				0010: P1D5o <O> <open-drain> 0011: SD1 <O> 0100: TCON[3] <O> 0101: TCON[7] <O> 0110: SPDIF1 <O> 111: HCSCL <IO> <open drain> 0111: PWM2 <O> <push-pull> 1000: PWM2 <O> <open-drain> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O>	
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Register: PIN_SHARE_CTRL22 0xDF					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P1D6	3:0	R/W	0x00	Pin70 (PAD_TCON9) 0000: P1D6i <I> 0001: P1D6o <O> <push-pull> 0010: P1D6o <O> <open-drain> 0011: SD2 <O> 0100: TCON[9] <O> 0101: TCON[11] <O> 0110: SPDIF2 <O> 111: HCSDA <IO> <open drain> 0111: PWM4 <O> <push-pull> 1000: PWM4 <O> <open-drain> 1001: TEST_PIN0 <O> 1010: TEST_PIN1 <O> 1011: DUMMY <O>	

Register: PIN_SHARE_CTRL23 0xE0					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P1D7	3:0	R/W	0x00	Pin71 (PAD_TCON8) 0000: P1D7i <I> 0001: P1D7o <O> <push-pull> 0010: PWM5 <O> <push-pull> 0011: SD3 <O> 0100: TCON[8] <O> 0101: TCON[10] <O> 0110: SPDIF3 <O> 0111: PWM1 <O> <push pull> 0010: P1D7o <O> <open-drain> 0011: PWM1 <O> <push-pull> 0100: PWM1 <O> <open-drain> 0101: PWM5 <O> <push-pull> 0110: PWM5 <O> <open-drain> 0111: TCON[8] <O> 1000: TCON[10] <O> 1001: SD3 <O> 1010: SPDIF3 <O> 1011: TEST_PIN0 <O> 1100: TEST_PIN1 <O> 1101: DUMMY <O>	

Register: PIN_SHARE_CTRL24	0xE1
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Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PCD2	3:0	R/W	0x00	Pin72 (PAD_TCON6) 0000: PCD2i <I> <default> 0001: PCD2o <O> <push-pull> 0010: TCON[6] <O> 0011: TCON[12] <O> 0100: PWM3 <O> <push-pull> 0101: PWM3 <O> <open-drain> 0010: PCD2o <O> <open-drain> 0011: PWM3 <O> <push-pull> 0100: PWM3 <O> <open-drain> 0101: TCON[6] <O> 0110: TCON[12] <O> 0111: TEST_PIN0 <O> 1000: TEST_PIN1 <O> 1001: DUMMY <O>	

Register:: PIN_SHARE_CTRL25 0xE2					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	R/W	0x00	Reserved	
P9PA	1:0	R/W	0x00	Pin74-83 (Pin74-Pin78 P9.0~P9.4) (Pin79-Pin83 PA.0~PA.4) 00: None <default> 00: Hi-Z <default> 01: P9PAi <I> 10: P9PAo <O> (push-pull)* 11: P9PAo <O> (Open-drain) ie. active if single-port LVDS without E/O swap *(for Pin 74,75,76, 77, 78,79,80,81,82,83 , 0xB6 0xE3 is effectively only if 0xA9 0xE2(Bit7:6)=2'b10) Pin 74,75,76,77,78,79,80,81,82,83 : Pin share for P9PAo(push-pull) , Audio IIS and Audio SPDIF .	

(for Pin 74,75,78,79 0xB6 0xE3 is effectively only if 0xA9 0xE2(Bit7:6)=2'b10)

Register:: PIN_SHARE_CTRL26 0xE3					
Name	Bits	Read/ Write	Reset State	Comments	Config
P9D0	7:6	R/W	0x00	Pin74 00: P9D0o (push-pull) <O> 01: IIS_SD0 <O> 10: SPDIF0 <O> 11: Reserved 11: DUMMY <O> TXO3+_8b when DISP_TYPE(8C-00) set to LVDS	
P9D1	5:4	R/W	0x00	Pin75 00: P9D1o (push-pull) <O> 01: IIS_MCK <O> 10: SPDIF1 <O> 11: Reserved 11: DUMMY <O> TXO3-_8b when DISP_TYPE(8C-00) set to LVDS	

P9D4	3:2	R/W	0x00	Pin78 00: P9D4o (push-pull) <O> 01: IIS_SCK <O> 10: SPDIF2 <O> 11: Reserved 11: DUMMY <O> TXO2+_8b when DISP_TYPE(8C-00) set to LVDS	
PAD0	1:0	R/W	0x00	Pin79 00: PAD0o (push-pull) <O> 01: IIS_WS <O> 10: SPDIF3 <O> 11: Reserved 11: DUMMY <O> TXO2-_8b when DISP_TYPE(8C-00) set to LVDS	

Register: PIN_SHARE_CTRL27 0xE4					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P5D2	3:0	R/W	0x00	Pin96 (PAD_PWM0) 0000: P5D2i <I> 0001: P5D2o <O> <push-pull> 10: DCLK <O> 0010: P5D2o <O> <open-drain> 0011: PWM0 <O> <push-pull> 0100: PWM0 <O> <open-drain> 0101: TEST_PIN2 <O> 0110: TEST_PIN3 <O> 0111: DUMMY <O> Not effective when LVDS 10bit	

Register: PIN_SHARE_CTRL28 0xE5					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P5D3	3:0	R/W	0x00	Pin97 (PAD_PWM1) 0000: P5D3i <I> 0001: P5D3o <O> <push-pull> 0010: P5D3o <O> <open-drain> 0011: PWM1 <O> <push-pull> 100: DVS <O> 0100: PWM1 <O> <open-drain> 0101: TCON[S0] <O> 0110: TEST_PIN2 <O> 0111: TEST_PIN3 <O> 1000: DUMMY <O> Not effective when LVDS 10bit	

Register: PIN_SHARE_CTRL29 0xE6					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P5D4	3:0	R/W	0x00	Pin98 (PAD_PWM2) 0000: P5D4i <I> 0001: P5D4o <O> <push-pull> 0010: P5D4o <O> <open-drain> 0011: PWM2 <O> <push-pull> 0100: PWM2 <O> <open-drain>	

				0101: TCON[13] <O> 0110: TCON[15] <O> 0111: TEST_PIN2 <O> 1000: TEST_PIN3 <O> 1001: DUMMY <O> Not effective when LVDS 10bit	
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Register: PIN_SHARE_CTRL2A 0xE7					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P5D5	3:0	R/W	0x00	Pin99 (PAD_PWM3) 0000: P5D5i <I> 0001: P5D5o <O> <push-pull> 0010: P5D5o <O> <open-drain> 0011: PWM3 <O> <push-pull> 0100: TCON[6] <O> 0101: TCON[11] <O> 0110: PWM3 <O> <open drain> 0111: TCON[0] <O> 0100: PWM3 <O> <open-drain> 0101: TCON[0] <O> 0110: TCON[6] <O> 0111: TCON[11] <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O> Not effective when LVDS 10bit	

Register: PIN_SHARE_CTRL2B 0xE8					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:5	R/W	0x00	Reserved	
P5D6	4:0	R/W	0x00	Pin100 (PAD_PWM4) 00000: P5D6i <I> 00001: P5D6o <O> <push-pull> 00010: P5D6o <O> <open-drain> 00011: PWM4 <O> <push-pull> 0100: TCON[3] <O> 0101: TCON[12] <O> 0110: PWM4 <O> <open drain> 0111: TCON[S1] <O> 00100: PWM4 <O> <open-drain> 00101: TCON[S1] <O> 00110: TCON[3] <O> 00111: TCON[12] <O> 01000: FIELD <O> 01001: DHS <O> 01010: DVS <O> 01011: DENA <O> 01100: DCLK <O> 01101: L_R <O> 01110: TEST_PIN2 <O> 01111: TEST_PIN3 <O> 10000: DUMMY <O>	

Register: PIN_SHARE_CTRL2C 0xE9					
Name	Bits	Read/ Write	Reset	Comments	Config

		Write	State	
Reserved	7:4	R/W	0x00	Reserved
P5D7	3:0	R/W	0x00	Pin101 (PAD_PWM5) 0000: P5D7i <I> 0001: P5D7o <O> <push-pull> 0010: TCON[14] <O> 0010: P5D7o <O> <open-drain> 0011: PWM5 <O> <push-pull> 0100: PWM5 <O> <open-drain> 0101: TCON[14] <O> 0110: DHS <O> 0111: DVS <O> 1000: DENA <O> 1001: DCLK <O> 1010: TEST_PIN2 <O> 1011: TEST_PIN3 <O> 1100: DUMMY <O>

Register: PIN_SHARE_CTRL2D 0xEA					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P7D6	3:0	R/W	0x00	Pin102 (PAD_SPDIF3) 0000: P7D6i <I> 0001: P7D6o <O> <push-pull> 0010: P7D6o <O> <open-drain> 0011: PWM0 <O> <push-pull> 0100: SD3 <O> 0101: SPDIF3 <O> 0110: TCON[10] <O> 0111: PWM0 <O> <open-drain> 0100: PWM0 <O> <open-drain> 0101: TCON[10] <O> 0110: SD3 <O> 0111: SPDIF3 <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O>	

Register: PIN_SHARE_CTRL2E 0xEB					
Name	Bits	Read/ Write	Reset State	Comments	Config
P1D2_3	7:6	R/W	0	Pin103 (PAD_SPDIF2) 00: normal output(refer 0xEB[3:0]) <default> 01: IICSCL <IO> <open-drain> 10: IICSCL_AUX <IO> <open-drain> Pin104 (PAD_SPDIF1) 00: normal output(refer 0xEC[3:0]) <default> 01: IICSDA <IO> <open-drain> 10: IICSDA_AUX <IO> <open-drain> IIC_AUX effective only if Page10 0xBD[1] = 1	
Reserved	5:4	R/W	0x00	Reserved	
P7D5	3:0	R/W	0x00	Pin103 (PAD_SPDIF2) 0000: P7D5i <I> 0001: P7D5o <O> <push-pull> 0010: P7D5o <O> <open-drain> 0011: PWM1 <O> <push-pull> 0100: SD2 <O>	

				0101: SPDIF2 <O> 0110: TCON[8] <O> 111: HCSCL <IO> <open-drain> 0100: PWM1 <O> <open-drain> 0101: TCON[8] <O> 0110: SD2 <O> 0111: SPDIF2 <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O> Effective only if Page10 0xBA[4] = 0	
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Register: PIN_SHARE_CTRL2F 0xEC					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P7D4	3:0	R/W	0x00	Pin104 (PAD_SPDIF1) 0000: P7D4i <I> 0001: P7D4o <O> <push-pull> 0010: P7D4o <O> <open-drain> 0011: SD1 <O> 0100: IRQB <O> 0101: TCON[5] <O> 0110: SPDIF1 <O> 111: HCSDA <IO> <open-drain> 0111: TEST_PIN2 <O> 1000: TEST_PIN3 <O> 1001: DUMMY <O>	

Register: PIN_SHARE_CTRL30 0xED					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P8D0	3:0	R/W	0x00	Pin105 (PAD_SPDIF0) 0000: P8D0i <I> 0001: P8D0o <O> <push-pull> 0010: P8D0o <O> <open-drain> 0011: TCON[9] <O> 0100: SD0 <O> 0101: SPDIF0 <O> 0110: AUX_TXDATA<I> 0111: TCON[6] <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O>	

Register: PIN_SHARE_CTRL31 0xEE					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P8D1	3:0	R/W	0x00	Pin108 (PAD_MCK) 0000: P8D1i <I> 0001: P8D1o <O> <push-pull> 0010: P8D1o <O> <open-drain> 0011: CLKO <O> 0100: MCK <O> 0101: TCON[7] <O>	

				0110: AUX_OE <I> 0111: TEST_PIN2 <O> 1000: TEST_PIN3 <O> 1001: DUMMY <O>	
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Register: PIN_SHARE_CTRL32 0xEF					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P3D2	3:0	R/W	0x00	Pin109 (PAD_SCK) 0000: P3D2i <I> 0001: P3D2o <O> <push-pull> 0010: P3D2o <O> <open-drain> 0011: INT0 <I> 0100: TCON[3] <O> 0101: SCK <O> 0110: AUX_D1 <O> 0111: PWM2 <O> <open-drain> 0111: PWM2 <O> <push-pull> 1000: PWM2 <O> <open-drain> 1001: TEST_PIN2 <O> 1010: TEST_PIN3 <O> 1011: DUMMY <O>	

Register: PIN_SHARE_CTRL33 0xF0					
Name	Bits	Read/ Write	Reset State	Comments	Config
HS_MIRROR	7	R/W	0x0	Pin110~Pin114 Mirror 0:Pin110 WS, Pin111 SD0, Pin112 SD1, Pin113 SD2, Pin114 SD3 1:Pin110 SD1, Pin111 SD0, Pin112 WS, Pin113 SCK, Pin114 MCK	
Reserved	7:4	R/W	0x00	Reserved	
P3D3	3:0	R/W	0x00	Pin110 (PAD_WS) 0000: P3D3i <I> <default> 0001: P3D3o <O> <open drain> 0010: P3D3o <O> <push pull> 0011: INT1 <I> 0100: TCON[6] <O> 0101: WS <O> 0110: TCON[2] <O> 0111: TCON[7] <O> 0001: P3D3o <O> <push-pull> 0010: P3D3o <O> <open-drain> 0011: TCON[2] <O> 0100: TCON[6] <O> 0101: TCON[7] <O> 0110: INT1 <I> 0111: WS <O> 1000: SD1 <O> 1001: TEST_PIN2 <O> 1010: TEST_PIN3 <O> 1011: DUMMY <O> If user need "HS_SD1" for Pin 110, PIN_SHARE_CTRL0D :0xE9:Bit 7→"b1" PIN_SHARE_CTRL0D:0xE9:Bit 6:4→"b101"	

Register: PIN_SHARE_CTRL34	0xF1
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Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P3D4	3:0	R/W	0x0	Pin111 (PAD_SD0) 0000: P3D4i <I> <default> 0001: P3D4o <O> <open drain> 0010: P3D4o <O> <push pull> 0011: T0 <I> 0100: TCON[4] <O> 0101: SD0 <O> 0110: SPDIF0 <O> 0111: TCON[7] <O> 0001: P3D4o <O> <push-pull> 0010: P3D4o <O> <open-drain> 0011: TCON[4] <O> 0100: TCON[7] <O> 0101: T0 <I> 0110: SD0 <O> 0111: SPDIF0 <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O>	

Register: PIN_SHARE_CTRL35 0xF2					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P3D5	3:0	R/W	0x0	Pin112 (PAD_SD1) 0000: P3D5i <I> <default> 0001: P3D5o <O> <open drain> 0010: P3D5o <O> <push pull> 0011: T1 <I> 0100: TCON[9] <O> 0101: SD1 <O> 0110: SPDIF1 <O> 0111: TCON[5] <O> 0001: P3D5o <O> <push-pull> 0010: P3D5o <O> <open-drain> 0011: TCON[5] <O> 0100: TCON[9] <O> 0101: T1 <I> 0110: SD1 <O> 0111: SPDIF1 <O> 1000: WS <O> 1001: TEST_PIN2 <O> 1010: TEST_PIN3 <O> 1011: DUMMY <O> If user need "HS_WS" for Pin 112, PIN_SHARE_CTRL0D :0xE9:Bit 7→"b1" PIN_SHARE_CTRL0E :0xEB:Bit 7:5→"b101"	

Register: PIN_SHARE_CTRL36 0xF3					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P3D6	3:0	R/W	0x0	Pin113 (PAD_SD2) 0000: P3D6i <I> <default> 0001: P3D6o <O> <open drain>	

				0010: P3D6o <O> <push pull> 0011: TCON[1] <O> 0100: SD2 <O> 0101: SPDIF2 <O> 0110: AUX_D2 <O> 0111: TCON[11] <O> 1000: SCK <O> 0001: P3D6o <O> <push-pull> 0010: P3D6o <O> <open-drain> 0011: TCON[1] <O> 0100: TCON[11] <O> 0101: SD2 <O> 0110: SPDIF2 <O> 0111: AUX_D2 <O> 1000: SCK <O> 1001: TEST_PIN2 <O> 1010: TEST_PIN3 <O> 1011: DUMMY <O> If user need "HS_SCK" for Pin 113, PIN_SHARE_CTRL0D :0xE9:Bit 7→"b1" PIN_SHARE_CTRL10 :0xEC:Bit 7:5→"b100"	
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Register: PIN_SHARE_CTRL37 0xF4					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
P3D7	3:0	R/W	0x0	Pin114 (PAD_SD3) 0000: P3D7i <I> <default> 0001: P3D7o <O> <open drain> 0010: P3D7o <O> <push pull> 0011: TCON[13] <O> 0100: SD3 <O> 0101: SPDIF3 <O> 0110: PWM4 <O> <push pull> 0111: TCON[0] <O> 0001: P3D7o <O> <push-pull> 0010: P3D7o <O> <open-drain> 0011: PWM4 <O> <push-pull> 0100: PWM4 <O> <open-drain> 0101: TCON[0] <O> 0110: TCON[13] <O> 0111: SD3 <O> 1000: SPDIF3 <O> 1001: MCK <O> 1010: TEST_PIN2 <O> 1011: TEST_PIN3 <O> 1100: DUMMY <O> If user need "HS_MCK" for Pin 114, PIN_SHARE_CTRL0D :0xE9:Bit 7→"b1" PIN_SHARE_CTRL12 :0xED:Bit 7:4→"b100"	

Register: PIN_SHARE_CTRL38 0xF5					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PCD1	3:0	R/W	0x00	Pin119 (PAD_PWM5) 0000: PCD1i <I> <default> 0001: PCD1o <O> <open drain> 0010: PCD1o <O> <push pull>	

				0011: PWM5 <O> <push pull> 0100: SPIFI <O> 0101: PWM5 <O> <open drain> 0110: PWM1 <O> <push pull> 0111: PWM1 <O> <open drain> 0001: PCD1o <O> <push-pull> 0010: PCD1o <O> <open-drain> 0011: PWM1 <O> <push-pull> 0100: PWM1 <O> <open-drain> 0101: PWM5 <O> <push-pull> 0110: PWM5 <O> <open-drain> 0111: SPDIF1 <O> 1000: TEST_PIN2 <O> 1001: TEST_PIN3 <O> 1010: DUMMY <O> (Pin 119 : Power on latch Pin) (when AC Power On , Power on latch pin must be "High") Please don't let Pin119 be "Input Pin".	
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Register: PIN_SHARE_CTRL39 0xF6					
Name	Bits	Read/ Write	Reset State	Comments	Config
DDC3	7	R/W	0x0	Pin121 (PAD_DDCSCL3) 0: DDCSCL3 <IO> <open-drain> <default> 1: normal output(refer 0xF7[2:0]) Pin122 (PAD_DDCSDA3) 0: DDCSDA3 <IO> <open-drain> <default> 1: normal output(refer 0xF8[2:0])	
Reserved	6:3	R/W	0x00	Reserved	

Register: PIN_SHARE_CTRL3A 0xF7					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
DDCSDA3	2:0	R/W	0x00	Pin122 (PAD_DDCSDA3) 000: P7D2i <I> 001: P7D2o <O> <open drain> 010: P7D2o <O> <push pull> 001: P7D2o <O> <push-pull> 010: P7D2o <O> <open-drain> 011: AUX_CH_N1 100: TEST_PIN2 <O> 101: TEST_PIN3 <O> 110: DUMMY <O>	

Register: PIN_SHARE_CTRL3B 0xF8					
Name	Bits	Read/ Write	Reset	Comments	Config

		Write	State		
DDC2	7	R/W	0	Pin123 (PAD_DDCSDA2) 0: DDCSDA2 <IO> <open-drain> <default> 1: normal output(refer 0xF9[2:0]) Pin124 (PAD_DDCSCL2) 0: DDCSCL2 <IO> <open-drain> <default> 1: normal output(refer 0xFA[2:0])	
Reserved	6:3	R/W	0x00	Reserved	
DDCSDA2	2:0	R/W	0x00	Pin123 (PAD_DDCSDA2) 000: P7D1i <I> 001: P7D1o <O> <open drain> 010: P7D1o <O> <push pull> 001: P7D1o <O> <push-pull> 010: P7D1o <O> <open-drain> 011: AUX_CH_N0 100: TEST_PIN2 <O> 101: TEST_PIN3 <O> 110: DUMMY <O>	

Register: PIN_SHARE_CTRL3C 0xF9					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:3	R/W	0x00	Reserved	
DDCSCL2	2:0	R/W	0x00	Pin124 (PAD_DDCSCL2) 000: P7D0i <I> 001: P7D0o <O> <open drain> 010: P7D0o <O> <push pull> 001: P7D0o <O> <push-pull> 010: P7D0o <O> <open-drain> 011: AUX_CH_P0 100: TEST_PIN2 <O> 101: TEST_PIN3 <O> 110: DUMMY <O>	

Register: PIN_SHARE_CTRL3D 0xFA					
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:4	R/W	0x00	Reserved	
PCD0	3:0	R/W	0x00	Pin126 (PAD_CEC) 0000: PCD0i <I> <default> 0001: PCD0o <O> <open drain> 0010: PCD0o <O> <push pull> 0011: PWM1 <O> <push pull> 0100: PWM0 <O> <open-drain> 0101: SPDIF2 <O> 0110: PWM1 <O> <open drain> 0111: TCON[14] <O> 0001: PCD0o <O> <push-pull> 0010: PCD0o <O> <open-drain> 0011: PWM0 <O> <push-pull> 0100: PWM0 <O> <open-drain> 0101: PWM1 <O> <push-pull> 0110: PWM1 <O> <open-drain> 0111: TCON[14] <O> 1000: SPDIF2 <O> 1001: CEC <IO> 1010: TEST_PIN2 <O> 1011: TEST_PIN3 <O>	

			1100: DUMMY <O>	
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Ultra Vivid (Page 11)
0x11A0 Reserved
I Domain DLTI

Register::I_DLTI_CTRL_0						0x11A1
Name	bits	R/W/D	Reset State	Comments		Config
Dummy	7:5	--	0	Reserved		
Idclti_test_mode	4	R/W	0	1'b0: { fir_se_low, fir_lt_up, diff_st_div_4, diff_st_div_2_6, diff_st_div_1_3_5_7, blending_gain [3:0], sign_1_2, undo_flag, undo_counter[2:0], 1'b0; case_a, case_b, case_c, case_d, case_e, dir_l_2, dir_l_3, dir_r_2, dir_r_3, b_le_f, f_le_c, b_le_c, can_le_max, min_le_cad, 1'b0} 1'b1: { cr_w_lt0, cr_w_st0, cr_pe_bypass, cr_deltaout_stg1 [1:0], cr_deltaout_stg2[1:0], cr_wpn_bt_ln_stg1, cr_ln_bt_xfn_stg1, cr_xfn_bt_xpn_stg1, cr_wpn_bt_ln_stg2, cr_ln_bt_xfn_stg2, cr_xfn_bt_xpn_stg2, 2'b00 ; cb_w_lt0, cb_w_st0, cb_pe_bypass, cb_deltaout_stg1 [1:0], cb_deltaout_stg2[1:0], cb_wpn_bt_ln_stg1, cb_ln_bt_xfn_stg1, cb_xfn_bt_xpn_stg1, cb_wpn_bt_ln_stg2, cb_ln_bt_xfn_stg2, cb_xfn_bt_xpn_stg2, 2'b00, } ;		
New_function_blend	3	R/W	0	New function blend enable 0: disable 1: enable		Cc:m_reg_vc_IDLTI_NewFunc_Ble_nd_Enable
Ch1_Lope_det_en	2	R/W	0	Ch1 llope detection enable: 0: disable 1: enable		Cc:m_reg_vc_IDLTI_Lope_Det_Enable
Ch1_Filter_det_en	1	R/W	1	Ch1 high pass detection enable: 0: disable 1: enable		Cc:m_reg_vc_IDLTI_Filter_Det_Enable
Ch1_dliti_en	0	R/W/D	0	Ch1 dliti function enable: 0: disable 1: enable		Cc:m_reg_vc_IDLTI_Enable

Register::I_DLTI_CTRL_1						0x11A2
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
Ch1_lope_search_range_left	5:4	R/W	3	Ch1 mean search range at left side: Valid range: 1~3		Cc:m_reg_vc_IDLTI_Lope_Search_Range_Left
Ch1_lope_search_range_right	3:2	R/W	3	Ch1 mean search range at right sode: Valid range: 1~3		Cc:m_reg_vc_IDLTI_Lope_Search_Range_Right
Ch1_mean_search_range	1:0	R/W	3	Ch1 mean search range: Valid range: 1~3		Cc:m_reg_vc_IDLTI_Mean_Search_Range

Register::I_DLTI_CTRL_2						0x11A3
Name	bits	R/W/D	Reset State	Comments		Config
Undo_pixel	7:6	R/W	3	前後 n 點不作 IDLTI, 但最外面的(3-n)個點用 blending valid range: 0~3.		Cc:m_reg_v c_IDLTI_U ndo_Pixel
Ch1_dlти_gain	5:0	R/W	5	Ch1 dlти adjustment gain U(3.3). Valid range:1/8~63/8 Default:5/8		Cc:m_reg_v c_IDLTI_G ain

Register::I_DLTI_UPPER_TH_HSB						0x11A4
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	R/W	0	Reserved		
I_DLTI_UPPER_TH[9:8]	1:0	R/W	0x1	9:8 bits of Ch1 high pass filter upper threshold for blending. Valid range:0x01~0x3ff		Cc:m_reg_v c_I_Upper_Thd

Register::I_DLTI_UPPER_TH LSB						0x11A5
Name	bits	R/W/D	Reset State	Comments		Config
I_DLTI_UPPER_TH[7:0]	7:0	R/W	0x90	7:0 bit of Ch1 high pass filter upper threshold for blending. Valid range:0x01~0x3ff		Cc:m_reg_v c_I_Upper_Thd

Register::I_DLTI_LOWER_TH_HSB						0x11A6
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	R/W	0	Reserved		
I_DLTI_LOWER_TH[9:8]	1:0	R/W	0x0	9:8 bits of Ch1 high pass filter lower threshold for blending. Valid range: 0x01~0x3ff		Cc:m_reg_v c_I_Lower_Thd

Register::I_DLTI_LOWER_TH LSB						0x11A7
Name	bits	R/W/D	Reset State	Comments		Config
I_DLTI_LOWER_TH[7:0]	7:0	R/W	0x78	7:0 bit of Ch1 high pass filter lower threshold for blending. Valid range: 0x01~0x3ff		Cc:m_reg_v c_I_Lower_Thd

Register::I_DLTI_C0_HSB						0x11A8
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:1	R/W	0	Reserved		
I_DLTI_C0[8]	0	R/W	0x0	Bit 8 of Ch1 high pass filter coefficients c0:S(0.8) Valid range: 0x01~0x1ff 205 = 0xcd There ia a 9 taps filter: [c4 c3 c2 c1 c0 c1 c2 c3 c4]		Cc:m_reg_v c_I_Filter_C 0:s

Register::I_DLTI_C0 LSB						0x11A9
Name	bits	R/W/D	Reset State	Comments		Config

I_DLTI_C0[7:0]	7:0	R/W	0xcd	7:0 bits of Ch1 hign pass filter coefficients c0:S(0.8) Valid range: 0x01~0x1ff 205 = 0xcd There ia a 9 taps filter: [c4 c3 c2 c1 c0 c1 c2 c3 c4]	Cc:m_reg_v c_I_Filter_C 0:s
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Register::I_DLTI_C1_HSB 0x11AA					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	R/W	0	Reserved	
I_DLTI_C1[8]	0	R/W	0x1	Bit 8 of Ch1 hign pass filter coefficients c1:S(0.8) Valid range: 0x01~0x1ff -2 = 0x1fe in 2's complement	Cc:m_reg_v c_I_Filter_C 1:s

Register::I_DLTI_C1 LSB 0x11AB					
Name	bits	R/W/D	Reset State	Comments	Config
I_DLTI_C1[7:0]	7:0	R/W	0xe0	7:0 bits of Ch1 hign pass filter coefficients c1:S(0.8) Valid range: 0x01~0x1ff -2 = 0x1fe in 2's complement	Cc:m_reg_v c_I_Filter_C 1:s

Register::I_DLTI_C2_HSB 0x11AC					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	R/W	0	Reserved	
I_DLTI_C2[8]	0	R/W	0x1	Bit 8 of Ch1 hign pass filter coefficients c2:S(0.8) Valid range: 0x01~0x1ff -17 = 0x1ef in 2's complement	Cc:m_reg_v c_I_Filter_C 2:s

Register::I_DLTI_C2 LSB 0x11AD					
Name	bits	R/W/D	Reset State	Comments	Config
I_DLTI_C2[7:0]	7:0	R/W	0xef	7:0 bits of Ch1 hign pass filter coefficients c2:S(0.8) Valid range: 0x01~0x1ff -17 = 0x1ef in 2's complement	Cc:m_reg_v c_I_Filter_C 2:s

Register::I_DLTI_C3_HSB 0x11AE					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	R/W	0	Reserved	
I_DLTI_C3[8]	0	R/W	0x1	Bit 8 of Ch1 hign pass filter coefficients c3:S(0.8) Valid range: 0x01~0x1ff -16 = 0x1f0 in 2's complement	Cc:m_reg_v c_I_Filter_C 3:s

Register::I_DLTI_C3 LSB 0x11AF					
Name	bits	R/W/D	Reset State	Comments	Config
I_DLTI_C3[7:0]	7:0	R/W	0xf0	7:0 bits of Ch1 hign pass filter coefficients c3:S(0.8) Valid range: 0x01~0x1ff -16 = 0x1f0 in 2's complement	Cc:m_reg_v c_I_Filter_C 3:s

Register::I_DLTI_C4_HSB 0x11B0					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	R/W	0	Reserved	

I_DLTI_C4[8]	0	R/W	0x1	Bit 8 of Ch1 high pass filter coefficients c4:S(0.8) Valid range: 0x01~0x1ff -22 = 0x1ea in 2's complement	Cc:m_reg_v c_I_Filter_C 4:s
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Register::I_DLTI_C4_LSB 0x11B1					
Name	bits	R/W/D	Reset State	Comments	Config
I_DLTI_C4[7:0]	7:0	R/W	0xea	7:0 bits of Ch1 high pass filter coefficients c4:S(0.8) Valid range: 0x01~0x1ff -22 = 0x1ea in 2's complement	Cc:m_reg_v c_I_Filter_C 4:s

0x11B2 Reserved

I Domain DCTI

Register:: I_DCTi_CTRL						0x11B3
Name	Bits	Read/ Write	Reset State	Comments		Config
Dcti_enable	7	R/W/D	0	Function enable		cc:m_reg_vc_IDCTi_Enable
Reserved	6:2	-	-	Reserved		
Prevent_PE	1	R/W	1	Prevent Phase Error Mode 0: Disable 1: Enable		cc:m_reg_vc_IDCTi_PE_Pevent
2nd_DCTi_Enable_d	0	R/W	1	Gain Control for 2nd DCTi 0: Disable 1: Enable		cc:m_reg_vc_IDCTi_2nd_Enable

Register:: I_DCTi_1st_TH_Value						0x11B4
Name	Bits	Read/ Write	Reset State	Comments		Config
Reserved	7:6	-	-	Reserved		
Th_Value	5:0	R/W	1E	Up and Down Limit for DCTi_Gain Result Value (6-bit) Valid Range: 0~63		cc:m_reg_vc_IDCTi_Gain_Th

Register:: I_DCTi_1 st _GAIN_Value						0x11B5
Name	Bits	Read/ Write	Reset State	Comments		Config
Reserved	7:5	-	-	Reserved		
Gain_Value	4:0	R/W	0A	Adjust DCTi Gain Value Valid Range: 0~31		cc:m_reg_vc_IDCTi_Gain_Value

Register:: I_DCTi_2nd_TH_Value						0x11B6
Name	Bits	Read/ Write	Reset State	Comments		Config
Reserved	7:6	-	-	Reserved		
Th_Value	5:0	R/W	1E	Up and Down Limit for DCTi_Gain Result Value Valid Range: 0~63		cc:m_reg_vc_IDCTi_2nd_Th

Register:: I_DCTi_2nd_GAIN_Value						0x11B7
Name	Bits	Read/ Write	Reset State	Comments		Config
Reserved	7:5	-	-	Reserved		
Gain_Value	4:0	R/W	0A	Adjust DCTi Gain Value Valid Range: 0~31		cc:m_reg_vc_IDCTi_2nd_Gain_Value

0x11B8 is reserved

Scaler Peaking

Vertical peaking before scale-up function

Register:: SCALER PEAKING_C0						0x11B9
Name	Bits	Read/Write	Reset State	Comments		Config
VPK_VCTI_HW	7	R/W	0	Enable VPK/VCTI highlight window 0 : disable HW 1 : enable This setting is effective in both VPK and VCTI		Cc:reg_vc_s caleup_pk_v cti_hw
VPK_VCTI_HW_CTRL	6	R/W	0	0: VPK/VCTI used inside highlight window. 1: VPK/VCTI used outside highlight window.		
PK_EN	5	R/W/D	0	Peaking Control 0:Disable 1:Enable		Cc:reg_vc_s caleup_Peak En
PK_Mask_C0	4:0	R/W	0x8	Peaking Mask coefficient C0 S(5, 0) 5 bits signed integer, range: -16 ~ 15 (2's complement implement)		Cc:reg_vc_s caleup_pk_ mask_c0

Register:: SCALER_PEAKING_C1C2						0x11BA
Name	Bits	Read/Write	Reset State	Comments		Config
PK_Mask_C1	7:4	R/W	0xf	Peaking Mask coefficient C1 S(4, 0) 4 bits signed integer, range: -8 ~ 7 (2's complement implement)		Cc:reg_vc_s caleup_pk_ mask_c1
PK_Mask_C2	3:0	R/W	0xf	Peaking Mask coefficient C2 S(4, 0) 4 bits signed integer, range: -8 ~ 7 (2's complement implement)		Cc:reg_vc_s caleup_pk_ mask_c2

Register:: SCALER_PEAKING_C3						0x11BB
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:6	-	0	Reserved		
PK_Mask_C3	5:2	R/W	0xf	Peaking Mask coefficient C3 S(4, 0) 4 bits signed integer, range: -8 ~ 7 (2's complement implement)		Cc:reg_vc_s caleup_pk_ mask_c3
PK_ShiftBit	1:0	R/W	0x0	Peaking Mask coefficient C3 U(2, 0) 2 bits unsigned integer, range: 0 ~ 3		Cc:reg_vc_s caleup_pk_s hiftbit

Register:: SCALER_PEAKING_CORING						0x11BC
Name	Bits	Read/Write	Reset State	Comments		Config
PK_CORING	7:0	R/W	8	Peaking Coring (LSB 8 bits of Coring value)		cc:reg_vc_s caleup_Cori ng

Register:: SCALER_PEAKING_X1						0x11BD
Name	Bits	Read/Write	Reset State	Comments		Config
PK_X1	7:0	R/W	16	Peaking X1 (LSB 8 bits of X1 value)		cc:reg_vc_s

					caleup_X1
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Register:: SCALER_PEAKING_OFFSET					0x11BE
Name	Bits	Read/ Write	Reset State	Comments	Config
PK_OFFSET	7:0	R/W	8	Peaking Offset in X1 (LSB 8 bits of Offset value)	Cc:reg_vc_s caleup_PK_Offset

Register:: SCALER_PEAKING_LIMIT					0x11BF
Name	Bits	Read/ Write	Reset State	Comments	Config
PK_LMTP	7:4	R/W	4	Peaking Positive Limit $Lmt_P = Value * 32$	Cc:reg_vc_s caleup_nDP wlmt
PK_LMTN	3:0	R/W	4	Peaking Negative Limit $Lmt_N = Value * 32$	Cc:reg_vc_s caleup_nDP blmt

Register:: SCALER_PEAKING_GAIN					0x11C0
Name	Bits	Read/ Write	Reset State	Comments	Config
PK_G1	7:4	R/W	4	Peaking Gain1 $Gain1 = 2 * Value / 8$	Cc:reg_vc_s caleup_nDP gain
PK_G2	3:0	R/W	8	Peaking Gain2 $Gain2 = 2 * Value / 8$	Cc:reg_vc_s caleup_nDP gain2

VCTI

Vertical CTI before ScaleUp

Register:: SR_VCTI_CTRL						0x11C1
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:4	-	0-	Reserved		
VCTI_SELECT	3:2	R/W	0	Vertical-CTI Select (see Note for VCTI_SELECT) 0: type 0 1: type 1 2: type 2 3: type 3 → when reg_vc_scaleup_V6tap_en = 1 (no use)		cc:reg_vc_s calup_vcti_s elect
VCTI_EN	1	R/W/D	0	Vertical-CTI Control 0: Disable 1: Enable → Restriction: when reg_vc_scaleup_vzoomen = 1		cc:reg_vc_s calup_vcti_en
VCTI_LOW_PASS_FILTER_ER_EN	0	R/W	0x0	Enable low pass filter before VCTI 0: Disable 1: Enable		cc:reg_lowpass_before_vcti_en

Register:: SR_VCTI_TYPE3_Thd (no use)						0x11C2
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:6	-	0	Reserved		
VCTI_Type3_Thd	5:0	R/W	0xA	Vertical-CTI Type3 Threshold Range:0~63 Default value:0xA		Cc:reg_vc_s caleup_vcti_type3_thd

Register:: SR_VCTI_GAIN						0x11C3
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7	-	-	Reserved		
VCTI_GAIN	6:0	R/W	0x18	Vertical-CTI Gain <i>U(3,4) 3 bits unsigned integer, 4 bits fractional number</i> <i>range: 1/16 ~ 127/16</i>		cc:reg_vc_s calup_vcti_gain

Register:: SR_VCTI_LPF_LBOUND2_HSB						0x11C4
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	-	0			
SR_VCTI_LPF_LBOUN_D2[9:8]	1:0	R/W	0x0	9:8 bits of Low bound 2 for strong low pass filter before VCTI Range : 0~1023		cc:reg_vcti_lpf_lowbound2

Register:: SR_VCTI_LPF_LBOUND2 LSB						0x11C5
Name	bits	R/W/D	Reset State	Comments		Config
SR_VCTI_LPF_LBOUN_D2[7:0]	7:0	R/W	0x0A	7:0 bits of Low bound 2 for strong low pass filter before VCTI Range : 0~1023		cc:reg_vcti_lpf_lowbound2

Register:: SR_VCTI_LPF_HBOUND2_HSB						0x11C6
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	-	0	Reserved		
SR_VCTI_LPF_HBOUN	1:0	R/W	0x0	9:8 bits of High bound 2 for strong low pass filter before VCTI		cc:reg_vcti

D2[9:8]				Range : 0~1023	lpf_highbound2
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Register:: SR_VCTI_LPF_HBOUND2_LSB					0x11C7
Name	bits	R/W/D	Reset State	Comments	Config
SR_VCTI_LPF_HBOUN D2[7:0]	7:0	R/W	0x96	7:0 bits of High bound 2 for strong low pass filter before VCTI Range : 0~1023	cc:reg_vcti_lpf_highbound2

Register:: SR_VCTI_LPF_LBOUND1_HSB					0x11C8
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_VCTI_LPF_LBOUN D1[9:8]	1:0	R/W	0x0	9:8 bits of Low bound 1 for strong low pass filter before VCTI Range : 0~1023	cc:reg_vcti_lpf_lowbound1

Register:: SR_VCTI_LPF_LBOUND1_LSB					0x11C9
Name	Bits	Read/Write	Reset State	Comments	Config
SR_VCTI_LPF_LBOUN D1[7:0]	7:0	R/W	0x0	7:0 bits of Low bound 1 for strong low pass filter before VCTI Range : 0~1023	cc:reg_vcti_lpf_lowbound1

Register:: SR_VCTI_LPF_HBOUND1_HSB					0x11CA
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_VCTI_LPF_HBOUN D1[9:8]	1:0	R/W	0x0	9:8 bits of High bound 1 for strong low pass filter before VCTI Range : 0~1023	cc:reg_vcti_lpf_highbound1

Register:: SR_VCTI_LPF_HBOUND1_LSB					0x11CB
Name	Bits	Read/Write	Reset State	Comments	Config
SR_VCTI_LPF_HBOUN D1[7:0]	7:0	R/W	0x64	7:0 bits of High bound 1 for strong low pass filter before VCTI Range : 0~1023	cc:reg_vcti_lpf_highbound1

Register:: VPK_VCTI_HLW_H_START_HIGH					0x11CC
Name	Bits	Read/Write	Reset State	Comments	Config
reserved	7:4	--	--	reserved	
VPK_HLW_HSTART_high	3:0	R/W	0	Highlight window horizontal start[11:8] VPK/VCTI HLW Horizontal position refers to timing of S domain	

Register:: VPK_VCTI_HLW_H_START_LOW					0x11CD
Name	Bits	Read/Write	Reset State	Comments	Config
VPK_HLW_HSTART_low	7:0	R/W	0x00	Highlight window horizontal start[7:0]	

Register:: VPK_VCTI_HLW_H_END_HIGH						0x11CE
Name	Bits	Read/Write	Reset State	Comments		Config
reserved	7:4	--	--	reserved		
VPK_HLW_HEND_hi	3:0	R/W	0	Highlight window horizontal end[11:8]		

Register:: VPK_VCTI_HLW_H_END_LOW						0x11CF
Name	Bits	Read/Write	Reset State	Comments		Config
VPK_HLW_HEND_low	7:0	R/W	0x00	Highlight window horizontal end[7:0]		

Register:: VPK_VCTI_HLW_V_START_HIGH						0x11D0
Name	Bits	Read/Write	Reset State	Comments		Config
reserved	7:4	--	--	reserved		
VPK_HLW_VSTART_high	3:0	R/W	0	Highlight window vertical start[11:8] VPK/VCTI HLW Vertical position refers to timing of D domain		

Register:: VPK_VCTI_HLW_V_START_LOW						0x11D1
Name	Bits	Read/Write	Reset State	Comments		Config
VPK_HLW_VSTART_low	7:0	R/W	0x00	Highlight window vertical start[7:0]		

Register:: VPK_VCTI_HLW_V_END_HIGH						0x11D2
Name	Bits	Read/Write	Reset State	Comments		Config
reserved	7:4	--	--	reserved		
VPK_HLW_VEND_high	3:0	R/W	0	Highlight window vertical start[11:8]		

Register:: VPK_VCTI_HLW_V_END_LOW						0x11D3
Name	Bits	Read/Write	Reset State	Comments		Config
VPK_HLW_VEND_low	7:0	R/W	0x00	Highlight window vertical end[7:0]		

Register:: IDCLTI_HLW_Hor_start_H						0x11D4
Name	Bits	Read/Write	Reset State	Comments		Config
reserved	7:4	--	--	reserved		
IDCLTI_Win_hstart[11:8]	3:0	R/W	0	IDCLTI Highlight window horizontal start[11:8]		

Register:: IDCLTI_HLW_Hor_start_L						0x11D5
Name	Bits	Read/Write	Reset State	Comments		Config
IDCLTI_Win_hstart[7:0]	7:0	R/W	0	IDCLTI Highlight window horizontal start[7:0]		

Register:: IDCLTI_HLW_Hor_end_H					0x11D6
Name	Bits	Read/Write	Reset State	Comments	Config
reserved	7:4	--	--	reserved	
IDCLTI_Win_hend[11:8]	3:0	R/W	0	IDCLTI Highlight window horizontal end[11:8]	

Register:: IDCLTI_HLW_Hor_end_L					0x11D7
Name	Bits	Read/Write	Reset State	Comments	Config
IDCLTI_Win_hend[7:0]	7:0	R/W	0	IDCLTI Highlight window horizontal end[7:0]	

Register:: IDCLTI_HLW_Ver_start_H					0x11D8
Name	Bits	Read/Write	Reset State	Comments	Config
reserved	7:4	--	--	reserved	
IDCLTI_Win_vstart[11:8]	3:0	R/W	0	IDCLTI Highlight window Vertical start[11:8]	

Register:: IDCLTI_HLW_Ver_start_L					0x11D9
Name	Bits	Read/Write	Reset State	Comments	Config
IDCLTI_Win_vstart[7:0]	7:0	R/W	0	IDCLTI Highlight window vertical start[7:0]	

Register:: IDCLTI_HLW_Ver_end_H					0x11DA
Name	Bits	Read/Write	Reset State	Comments	Config
reserved	7:4	--	--	reserved	
IDCLTI_Win_vend[11:8]	3:0	R/W	0	IDCLTI Highlight window Vertical end[11:8]	

Register:: IDCLTI_HLW_Ver_end_L					0x11DB
Name	Bits	Read/Write	Reset State	Comments	Config
IDCLTI_Win_vend[7:0]	7:0	R/W	0	IDCLTI Highlight window vertical end[7:0]	

Register:: IDCLTI_HLW_ctrl					0x11DC
Name	Bits	Read/Write	Reset State	Comments	Config
reserved	7:2	--	--	reserved	
IDCLTI_HW	1	R/W	0	Enable IDCLTI highlight window 0 : disable HW 1 : enable This setting is effective in both IDCLTI	
IDLCTI_HW_CTRL	0	R/W	0	0: IDCLTI used inside highlight window. 1: IDCLTI used outside highlight window.	

0x11DD~0x11EF are reserved

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D Domain DLTi

Register:: D_DLTi_Options					0x11F0
Name	Bits	Read/Write	Reset State	Comments	Config
vivid_test_mode	7:6	R/W	0	2'b00: { st_pol_past[1:0], st_pol_future[1:0], w_sel_past[1:0], w_sel_future[1:0], wpn_bt_ln, ln_bt_xfn, xfn_bt_xpn, ovth, decnt[2:0], status0[1:0], signi_p1_store[1:0], signi_f1_store[1:0], precond_hit[3:0], ch_past_long, ch_ori_long, ch_past_near, ch_ori_near, equal } 2'b01: { cr_w_lt0, cr_w_st0, cr_pe_bypass, cr_deltaout_stg1 [1:0], cr_deltaout_stg2[1:0], cr_wpn_bt_ln_stg1, cr_ln_bt_xfn_stg1, cr_xfn_bt_xpn_stg1, cr_wpn_bt_ln_stg2, cr_ln_bt_xfn_stg2, cr_xfn_bt_xpn_stg2, 2'b00 ; cb_w_lt0, cb_w_st0, cb_pe_bypass, cb_deltaout_stg1 [1:0], cb_deltaout_stg2[1:0], cb_wpn_bt_ln_stg1, cb_ln_bt_xfn_stg1, cb_xfn_bt_xpn_stg1, cb_wpn_bt_ln_stg2, cb_ln_bt_xfn_stg2, cb_xfn_bt_xpn_stg2, 2'b00 } ; 2'b10: { dvs_dlyout, dhs_dlyout, colin_den_dlyout, inwin_den_dlyout, dvs_2pk, main_en_2pk, shpnrcm_region[1:0], shpnrc_weight_sum[8:0], gain_pow_new_tmp_d[9:0], 2'b0 } ; 2'b11: reserved	
M_DLTi_EN	5	R/W/D	0	Enable D domain DLTi 0: disable 1: enable	cc:reg_vc_DL Ti_Enable
HF_Th_Enabled	4	R/W	1	Check High Frequency Line Data for skip DLTi Process. 0: Disable 1: Enable	cc:m_reg_vc_DL Ti_HF_Ena bled
Advance_Delay	3	R/W	0	Advance Delay Points 0: Disable 1: Enable	cc:m_reg_vc_DL Ti_Opt_Ad v
Prevent_Long	2	R/W	1	Prevent Edge on Long distances 0: Disable 1: Enable	cc:m_reg_vc_DL Ti_Opt_Lo ng
Prevent_Near	1	R/W	1	Prevent 2 points too close. 0: Disable 1: Enable	cc:m_reg_vc_DL Ti_Opt_Ne ar
Prevent_Contour	0	R/W	1	Prevent contour 0: Disable 1: Enable	cc:m_reg_vc_DL Ti_Opt_Co ntour_Enable

Register:: D_DLTi_Value_0					0x11F1
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7	-	0	Reserved	
HF_Th_Value	6:0	R/W	0x2A	Threshold Value for check high frequency data Valid Range: 0~128 (128+), Default Value: 42 (8-bit),	cc:m_reg_vc_DL Ti_HF_Val ue

Register:: D_DLTi_Value_1					0x11F2
Name	Bits	Read/Write	Reset State	Comments	Config
Prevent_Contour_Th	7:4	R/W	0x6	Prevent contour threshold (4-bit) Valid Range: 0~15, Default Value: 6 (8-bit), 24 (10-bit)	cc:m_reg_vc_DL Ti_Opt_Co ntour_Th
Gain_Value	3:0	R/W	0x05	Adjust DLTi Gain Value(4-bit)	cc:m_reg_vc_

				Valid Range: 0~15 (8-bit)	DLTi_Gain_Value
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Register:: D_DLTI_Value_2					0x11F3
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:6	-	-	Reserved	
Th_Value	5:0	R/W	0x1E	Up and Down Limit for DLTI_Gain Result Value (6-bit) Valid Range: 0~63 (8-bit),	cc:m_reg_vc_DLTI_Gain_Th

D Domain DCTI

Register:: D_DCTi_CTRL 0x11F4					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:3	-	-	Reserved	
Prevent_PE	2	R/W/D	1	Prevent Phase Error Mode 0: Disable 1: Enable	cc:m_reg_vc_DCTi_PE_Prevent
M_DCTI_EN	1	R/W	0	Enable D domain DCTI 0: disable 1: enable	cc:reg_vc_DCTi_Enab le
2nd_DCti_Enabled	0	R/W	1	Gain Control for 2 nd DCTi 0: Disable 1: Enable	cc:m_reg_vc_DCTi_2 nd _Ena ble

Register:: D_DCTi_1st_TH_Value 0x11F5					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:6	-	-	Reserved	
Th_Value	5:0	R/W	1E	Up and Down Limit for DCTi_Gain Result Value (6-bit) Valid Range: 0~63 (8-bit),	cc:m_reg_vc_DCTi_Gain_Th

Register:: D_DCTi_1st_GAIN_VALUE 0x11F6					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:5	-	-	Reserved	
Gain_Value	4:0	R/W	0A	Adjust DCTi Gain Value(4-bit) Valid Range: 0~31 (8-bit)	cc:m_reg_vc_DCTi_Gain_Value

Register:: D_DCTi_2nd_TH_Value 0x11F7					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:6	-	-	Reserved	
Th_Value	5:0	R/W	1E	Up and Down Limit for DCTi_Gain Result Value (6-bit) Valid Range: 0~63 (8-bit),	cc:m_reg_vc_DCTi_2 nd _Th

Register:: D_DCTi_2nd_GAIN_Value 0x11F8					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:5	-	-	Reserved	
Gain_Value	4:0	R/W	0A	Adjust DCTi Gain Value(4-bit) Valid Range: 0~31 (8-bit)	cc:m_reg_vc_DCTi_2 nd _Gain_Value

UV Delay

Register:: UV_Delay					0x11F9
Name	Bits	Read/ Write	Reset State	Comments	Config
UV_Delay_En	7	R/W	0	Enable UV delay for color boundary Delay or advance U/V components, and after shifting repeat data on boundary 0: disable 1: enable	Cc:reg_vc_main_uv_delay_Enable
U_Delay	6:4	R/W	0	Set U delay Positive value: delay negative value: advance 000:0 001:-1 010:-2 101:1 110:2 011,100,111: reserved	Cc:reg_vc_main_u_delay
Reserved	3	-	0	Reserved	
V_Delay	2:0	R/W	0	Set V delay Positive value: delay negative value: advance 000:0 001:-1 010:-2 101:1 110:2 011,100,111: reserved	Cc:reg_vc_main_v_delay

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Sharpness

Register::SR_SHP_CTRL							0x12A0
Name	bits	R/W/D	Reset State	Comments			Config
Ver_HPF_C	7	R/W/D	0x0	Coefficients of Vertical High-pass Filter (Select Sharpness 1D mode or 2D mode) 0: 1D mode, coef: [0 ; 0; 0] (undo vertical high pass filter) 1: 2D mode, coef: [-1; 2 ; -1]			cc:m_reg_vc_2D_PC_Ver_HPF_C
M_Sharp_EN	6	R/W/D	0	Enable Main Channel Sharpness(include 1D and 2D) 0: disable 1: enable			cc:reg_vc_Sharpness_Enable
Dummy	5	-	0	Reserved			
CLP_Enable	4	R/W/D	1	Chrominance Low-pass Enable 0: Disable 1: Enable			cc:m_reg_vc_CLP_Enable
RIPV_Enable	3	R/W/D	1	Reduced Isolated Peak Value Enable 0: Disable 1: Enable			cc:m_reg_vc_RIPV_Enable
ECS_Enable	2	R/W/D	1	Ease Contour and Sawtooth Enable 0: Disable 1: Enable			cc:m_reg_vc_ECS_Enable
EMF_Enable	1	R/W/D	1	Extend Medain Filter Enable (when Peaking_Enable=1) 0: Disable 1: Enable			cc:m_reg_vc_EMF_Enable
Peaking_Enable	0	R/W/D	1	Peaking and Coring Enable (when Sharpness_EN =1) 0: Disable 1: Enable			cc:m_reg_vc_Peaking_Enable

Register::SR_SHP_BIST_CTRL							0x12A1
Name	bits	R/W/D	Reset State	Comments			Config
Reserved	7:4	-	0x0	Reserved			
SHP_BIST_ENABLE	3	R/W	0x0	Sharpness BIST_En 0: BIST disable (Default) 1: BIST enable			
SHP_BIST_PERIOD_PR_O	2	R	0x0	SharpnessBIST_Period Progress 0: BIST is running 1: BIST is done (Default)			
SHP_BIST_TEST_Result_EVEN	1	R	0x0	SharpnessBIST Test Result Mem even (It will go low first during BIST period) 0: SRAM OK 1: SRAM Fail			
SHP_BIST_TEST_Result_ODD	0	R	0x0	SharpnessBIST Test Result Mem odd (It will go low first during BIST period) 0: SRAM OK 1: SRAM Fail			

Peaking Coefficient

Register::SR_PEAKING_FILTER_0							0x12A2
Name	bits	R/W/D	Reset State	Comments			Config

Ver_HPF_Gain	7:6	R/W	0x1	Gain for Vertical High-pass Filter 00: 1 01: 1/2 10: 1/4 11: 1/8	cc:m_reg_v c_2D_PC_V er_HPF_Gai n
Sh_B0	5:4	R/W	`d0	SHRR(c[i]*x[n-i], 4+Sh_B0) (Sh_B0 : 0~3) 00:Default	Cc: m_reg_vc_P C_Shift_B0
Sh_B1	3:2	R/W	`d0	SHRR(SUM(SHRR(c[i]*x[n-i], 4+Sh_B0)), 2+Sh_B1) (Sh_B1 : 0~3) 00:Default	Cc: m_reg_vc_P C_Shift_B1
Dummy	1:0	-	0	Reserved	

Register::SR_PEAKING_FILTER_C0_HSB 0x12A3					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	-	0	Reserved	
SR_PEAKING_FILTER_C0[8]	0	R/W	`d1	Bit 8 of Horizontal Peaking Filter Coefficient C0 (C0 : 0~511)	cc:m_reg_v c_PC_Hor_Filter_C0

Register::SR_PEAKING_FILTER_C0_LSB 0x12A4					
Name	bits	R/W/D	Reset State	Comments	Config
SR_PEAKING_FILTER_C0[7:0]	7:0	R/W	`d26	7:0 bits of Horizontal Peaking Filter Coefficient C0 (C0 : 0~511)	cc:m_reg_v c_PC_Hor_Filter_C0

Register::SR_PEAKING_FILTER_C1_HSB 0x12A5					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:1	-	0	Reserved	
SR_PEAKING_FILTER_C1[8]	0	R/W	`d0	Bit 8 of Horizontal Peaking Filter Coefficient C1 (C1 : -256~255 2's Complement) -73 = 0xB7 in 2's complement	cc:m_reg_v c_PC_Hor_Filter_C1:s

Register::SR_PEAKING_FILTER_C1_LSB 0x12A6					
Name	bits	R/W/D	Reset State	Comments	Config
SR_PEAKING_FILTER_C1[7:0]	7:0	R/W	`d73	7:0 bits of Horizontal Peaking Filter Coefficient C1 (C1 : -256~255 2's Complement) -73 = 0xB7 in 2's complement	cc:m_reg_v c_PC_Hor_Filter_C1:s

Register::SR_PEAKING_FILTER_C2 0x12A7					
Name	Bits	R/W/D	Reset State	Comments	Config
C2	7:0	R/W	`d10	Horizontal Peaking Filter Coefficient C2 (C2 : -128~127 2's Complement)	cc:m_reg_v c_PC_Hor_Filter_C2:s

Register::SR_PEAKING_FILTER_C3 0x12A8					
Name	Bits	R/W/D	Reset State	Comments	Config
Reserved	7	R/W	`d0	Reserved	
C3	6:0	R/W	`d0	Horizontal Peaking Filter Coefficient C3	cc:m_reg_v

				(C3 : -64~63 2's Complement)	c_PC_Hor_Filter_C3:s
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Register::SR_PEAKING_FILTER_C4					0x12A9
Name	Bits	R/W/D	Reset State	Comments	Config
Reserved	7	R/W	`d0	Reserved	
C4	6:0	R/W	`d0	Horizontal Peaking Filter Coefficient C4 (C4 : -64~63 2's Complement)	cc:m_reg_v c_PC_Hor_Filter_C4:s

Register::SR_PEAKING_FILTER_C5					0x12AA
Name	Bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	R/W	`d0	Reserved	
C5	5:0	R/W	`d0	Horizontal Peaking Filter Coefficient C5 (C5 : -32~31 2's Complement)	cc:m_reg_v c_PC_Hor_Filter_C5:s

Register::SR_PEAKING_GAIN_Blr					0x12AB
Name	bits	R/W/D	Reset State	Comments	Config
Gain_Blr	7:0	R/W	0	Gain Value for Low-pass at Center Range in Peaking and Coring (Gain_Blr : 0/64~255/64)	cc:m_reg_v c_PC_Gain_Blr

Register::SR_PEAKING_GAIN_Pos					0x12AC
Name	bits	R/W/D	Reset State	Comments	Config
Gain_Pos	7:0	R/W	`d48	Gain Value for High-pass or Band-pass at Positive Range in Peaking and Coring (Gain_Pos : 0/64~255/64)	cc:m_reg_v c_PC_Gain_Pos

Register::SR_PEAKING_GAIN_Neg					0x12AD
Name	bits	R/W/D	Reset State	Comments	Config
Gain_Neg	7:0	R/W	`d64	Gain Value for High-pass or Band-pass at Negative Range in Peaking and Coring (Gain_Neg : 0/64~255/64)	cc:m_reg_v c_PC_Gain_Neg

Register::SR_PEAKING_BOUND_HV_Pos_HSB					0x12AE
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:2	--	0	Reserved	
SR_PEAKING_BOUND_HV_Pos[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023)	cc:m_reg_v c_PC_HV_Pos

Register::SR_PEAKING_BOUND_HV_Pos_LSB					0x12AF
Name	bits	R/W/D	Reset State	Comments	Config
SR_PEAKING_BOUND_HV_Pos[7:0]	7:0	R/W	`d72	7:0 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023)	cc:m_reg_v c_PC_HV_Pos

Register::SR_PEAKING_BOUND_HV_Neg_HSB						0x12B0
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	--	0	Reserved		
SR_PEAKING_BOUND_HV_Neg[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023)		cc:m_reg_v c_PC_HV_Neg

Register::SR_PEAKING_BOUND_HV_Neg_LSB						0x12B1
Name	bits	R/W/D	Reset State	Comments		Config
SR_PEAKING_BOUND_HV_Neg[7:0]	7:0	R/W	`d96	7:0 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023)		cc:m_reg_v c_PC_HV_Neg

Register::SR_PEAKING_BOUND_LV						0x12B2
Name	bits	R/W/D	Reset State	Comments		Config
LV	7:0	R/W	`d16	Coring Low Level for Peaking and Coring (LV : 0~255)		cc:m_reg_v c_PC_LV

0x12B3 is reserved

Peaking EMF

Register::SR_PEAKING_EMF_Offset_HSB						0x12B4
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7	-	0	Reserved		
EMF_Shift	6:4	R/W	0x5	Delta Shift Bit of Extend Median Filter for Peaking and Coring (EMF_Shift : 0~7)		cc:m_reg_v c_PC_EMF_Shift
Reserved	3	-	0	Reserved		
SR_PEAKING_EMF_Seg0_Offset[10:8]	2:0	R/W	0x0	10:8 bits of Offset of Segment_0 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 0		cc:m_reg_v c_EMF_seg0_offset

Register::SR_PEAKING_EMF_Offset_LSB						0x12B5
Name	bits	R/W/D	Reset State	Comments		Config
SR_PEAKING_EMF_Seg0_Offset[7:0]	7:0	R/W	0x0	7:0 bits of Offset of Segment_0 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 0		cc:m_reg_v c_EMF_seg0_offset

Register::SR_PEAKING_EMF_Range						0x12B6
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	-	0	Reserved		
EMF_Range	5:4	R/W	0x1	Range of 1D and 2D Extend Median Filter 00: 1x3 01: 1x5 10: 3x3 11: 3x5 (Restriction for Main EMF:		cc:m_reg_v c_EMF_Range

				Shp1D(ver_hpf_c=0)=>range=0x0 or 0x1 Shp2D(ver_hpf_c=1)=>range=0x0 ~ 0x3) (Sub emf_range is forced to 1x5)	
Reserved	3	-	0	Reserved	
Seg0_Gain_Sel	2:0	R/W	0x6	Gain Selection of Segment_0 for Modified Extend Median Filter: delta1= gain* delta + offset Default Value: 110 (gain=4)	cc:m_reg_v c_EMF_seg 0_gain_sel

Register::SR_PEAKING_EMF_Gain 0x12B7					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7	-	0	Reserved	
Seg1_Gain_Sel	6:4	R/W	0x0	Gain Selection of Segment_1 for Modified Extend Median Filter: delta1= gain* delta + offset Default Value: 000 (gain=-2)	cc:m_reg_v c_EMF_seg 1_gain_sel
Reserved	3	-	0	Reserved	
Seg2_Gain_Sel	2:0	R/W	0x0	Gain Selection of Segment_2 for Modified Extend Median Filter: delta1= gain* delta + offset Default Value: 000 (gain=-2)	cc:m_reg_v c_EMF_seg 2_gain_sel

Register::SR_PEAKING_EMF_OFFSET_0 0x12B8					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7	--	0	Reserved	
WtSum_level	6:4	R/W	0x6	Weighting Sum Level (MSB is sign bit, use 2's complement) (Valid range: -3~3) Default Value: -2 (110)	Cc:m_reg_v c_WtSum_l evel
Reserved	3:1	--	0	Reserved	
WtSum_enable	0	R/W	0x0	Weighting Sum Enable 0: disable 1: enable (when Ver_HPF_C =1)	Cc:m_reg_v c_WtSum_e nable

Register::SR_PEAKING_EMF_OFFSET_1_HSB 0x12B9					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:3	--	0	Reserved	
SR_PEAKING_EMF_OF FSET_Seg1_Offset[10:8]	2:0	R/W	0x6	10:8 bits of Offset of Segment_1 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 1536	cc:m_reg_v c_EMF_seg 1_offset

Register::SR_PEAKING_EMF_OFFSET_1_LSB 0x12BA					
Name	bits	R/W/D	Reset State	Comments	Config
SR_PEAKING_EMF_OF FSET_Seg1_Offset[7:0]	7:0	R/W	0x00	7:0 bits of Offset of Segment_1 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 1536	cc:m_reg_v c_EMF_seg 1_offset

Register::SR_PEAKING_EMF_OFFSET_2_HSB 0x12BB					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:3	--	0	Reserved	
SR_PEAKING_EMF_OF FSET_Seg2_Offset[10:8]	2:0	R/W	0x6	10:8 bits of Offset of Segment_2 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 1536	cc:m_reg_v c_EMF_seg 2_offset

Register::SR_PEAKING_EMF_OFFSET_2_LSB						0x12BC	
Name	bits	R/W/D	Reset State	Comments			Config
SR_PEAKING_EMF_OF FSET_Seg2_Offset[7:0]	7:0	R/W	0x00	7:0 bits of Offset of Segment_2 for Modified Extend Median Filter: (Seg0_Offset : 0~2047) Default Value: 1536			cc:m_reg_vc_c_EMF_seg2_offset

EMF_MKII

Register::DM_EMFMK2_CTRL_0						0x12BD	
Name	bits	R/W/D	Reset State	Comments			Config
Reserved	7:5	R/W	0	Reserved			
DeclineBit	4:3	R/W	0	To decrease EMF affect Valid range:0~3			Cc:m_reg_vc_EMFMk2_DeclineBit
BlendStepBit	2:0	R/W	0x5	Blend step = 1<< BlendStepBit Valid range:0~7			Cc:m_reg_vc_EMFMk2_BlendDeltaBit

Register::DM_EMFMK2_CTRL_1						0x12BE	
Name	bits	R/W/D	Reset State	Comments			Config
Reserved	7	-	0	Reserved			
AOV_Range	6	R/W	0	0: 11 tap AOV 1: 5 tap AOV			Cc:m_reg_vc_EMFMk2_AOVRANGE
EMF_Mk2_debug	5	R/W	0	0: disable EMF_MkII debug mode 1: enable EMF_MkII debug mode			Cc:m_reg_vc_EMFMk2_debug
EMF_mode_sel	4	R/W	0	0: EMF mode 1 (original EMF) 1: EMF mode 2 (Enable EMF_MkII)			Cc:m_reg_vc_EMF_mode_sel
Reserved	3:2	-	0	Reserved			
DM_EMFMK2_LowBnd[9:8]	1:0	R/W	0	9:8 bits of Lower bound of blending process Valid range:0~1023			Cc:m_reg_vc_EMFMk2_LowBnd

Register::DM_EMFMK2_CTRL_2						0x12BF	
Name	bits	R/W/D	Reset State	Comments			Config
DM_EMFMK2_LowBnd[7:0]	7:0	R/W	0x64	7:0 bits of Lower bound of blending process Valid range:0~1023			Cc:m_reg_vc_EMFMk2_LowBnd

EMF Gain Select Table

Gain Select	0	1	2	3	4	5	6
Gain Value	-2	-1	-1/2	-1/4	1	2	4

Peaking ECS

Register::SR_ECS_CTRL_0						0x12C0
Name	bits	R/W/D	Reset State	Comments		Config
Contour_Side	7:6	R/W	0	Contour Side for Ease Contour and Sawtooth. 00 : Two Side 01 : Left Side 10 : Right Side 11 : Reserved		cc:m_reg_v c_ECS_Con tour_Side
Contour_PxlSel	5:4	R/W	0	Contour Pixel Select for Ease Contour and Sawtooth. 00 : 5 pixels 01 : 7 pixels 10 : 9 pixels 11 : Reserved		cc:m_reg_v c_ECS_Con tour_PxlSel
Sawtooth_Step	3:0	R/W	4	Sawtooth Step for Ease Contour and Sawtooth. (Sawtooth_Step : 0~15)		cc:m_reg_v c_ECS_Saw tooth_Step

Register::SR_ECS_CTRL_1						0x12C1
Name	bits	R/W/D	Reset State	Comments		Config
Right_Neg_Sign	7:6	R/W	0	Sign of Saw-tooth del in Right and Negative Side 00 : Yo=Yi-del (Default) 01 : Yo=Yi+del 10 : Yo=Yi 11 : Reserved		cc:m_reg_v c_ECS_Rig ht_Neg_Sig n
Right_Pos_Sign	5:4	R/W	1	Sign of Saw-tooth del in Right and Positive Side 00 : Yo=Yi-del 01 : Yo=Yi+del (Default) 10 : Yo=Yi 11 : Reserved		cc:m_reg_v c_ECS_Rig ht_Pos_Sign
Left_Neg_Sign	3:2	R/W	1	Sign of Saw-tooth del in Left and Negative Side 00 : Yo=Yi-del 01 : Yo=Yi+del (Default) 10 : Yo=Yi 11 : Reserved		cc:m_reg_v c_ECS_Left _Neg_Sign
Left_Pos_Sign	1:0	R/W	0	Sign of Saw-tooth del in Left and Positive Side 00 : Yo=Yi-del (Default) 01 : Yo=Yi+del 10 : Yo=Yi 11 : Reserved		cc:m_reg_v c_ECS_Left _Pos_Sign

Register:: SR_ECS_THL_Noise_HSB						0x12C2
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	--	0	Reserved		
SR_ECS_THL_Noise_Level[9:8]	1:0	R/W	`d0	9:8 bits of Contour Noise Level for Ease Contour and Sawtooth. (Contour_Noise_Level : 0~1023)		cc:m_reg_v c_ECS_No ise_Leve

Register::SR_ECS_THL_Noise_LSB						0x12C3
Name	bits	R/W/D	Reset	Comments		Config

			State		
SR_ECS_THL_Noise_Level[7:0]	7:0	R/W	`d16	7:0 bits of Contour Noise Level for Ease Contour and Sawtooth. (Contour_Noise_Level : 0~1023)	cc:m_reg_vc_ECS_Noise_Level

Register:: SR_ECS_THL_Contour_HSB					0x12C4
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:2	--	0	Reserved	
SR_ECS_THL_Contour_Contour_Thd[9:8]	1:0	R/W	`d0	9:8 bits of Contour Threshold for Ease Contour and Sawtooth. (Contour_Thd : 0~1023)	cc:m_reg_vc_ECS_Contour_Thd

Register:: SR_ECS_THL_Contour_LSB					0x12C5
Name	bits	R/W/D	Reset State	Comments	Config
SR_ECS_THL_Contour_Contour_Thd[7:0]	7:0	R/W	`d64	7:0 bits of Contour Threshold for Ease Contour and Sawtooth. (Contour_Thd : 0~1023)	cc:m_reg_vc_ECS_Contour_Thd

Register:: SR_ECS_THL_Sawtooth_HSB					0x12C6
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:2	--	0	Reserved	
SR_ECS_THL_Sawtooth_Sawtooth_Thd[9:8]	1:0	R/W	1	9:8 bits of Sawtooth Threshold for Ease Contour and Sawtooth. (Sawtooth_Thd : 0~1023)	cc:m_reg_vc_ECS_Sawtooth_Thd

Register:: SR_ECS_THL_Sawtooth_LSB					0x12C7
Name	bits	R/W/D	Reset State	Comments	Config
SR_ECS_THL_Sawtooth_Sawtooth_Thd[7:0]	7:0	R/W	0x00	7:0 bits of Sawtooth Threshold for Ease Contour and Sawtooth. (Sawtooth_Thd : 0~1023)	cc:m_reg_vc_ECS_Sawtooth_Thd

RIPV

Register:: SR_RIPV_DATA					0x12C8
Name	bits	R/W/D	Reset State	Comments	Config
Ratio	7:4	R/W	0x7	Ratio for Reduced Isolated Peak Value (Ratio : 0/8~15/8)	cc:m_reg_vc_RIPV_Ratio
Reserved	3	-	0	Reserved	
PxlSel	2	R/W	0x1	Reduced Isolated Peak Value Pixel Select (Pixel Select=0 : 3 pixel , Pixel Select=1 : 5 pixel)	cc:m_reg_vc_RIPV_PxlSel
SR_RIPV_DATA_Thd[9:8]	1:0	R/W	`d0	9:8 bits of Threshold Value for Reduced Isolated Peak Value (Threshold : 0~1023)	cc:m_reg_vc_RIPV_Thd

Register:: SR_RIPV_Thd					0x12C9
Name	bits	R/W/D	Reset State	Comments	Config

SR_RIPV_DATA _Thd[7:0]	7:0	R/W	`d64	7:0 bits of Threshold Value for Reduced Isolated Peak Value (Threshold : 0~1023)	cc:m_reg_v c_RIPV_Th d
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Chroma Lowpass

Register::SR_CHROMA_LOWPASS 0x12CA					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:5	--	0	Reserved	
Blur_Fac	4:0	R/W	8	Blur Factor for Chrominance Low Pass (Blur_Fac : 0~31)	cc:m_reg_v c_CLP_Blur _Fac

Auto Sharpness

Register::SR_AUTO_SHP_CTRL 0x12CB					
Name	bits	R/W/D	Reset State	Comments	Config
Dummy	7:6	--	0	Reserved	
Finish_Flag	5	R	0	this bit will be set to 1, if one frame summation is done this bit will be set to 0, when auto sharpness enable is set to 0	
Enable	4	R/W	0	Auto Sharpness Enable <u>(It will be auto cleared after one frame summation done)</u> 0 : Disable 1 : Enable	cc:m_reg_v c_Auto_SH P_Enable
Shift_Bit	3:0	R/W	8	Auto Sharpness FIR Data Shift Right Bits. (Shift_Bit : 0~15)	cc:m_reg_v c_AUTO_S HP_Shift_B it

Register::SR_AUTO_SHP_BIN0_OFFSET 0x12CC					
Name	bits	R/W/D	Reset State	Comments	Config
BIN0_Offset	7:0	R/W	0	Auto Sharpness Bin[0] Offset (BIN0_Offset : 0~255)	cc:m_reg_v c_AUTO_S HP_BIN0_ Offset

Register::SR_AUTO_SHP_Y_LB 0x12CD					
Name	bits	R/W/D	Reset State	Comments	Config
Y_LB	7:0	R/W	0	Auto Sharpness Y Range Lower Bound (Y_LB : 0*2~255*2)	cc:m_reg_v c_AUTO_S HP_Y_LB

Register::SR_AUTO_SHP_Y_UB 0x12CE					
Name	bits	R/W/D	Reset State	Comments	Config
Y_UB	7:0	R/W	`d255	Auto Sharpness Y Range Upper Bound (Y_UB : 0*2+513~255*2+513)	cc:m_reg_v c_AUTO_S HP_Y_UB

Register::SR_AUTO_SHP_FIR_COUNT_00_H						0x12CF
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_00[21:16]	5:0	R	0	21:16 bits FIR_Count[0]. (FIR_Count[0] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[0]

Register::SR_AUTO_SHP_FIR_COUNT_00_M						0x12D0
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_00[15:8]	7:0	R	0	15:8 bits FIR_Count[0]. (FIR_Count[0] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[0]

Register::SR_AUTO_SHP_FIR_COUNT_00_L						0x12D1
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_00[7:0]	7:0	R	0	7:0 bits of FIR_Count[0]. (FIR_Count[0] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[0]

Register::SR_AUTO_SHP_FIR_COUNT_01_H						0x12D2
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_01[21:16]	5:0	R	0	21:16 bits FIR_Count[1]. (FIR_Count[1] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[1]

Register::SR_AUTO_SHP_FIR_COUNT_01_M						0x12D3
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_01[15:8]	7:0	R	0	15:8 bits FIR_Count[1]. (FIR_Count[1] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[1]

Register::SR_AUTO_SHP_FIR_COUNT_01_L						0x12D4
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_01[7:0]	7:0	R	0	7:0 bits of FIR_Count[1]. (FIR_Count[1] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[1]

Register::SR_AUTO_SHP_FIR_COUNT_02_H						0x12D5
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_02[21:16]	5:0	R	0	21:16 bits FIR_Count[2]. (FIR_Count[2] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[2]

Register::SR_AUTO_SHP_FIR_COUNT_02_M						0x12D6
Name	bits	R/W/D	Reset State	Comments		Config

SR_AUTO_SHP_FIR_C OUNT_02[15:8]	7:0	R	0	15:8 bits FIR_Count[2]. (FIR_Count[2] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[2]
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Register::SR_AUTO_SHP_FIR_COUNT_02_L					0x12D7
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_02[7:0]	7:0	R	0	7:0 bits of FIR_Count[2]. (FIR_Count[2] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[2]

Register::SR_AUTO_SHP_FIR_COUNT_03_H					0x12D8
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_03[21:16]	5:0	R	0	21:16 bits FIR_Count[3]. (FIR_Count[3] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[3]

Register::SR_AUTO_SHP_FIR_COUNT_03_M					0x12D9
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_03[15:8]	7:0	R	0	15:8 bits FIR_Count[3]. (FIR_Count[3] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[3]

Register::SR_AUTO_SHP_FIR_COUNT_03_L					0x12DA
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_03[7:0]	7:0	R	0	7:0 bits of FIR_Count[3]. (FIR_Count[3] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[3]

Register::SR_AUTO_SHP_FIR_COUNT_04_H					0x12DB
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_04[21:16]	5:0	R	0	21:16 bits FIR_Count[4]. (FIR_Count[4] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[4]

Register::SR_AUTO_SHP_FIR_COUNT_04_M					0x12DC
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_04[15:8]	7:0	R	0	15:8 bits FIR_Count[4]. (FIR_Count[4] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[4]

Register::SR_AUTO_SHP_FIR_COUNT_04_L					0x12DD
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_04[7:0]	7:0	R	0	7:0 bits of FIR_Count[4]. (FIR_Count[4] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[4]

Register::SR_AUTO_SHP_FIR_COUNT_05_H						0x12DE
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_05[21:16]	5:0	R	0	21:16 bits FIR_Count[5]. (FIR_Count[5] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[5]

Register::SR_AUTO_SHP_FIR_COUNT_05_M						0x12DF
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_05[15:8]	7:0	R	0	15:8 bits FIR_Count[5]. (FIR_Count[5] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[5]

Register::SR_AUTO_SHP_FIR_COUNT_05_L						0x12E0
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_05[7:0]	7:0	R	0	7:0 bits of FIR_Count[5]. (FIR_Count[5] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[5]

Register::SR_AUTO_SHP_FIR_COUNT_06_H						0x12E1
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_06[21:16]	5:0	R	0	21:16 bits FIR_Count[6]. (FIR_Count[6] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[6]

Register::SR_AUTO_SHP_FIR_COUNT_06_M						0x12E2
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_06[15:8]	7:0	R	0	15:8 bits FIR_Count[6]. (FIR_Count[6] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[6]

Register::SR_AUTO_SHP_FIR_COUNT_06_L						0x12E3
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_06[7:0]	7:0	R	0	7:0 bits of FIR_Count[6]. (FIR_Count[6] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[6]

Register::SR_AUTO_SHP_FIR_COUNT_07_H						0x12E4
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_07[21:16]	5:0	R	0	21:16 bits FIR_Count[7]. (FIR_Count[7] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[7]

Register::SR_AUTO_SHP_FIR_COUNT_07_M						0x12E5
Name	bits	R/W/D	Reset State	Comments		Config

SR_AUTO_SHP_FIR_C OUNT_07[15:8]	7:0	R	0	15:8 bits FIR_Count[7]. (FIR_Count[7] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[7]
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Register::SR_AUTO_SHP_FIR_COUNT_07_L					0x12E6
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_07[7:0]	7:0	R	0	7:0 bits of FIR_Count[7]. (FIR_Count[7] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[7]

Register::SR_AUTO_SHP_FIR_COUNT_08_H					0x12E7
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_08[21:16]	5:0	R	0	21:16 bits FIR_Count[8]. (FIR_Count[8] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[8]

Register::SR_AUTO_SHP_FIR_COUNT_08_M					0x12E8
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_08[15:8]	7:0	R	0	15:8 bits FIR_Count[8]. (FIR_Count[8] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[8]

Register::SR_AUTO_SHP_FIR_COUNT_08_L					0x12E9
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_08[7:0]	7:0	R	0	7:0 bits of FIR_Count[8]. (FIR_Count[8] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[8]

Register::SR_AUTO_SHP_FIR_COUNT_09_H					0x12EA
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_09[21:16]	5:0	R	0	21:16 bits FIR_Count[9]. (FIR_Count[9] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[9]

Register::SR_AUTO_SHP_FIR_COUNT_09_M					0x12EB
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_09[15:8]	7:0	R	0	15:8 bits FIR_Count[9]. (FIR_Count[9] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[9]

Register::SR_AUTO_SHP_FIR_COUNT_09_L					0x12EC
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_09[7:0]	7:0	R	0	7:0 bits of FIR_Count[9]. (FIR_Count[9] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[9]

Register::SR_AUTO_SHP_FIR_COUNT_10_H						0x12ED
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_COUNT_10[21:16]	5:0	R	0	21:16 bits FIR_Count[10]. (FIR_Count[10] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[10]

Register::SR_AUTO_SHP_FIR_COUNT_10_M						0x12EE
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_COUNT_10[15:8]	7:0	R	0	15:8 bits FIR_Count[10]. (FIR_Count[10] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[10]

Register::SR_AUTO_SHP_FIR_COUNT_10_L						0x12EF
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_COUNT_10[7:0]	7:0	R	0	7:0 bits of FIR_Count[10]. (FIR_Count[10] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[10]

Register::SR_AUTO_SHP_FIR_COUNT_11_H						0x12F0
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_COUNT_11[21:16]	5:0	R	0	21:16 bits FIR_Count[11]. (FIR_Count[11] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[11]

Register::SR_AUTO_SHP_FIR_COUNT_11_M						0x12F1
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_COUNT_11[15:8]	7:0	R	0	15:8 bits FIR_Count[11]. (FIR_Count[11] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[11]

Register::SR_AUTO_SHP_FIR_COUNT_11_L						0x12F2
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_COUNT_11[7:0]	7:0	R	0	7:0 bits of FIR_Count[11]. (FIR_Count[11] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[11]

Register::SR_AUTO_SHP_FIR_COUNT_12_H						0x12F3
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_COUNT_12[21:16]	5:0	R	0	21:16 bits FIR_Count[12]. (FIR_Count[12] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp_Count[12]

Register::SR_AUTO_SHP_FIR_COUNT_12_M						0x12F4
Name	bits	R/W/D	Reset State	Comments		Config

SR_AUTO_SHP_FIR_C OUNT_12[15:8]	7:0	R	0	15:8 bits FIR_Count[12]. (FIR_Count[12] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[12]
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Register::SR_AUTO_SHP_FIR_COUNT_12_L					0x12F5
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_12[7:0]	7:0	R	0	7:0 bits of FIR_Count[12]. (FIR_Count[12] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[12]

Register::SR_AUTO_SHP_FIR_COUNT_13_H					0x12F6
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_13[21:16]	5:0	R	0	21:16 bits FIR_Count[13]. (FIR_Count[13] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[13]

Register::SR_AUTO_SHP_FIR_COUNT_13_M					0x12F7
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_13[15:8]	7:0	R	0	15:8 bits FIR_Count[13]. (FIR_Count[13] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[13]

Register::SR_AUTO_SHP_FIR_COUNT_13_L					0x12F8
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_13[7:0]	7:0	R	0	7:0 bits of FIR_Count[13]. (FIR_Count[13] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[13]

Register::SR_AUTO_SHP_FIR_COUNT_14_H					0x12F9
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--	0	Reserved	
SR_AUTO_SHP_FIR_C OUNT_14[21:16]	5:0	R	0	21:16 bits FIR_Count[14]. (FIR_Count[14] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[14]

Register::SR_AUTO_SHP_FIR_COUNT_14_M					0x12FA
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_14[15:8]	7:0	R	0	15:8 bits FIR_Count[4]. (FIR_Count[14] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[14]

Register::SR_AUTO_SHP_FIR_COUNT_14_L					0x12FB
Name	bits	R/W/D	Reset State	Comments	Config
SR_AUTO_SHP_FIR_C OUNT_14[7:0]	7:0	R	0	7:0 bits of FIR_Count[14]. (FIR_Count[14] : 0~2048*1192)	cc:m_reg_v c_Auto_Shp _Count[14]

Register::SR_AUTO_SHP_FIR_COUNT_15_H						0x12FC
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:6	--	0	Reserved		
SR_AUTO_SHP_FIR_C OUNT_15[21:16]	5:0	R	0	21:16 bits FIR_Count[15]. (FIR_Count[15] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[15]

Register::SR_AUTO_SHP_FIR_COUNT_15_M						0x12FD
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_15[15:8]	7:0	R	0	15:8 bits FIR_Count[15]. (FIR_Count[15] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[15]

Register::SR_AUTO_SHP_FIR_COUNT_15_L						0x12FE
Name	bits	R/W/D	Reset State	Comments		Config
SR_AUTO_SHP_FIR_C OUNT_15[7:0]	7:0	R	0	7:0 bits of FIR_Count[15]. (FIR_Count[15] : 0~2048*1192)		cc:m_reg_v c_Auto_Shp _Count[15]

0x12FF is reserved

Ultra Vivid (Page 13)

Color Dependent Sharpness

Register:: SR_CDS_CTRL 0x13A0					
Name	Bits	Read/Write	Reset State	Comments	Config
Dummy	7	--	--	Reserved	
CDS_CM5_Enable	6	R/W	0	CM5 Enable (Color Modifier 5 : Blue) 0: Disable 1: Enable Valid Range: 0~1, Default Value: 0	cc:m_reg_vc_CDS_CM5_Enable
CDS_CM1_Enable	5	R/W	0	CM1 Enable (Color Modifier 1 : Flesh-tone) 0: Disable 1: Enable Valid Range: 0~1, Default Value: 0	cc:m_reg_vc_CDS_CM1_Enable
CDS_Enable	4	R/W/D	0	Color Dependent Sharpness Enable 0: Disable 1: Enable Valid Range: 0~1, Default Value: 0	cc:m_reg_vc_CDS_Enable
Dummy	3:2	--	--	Reserved	
CDS_Debug	1:0	R/W	0	Color Dependent Sharpness Debug Mode 00: Disable debug mode 01: CM1 debug 10: CM5 debug 11: Reserved	Cc:m_reg_vc_CDS_Debug_Mode

Register:: SR_CDS_CM1_CONTI_CTRL 0x13A1					
Name	Bits	Read/Write	Reset State	Comments	Config
CDS_Conti_Area	7:4	R/W	0x3	Color Dependent Sharpness Continuity Area (Conti_Area: 0~15) Default Value: 0x3	cc:m_reg_vc_CDS_Conti_area
Reserved	3:1	-	0	Reserved	
CDS_Conti_Enable	0	R/W	0x0	Color Dependent Sharpness Continuity Enable 0: Disable 1: Enable	cc:m_reg_vc_CDS_Conti_enable

Register:: SR_CDS_CM1_U_BOUND_U_0_HSB 0x13A2					
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_CDS_CM1_U_BOUND_U_0[9:8]	1:0	R/W	0x1	9:8 bits of Upper Bound of U of CM1 Default Value: `d480	cc:m_reg_vc_CDS_CM1_U_UB_0

Register:: SR_CDS_CM1_U_BOUND_U_0_LSB 0x13A3					
Name	Bits	Read/Write	Reset State	Comments	Config
SR_CDS_CM1_U_BOUND_U_0[7:0]	7:0	R/W	0xE0	7:0 bits of Upper Bound of U of CM1 Default Value: `d480	cc:m_reg_vc_CDS_CM1_U_UB_0

Register:: SR_CDS_CM1_L_BOUND_U_0_HSB 0x13A4					
Name	Bits	Read/Write	Reset State	Comments	Config

Reserved	7:2	-	0	Reserved	
SR_CDS_CM1_L_BOUND_U_0[9:8]	1:0	R/W	0x1	9:8 bits of Lower Bound of U of CM1 Default Value:`d360	cc:m_reg_vc_ CDS_CM1_U_ LB_0

Register:: SR_CDS_CM1_L_BOUND_U_0_LSB					0x13A5
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_L_BOUND_U_0[7:0]	7:0	R/W	0x68	7:0 bits Lower Bound of U of CM1 Default Value:`d360	cc:m_reg_vc_ CDS_CM1_U_ LB_0

Register:: SR_CDS_CM1_U_BOUND_V_0_HSB					0x13A6
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_CDS_CM1_U_BOUND_V_0[9:8]	1:0	R/W	0x2	9:8 bits of Upper Bound of V of CM1 Default Value:`d650	cc:m_reg_vc_ CDS_CM1_V_ UB_0

Register:: SR_CDS_CM1_U_BOUND_V_0_LSB					0x13A7
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_U_BOUND_V_0[7:0]	7:0	R/W	0x8A	7:0 bits of Upper Bound of V of CM1 Default Value:`d650	cc:m_reg_vc_ CDS_CM1_V_ UB_0

Register:: SR_CDS_CM1_L_BOUND_V_0_HSB					0x13A8
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	-	0		
SR_CDS_CM1_L_BOUND_V_0[9:8]	1:0	R/W	0x2	9:8 bits of Lower Bound of V of CM1 Default Value:`d560	cc:m_reg_vc_ CDS_CM1_V_ LB_0

Register:: SR_CDS_CM1_L_BOUND_V_0_LSB					0x13A9
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_L_BOUND_V_0[7:0]	7:0	R/W	0x30	7:0 bits of Lower Bound of V of CM1 Default Value:`d560	cc:m_reg_vc_ CDS_CM1_V_ LB_0

Register:: SR_CDS_CM5_U_BOUND_U_0_HSB					0x13AA
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	--	--		
SR_CDS_CM5_U_BOUND_U_0[9:8]	1:0	R/W	0x3	9:8 bits of Upper Bound of U of CM5 Default Value:`d1000	cc:m_reg_vc_ CDS_CM5_U_ UB_0

Register:: SR_CDS_CM5_U_BOUND_U_0_LSB					0x13AB
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM5_U_BOUND_U_0[7:0]	7:0	R/W	0xE8	7:0 bits of Upper Bound of U of CM5 Default Value:`d1000	cc:m_reg_vc_ CDS_CM5_U_ UB_0

Register:: SR_CDS_CM5_L_BOUND_U_0_HSB						0x13AC
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	--			
SR_CDS_CM5_L_BOUND_U_0[9:8]	1:0	R/W	0x2	9:8 bits of Lower Bound of U of CM5 Default Value:`d600		cc:m_reg_vc_CDS_CM5_U_LB_0

Register:: SR_CDS_CM5_L_BOUND_U_0 LSB						0x13AD
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_L_BOUND_U_0[7:0]	7:0	R/W	0x58	7:0 bits of Lower Bound of U of CM5 Default Value:`d600		cc:m_reg_vc_CDS_CM5_U_LB_0

Register:: SR_CDS_CM5_U_BOUND_V_0 HSB						0x13AE
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	--			
SR_CDS_CM5_U_BOUND_V_0[9:8]	1:0	R/W	0x1	9:8 bits of Upper Bound of V of CM5 Default Value:`d460		cc:m_reg_vc_CDS_CM5_V_UB_0

Register:: SR_CDS_CM5_U_BOUND_V_0 LSB						0x13AF
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_U_BOUND_V_0[7:0]	7:0	R/W	0xCC	7:0 bits of Upper Bound of V of CM5 Default Value:`d460		cc:m_reg_vc_CDS_CM5_V_UB_0

Register:: SR_CDS_CM5_L_BOUND_V_0 HSB						0x13B0
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	--			
SR_CDS_CM5_L_BOUND_V_0[9:8]	1:0	R/W	0x1	9:8 bits of Lower Bound of V of CM5 Default Value:`d360		cc:m_reg_vc_CDS_CM5_V_LB_0

Register:: SR_CDS_CM5_L_BOUND_V_0 LSB						0x13B1
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_L_BOUND_V_0[7:0]	7:0	R/W	0x68	7:0 bits of Lower Bound of V of CM5 Default Value:`d360		cc:m_reg_vc_CDS_CM5_V_LB_0

Register:: SR_CDS_PEAKING_GAIN_BLR_CM1						0x13B2
Name	bits	R/W/D	Reset State	Comments		Config
Gain_Blr	7:0	R/W	0	Gain Value for Low-pass at Center Range in Peaking and Coring (Gain_Blr : 0/64~255/64) Default Value: 0		cc:m_reg_vc_CDS_Gain_Blr_1

Register:: SR_CDS_PEAKING_GAIN_POS_CM1						0x13B3
Name	bits	R/W/D	Reset	Comments		Config

			State		
Gain_Pos	7:0	R/W	`d38	Gain Value for High-pass or Band-pass at Positive Range in Peaking and Coring (Gain_Pos : 0/64~255/64) Default Value: 38	cc:m_reg_v c_CDS_Gain_Pos_1

Register::SR_CDS_PEAKING_GAIN_NEG_CM1					0x13B4
Name	bits	R/W/D	Reset State	Comments	Config
Gain_Neg	7:0	R/W	`d54	Gain Value for High-pass or Band-pass at Negative Range in Peaking and Coring (Gain_Neg : 0/64~255/64) Default Value: 54	cc:m_reg_v c_CDS_Gain_Neg_1

Register::SR_CDS_PEAKING_HV_POS_CM1_HSB					0x13B5
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_CDS_PEAKING_HV_POS_CM1[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023) Default Value: 52	cc:m_reg_v c_CDS_HV_Pos_1

Register::SR_CDS_PEAKING_HV_POS_CM1_LSB					0x13B6
Name	bits	R/W/D	Reset State	Comments	Config
SR_CDS_PEAKING_HV_POS_CM1[7:0]	7:0	R/W	`d52	7:0 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023) Default Value: 52	cc:m_reg_v c_CDS_HV_Pos_1

Register::SR_CDS_PEAKING_HV_NEG_CM1_HSB					0x13B7
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
SR_CDS_PEAKING_HV_NEG_CM1[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023) Default Value: 66	cc:m_reg_v c_CDS_HV_Neg_1

Register::SR_CDS_PEAKING_HV_NEG_CM1_LSB					0x13B8
Name	bits	R/W/D	Reset State	Comments	Config
SR_CDS_PEAKING_HV_NEG_CM1[7:0]	7:0	R/W	`d66	7:0 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023) Default Value: 66	cc:m_reg_v c_CDS_HV_Neg_1

Register::SR_CDS_PEAKING_LV_CM1					0x13B9
Name	bits	R/W/D	Reset State	Comments	Config
LV	7:0	R/W	`d16	Coring Low Level for Peaking and Coring (LV : 0~255) Default Value: 16	cc:m_reg_v c_CDS_LV_1

Register::SR_CDS_PEAKING_GAIN_BLR_CM5					0x13BA
Name	bits	R/W/D	Reset State	Comments	Config
Gain_Blr	7:0	R/W	0	Gain Value for Low-pass at Center Range in Peaking and Coring (Gain_Blr : 0/64~255/64) Default Value: 0	cc:m_reg_v c_CDS_Gain_Blr_5

Register::SR_CDS_PEAKING_GAIN_POS_CM5						0x13BB
Name	bits	R/W/D	Reset State	Comments		Config
Gain_Pos	7:0	R/W	`d18	Gain Value for High-pass or Band-pass at Positive Range in Peaking and Coring (Gain_Pos : 0/64~255/64) Default Value: 18		cc:m_reg_v c_CDS_Gain_Pos_5

Register::SR_CDS_PEAKING_GAIN_NEG_CM5						0x13BC
Name	bits	R/W/D	Reset State	Comments		Config
Gain_Neg	7:0	R/W	`d34	Gain Value for High-pass or Band-pass at Negative Range in Peaking and Coring (Gain_Neg : 0/64~255/64) Default Value: 34		cc:m_reg_v c_CDS_Gain_Neg_5

Register::SR_CDS_PEAKING_HV_POS_CM5_HSB						0x13BD
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	-	0	Reserved		
SR_CDS_PEAKING_HV_POS_CM5[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023) Default Value: 22		cc:m_reg_v c_CDS_HV_Pos_5

Register::SR_CDS_PEAKING_HV_POS_CM5_LSB						0x13BE
Name	bits	R/W/D	Reset State	Comments		Config
SR_CDS_PEAKING_HV_POS_CM5[7:0]	7:0	R/W	`d22	7:0 bits of Coring High Level of Positive Range for Peaking and Coring (HV_Pos : 0~1023) Default Value: 22		cc:m_reg_v c_CDS_HV_Pos_5

Register::SR_CDS_PEAKING_HV_NEG_CM5_HSB						0x13BF
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7:2	-	0	Reserved		
SR_CDS_PEAKING_HV_NEG_CM5[9:8]	1:0	R/W	`d0	9:8 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023) Default Value: 46		cc:m_reg_v c_CDS_HV_Neg_5

Register::SR_CDS_PEAKING_HV_NEG_CM5_LSB						0x13C0
Name	bits	R/W/D	Reset State	Comments		Config
SR_CDS_PEAKING_HV_NEG_CM5[7:0]	7:0	R/W	`d46	7:0 bits of Coring High Level of Negative Range for Peaking and Coring (HV_Neg : 0~1023) Default Value: 46		cc:m_reg_v c_CDS_HV_Neg_5

Register::SR_CDS_PEAKING_LV_CM5						0x13C1
Name	bits	R/W/D	Reset State	Comments		Config
LV	7:0	R/W	`d16	Coring Low Level for Peaking and Coring (LV : 0~255) Default Value: 16		cc:m_reg_v c_CDS_LV_5

Register:: SR_CDS_CM1_U_BOUND_U_1_HSB						0x13C2
Name	Bits	Read/ Write	Reset State	Comments		Config

Reserved	7:2	--	--		
SR_CDS_CM1_U_BOUND_U_1[9:8]	1:0	R/W	0x1	9:8 bits of Upper Bound of U of CM1 Default Value:`d480	cc:m_reg_vc_ CDS_CM1_U _UB_1

Register:: SR_CDS_CM1_U_BOUND_U_1 LSB					0x13C3
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_U_BOUND_U_1[7:0]	7:0	R/W	0xE0	7:0 bits of Upper Bound of U of CM1 Default Value:`d480	cc:m_reg_vc_ CDS_CM1_U _UB_1

Register:: SR_CDS_CM1_L_BOUND_U_1 HSB					0x13C4
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	--	-		
SR_CDS_CM1_L_BOUND_U_1[9:8]	1:0	R/W	0x1	9:8 bits of Lower Bound of U of CM1 Default Value:`d360	cc:m_reg_vc_ CDS_CM1_U _LB_1

Register:: SR_CDS_CM1_L_BOUND_U_1 LSB					0x13C5
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_L_BOUND_U_1[7:0]	7:0	R/W	0x68	7:0 bits of Lower Bound of U of CM1 Default Value:`d360	cc:m_reg_vc_ CDS_CM1_U _LB_1

Register:: SR_CDS_CM1_U_BOUND_V_1 HSB					0x13C6
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	--	--		
SR_CDS_CM1_U_BOUND_V_1[9:8]	1:0	R/W	0x2	9:8 bits of Upper Bound of V of CM1 Default Value:`d650	cc:m_reg_vc_ CDS_CM1_V _UB_1

Register:: SR_CDS_CM1_U_BOUND_V_1 LSB					0x13C7
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_U_BOUND_V_1[7:0]	7:0	R/W	0x8A	7:0 bits of Upper Bound of V of CM1 Default Value:`d650	cc:m_reg_vc_ CDS_CM1_V _UB_1

Register:: SR_CDS_CM1_L_BOUND_V_1 HSB					0x13C8
Name	Bits	Read/ Write	Reset State	Comments	Config
Reserved	7:2	--	-		
SR_CDS_CM1_L_BOUND_V_1[9:8]	1:0	R/W	0x2	9:8 bits of Lower Bound of V of CM1 Default Value:`d560	cc:m_reg_vc_ CDS_CM1_V _LB_1

Register:: SR_CDS_CM1_L_BOUND_V_1 LSB					0x13C9
Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM1_L_BOUND_V_1[7:0]	7:0	R/W	0x30	7:0 bits of Lower Bound of V of CM1 Default Value:`d560	cc:m_reg_vc_ CDS_CM1_V _LB_1

Register:: SR_CDS_CM5_U_BOUND_U_1_HSB						0x13CA
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	--			
SR_CDS_CM5_U_BOUND_U_1[9:8]	1:0	R/W	0x3	9:8 bits of Upper Bound of U of CM5 Default Value:`d1000		cc:m_reg_vc_CDS_CM5_U_UB_1

Register:: SR_CDS_CM5_U_BOUND_U_1_LSB						0x13CB
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_U_BOUND_U_1[7:0]	7:0	R/W	0xE8	7:0 bits of Upper Bound of U of CM5 Default Value:`d1000		cc:m_reg_vc_CDS_CM5_U_UB_1

Register:: SR_CDS_CM5_L_BOUND_U_1_HSB						0x13CC
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	-			
SR_CDS_CM5_L_BOUND_U_1[9:8]	1:0	R/W	0x2	9:8 bits of Lower Bound of U of CM5 Default Value:`d600		cc:m_reg_vc_CDS_CM5_U_LB_1

Register:: SR_CDS_CM5_L_BOUND_U_1_LSB						0x13CD
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_L_BOUND_U_1[7:0]	7:0	R/W	0x58	7:0 bits of Lower Bound of U of CM5 Default Value:`d600		cc:m_reg_vc_CDS_CM5_U_LB_1

Register:: SR_CDS_CM5_U_BOUND_V_1_HSB						0x13CE
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	--			
SR_CDS_CM5_U_BOUND_V_1[9:8]	1:0	R/W	0x1	9:8 bits of Upper Bound of V of CM5 Default Value:`d460		cc:m_reg_vc_CDS_CM5_V_UB_1

Register:: SR_CDS_CM5_U_BOUND_V_1_LSB						0x13CF
Name	Bits	Read/Write	Reset State	Comments		Config
SR_CDS_CM5_U_BOUND_V_1[7:0]	7:0	R/W	0xCC	7:0 bits of Upper Bound of V of CM5 Default Value:`d460		cc:m_reg_vc_CDS_CM5_V_UB_1

Register:: SR_CDS_CM5_L_BOUND_V_1_HSB						0x13D0
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	--	-			
SR_CDS_CM5_L_BOUND_V_1[9:8]	1:0	R/W	0x1	9:8 bits of Lower Bound of V of CM5 Default Value:`d360		cc:m_reg_vc_CDS_CM5_V_LB_1

Register:: SR_CDS_CM5_L_BOUND_V_1_LSB						0x13D1
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Name	Bits	Read/ Write	Reset State	Comments	Config
SR_CDS_CM5_L_BOUND_V_1[7:0]	7:0	R/W	0x68	7:0 bits of Lower Bound of V of CM5 Default Value: `d360	cc:m_reg_vc_CDS_CM5_V_LB_1

0x13D2, 0x13D3 are reserved

[Note]

1. Color Dependent Sharpness is available for CM1(flesh tone) and CM5(blue).
2. The bounds of color modifier is rectangular.
3. CM1 的框與 CM5 的框可以重疊
4. 一個 CM 有 2 個框，同一個 CM 的框可以重疊

SKIPIR

Register::SR_SKIPIR_CTRL1						0x13D4
Name	bits	R/W/D	Reset State	Comments	Config	
Reserved	7:6	-	0	Reserved		
Islet_mode_sel	5	R/W	1	Islet mode selection 0: mode 1 1: mode 2	cc:m_reg_vc_SKIPIR_Islet_mode_sel	
RevLV_en	4	R/W	1	Ring LV mode enable 0: disable 1: enable	cc:m_reg_vc_SKIPIR_RevLV_en	
RevGain_en	3	R/W	0	Ring Gain mode enable 0: disable 1: enable	cc:m_reg_vc_SKIPIR_RevGain_en	
IsletLV_en	2	R/W	1	Islet LV mode enable 0: disable 1: enable	cc:m_reg_vc_SKIPIR_IsletLV_en	
IsletGain_en	1	R/W	0	Islet Gain mode enable 0: disable 1: enable	cc:m_reg_vc_SKIPIR_IsletGain_en	
SKIPIR_en	0	R/W/D	0	SKIPIR enable 0: disable 1: enable	cc:m_reg_vc_SKIPIR_SKIPIR_en	

Register::SR_SKIPIR_CTRL2						0x13D5
Name	bits	R/W/D	Reset State	Comments	Config	
Reserved	7	R/W	0	Reserved		
OceanSFT	6:4	R/W	0x3	Ocean power level 0→7 : weak → strong Right shift value: +3 → -4	cc:m_reg_vc_SKIPIR_OceanSFT	
Reserved	3	R/W	0	Reserved		
IsletSFT	2:0	R/W	0x3	Islet power level 0→7 : weak → strong Right shift value: +3 → -4	cc:m_reg_vc_SKIPIR_IsletSFT	

Register::SR_SKIPIR_CTRL3						0x13D6
Name	bits	R/W/D	Reset State	Comments	Config	
Reserved	7	R/W	0	Reserved		

IsletLVSFT	6:4	R/W	0x3	IsletLV level 0→7 : weak → strong Right shift value: +3 → -4	cc:m_reg_vc_SKIPIR_IsletLVSFT
reserved	3	R/W	0	reserved	
IsletGainSFT	2:0	R/W	0x1	IsletGainOffset level 0→7 : weak → strong Right shift value: 1 → -6	cc:m_reg_vc_SKIPIR_IsletGainSFT

Register::SR_SKIPIR_CTRL4					0x13D7
Name	bits	R/W/D	Reset State	Comments	Config
reserved	7	R/W	0	reserved	
RevLVSFT	6:4	R/W	0x3	RingLV level 0→7 : weak → strong Right shift value: +3 → -4	cc:m_reg_vc_SKIPIR_RevLVSFT
reserved	3	R/W	0	Reserved	
RevGainSFT	2:0	R/W	0x1	RingGainOffset level 0→7 : weak → strong Right shift value: 1 → -6	cc:m_reg_vc_SKIPIR_RevGainSFT

Register::SR_SKIPIR_CTRL5					0x13D8
Name	bits	R/W/D	Reset State	Comments	Config
IsletMode1_th	7:0	R/W	0xff	Islet is depent on (IsletMode1_th-OceanPWR)	Cc:m_reg_vc_SKIPIR_IsletMode1Th

Register::SR_SKIPIR_CTRL6					0x13D9
Name	bits	R/W/D	Reset State	Comments	Config
sharp_grayscale	7	R/W	0	0: u ,v free. 1: u = v = 512 (10 bit gray)	Cc:m_reg_vc_Sharpness_grayscale
Islet_EnlargeAOV	6:4	R/W	0x4	Amplitude of Vibration level 0→7 : weak → strong Right shift value: +3 → -4	cc:m_reg_vc_SKIPIR_EnlargeAOV
IsletRange	3:0	R/W	2	islet range when calculating islet power. Valid range from 1~5	cc:m_reg_vc_SKIPIR_IsletRange

Register::SR_SKIPIR_ISLETLV_U					0x13DA
Name	bits	R/W/D	Reset State	Comments	Config
IsletLV_upbnd	7:0	R/W	0xff	Upper bound of IsletLV	Cc:m_reg_vc_SKIPIR_IsletLV_upbnd

Register::SR_SKIPIR_ISLETGAIN_U					0x13DB
Name	bits	R/W/D	Reset State	Comments	Config
IsletGain_upbnd	7:0	R/W	0xff	Upper bound of IsletGainOffset	Cc:m_reg_vc_SKIPIR_IsletGain_upbnd

Register::SR_SKIPIR_REVLV_U					0x13DC
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Name	bits	R/W/D	Reset State	Comments	Config
RevLV_upbnd	7:0	R/W	0xff	Upper bound of RevLV	Cc:m_reg_vc_SKIPIR_RevLV_upbnd

Register::SR_SKIPIR_REVLVGAIN_U					0x13DD
Name	bits	R/W/D	Reset State	Comments	Config
RevGain_upbnd	7:0	R/W	0xff	Upper bound of RevGainOffset	Cc:m_reg_vc_SKIPIR_RevGain_upbnd

Register::SR_SKIPIR_DEBUG					0x13DE
Name	bits	R/W/D	Reset State	Comments	Config
reserved	7	R/W	0	Reserved	
Debug_sharp_D2SFT	6:4	R/W	0	D2 level for sharpness debug mode. 0→7 : weak → strong Right shift value: 0 → -7	Cc:m_reg_vc_Sharpness_debug_d2sft
reserved	3	R/W	0	Reserved	
Debug_sharp	2	R/W	0	Debug mode of sharpness Priority : Debug_IsletLV > Debug_RevLV> Debug_sharp	Cc:m_reg_vc_Sharpness_debug
Debug_RevLV	1	R/W	0	Debug mode of RevLV 0: disable 1: enable: output RevLV to Y channel. (if RevLV_en==0, output 0 to Y channel) Priority : Debug_IsletLV > Debug_RevLV> Debug_sharp	Cc:m_reg_vc_SKIPIR_RevLV_debug
Debug_IsletLV	0	R/W	0	Debug mode of isletLV 0: disable 1: enable: output IsletLV to Y channel. (if IsletLV_en==0, output 0 to Y channel) Priority : Debug_IsletLV > Debug_RevLV> Debug_sharp	Cc:m_reg_vc_SKIPIR_IsletLV_debug

Dnoise

Register::SR_DNoise_CTRL					0x13DF
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	-	0	Reserved	
DNoise_AOVRange	3	R/W	0	0:11 tap 1: 5 tap	Cc:m_reg_vc_DNoise_AOVRange
DNoise_mode	2	R/W	0	0: use Amplitude Of Vibration to define noise zone 1: use d1 to define noise zone	Cc:m_reg_vc_DNoise_mode
DNoise_Gain_en	1	R/W/D	0	Gain mode 0 : disable 1 : enable To enable this function, SKIPIR_en must =1	Cc:m_reg_vc_DNoise_Gain_en
DNoise_LV_en	0	R/W/D	0	LV mode 0 : disable 1 : enable To enable this function, SKIPIR_en must =1	Cc:m_reg_vc_DNoise_LV_en

Register::SR_DNoise_GAIN_LV						0x13E0
Name	bits	R/W/D	Reset State	Comments		Config
Reserved	7	R/W	0	reserved		
DNoise_GainSFT	6:4	R/W	0x1	DNoise_Gain level 0→7 : weak → strong Right shift value: +1 → -6		Cc:m_reg_vc_DNoise_Gain_SFT
Reserved	3	R/W	0	reserved		
DNoise_LVSFT	2:0	R/W	0	DNoise_LV level 0→7 : weak → strong Right shift value: +3 → -4		Cc:m_reg_vc_DNoise_LVSFT

Register::SR_DNoise_GAIN_U_BAND						0x13E1
Name	bits	R/W/D	Reset State	Comments		Config
DNoise_Gain_upbnd	7:0	R/W	0xff	Upper bound of gain mode effect		Cc:m_reg_vc_DNoise_Gain_upbnd

Register::SR_DNoise_LV_U_BAND						0x13E2
Name	bits	R/W/D	Reset State	Comments		Config
DNoise_LV_upbnd	7:0	R/W	0xff	Upper bound of lv mode effect		Cc:m_reg_vc_DNoise_LV_upbnd

Register::SR_DNoise_NOISE_GAIN_TH						0x13E3
Name	bits	R/W/D	Reset State	Comments		Config
DNoise_Noise_gain_th	7:0	R/W	0x14	Threshold to define noise zone of gain mode		Cc:m_reg_vc_DNoise_Noise_gain_th

Register::SR_DNoise_NOISE_LV_TH						0x13E4
Name	bits	R/W/D	Reset State	Comments		Config
DNoise_Noise_LV_th	7:0	R/W	0x14	Threshold to define noise zone of lv mode		Cc:m_reg_vc_DNoise_Noise_LV_th

0x13E5~0x13FF are reserved

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RGBtoYCC before SR (8 bits In / 10 bits Out)

Register::: SR_RGB2YCC_CTRL						0x14A0
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:4	-	0	Reserved		
Enable	3	R/W	0	0 : disable 1 : enable		Cc:reg_sr_rgb2ycc_enable
Y_Out_Shift_Enable	2	R/W	0	0 : disable (bypass) 1 : +64 independent with bit 3		Cc:reg_sr_rgb2ycc_y_shift
CbCr_Out_Shift_Enable	1	R/W	1	0 : disable (bypass) 1 : +512 independent with bit 3		Cc:reg_sr_rgb2ycc_cbcshift
type	0	R/W	0	Type of Coefficients 0: 601 1: 709		Cc:reg_sr_rgb2ycc_coef_type

$$Y = (h00*R + h01*G + h02*B)$$

$$Cb = (h10*R + h11*G + h12*B) + 512$$

$$Cr = (h20*R + h21*G + h22*B) + 512$$

All h coefficients are 2's complement with 4-bit signed-extension, 2-bit integer and 10-bit fractional number. (0x0400 means 1.0)

In 601 they are [0132h, 0259h, 0074h, FF54h, FEADh, 0200h, 0200h, FE54h, FFADh]

In 709 they are [00D9h, 02DCh, 0049h, FF8Bh, FE76h, 0200h, 0200h, FE2Fh, FFD2h]

YCCtoRGB after SR (10bits In / 10bits Out)

Register::: SR_YCC2RGB_CTRL						0x14A1
Name	Bits	Read/Write	Reset State	Comments		Config
Dummy	7:4	R/W	0	Reserved		
Y_Signed	3	R/W	0	Y signed selection 0 : (Y-64) Unsigned 1 : (Y-64) Signed		Cc:reg_sr_ycc2rgb_y_signed
Cb_Cr_Clamp	2	R/W	0	Cb Cr Clamp 0: Bypass 1: Cb-(512), Cr-(512)		Cc:reg_sr_ycc2rgb_cbcrcclamp
Y_Clamp	1	R/W	0	Y Clamp 0: Bypass 1: Y-(64)		Cc:reg_sr_ycc2rgb_y_clamp
Enable	0	R/W	0	Enable YUV to RGB Conversion 0: Disable YUV-to-RGB conversion 1: Enable YUV-to-RGB conversion		Cc:reg_sr_ycc2rgb_enable

Register::: YUV_RGB_COEF_K11_HSB						0x14A2
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:4	-	0	Reserved		
YUV_RGB_COEF_K11[11:8]	3:0	R/W	0x00	11:8 bits of K11		Cc:reg_sr_ycc2rgb_k11

Register:: YUV_RGB_COEF_K11 LSB					0x14A3
Name	Bits	Read/Write	Reset State	Comments	Config
YUV_RGB_COEF_K11[7:0]	7:0	R/W	0x00	7:0 bits of K11	Cc:reg_sr_ycc2rgb_k11

Register:: YUV_RGB_COEF_K13 HSB					0x14A4
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:3	-	0	Reserved	
YUV_RGB_COEF_K13[10::8]	2:0	R/W	0x00	10:8 bits of K13	Cc:reg_sr_ycc2rgb_k13

Register:: YUV_RGB_COEF_K13 LSB					0x14A5
Name	Bits	Read/Write	Reset State	Comments	Config
YUV_RGB_COEF_K13[7:0]	7:0	R/W	0x00	7:0 bits of K13	Cc:reg_sr_ycc2rgb_k13

Register:: YUV_RGB_COEF_K22 HSB					0x14A6
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
YUV_RGB_COEF_K22[9:8]	1:0	R/W	0x00	9:8 bits of K22	Cc:reg_sr_ycc2rgb_k22

Register:: YUV_RGB_COEF_K22 LSB					0x14A7
Name	Bits	Read/Write	Reset State	Comments	Config
YUV_RGB_COEF_K22[7:0]	7:0	R/W	0x00	7:0 bits of K22	Cc:reg_sr_ycc2rgb_k22

Register:: YUV_RGB_COEF_K23 HSB					0x14A8
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:2	-	0	Reserved	
YUV_RGB_COEF_K23[9:8]	1:0	R/W	0x00	9:8 bits of K23	Cc:reg_sr_ycc2rgb_k23

Register:: YUV_RGB_COEF_K23 LSB					0x14A9
Name	Bits	Read/Write	Reset State	Comments	Config
YUV_RGB_COEF_K23[7:0]	7:0	R/W	0x00	7:0 bits of K23	Cc:reg_sr_ycc2rgb_k23

Register:: YUV_RGB_COEF_K32 HSB					0x14AA
Name	Bits	Read/Write	Reset State	Comments	Config
Reserved	7:4	-	0	Reserved	
YUV_RGB_COEF_K32[11:8]	3:0	R/W	0x00	11:8 bits of K32	Cc:reg_sr_ycc2rgb_k32

Register:: YUV_RGB_COEF_K32 LSB					0x14AB
Name	Bits	Read/Write	Reset State	Comments	Config
YUV_RGB_COEF_K32[7:0]	7:0	R/W	0x00	7:0 bits of K32	Cc:reg_sr_ycc2rgb_k32

Register:: YUV_RGB_R_OFFSET_HSB						0x14AC
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:6	-	0	Reserved		
YUV_RGB_R_OFFSET[13:8]	5:0	R/W	0x00	13:8 bits of R_OFFSET	Cc:reg_sr_ycc2rgb_r_offset	

Register:: YUV_RGB_R_OFFSET LSB						0x14AD
Name	Bits	Read/ Write	Reset State	Comments	Config	
YUV_RGB_R_OFFSET[7:0]	7:0	R/W	0x00	7:0 bits of R_OFFSET	Cc:reg_sr_ycc2rgb_r_offset	

Register:: YUV_RGB_G_OFFSET_HSB						0x14AE
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:6	-	0	Reserved		
YUV_RGB_G_OFFSET[13:8]	5:0	R/W	0x00	13:8 bits of G_OFFSET	Cc:reg_sr_ycc2rgb_g_offset	

Register:: YUV_RGB_G_OFFSET LSB						0x14AF
Name	Bits	Read/ Write	Reset State	Comments	Config	
YUV_RGB_G_OFFSET[7:0]	7:0	R/W	0x00	7:0 bits of G_OFFSET	Cc:reg_sr_ycc2rgb_g_offset	

Register:: YUV_RGB_B_OFFSET_HSB						0x14B0
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:6	-	0	Reserved		
YUV_RGB_B_OFFSET[13:8]	5:0	R/W	0x00	13:8 bits of B_OFFSET	Cc:reg_sr_ycc2rgb_b_offset	

Register:: YUV_RGB_B_OFFSET LSB						0x14B1
Name	Bits	Read/ Write	Reset State	Comments	Config	
YUV_RGB_B_OFFSET[7:0]	7:0	R/W	0x00	7:0 bits of B_OFFSET	Cc:reg_sr_ycc2rgb_b_offset	

Register:: YUV_RGB_R_GAIN_HSB						0x14B2
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:2	-	0	Reserved		
YUV_RGB_R_GAIN[9:8]	1:0	R/W	0x00	9:8 bits of R_GAIN	Cc:reg_sr_ycc2rgb_r_gain	

Register:: YUV_RGB_R_GAIN LSB						0x14B3
Name	Bits	Read/ Write	Reset State	Comments	Config	
YUV_RGB_R_GAIN[7:0]	7:0	R/W	0x00	7:0 bits of R_GAIN	Cc:reg_sr_ycc2rgb_r_gain	

Register:: YUV_RGB_G_GAIN_HSB						0x14B4
Name	Bits	Read/ Write	Reset State	Comments	Config	
Reserved	7:2	-	0	Reserved		
YUV_RGB_G_GAIN[9:8]	1:0	R/W	0x00	9:8 bits of G_GAIN	Cc:reg_sr_ycc2rgb_g_gain	

Register:: YUV_RGB_G_GAIN LSB						0x14B5
Name	Bits	Read/ Write	Reset State	Comments	Config	
YUV_RGB_G_GAIN[7:0]	7:0	R/W	0x00	7:0 bits of G_GAIN	Cc:reg_sr_ycc2rgb_g_gain	

Register:: YUV_RGB_B_GAIN_HSB						0x14B6
Name	Bits	Read/Write	Reset State	Comments		Config
Reserved	7:2	-	0	Reserved		
YUV_RGB_B_GAIN[9:8]	1:0	R/W	0x00	9:8 bits of B_GAIN		Cc:reg_sr_ycc2rgb_b_gain

Register:: YUV_RGB_B_GAIN LSB						0x14B7
Name	Bits	Read/Write	Reset State	Comments		Config
YUV_RGB_G_GAIN[7:0]	7:0	R/W	0x00	7:0 bits of B_GAIN		Cc:reg_sr_ycc2rgb_b_gain

$$\text{YCC/RGB matrix} \begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} K_{11} & 0 & K_{13} \\ K_{11} & -K_{22} & -K_{23} \\ K_{11} & K_{32} & 0 \end{bmatrix} \begin{bmatrix} Y \text{ or } (Y-64) \\ \text{Cb or } (\text{Cb}-512) \\ \text{Cr or } (\text{Cr}-512) \end{bmatrix} + \begin{bmatrix} R_{\text{offset}} \\ G_{\text{offset}} \\ B_{\text{offset}} \end{bmatrix}$$

Then,

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} R_{\text{gain}} \times R' \\ G_{\text{gain}} \times G' \\ B_{\text{gain}} \times B' \end{bmatrix}$$

Where

- Y: S(11,2)
- Cb, Cr: S(10,2)
- K11: U(12, 10) 12 bits, 2 bit integer and 10-bit fractional bits. (Default: 0x0400h)
- K13: U(11, 10) 11 bits, 1 bit integer and 10-bit fractional bits (Default: 0x048Fh)
- K22, K23: U(10, 10) 10 bits, all fractional bits (Default: K22: 0x0194h, K23: 0x0252h)
- K32: U(12, 10) 12 bits, 2 bit integer and 10-bit fractional bits (Default: 0x0820h)
- K11': S(15,4)
- Roffset, Goffset, Boffset: S(14,4) 14 bits, 10 bit signed integer and 4-bit fractional bits. (Default: 0x000h)
- K13': S(15,4)
- K22', K23': S(11,2)
- K32': S(13,2)
- Rgain, Ggain, Bgain: U(10, 9) 10bits, 1 bit integer and 9-bit fractional bits. (Default: 0x0200h)

Operation	Description
K11' = K11 * Y	U(12,10) * S(11,2) = S(23,12) truncating to S(15,4)
K13' = K13 * V	U(11,10) * S(10,2) = S(21,12) truncating to S(13,4)
R'' = K11' + K13'	S(15,4) + S(13,4) = S(15,4)
R' = R'' + Roffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
K22' = K22 * U	U(10,10) * S(11,2) = S(21,12) truncating to S(13,4)
K23' = K23 * V	U(10,10) * S(10,2) = S(20,12) truncating to S(13,4)
G'' = K11' - K22' - K23'	S(15,4) + S(13,4) + S(13,4) = S(15,4)
G' = G'' + Goffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
K32' = K32 * U	U(12,10) * S(10,2) = S(22,12) truncating to S(14,4)
B'' = K11' + K32'	S(15,4) + S(14,4) = S(15,4)
B' = B'' + Boffset	S(15,4) + S(14,4) = S(15,4) truncating to S(13,2)
R=Rgain*R'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)
G=Ggain*G'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)
B=Bgain*B'	U(10,9)*S(13,2)=S(23,11) rounding to U(10,0) (clamp)

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Register::TC1_HE_LSB 0xA4-65					
Name	Bits	R/W	Default	Comments	Config
TCON1_HEND[7:0]	7:0	R/W	0x2c	Low Byte [7:0] Pixel count [7:0] at which TCON goes inactive	

If the register number is large than display format, the horizontal component is always on.

Real TCON_HS = TCON_HS-4, Real TCON_HS = TCON_HS-4

Register::TC1_CTRL 0xA4-66					
Name	Bits	R/W	Default	Comments	Config
TCON1_EN	7	R/W	0x1	TCON [1] Enable (Local) 0: Disable (TCON [0] output clamp to '0') (Default) 1: Enable	
TCON1_INV	6	R/W	0x0	Polarity Control 0: Normal output (Default) 1: Inverted output	
TCON2_PWM	5	R/W	0x0	TCON[2] gated by PWM (reference) Enable 0: Disable 1: Enable	
TCON1_MASK_N	4	R/W	0x0	Mask_flag_N enable 0: Disable 1: Enable (refer to 0xA4-67) Value= 0x0: 1 line, 0x1: 2 line, 0x7: 8 line	
TCON1_TOG_EN	3	R/W	0x0	Toggle Circuit Enable/Disable 0: Normal TCON output (Default) 1: Toggle Circuit enable When using toggle circuit enable mode, the TCON[n] will be 1 clock earlier than TCON[n-1] and then toggling together, finally output will be 1 clock delay comparing to toggling result.	
RESERVED	2:0	--	--	Reserved	

Register:: TC1_SETTING 0xA4-67					
Name	Bits	R/W	Default	Comments	Config
TCON1_VSTART[12]	7	R/W	0	Extended Bit [12], Line number [12] of TCON1 Vstart	
TCON1_VEND[12]	6	R/W	0	Extended Bit [12], Line number [12] of TCON1 Vend	
TCON1_HSTART[12]	5	R/W	0	Extended Bit [12], Line number [12] of TCON1 Hstart	
TCON1_HEND[12]	4	R/W	0	Extended Bit [12], Line number [12] of TCON1 Hend	
RESERVED	3	--	--	reserved	
TCON1_MASK	2:0	R/W	0	Mask flag of TCON1	

TCON[0]

STHO

Vertical

Register::TC0_VS LSB 0xA4-68					
Name	Bits	R/W	Default	Comments	Config
TCON0_VSTART[7:0]	7:0	R/W	0x00	Low Byte [7:0] Line number [7:0] at which TCON control generation begins	

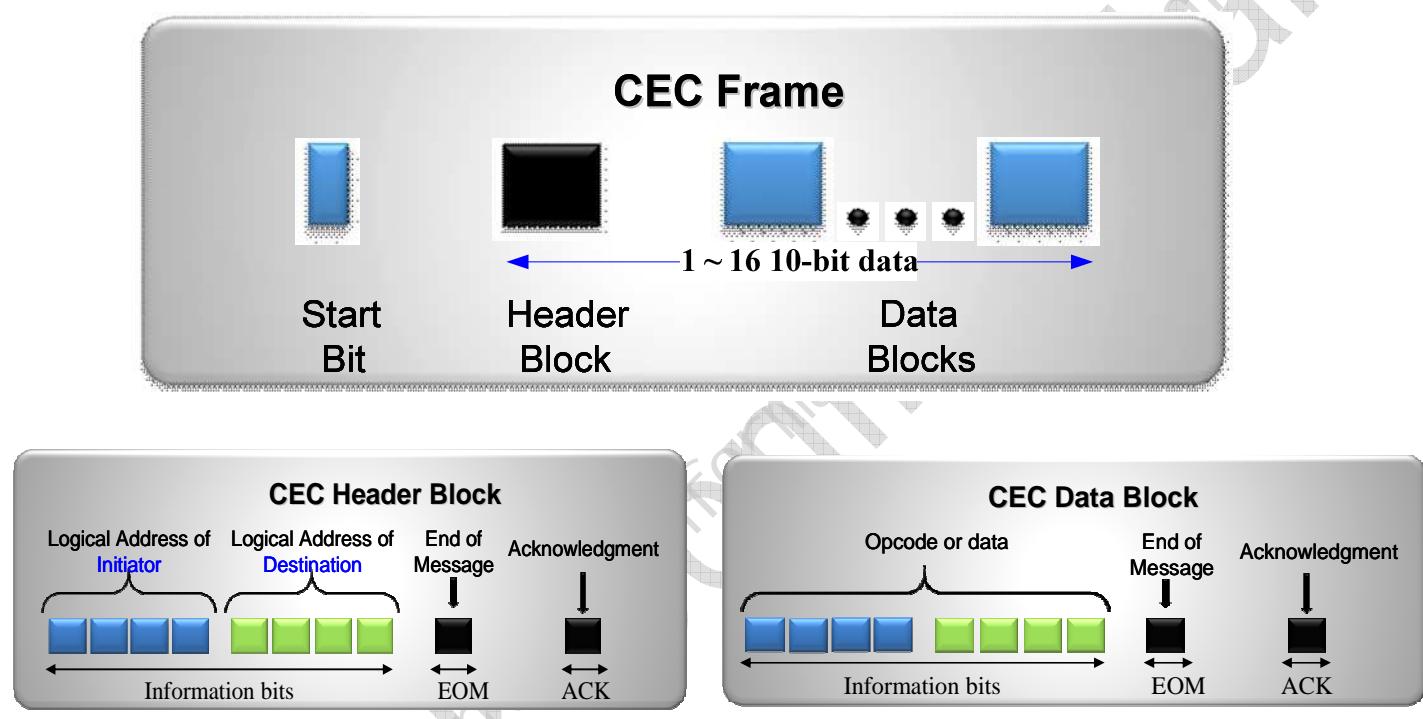
Register::TC0_VSE_MSB 0xA4-69					
Name	Bits	R/W	Default	Comments	Config
TCON0_VSTART[11:8]	7:4	R/W	0x0	High Byte [11:8]	

				Line number [11:8] at which TCON control generation begins	
TCON0_VEND[11:8]	3:0	R/W	0x0	High Byte [11:8] Line number [11:8] at which TCON control generation ends	

Overall CEC Function Block (Page 18)

The CEC is a serial, bi-directional interface based on an open drain, wired or, active low architecture which is described in the HDMI Specification, Supplement 1.

The structure of a CEC message consists of a start bit at the beginning of any message, and a minimum one up to a maximum sixteen 10-bit binary words containing an 8 bit word, an active high end of message (EOM) bit, and an ACK bit, transmitted as a 1 by the source and responded to appropriately by the destination device(s).



Name	Description
Start	Special start “bit”
Header block	Source and destination address
Data block 1 (opcode block)	Opcode
Data block 2.... (operand blocks)	Operand specific to opcode

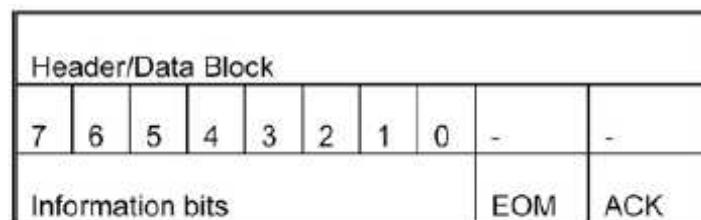
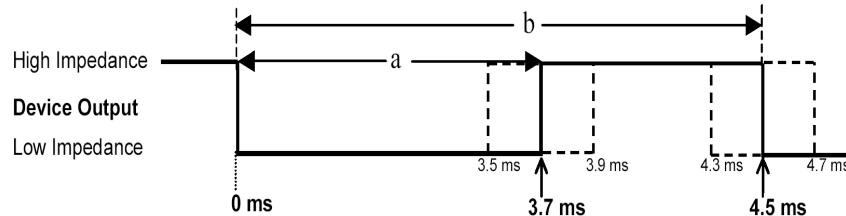
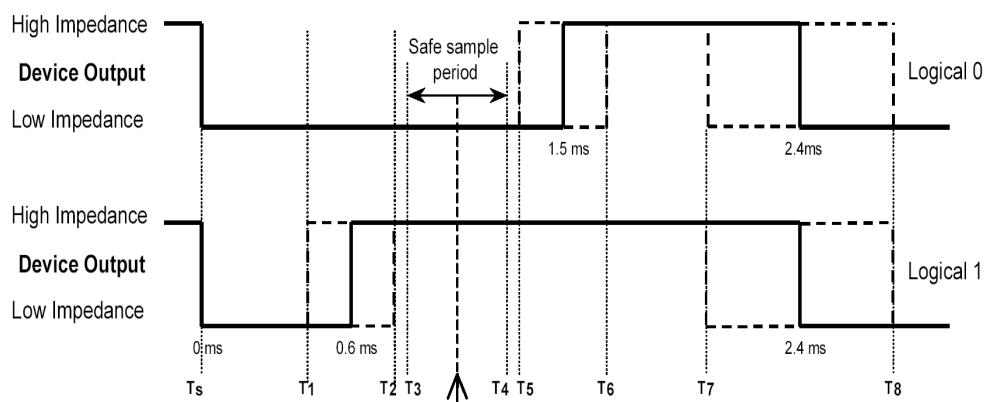


Fig. CEC frame/header block/data block and its definition

The following figure and table illustrate the typical timing of start bit, data bit and ACK of initiator and follower.

**Fig. CEC Start bit pulse format showing minimum and maximum tolerances****Fig. CEC Timing Diagram for Follower Asserted Bit**

Ts	0ms	The bit start event.
T1	0.4ms	The earliest time for a low - high transition when indicating a logical 1.
T2	0.8ms	The latest time for a low - high transition when indicating a logical 1.
T3	0.85ms	The earliest time it is safe to sample the signal line to determine its state.
T4	1.25ms	The latest time it is safe to sample the signal line to determine its state.
T5	1.3ms	The earliest time a device is permitted return to a high impedance state (logical 0).
T6	1.7ms	The latest time a device is permitted return to a high impedance state (logical 0).
T7	2.05ms	The earliest time for the start of a following bit.
T8	2.75ms	The latest time for the start of a following bit.

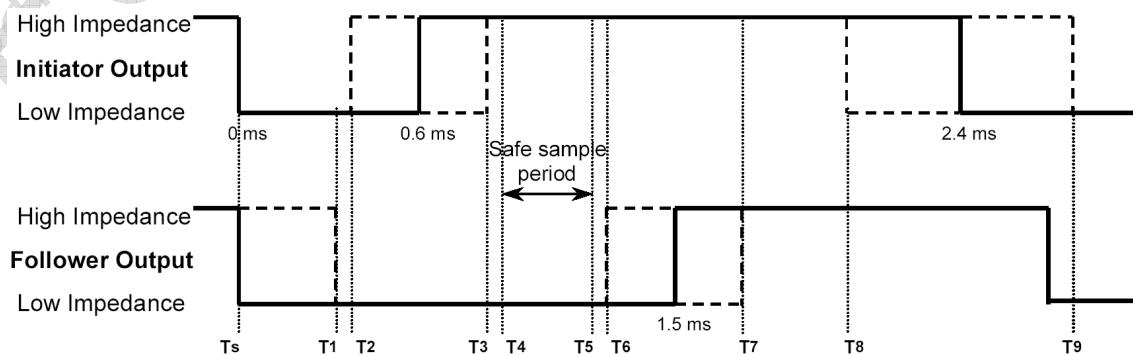
Table. CEC Bit Timing Definition

Fig. CEC Timing Diagram for Follower Asserted Bit

Ts	0ms	The bit start event.
T1	0.35ms	The latest response time for a follower to go to the low impedance state.
T2	0.4ms	The earliest the initiator can return to high impedance when transmitting a logical 1.
T3	0.8ms	The latest the initiator can return to high impedance when transmitting a logical 1.
T4	0.85ms	The earliest time at which the bit state on the CEC line is valid for reading.
T5	1.25ms	The latest time at which the bit state on the CEC line is valid for reading.
T6	1.3ms	The earliest time the follower is permitted return to a high impedance state.
T7	1.7ms	The latest time the follower is permitted return to a high impedance state.
T8	2.05ms	The earliest time for the start of a following bit.
T9	2.75ms	The latest time for the start of a following bit.

Table. CEC Timing Diagram for Follower Asserted Bit Definition

This CEC bus is register programmable to generate/test for these bit timings and the allowed deviations for robust error checking in both transmitter and receiver modes.

The CEC bus is available to any device that wants to transmit and is monitored by all devices for activity, both to avoid bus collisions in the case of 2 or more transmitters, and to receive messages. The bus arbitration commences with the leading edge of the start bit and continues until the end of the initiator address bits within the header block. During this period the initiator shall monitor the CEC line and if whilst in high impedance state it detects low impedance then it shall assume that it has lost the arbitration to a second initiator. It should be noted that this process gives priority to the logical address with the most leading zeros and, ultimately, the TV.

Before attempting to transmit or re-transmit a frame, a device shall ensure that the CEC line has been inactive for a number of bit periods. This signal free time is defined as the time since the start of the final bit of the previous frame. The length of the required signal free time depends on the current status of the control signal line and the initiating device. The different signal free times required are summarized in the following table.

Precondition	Signal Free Time
Present initiator wants to send another frame immediately after its previous frame	7-bit periods
New initiator wants to send a frame	5-bit periods
Previous attempt to send frame unsuccessful	3-bit periods

Table. CEC Signal Free Time

As initiator get the bus and the second 4 bits within the header block (the destination address) is received by the receiver with that address assigned, receiver will respond to with an zero ACK bit if it is capable of acting on the message and not responded to (a one ACK bit sourced by the transmitter) if it can't. In the case of a one ACK bit, the transmitting device will attempt one retry after the last falling edge of the last word it transmitted.

A special case is a broadcast message, where the destination address bits are all high. In that case, all devices on the bus receive the message and do not respond if they are able to act on the message and respond with a zero ACK bit if they cannot. In the case of a zero ACK bit response to a broadcast message, the transmitter will attempt one retry after the last falling edge of the last word it transmitted. If the second attempt gets the same improper response, the CPU is interrupted with the correct status information.

The CEC PAD is required to have a 90% to 10% fall time of 50 us max and 10% to 90% rise time of 250 us max. The slew rate requirement allows a minimum rise/fall time of 33 us. The rise/fall time is a function of a clocked DAC architecture and is controlled within a narrow range by a register programmable clock and is independent of process and temperature

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CEC Digital Function

Register:: CEC_CR0_1						0x18A0
Name	bits	R/W/D	Reset State	Comments		Config
cec_mode	7:6	R/W	0x0	CDC mode selection 00: disable CEC function 01: enable CEC normal operation 10: dac test mode (PAD output test mode) 11: digital self loop back test mode (self cec_tx connect self cec_rx)		cc: reg_0
test_mode_pad_data	5	R/W	0x0	PAD_CEC control in dac test mode 0: PAD_CEC output low 1: PAD_CEC output high Note: this bit is active only when dac test mode		cc: reg_1
test_mode_pad_en	4	R/W	0x0	dac test mode control 0: disable (output high impedance) 1: enable (PAD output enable), PAD_CEC is determined by test_mode_pad_data Note: this bit is active only when dac test mode		cc: reg_2
logical_addr	3:0	R/W	0xF	CEC device's logical/local address		cc: reg_3

Register:: CEC_CR0_1_1						0x18A1
Name	bits	R/W/D	Reset State	Comments		Config
cec_input_clk_sel	7	R/W	0x0	cec input clock selection: 0: OSC clock 1: non-divided M2PLL clock		
cec_input_clk_en	6	R/W	0x1	Enable cec input clk		
logical_addr_rx_rsv	5:4	R/W	0x0	reserved		
cec_data_sel	3	R/W	0x0	reserved		
cec_cr_rsv0	2:0	R/W	0x0	reserved		

Register:: CEC_CR_RSV_1						0x18A2
Name	bits	R/W/D	Reset State	Comments		Config
cec_cr_rsv1	7:4	R/W	0	reserved		
bit_cnt	3:0	R/W	0	Read bit counter of CEC signal		

The following two registers is to set timer enable pulse for cec_tx and cec_rx use. Note that when cec_mode = 0, timer enable pulse = 0, i.e., disable circuit function.

Register:: CEC_CR0_2						0x18A3
Name	bits	R/W/D	Reset State	Comments		Config
timer_div	7:0	R/W	0x14	DAC ENP(Enable Pulse) divides into Timer Enable Pulse. And Timer Enable Pulse is equal to Input Sample Enable Pulse. It's the target frequency is 40k(25us) dac_enp timer_div timer_enp 0.8MHz 20 0.04MHz		cc: reg_4

				1MHz 25 0.04MHz CEC clock frequency is used for the bit timers in the cec receiver and cec transmitter modes. Formula: timer_enp = dac_enp/timer_div PS: 0 means div 256, and this enp signal is for cec_tx and cec_rx use *0x15 for monitor	
--	--	--	--	---	--

Register:: CEC_CR0_3					0x18A4
Name	bits	R/W/D	Reset State	Comments	Config
pre_div	7:0	R/W	0xCA	Divisor for CEC DAC Clock BusCLK CECDIV CK_CEC 162 202(0xCA) 0.8019MHz 27MHz 33(0x21) 0.8182MHz (OSC) 14.318MHz 18(0x12) 0.7954MHz (OSC) 243MHz 243(0XF3) 1.0 MHz (MP2LL) Formula: dac_enp = bus_clk/pre_div PS: 0 means div 256	cc: reg_5

Register:: CEC_CR0_4					0x18A5
Name	bits	R/W/D	Reset State	Comments	Config
unreg_ack_en	7	R/W	0x0	If cec_rx's logical addr = 0xF, when receiving a broadcast signal (destination addr = 0xF) 0: CEC will ack to unregistered initiator address (0xF)->(0xF) [response ack] 1: NAK [not to response ack]	cc: reg_6
cec_cr0_4_rsv	6:5	R/W	0x0	reserved	
pad_rise_time	4:0	R/W	0x04	Waiting time from low-to-high impedance. *Note: (Default) 4*25us = 100us.	cc: reg_7

Register:: CEC_CR0_5					0x18A6
Name	bits	R/W/D	Reset State	Comments	Config
broadcast_ctrl	7	R/W	0x0	If receive broadcast message, broadcast control selection: 0: HW mode 1: FW mode	
broadcast_ctrl_fw	6	R/W	0x1	FW decide ACK/NACK 0: NACK 1: ACK	
ack_bit_ctrl_mode	5	R/W	0x0	Control ack behavior mode 0: HW mode 1: FW mode	
ack_bit_fw	4	R/W	0x0	When ack_bit_ctrl_mode=1, ACK/NACK by ack_bit_fw to decide Single message:0 meas ACK, 1: NACK Broadcast message: 0 meas NACK, 1: ACK	
ack_cond	3	R/W	0x0	The condition for CEC_RX to give ACK/NACK 0: rx receive 8-bit valid LA and match rx's LA 1: rx just receive 8-bit valid LA	
eom_bit	2	R	0x0	Read real-time eom bit	wclr_out
cec_cr0_rsv0	1:0	R/W	0x0	reserved	

*Note: single-message_case's ack behavior:

When receive 8-bit valid header LA data:

(1) if initiator's LA = F(i.e., un-registered CEC_device), CEC_Rx gives NACK.

(2) if (1) is not satisfied, when initiator's LA = reg_logical_addr (i.e., the functional-same device exists in cec system), CEC_Rx gives ACK; otherwise, CEC_Rx gives NACK.

*Note: broadcast_case's ack behavior:

(1) if not receiving broadcast message(i.e., follow's LA ≠ F), CEC_Rx gives NACK.

(2) if receiving broadcast message:

1. HW mode: there are two cases for determining ACK/NACK behavior:

Case1: if initiator's LA ≠ reg_logical_addr (i.e., initiator is not myself), CEC_Rx gives ACK.

Case2: if initiator's LA=reg_logical_addr(i.e., the functional-same device exists in cec system):

<1> reg_logical_addr ≠ F, CEC_Rx gives NACK.

<2> reg_logical_addr =F, FW uses unreg_ack_en to decide to give ACK/NACK.

2. FW mode: by broadcast_ctrl_fw setting

Register:: CEC_CRO RSV 1						0x18A7
Name	bits	R/W/D	Reset State	Comments		Config
cec_cr0_rsv1	7:4	R/W	0	Reserved		
standby_tx_en	3	R	0	Read standby mode status: 0: compare opcode unsuccessfully 1: compare opcode successfully		
ack_bit	2	R	0	Read ack bit data		
rx_low_impedance_irq_en	1	R/W	0	IRQ as long as rx_low_impedance occurs		
rx_low_impedance_flag	0	R	0	Read rx_low_impedance status Note: write 1 clear		Wclr_out

Register:: CEC_RTCR0_1						0x18A8
Name	bits	R/W/D	Reset State	Comments		Config
cec_pad_in	7	R	-	Input PAD CEC signal		cc: reg_8
lattest_rx_rsv	6	R/W	0	Reserved		
cec_int_clr	5	R	-	Write 1 to clear cec_tx_int, cec_rx_int, and standby_rx_hit_opcode	cc: reg_9 WCLR_OUT	
lattest	4	R	-	1: the latest initiator own CEC bus is this device		cc: reg_11
retry_no	3:0	R/W	0x5	Maximum re-transmission times for a single cec frame, when device is a initiator and device detect rx_low_impedance error. In cec_tx continuous mode, retry is inactive. *Note: Re-transmission can be attempted up to 5 times for a single cec message and shall be attempted at least once.		cc: reg_12

Register:: CEC_RTCR0_2						0x18A9
Name	bits	R/W/D	Reset State	Comments		Config
wt_cnt_sel	7	R/W	0	Retry wait time counter selection: 0: by reg_tx_data_low 1: by reg_wt_cnt_set		
broadcast_addr	6	R	0	Check initiator behavior 0: initiator is transmitting single message 1: initiator is broadcasting This flag occurs when follower's LA is equal to 1111, i.e., cec_tx is broadcasting, or this flag = 0 (single message).		cc: reg_13
wt_cnt	5:0	R	-	Retry Wait Time *note: increase 1 per 0.6ms (reg_tx_data_low/reg_wt_cnt_set)		cc: reg_10

Register:: CEC_RTCR0_RSV_0						0x18AA
Name	bits	R/W/D	Reset State	Comments		Config
wt_cnt_set	7:0	R/W	0x18	Wait time setting Time = timer_enp*wt_cnt_set		

The following is to set CEC Rx control signal

Register:: CEC_RxCR0_1						0x18B0
Name	bits	R/W/D	Reset State	Comments		Config
rx_en	7	R	0	Write 1 to enable cec_rx and can read cec_Rx's status. As CEC_enable=1 and CECRxEn=0, Rx will ACK the transaction which destination address is the same with CECLOCADDR or 0xF (broadcast case)		cc: reg_14 WCLR_OUT
rx_reset	6	R	0x0	Write 1 to reset Rx State and its FIFO status After finishing each transaction, software should reset Rx part to clear CECRxEOM, CECRxINT and CECRxFIFOov status bits.		cc: reg_15 WCLR_OUT
rx_continuous	5	R/W	0x0	cec_rx's mode selection: 0 : Normal mode 1 : Continuous mode *Note: In continuous mode, rx_int will be set to 1 when receiving EOM or new 8 sets of 10-bit valid data. In normal mode, rx_int will be set to 1 when receiving EOM.		cc: reg_16
rx_int_en	4	R/W	0x0	0 : CEC Rx interrupt disable 1 : CEC Rx interrupt enable If enabled, hardware will trigger IRQ when per 8 bytes received or receive EOM		cc: reg_17
init_addr	3:0	R	0xf	The latest Initiator Logical Address (when device is a follower)		cc: reg_18

Register:: CEC_RxCR0_2						0x18B1
Name	bits	R/W/D	Reset State	Comments		Config
rx_eom	7	R	-	Check whether cec_rx received data's EOM or not. *Note: when CEC_Rx receive data's EOM, rx_en will be reset to 0 and rx_int will be set to 1. *note: FW can set rx_rst to clear this bit.		cc: reg_19
rx_int	6	R	-	CEC_Rx interrupt pending (write 1 to clear) Also clear special cmd int (special opcode int)		cc: reg_20 WCLR_OUT
rx_fifo_ov	5	R	-	CEC_Rx 16-byte FIFO status 0 : no overflow 1 : overflow		cc: reg_21
rx_fifo_cnt	4:0	R	-	The number of byte has been received by CEC_Rx *note: FW can set rx_rst to clear rx_fifo_cnt		cc: reg_22

* rx_int flag coours as long as the following event occurs:

(1) two modes:

- <1> continuous mode: rx_int will be set to 1 when receiving EOM or new 8 byte valid data.
- <2> normal mode: rx_int will be set to 1 when receiving EOM.

(2) cec rx fifo overflow.

(3) when cec_rx is dealing with CEC data, receive another start-bit data, i.e., another CEC frame comes.

Register::: CEC_RxCR0_RSV_0					0x18B2
Name	bits	R/W/D	Reset State	Comments	Config
cec_header_eom	7	R	-	Check whether cec_rx received header's EOM signal. When this flag occurs, it represents polling message.	Wclr_out
retry_clr_cnt	6	R/W	0	When retry occurs, enable clear time counter	
retry_number	5:2	R	0	CEC Tx Retry number	
retry_no_clr	1	R	0	Reset retry number to 5	wclr_out
cec_rxcr0_rsv0	0	R/W	0	Reserved	

Register::: CEC_RxCR0_RSV_1					0x18B3
Name	bits	R/W/D	Reset State	Comments	Config
rx_st	7:0	R	0	CEC Rx FSM status	

The following is to set CEC Tx control signal

Register::: CEC_TxCR0_1					0x18B4
Name	bits	R/W/D	Reset State	Comments	Config
tx_addr_en	7	R/W	0x0	Select CEC_Tx's logical address 0: by logical_addr 1: by tx_addr	cc: reg_23
tx_addr	6:3	R/W	0x0	CEC_Tx's logical address by FW setting	cc: reg_24
tx_en	2	R	-	Write 1 to enable CEC Tx transmission. And this bit can read back CEC Tx enable status. *Note: Tx will detect signal free time, and then transmission and re-try automatically.	cc: reg_25 WCLR_OUT
tx_reset	1	R	0x0	Write 1 to reset CEC Tx State and its FIFO status. After finishing each transaction, software should reset CEC Tx to clear CECTxEOM, CECTxINT and CECTxFIFOud status bits.	cc: reg_26 wclr_out
tx_continuous	0	R/W	0x0	CEC_Tx mode selection 0: Normal mode 1: Continuous mode, FW should clear this bit as the last byte is written into CEC Tx FIFO to indicate the end of transmitting data.	cc: reg_27

*Note: continuous/normal mode behavior

Continuous mode: when tx/rx transmit/receive 8 data, tx_int/rx_int will occur.

Normal mode: when tx/rx already transmit/receive all the data, tx_int/rx_int will occur.

Register::: CEC_TxCR0_2					0x18B5
Name	bits	R/W/D	Reset State	Comments	Config
tx_int_en	7	R/W	0x0	Tx_int control 0 : tx_int disable 1 : tx_int enable *note: if enabled, HW trigger interrupt per 8-bytes data transmitted or EOM	cc: reg_28
dest_addr	6:3	R/W	0x0	Destination Address by FW setting (when device is a initiator)	cc: reg_29
tx_eom	2	R	-	The transmission has ended.	cc: reg_30
tx_int	1	R	-	CEC Tx interrupt.	cc: reg_31

				Note: write 1 to clear	WCLR_OUT
cec_txcr0_2_rsv	0	R/W	0	Reserved	

*note: header's follower address determination:

1. normal mode: by dest_addr setting

2. compare_opcode mode: when received wanted command, cec_tx decides to give ACK. Header's follower address is set by cec_tx's initiator address or by register setting.

*note: tx_int will trigger as long as the following cases occur:

1. tx_fifo underflow.

2. in header/data high state, rx_low_impedance occurs...so on.

Register:: CEC_TxCR0_3					0x18B6
Name	bits	R/W/D	Reset State	Comments	Config
cec_txcr0_3_rsv	7:6	R/W	0	reserved	
tx_fifo_ud	5	R	-	CEC_Tx 16-byte FIFO status 0 : no underflow 1 : underflow	cc: reg_32
tx_fifo_cnt	4:0	R	-	The number of byte will been transmitted by CEC Tx *note: FW can set tx_rst to clear tx_fifo_cnt.	cc: reg_33

Register:: CEC_TxCR0_RSV_0					0x18B7
Name	bits	R/W/D	Reset State	Comments	Config
cec_txcr0_rsv0	7:3	R/W	0	reserved	
main_st[1:0]	2:1	R	0	CEC Rx main FSM status	

Register:: CEC_TxCR0_RSV_1					0x18B8
Name	bits	R/W/D	Reset State	Comments	Config
tx_st[7:0]	7:0	R	0	Cec Tx FSM status	

Note : the following table illustrates the status with the combination of CECTxEn, CECTxEOM, CECTxINT and CECTxContinue after transmitting.

	CECTxEn	CECTxEOM	CECTxINT	CECTxContinue
Complete transmission incorrectly and not in Continue Mode	0	0	1	0
Complete transmission correctly and not in Continue Mode	0	1	1	0
Complete transmission incorrectly and in Continue Mode	0	0	1	0
Transmitted 8 bytes correctly and still in Continue Mode, software should push data into Tx fifo as necessary	1	0	1	1
Complete transmission and in Continue Mode	0	1	1	0 (because software clear to 0 after pushing remaining datum into TX fifo)
TX fifo is underflow (in continue mode only) Note : this is the same with CECTxFIFOud=1	0	0	1	1

Register::: CEC_TxDR0					0x18B9
Name	bits	R/W/D	Reset State	Comments	Config
cec_txdr0_rsv	7	R/W	0	Reserved	
tx_add_cnt	6	R	-	Enable tx fifo_cnt setting	cc: reg_34 WCLR_OUT
rx_sub_cnt	5	R	-	Enable rx fifo_cnt setting	cc: reg_35 WCLR_OUT
fifo_cnt	4:0	R/W	0	The number of byte has been written/read by cec Tx/Rx	cc: reg_36

*Note: tx/rx_fifo_cnt usage:

(1) tx_add_cnt

<1> tx_fifo_cnt calculation:

0: tx_fifo_cnt = tx_fifo_cnt - tx_fifo_rd

1: tx_fifo_cnt = tx_fifo_cnt + tx_fifo_add - tx_fifo_rd

<2> tx_fifo_cnt in different mode:

In normal mode, tx_fifo_add = fifo_cnt.

In compare_opcode mode, tx_fifo_cnt = operand_number + 1

(2) rx_sub_cnt calculation:

0: rx_fifo_cnt = rx_fifo_cnt + rx_fifo_wr

1: rx_fifo_cnt = rx_fifo_cnt - fifo_cnt + rx_fifo_wr

Register::: CEC_TxDR0_RSV_0					0x18BA
Name	bits	R/W/D	Reset State	Comments	Config
cec_txdr0_rsv0	7:5	R/W	0	Reserved	
fifo_cnt_rx	4:0	R/W	0	reserved	

The following is to set Tx fifo information bits, max transmitted information bits are 16 bytes.

Register::: CEC_TxDR1_1					0x18C0
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_0	7:0	R/W	0	Information bits of data block 0 which cec tx transmitted	cc: reg_37

Register::: CEC_TxDR1_2					0x18C1
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_1	7:0	R/W	0	Information bits of data block 1 which cec tx transmitted	cc: reg_38

Register::: CEC_TxDR1_3					0x18C2
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_2	7:0	R/W	0	Information bits of data block 2 which cec tx transmitted	cc: reg_39

Register::: CEC_TxDR1_4					0x18C3
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_3	7:0	R/W	0	Information bits of data block 3 which cec tx transmitted	cc: reg_40

Register::: CEC_TxDR2_1					0x18C4
Name	bits	R/W/D	Reset State	Comments	Config

tx_fifo_4	7:0	R/W	0	Information bits of data block 4 which cec tx transmitted	cc: reg_41
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Register:: CEC_TxDR2_2 0x18C5					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_5	7:0	R/W	0	Information bits of data block 5 which cec tx transmitted	cc: reg_42

Register:: CEC_TxDR2_3 0x18C6					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_6	7:0	R/W	0	Information bits of data block 6 which cec tx transmitted	cc: reg_43

Register:: CEC_TxDR2_4 0x18C7					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_7	7:0	R/W	0	Information bits of data block 7 which cec tx transmitted	cc: reg_44

Register:: CEC_TxDR3_1 0x18C8					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_8	7:0	R/W	0	Information bits of data block 8 which cec tx transmitted	cc: reg_45

Register:: CEC_TxDR3_2 0x18C9					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_9	7:0	R/W	0	Information bits of data block 9 which cec tx transmitted	cc: reg_46

Register:: CEC_TxDR3_3 0x18CA					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_a	7:0	R/W	0	Information bits of data block 10 which cec tx transmitted	cc: reg_47

Register:: CEC_TxDR3_4 0x18CB					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_b	7:0	R/W	0	Information bits of data block 11 which cec tx transmitted	cc: reg_48

Register:: CEC_TxDR4_1 0x18CC					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_c	7:0	R/W	0	Information bits of data block 12 which cec tx transmitted	cc: reg_49

Register:: CEC_TxDR4_2 0x18CD					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_d	7:0	R/W	0	Information bits of data block 13 which cec tx transmitted	cc: reg_50

Register:: CEC_TxDR4_3 0x18CE					
Name	bits	R/W/D	Reset State	Comments	Config
tx_fifo_e	7:0	R/W	0	Information bits of data block 14 which cec tx transmitted	cc: reg_51

Register:: CEC_TxDR4_4 0x18CF					
Name	bits	R/W/D	Reset State	Comments	Config

tx_fifo_f	7:0	R/W	0	Information bits of data block 15 which cec tx transmitted	cc: reg_52
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Register:: CEC_TxDR_FIFO_RSV_0					0x18D0
Name	bits	R/W/D	Reset State	Comments	Config
cec_txdr_fifo_rsv0	7:0	R/W	0	reserved	

Register:: CEC_TxDR_FIFO_RSV_1					0x18D1
Name	bits	R/W/D	Reset State	Comments	Config
cec_txdr_fifo_rsv1	7:0	R/W	0	reserved	

Register:: CEC_TxDR_FIFO_RSV_2					0x18D2
Name	bits	R/W/D	Reset State	Comments	Config
cec_txdr_fifo_rsv2	7:0	R/W	0	reserved	

The following is to read Rx fifo information bits, max received information bits are 16 bytes.

Register:: CEC_RxDR1_1					0x18D3
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_0	7:0	R	0	Information bits of data block 0 which cec rx received	cc: reg_53

Register:: CEC_RxDR1_2					0x18D4
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_1	7:0	R	0	Information bits of data block 1 which cec rx received	cc: reg_54

Register:: CEC_RxDR1_3					0x18D5
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_2	7:0	R	0	Information bits of data block 2 which cec rx received	cc: reg_55

Register:: CEC_RxDR1_4					0x18D6
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_3	7:0	R	0	Information bits of data block 3 which cec rx received	cc: reg_56

Register:: CEC_RxDR2_1					0x18D7
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_4	7:0	R	0	Information bits of data block 4 which cec rx received	cc: reg_57

Register:: CEC_RxDR2_2					0x18D8
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_5	7:0	R	0	Information bits of data block 5 which cec rx received	cc: reg_58

Register:: CEC_RxDR2_3					0x18D9
Name	bits	R/W/D	Reset State	Comments	Config

rx_fifo_6	7:0	R	0	Information bits of data block 6 which cec rx received	cc: reg_59
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Register:: CEC_RxDR2_4 0x18DA					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_7	7:0	R	0	Information bits of data block 7 which cec rx received	cc: reg_60

Register:: CEC_RxDR3_1 0x18DB					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_8	7:0	R	0	Information bits of data block 8 which cec rx received	cc: reg_61

Register:: CEC_RxDR3_2 0x18DC					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_9	7:0	R	0	Information bits of data block 9 which cec rx received	cc: reg_62

Register:: CEC_RxDR3_3 0x18DD					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_a	7:0	R	0	Information bits of data block 10 which cec rx received	cc: reg_63

Register:: CEC_RxDR3_4 0x18DE					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_b	7:0	R	0	Information bits of data block 11 which cec rx received	cc: reg_64

Register:: CEC_RxDR4_1 0x18DF					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_c	7:0	R	0	Information bits of data block 12 which cec rx received	cc: reg_65

Register:: CEC_RxDR4_2 0x18E0					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_d	7:0	R	0	Information bits of data block 13 which cec rx received	cc: reg_66

Register:: CEC_RxDR4_3 0x18E1					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_e	7:0	R	0	Information bits of data block 14 which cec rx received	cc: reg_67

Register:: CEC_RxDR4_4 0x18E2					
Name	bits	R/W/D	Reset State	Comments	Config
rx_fifo_f	7:0	R	0	Information bits of data block 15 which cec rx received	cc: reg_68

Register:: CEC_Rx_FIFO_RSV_0 0x18E3					
Name	bits	R/W/D	Reset State	Comments	Config
cec_rx_fifo_rsv0	7:0	R/W	0	reserved	

Register:: CEC_Rx_FIFO_RSV_1 0x18E4					
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Name	bits	R/W/D	Reset State	Comments	Config
cec_rx_fifo_rsv1	7:0	R/W	0	reserved	

The following is to set CEC_Rx's start-bit and data-bit timing.

Register:: CEC_RxTCR0_1					0x18E5
Name	bits	R/W/D	Reset State	Comments	Config
rx_start_low	7:0	R/W	0x8C	The low-pulse duration of cec_rx start-bit timing. Minimum is 3.5ms, nominal is 3.7ms, and maximum is 3.9ms. low duration = timer_enp*rx_start_low	cc: reg_69

Register:: CEC_RxTCR0_2					0x18E6
Name	bits	R/W/D	Reset State	Comments	Config
rx_start_period	7:0	R/W	0Xbc	The period duration of cec_rx start-bit timing. Minimum is 4.3ms, nominal is 4.5ms, and maximum is 4.7ms. period duration = timer_enp*rx_start_period	cc: reg_70

Register:: CEC_RxTCR0_3					0x18E7
Name	bits	R/W/D	Reset State	Comments	Config
rx_data_sample	7:0	R/W	0x2A	The sample point of cec_rx data-bit timing. Minimum is 0.85ms, nominal is 1.05ms, and maximum is 1.25ms. sample point = timer_enp*rx_data_sample	cc: reg_71

Register:: CEC_RxTCR0_4					0x18E8
Name	bits	R/W/D	Reset State	Comments	Config
rx_data_period	7:0	R/W	0x52	The period duration of cec_rx data-bit timing. Minimum is 2.05ms, nominal is 2.4ms, and maximum is 2.75ms. Period duration = timer_enp*rx_data_period	cc: reg_72

Register:: CEC_RxTCR0_5					0x18E9
Name	bits	R/W/D	Reset State	Comments	Config
rx_start_high	7:0	R/W	0xA0	The high-pointduration of cec_rx start-bit timing. low duration = timer_enp*rx_start_high	

Register:: CEC_RxTCR0_RSV_1					0x18EA
Name	bits	R/W/D	Reset State	Comments	Config
dbit_wrong_irq_en	7	R/W	0	IRQ as long as dbit wrong occurs	
dbit_wrong_flag	6	R	0	rx receive data-bit whether is invalid. (write 1 clear)	Wclr_out
tx_rx_error_irq_en	5	R/W	0	IRQ as long as tx_rx_error occurs	
tx_rx_error_flag	4	R	0	Rx check whether tx's transmission error occurs. (write 1 clear)	Wclr_out
data_byte_valid_flag	3	R	0	rx receive 10-bit data-block data whether is valid. (write 1 clear)	Wclr_out
header_byte_valid_flag	2	R	0	rx receive 10-bit header-block data whether is valid.	Wclr_out

				(write 1 clear)	
sbit_valid_irq_en	1	R/W	0	IRQ as long as start-bit invalid occurs	
sbit_valid_flag	0	R	0	rx receive start-bit whether is invalid. (write 1 clear)	Wclr_out

The following is to set CEC_Tx's start-bit and data-bit timing.

Register:: CEC_TxTCR0_1 0x18F0					
Name	bits	R/W/D	Reset State	Comments	Config
tx_start_low	7:0	R/W	0x94	The low-pulse duration of cec_tx start-bit timing. Minimum is 3.5ms, nominal is 3.7ms, and maximum is 3.9ms. low duration = timer_enp*tx_start_low	cc: reg_73

Register:: CEC_TxTCR0_2 0x18F1					
Name	bits	R/W/D	Reset State	Comments	Config
tx_start_high	7:0	R/W	0x20	The high-pulse duration of cec_tx start-bit timing. Minimum is 0.8ms, medium is 1.0ms, and maximum is 1.2ms. high duration = timer_enp*tx_start_high	cc: reg_74

Register:: CEC_TxTCR1_1 0x18F2					
Name	bits	R/W/D	Reset State	Comments	Config
tx_data_low	7:0	R/W	0x18	The low-pulse duration of cec_tx data-bit timing. Minimum is 0.4ms, nominal is 0.6ms, and maximum is 0.8ms. low duration = timer_enp*tx_data_low	cc: reg_75

Register:: CEC_TxTCR1_2 0x18F3					
Name	bits	R/W/D	Reset State	Comments	Config
tx_data_01	7:0	R/W	0x24	The data-width duration of cec_tx data. tx_data_01 represents the region of cec_data. Data-width duration = timer_enp*tx_data_01	cc: reg_76

Register:: CEC_TxTCR1_3 0x18F4					
Name	bits	R/W/D	Reset State	Comments	Config
tx_data_high	7:0	R/W	0x24	The high-pulse duration of cec_tx data-bit timing. Nominal 0.9ms. high duration = timer_enp*tx_data_high	cc: reg_77

Register:: CEC_RxTCR1_ACK_0 0x18F5					
Name	bits	R/W/D	Reset State	Comments	Config
ack_data_ctrl	7	R/W	0	Control ACK's bit timing 0: control by tx_data_low/tx_data_01 1: control by tx_ack_data_low/tx_ack_data_01	
cec_line_err_ctrl	6	R/W	0	Control cec line error handling's low duration 0: control by tx_start_low 1: control by cec_line_err_low	

cec_rxctrl_rsv0	5:0	R/W	0	Reserved	
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Register:: CEC_RxTCR1_ACK_1						0x18F6	
Name	bits	R/W/D	Reset State	Comments			Config
tx_ack_data_low	7:0	R/W	0x18	The low-pulse duration of ack data-bit timing. Minimum is 0.4ms, nominal is 0.6ms, and maximum is 0.8ms. low duration = timer_enp*tx_ack_data_low			

Register:: CEC_RxTCR1_ACK_2						0x18F7	
Name	bits	R/W/D	Reset State	Comments			Config
tx_ack_data_01	7:0	R/W	0x24	The data-width duration of ack data. Data-width duration = timer_enp*tx_ack_data_01			

Register:: CEC_RxTCR1_ERR						0x18F8	
Name	bits	R/W/D	Reset State	Comments			Config
cec_line_err_low	7:0	R/W	0x94	When meet cec line error handling, DUT generate a low bit period duration. duration = timer_enp*tx_start_low			

Register:: CEC_RxTCR1_RSV_0						0x18F9	
Name	bits	R/W/D	Reset State	Comments			Config
cec_rxctrl_rsv1	7:0	R/W	0	Reserved			

Register:: CEC_TIMING_CTRL_0						0x18FB	
Name	bits	R/W/D	Reset State	Comments			Config
dac_counter	7:0	R/W	0x87	reserved			

Register:: CEC_TIMING_CTRL_1						0x18FC	
Name	bits	R/W/D	Reset State	Comments			Config
timer_counter	7:0	R/W	0x14	reserved			

Overall CEC Function Block (Page 19)

CEC Digital Function (to be continuous)

The following is used for stand-by wakeup mode. HW takes 1st received cec data to compare with 15 kinds of reg_compare_opcode.

When received opcode is only equal to the first four compare_opcode, i.e., compare_opcode_01, compare_opcode_02, compare_opcode_03 and compare_opcode_04, CEC Tx can send specific opcode and operand. Each opcode collocates max three operands.

compare_opcode_01 setting

Register:: GDI_CEC_COMPARE_OPCODE_01					0X19a0
Name	bits	R/W/D	Reset	Comments	Config

			State		
compare_opcode_01	7:0	R/W	0x0	This opcode setting value is to compare with received opcode	cc: reg_78

Register:: GDI_CEC_SEND_OPCODE_01					0x19a1
Name	bits	R/W/D	Reset State	Comments	Config
send_opcode_01	7:0	R/W	0x0	If compare_opcode_01 is equal to received opcode, then cec_tx will send the opcode of send_opcode_01 with operand	cc: reg_79

Register:: GDI_CEC_SEND_OPERAND_NUMBER_01					0x19a2
Name	bits	R/W/D	Reset State	Comments	Config
cec_send_01_rsv	7:2	R/W	0	Reserved	
operand_number_01	1:0	R/W	0x0	The number of operand with send_opcode_01 00: 0 01: 1 10: 2 11: 3	cc: reg_80

Register:: GDI_CEC_OPERAND_01					0x19a3
Name	bits	R/W/D	Reset State	Comments	Config
operand_01	7:0	R/W	0x0	Operand_01 If operand_number_01 >= 1, then send this byte	cc: reg_81

Register:: GDI_CEC_OPERAND_02					0x19a4
Name	bits	R/W/D	Reset State	Comments	Config
operand_02	7:0	R/W	0x0	Operand_02 If operand_number_01 >= 2, then send this byte	cc: reg_82

Register:: GDI_CEC_OPERAND_03					0x19a5
Name	bits	R/W/D	Reset State	Comments	Config
operand_03	7:0	R/W	0x0	Operand_03 If operand_number_01 >= 3, then send this byte	cc: reg_83

Register:: GDI_CEC_COMOP01_RSV_0					0x19a6
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop01_rsv0	7:0	R/W	0	reserved	

Register:: GDI_CEC_COMOP01_RSV_1					0x19a7
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop01_rsv1	7:0	R/W	0	reserved	

compare_opcode_02 setting

Register:: GDI_CEC_COMPARE_OPCODE_02						0x19a8
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_02	7:0	R/W	0	This opcode setting value is to compare with received opcode		cc: reg_84

Register:: GDI_CEC_SEND_OPCODE_02						0x19a9
Name	bits	R/W/D	Reset State	Comments		Config
send_opcode_02	7:0	R/W	0x0	If compare_opcode_02 is equal to received opcode, then cec_tx send the opcode of send_opcode_02 with operand		cc: reg_85

Register:: GDI_CEC_SEND_OPERAND_NUMBER_02						0x19aa
Name	bits	R/W/D	Reset State	Comments		Config
cec_send_02_rsv	7:2	R/W	0x0	Reserved		
operand_number_02	1:0	R/W	0x0	The number of operand with send_opcode_02 00: 0 01: 1 10: 2 11: 3		cc: reg_86

Register:: GDI_CEC_OPERAND_04						0x19ab
Name	bits	R/W/D	Reset State	Comments		Config
operand_04	7:0	R/W	0x0	Operand_04 If operand_number_02 >= 1, then send this byte		cc: reg_87

Register:: GDI_CEC_OPERAND_05						0x19ac
Name	bits	R/W/D	Reset State	Comments		Config
operand_05	7:0	R/W	0x0	Operand_05 If operand_number_02 >= 2, then send this byte		cc: reg_88

Register:: GDI_CEC_OPERAND_06						0x19ad
Name	bits	R/W/D	Reset State	Comments		Config
operand_06	7:0	R/W	0x0	Operand_06 If operand_number_02 >= 3, then send this byte		cc: reg_89

Register:: GDI_CEC_COMOP02_RSV_0						0x19ae
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_comop02_rsv0	7:0	R/W	0	reserved		

Register:: GDI_CEC_COMOP02_RSV_1						0x19af
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_comop02_rsv1	7:0	R/W	0	reserved		

compare_opcode_03 setting

Register:: GDI_CEC_COMPARE_OPCODE_03						0x19b0
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Name	bits	R/W/D	Reset State	Comments	Config
compare_opcode_03	7:0	R/W	0	This opcode setting value is to compare with received opcode	cc: reg_90

Register:: GDI_CEC_SEND_OPCODE_03					0x19b1
Name	bits	R/W/D	Reset State	Comments	Config
send_opcode_03	7:0	R/W	0x0	If compare_opcode_03 is equal to received opcode, then send the opcode of send_opcode_03 with operand	cc: reg_91

Register:: GDI_CEC_SEND_OPERAND_NUMBER_03					0x19b2
Name	bits	R/W/D	Reset State	Comments	Config
cec_send_03_rsv	7:2	R/W	0	Reserved	
operand_number_03	1:0	R/W	0x0	The number of operand with send_opcode_03 00: 0 01: 1 10: 2 11: 3	cc: reg_92

Register:: GDI_CEC_OPERAND_07					0x19b3
Name	bits	R/W/D	Reset State	Comments	Config
operand_07	7:0	R/W	0x0	Operand 07 If Operand_number_03 >= 1, then send this byte	cc: reg_93

Register:: GDI_CEC_OPERAND_08					0x19b4
Name	bits	R/W/D	Reset State	Comments	Config
operand_08	7:0	R/W	0x0	Operand 08 If Operand_number_03 >= 2, then send this byte	cc: reg_94

Register:: GDI_CEC_OPERAND_09					0x19b5
Name	bits	R/W/D	Reset State	Comments	Config
operand_09	7:0	R/W	0x0	Operand 09 If Operand_number_03 >= 3, then send this byte	cc: reg_95

Register:: GDI_CEC_COMOP03_RSV_0					0x19b6
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop03_rsv0	7:0	R/W	0	reserved	

Register:: GDI_CEC_COMOP03_RSV_1					0x19b7
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop03_rsv1	7:0	R/W	0	reserved	

compare_opcode_04 setting

Register:: GDI_CEC_COMPARE_OPCODE_04					0x19b8
Name	bits	R/W/D	Reset State	Comments	Config
compare_opcode_04	7:0	R/W	0x0	This opcode setting value is to compare with received opcode	cc: reg_96

Register:: GDI_CEC_SEND_OPCODE_04					0x19b9
Name	bits	R/W/D	Reset State	Comments	Config
send_opcode_04	7:0	R/W	0x0	If compare_opcode_04 is equal to received opcode, then send the opcode of Send_opcode_04 with operand	cc: reg_97

Register:: GDI_CEC_SEND_OPERAND_NUMBER_04					0x19ba
Name	bits	R/W/D	Reset State	Comments	Config
cec_send_04_rsv	7:2	R/W	0	Reserved	
operand_number_04	1:0	R/W	0x0	The number of operand with Send_opcode_04 00: 0 01: 1 10: 2 11: 3	cc: reg_98

Register:: GDI_CEC_OPERAND_10					0x19bb
Name	bits	R/W/D	Reset State	Comments	Config
operand_10	7:0	R/W	0x0	Operand 10 If Operand_number_04 >= 1, then send this byte	cc: reg_99

Register:: GDI_CEC_OPERAND_11					0x19bc
Name	bits	R/W/D	Reset State	Comments	Config
operand_11	7:0	R/W	0x0	Operand 11 If Operand_number_04 >= 2, then send this byte	cc: reg_100

Register:: GDI_CEC_OPERAND_12					0x19bd
Name	bits	R/W/D	Reset State	Comments	Config
operand_12	7:0	R/W	0x0	Operand 12 If Operand_number_04 >= 3, then send this byte	cc: reg_101

Register:: GDI_CEC_COMOP04_RSV_0					0x19be
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop04_rsv0	7:0	R/W	0	reserved	

Register:: GDI_CEC_COMOP04_RSV_1					0x19bf
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_comop04_rsv1	7:0	R/W	0	reserved	

compare_opcode_05 setting

Register:: GDI_CEC_COMPARE_OPCODE_05						0x19c0
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_05	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_102

compare_opcode_06 setting

Register:: GDI_CEC_COMPARE_OPCODE_06						0x19c1
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_06	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_103

compare_opcode_07 setting

Register:: GDI_CEC_COMPARE_OPCODE_07						0x19c2
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_07	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_104

compare_opcode_08 setting

Register:: GDI_CEC_COMPARE_OPCODE_08						0x19c3
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_08	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_105

compare_opcode_09 setting

Register:: GDI_CEC_COMPARE_OPCODE_09						0x19c4
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_09	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_106

compare_opcode_10 setting

Register:: GDI_CEC_COMPARE_OPCODE_10						0x19c5
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_10	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_107

compare_opcode_11 setting

Register:: GDI_CEC_COMPARE_OPCODE_11						0x19c6
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_11	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_108

compare_opcode_12 setting

Register:: GDI_CEC_COMPARE_OPCODE_12						0x19c7
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_12	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_109

compare_opcode_13 setting

Register:: GDI_CEC_COMPARE_OPCODE_13						0x19c8
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_13	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_110

compare_opcode_14 setting

Register:: GDI_CEC_COMPARE_OPCODE_14						0x19c9
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_14	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_111

compare_opcode_15 setting

Register:: GDI_CEC_COMPARE_OPCODE_15						0x19ca
Name	bits	R/W/D	Reset State	Comments		Config
compare_opcode_15	7:0	R/W	0x0	This opcode setting value is to compare with received opcode		cc: reg_112

Register:: GDI_CEC_TXOP_RSV_0						0x19cb
Name	bits	R/W/D	Reset State	Comments		Config
com_op_mode	7	R/W	0	Rx_fifo_compare data mode: 0: data keep compare when compare fail 1: data-by-data compare		
standby_addr_sel	6	R/W	0	In standby mode, follower's logical address selection: 0: HW direct reply command to initiator 1: FW setting by standby_ini_addr		
standby_ini_addr	5:2	R/W	0	In standby mode, follower addr by FW setting		
gdi_cec_txop_rsv0	1:0	R/W	0	reserved		

Register:: GDI_CEC_TXOP_RSV_1						0x19cc
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_txop_rsv1	7:0	R/W	0	reserved		

Register:: GDI_CEC_TXOP_RSV_2						0x19cd
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_txop_rsv2	7:0	R/W	0	reserved		

The following is to enable compare_opcode mode.

Register:: GDI_CEC_OPCODE_ENABLE_1						0x19d0
Name	bits	R/W/D	Reset State	Comments		Config
en_compare_opcode_15	7	R/W	0x0	Rx compare opcode enable or disable		cc: reg_113

				1:Enable 0:Disable	
en_compare_opcode_14	6	R/W	0x0	1:Enable 0:Disable	cc: reg_114
en_compare_opcode_13	5	R/W	0x0	1:Enable 0:Disable	cc: reg_115
en_compare_opcode_12	4	R/W	0x0	1:Enable 0:Disable	cc: reg_116
en_compare_opcode_11	3	R/W	0x0	1:Enable 0:Disable	cc: reg_117
en_compare_opcode_10	2	R/W	0x0	1:Enable 0:Disable	cc: reg_118
en_compare_opcode_09	1	R/W	0x0	1:Enable 0:Disable	cc: reg_119
en_compare_opcode_08	0	R/W	0x0	1:Enable 0:Disable	cc: reg_120

Register:: GDI_CEC_OPCODE_ENABLE_2					0x19d1
Name	bits	R/W/D	Reset State	Comments	Config
en_compare_opcode_07	7	R/W	0x0	1:Enable 0:Disable	cc: reg_121
en_compare_opcode_06	6	R/W	0x0	1:Enable 0:Disable	cc: reg_122
en_compare_opcode_05	5	R/W	0x0	1:Enable 0:Disable	cc: reg_123
en_compare_opcode_04	4	R/W	0x0	1:Enable 0:Disable	cc: reg_124
en_compare_opcode_03	3	R/W	0x0	1:Enable 0:Disable	cc: reg_125
en_compare_opcode_02	2	R/W	0x0	1:Enable 0:Disable	cc: reg_126
en_compare_opcode_01	1	R/W	0x0	1:Enable 0:Disable	cc: reg_127
cec_opcode_2_rsv	0	R/W	0x0	reserved	

The following flags are mainly for FW to know which one opcode is hit. These flags are valid when FW enables the corresponding registers. Ex: when en_compare_opcode_01 = 1, hit_compare_opcode_01 is valid.

Register:: GDI_CEC_HIT_OPCODE_0					0x19d2
Name	bits	R/W/D	Reset State	Comments	Config
hit_compare_opcode_15	7	R	0x0	The flag shows opcode_15 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_14	6	R	0x0	The flag shows opcode_14 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_13	5	R	0x0	The flag shows opcode_13 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_12	4	R	0x0	The flag shows opcode_12 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_11	3	R	0x0	The flag shows opcode_11 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_10	2	R	0x0	The flag shows opcode_10 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_09	1	R	0x0	The flag shows opcode_09 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_08	0	R	0x0	The flag shows opcode_08 is hit (write 1 clear)	Wclr_out

Register:: GDI_CEC_HIT_OPCODE_1					0x19d3
Name	bits	R/W/D	Reset State	Comments	Config
hit_compare_opcode_07	7	R	0x0	The flag shows opcode_07 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_06	6	R	0x0	The flag shows opcode_06 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_05	5	R	0x0	The flag shows opcode_05 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_04	4	R	0x0	The flag shows opcode_04 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_03	3	R	0x0	The flag shows opcode_03 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_02	2	R	0x0	The flag shows opcode_02 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_01	1	R	0x0	The flag shows opcode_01 is hit (write 1 clear)	Wclr_out
hit_compare_opcode_rsv0	0	R/W	0x0	reserved	

Register:: GDI_CEC_HIT_OPCODE_RSV_0					0x19d4
Name	bits	R/W/D	Reset	Comments	Config

			State		
gdi_cec_hit_opcode_rsv0	7:0	R/W	0x0	Reserved	

Register:: GDI_CEC_HIT_OPCODE_RSV_1					0x19d5
Name	bits	R/W/D	Reset State	Comments	Config
gdi_cec_hit_opcode_rsv1	7:0	R/W	0x0	Reserved	

Register:: CEC_FUN_DEBUG_0					0x19d6
Name	bits	R/W/D	Reset State	Comments	Config
cec_dig_dbg_sel	7:5	R/W	0x0	Cec digital debug selection: 000: cec dac ctrl 001: cec ebp gen 010: cec pwrsav 011: cec rx Others: cec tx	
cec_debug_sel	4	R/W	0x0	Debug data selection 0: cec digital 1: cec analog	
cec_fun_reserved0	3:0	R/W	0x0	reserved	

The following is set CEC_EN behavior:

Register:: CEC_FUN_RESERVED_1					0x19d7
Name	bits	R/W/D	Reset State	Comments	Config
cec_en_mode	7	R/W	0x0	Mode selection of cec_en to analog: 0: FW mode 1: HW mode	
cec_en_fw_db	6	R/W	0x1	Fw's cec_en control mode: 0: not double-buffered 1: double-buffered by HW	
cec_en_by_hw	5	R	-	Read hw's cec_en result Note: write 1 clear	Wclr_out
cec_en_ctrl_hw	4	R	-	This flag occurs as long as cec_en_by_hw occurs. Note: write 1 clear	Wclr_out
cec_en_ctrl_hw_irq_en	3	R/W	0x0	Enable cec_en_ctrl_hw's IRQ	
wait_time_mode	2	R/W	0x0	Keep wait time for cec_en_hw to disable, the start time is from cec_tx transmission ended. 0: disable 1: enable	
cec_en_la_cond	1	R/W	0x0	Receive 8-bit valid logical address, whether need to check follower's LA is equal to local's LA or broadcast message 0: check 1: not check	
cec_en_2_ana	0	R	0x0	cec_en to analog result	

Register:: CEC_INTCR_RSV_1					0x19d8
Name	bits	R/W/D	Reset State	Comments	Config
wait_time[15:8]	7:0	R/W/D	0x0	Wait time for hw's cec_en falling. Start point is dig_tx transmission ended. 1: 3*xtal_clk 2: 4*xtal_clk ...	

Register:: CEC_PS_RESERVED_0					0x19d9
Name	bits	R/W/D	Reset State	Comments	Config
wait_time[7:0]	7:0	R/W	0x1	Wait time for hw's cec_en falling	wport

*Note: wait_time[15:8] is double-buffered when wait_time[7:0] is written in.

Register:: CEC_FUN_RESERVED_4					0x19da
Name	bits	R/W/D	Reset State	Comments	Config
cec_fun_reserved4	7:0	R/W	0x0	reserved	

Register:: CEC_FUN_RESERVED_5					0x19db
Name	bits	R/W/D	Reset State	Comments	Config
cec_fun_reserved5	7:0	R/W	0x0	reserved	

CEC Digital Power Saving Mode Control

CEC power saving is to wake up HDMI function.

Register:: CEC_POWER_SAVING_MODE					0x19e0
Name	bits	R/W	Reset State	Comments	Config
cec_power_saving_en	7	R/W	0x0	Power saving mode enable 0: normal mode 1: power saving mode Note: this bit is used to enable gdi_wakeup_irq	cc: reg_128
cec_irq_en	6	R/W	0x0	CEC IRQ in power saving mode 0: disable 1: enable	cc: reg_129
cec_irq_inv	5	R/W	0x0	Inverse CEC IRQ 0: disable 1: enable	cc: reg_200
cec_all_irq_keep	4	R	0x0	When cec_all_irq occurs, this bit would be assigned to 1 by HW, and this IRQ would be pended until FW clear this bit(write 1 clear) Note: this bit is used for cec wakeup	cc: reg_130 Wclr_out
cec_msg_status_01	3	R	0x0	cec_msg_status_01 (write 1 clear)	cc: reg_201 Wclr_out
cec_msg_status_02	2	R	0x0	cec_msg_status_02 (write 1 clear)	cc: reg_202 Wclr_out

cec_wakeup_irq_keep	1	R	0x0	cec wakeup IRQ	Wclr_out
cec_pwrsav_rsv	0	R/W	0x0	Reserved	

*Note:

(1) cec_msg_status_01: this flag occurs as long as when (1) single-case(cec_rx's LA = logical_addr) or (2) broadcast- case, HW decides to give ACK.

Case(1): when cec_rx's LA = logical_addr, as long as cec_tx's LA is what cec_rx wants, HW gives ACK.

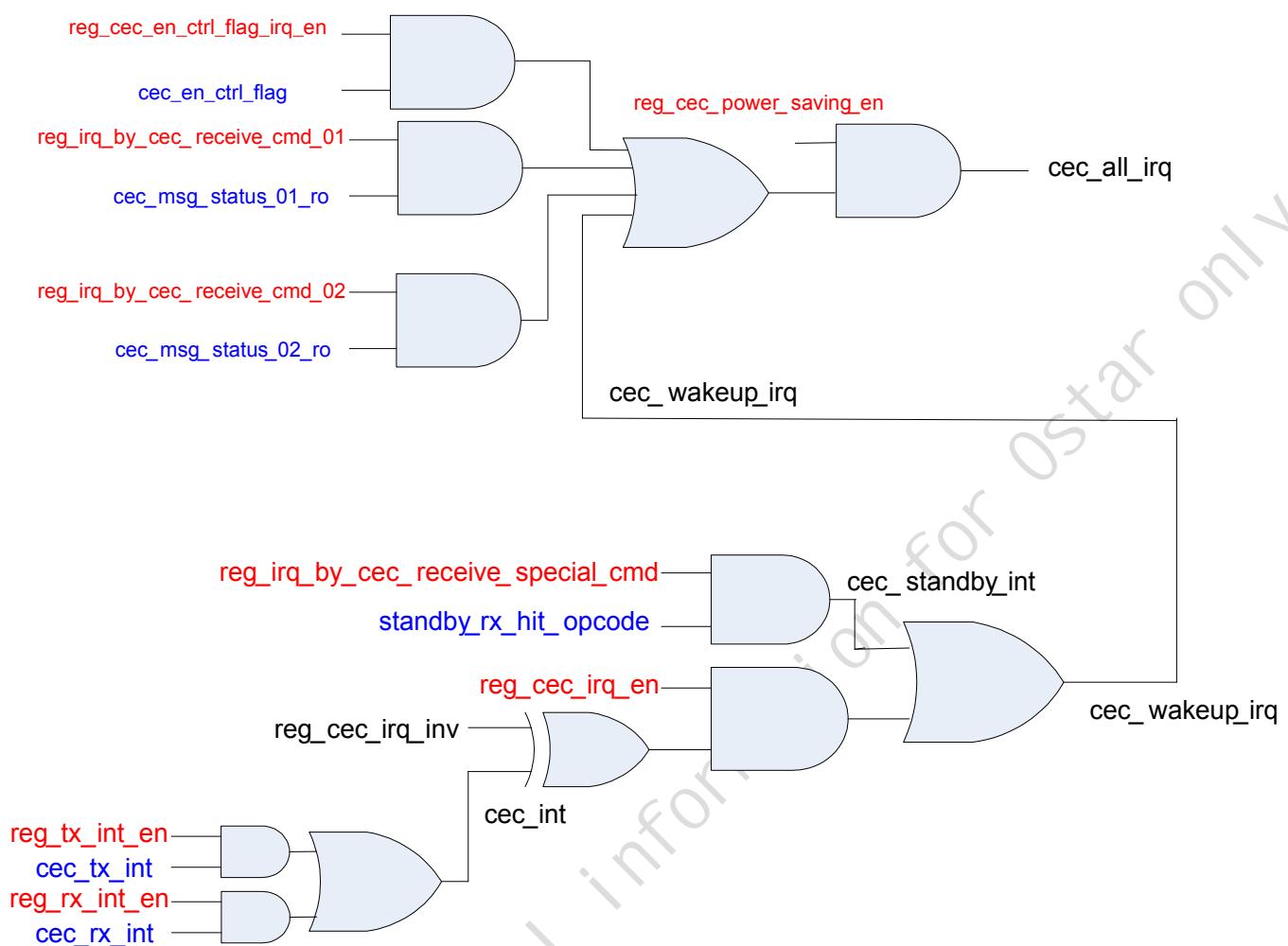
Case(2): as the below.

(2) cec_msg_status_02: this flag occurs as long as when in broadcast case, HW decides to give ACK.

Register:: CEC_POWER_SAVING_MODE_RSV_0						0x19e1
Name	bits	R/W/D	Reset State	Comments		Config
gdi_ps_mode_rsv0	7:0	R/W	0x0	Reserved		

Register:: CEC_POWER_SAVING_MODE_RSV_1						0x19e2
Name	bits	R/W/D	Reset State	Comments		Config
gdi_ps_mode_rsv1	7:0	R/W	0x0	Reserved		

GDI _wakeup_irq /CEC_wakeup_irq behavior:



Register::: CEC_INTCR_01						0x19e3
Name	bits	R/W	Reset State	Comments		Config
irq_by_cec_receive_cmd_01	7	R/W	0x0	IRQ control as long as when cec_msg_status_01 occurs 0: disable 1: enable		cc: reg_203
irq_by_cec_receive_cmd_02	6	R/W	0x0	IRQ control as long as cec_msg_status_02 occurs 0: disable 1: enable		cc: reg_204
irq_by_cec_receive_special_cmd	5	R/W	0x0	If CEC Rx receive command which is equal to one of compare_opcode_01~compare_opcode_15 (for its logic-address or broadcast), cec stand-by interrupt 0:disable 1:enable		cc: reg_131
cec_driver_en_ctrl	4	R/W	0x0	cec psm (to analog CEC) is determined by 0:Software(control by cec_driver_en_ctrl_by_sw) 1:Hardware		cc: reg_132
cec_driver_en_ctrl_by_sw	3	R/W	0x1	SW decide cec psm which is for analog CEC use 0:CEC driver signal disable 1:CEC driver signal enable		cc: reg_133
cec_int_rsv	2:0	R/W	0x0	reserved		

Register::: CEC_INTCR_02	0x19e4
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Name	bits	R/W/D	Reset State	Comments	Config
cec_int_keep	7	R	-	cec interrupt Note: write 1 clear	Wclr_out
cec_standby_int_keep	6	R	-	cec standby interrupt Note: write 1 clear	Wclr_out
standby_rx_hit_opcode	5	R	-	standby_rx_hit_opcode Note: write 1 clear	Wclr_out
cec_inter_rsv0	4:0	R/W	0x0	Reserved	

Register:: CEC_PS_RSV_0					0x19e5
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_rsv0	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RSV_1					0x19e6
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_rsv1	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RESERVED_1					0x19e7
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_reserved1	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RESERVED_2					0x19e8
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_reserved2	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RESERVED_3					0x19e9
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_reserved3	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RESERVED_4					0x19eA
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_reserved4	7:0	R/W	0x0	reserved	

Register:: CEC_PS_RESERVED_5					0x19eB
Name	bits	R/W/D	Reset State	Comments	Config
cec_ps_reserved5	7:0	R/W	0x0	reserved	

Analog CEC Tx Control

Register:: GDI_CEC_ANALOG_1						0x19f0
Name	bits	R/W/D	Reset State	Comments		Config
cec	7	R/W	0x1	CEC line driver enable 0: disable 1: enable Note: this bit is cec_en		
cec_entst	6	R/W	0x0	CEC entst		
cec_dr	5:4	R/W	1	CEC driver slew rate control 00: 1x 01: 2x 10: 3x 11: 4x		
reserved	3:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANALOG_2						0x19f1
Name	bits	R/W/D	Reset State	Comments		Config
reserved	7:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANA_RESERVED_0						0x19f2
Name	bits	R/W/D	Reset State	Comments		Config
reserved	7:0	R	0	reserved		

Register:: GDI_CEC_ANA_RESERVED_1						0x19f3
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_ana_reserved1	7:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANA_RESERVED_2						0x19f4
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_ana_reserved2	7:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANA_RESERVED_3						0x19f5
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_ana_reserved3	7:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANA_RESERVED_4						0x19f6
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_ana_reserved4	7:0	R/W	0x0	reserved		

Register:: GDI_CEC_ANA_RESERVED_5						0x19f7
Name	bits	R/W/D	Reset State	Comments		Config
gdi_cec_ana_reserved5	7:0	R/W	0x0	reserved		

GDI DFE (Page 1D)

DFE CONTROL

Register::L0_DFE_EN_1				0xA0	
Name	Bits	R/W	Default	Comments	Config
clk_inv_lane0	7	R/W	0x0	inverse the symbol-rate clock in adaptation loop, 0 : positive, 1 : negative	
timer_ctrl_en_lane0	6	R/W	0x1	Enable the timer to control adaptation-loop (0 : disable, 1: timer control)	
reduce_adapt_gain_lane0[1:0]	5:4	R/W	0x0	Reduce the all adaptation-loop's gain after settling (00 : no-change, 01 : 1/2, 10 : 1/4)	
rl_det_en_lane0	3	R/W	0x1	Enable run-length detection (0 : disable, 1 : enable)	
rl_det_mode_lane0	2	R/W	0x0	Blank out case-3 symbol (0 : bypass, 1: blank out)	
rl_threshold_lane0[1:0]	1:0	R/W	0x1	The threshold of run-length detection (00 : 6, 01 : 7, 10 : 8, 11 : 9)	

Register:: L0_DFE_EN_2				0xA1	
Name	Bits	R/W	Default	Comments	Config
dfe_adapt_en_lane0[7:0]	7:0	R/W	0xFF	Enable the LE, Vth-adjust, servo-loop, or tap0~4 adaptation loop (LE_en, Vth_en, servo_en, tap4_en, tap3_en, tap2_en, tap1_en, tap0_en)	

Register:: L0_LIMIT_INIT				0xA2	
Name	Bits	R/W	Default	Comments	Config
le_min_lane0[3:0]	7:4	R/W	0xF	Minimum of LE (-0 ~ -31)	
le_init_lane0[3:0]	3:0	R/W	0xC	Initial value of LE coefficient, effective only on mode 0/2 (bit[3:0] : -0~31)	

Register:: L0_INIT_1				0xA3	
Name	Bits	R/W	Default	Comments	Config
le_min_lane0[4]	7	R/W	0x0	Minimum of LE (-0 ~ -31)	e_mi n_la ne0[4]
le_init_lane0[4]	6	R/W	0x0	Initial value of LE coefficient, effective only on mode 0/2 (-0~31)	e_in i_t_lan e0[4]
init_rev1_lane0	5	R/W	0x0	Reserved	nit_r ev1_ lane 0
servo_init_lane0[4:0]	4:0	R/W	0x0F	Initial value of servo-loop coefficient (bit[7:0] : +0~+31)	

Register:: L0_INIT_2				0xA4	
Name	Bits	R/W	Default	Comments	Config
init_rev2_lane0[2:0]	7:5	R/W	0x0	Reserved	
tap0_init_lane0[4:0]	4:0	R/W	0x0C	Initial value of Tap0 coefficient (bit[4:0] : +0~+31)	

Register:: L0_INIT_3 0xA5					
Name	Bits	R/W	Default	Comments	Config
init_rev3_lane0[1:0]	7:6	R/W	0x0	Reserved	
tap1_init_lane0[5:0]	5:0	R/W	0x0C	Initial value of Tap1 coefficient (bit[5:0] : -0~64)	

Register:: L0_INIT_4 0xA6					
Name	Bits	R/W	Default	Comments	Config
init_rev4_lane0[1:0]	7:6	R/W	0x0	Reserved	
tap2_init_lane0[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L0_INIT_5 0xA7					
Name	Bits	R/W	Default	Comments	Config
init_rev5_lane0[1:0]	7:6	R/W	0x0	Reserved	
tap3_init_lane0[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L0_INIT_6 0xA8					
Name	Bits	R/W	Default	Comments	Config
init_rev6_lane0[1:0]	7:6	R/W	0x0	Reserved	
tap4_init_lane0[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L0_INIT_7 0xA9					
Name	Bits	R/W	Default	Comments	Config
init_rev7_lane0[3:0]	7:4	R/W	0x0	Reserved	
vth_init_lane0[3:0]	3:0	R/W	0x8	Initial value of V _{th} -adjust coefficient (bit[3:0] : +0~+15)	

Register:: L0_INIT_8 0xAA					
Name	Bits	R/W	Default	Comments	Config
load_in_init_lane0[7:0]	7:0	R/W	0x00	Load-in the initial value from register to adaptation loop (LE, Vth, servo, tap4, tap3, tap2, tap1, tap0)	

Register:: L0_STABLE_FLAG 0xAB					
Name	Bits	R/W	Default	Comments	Config
sf_threshold_lane0[1:0]	7:6	R/W	0x0	The total threshold of stable-flag (00 : 2, 01 : 4, 10 : 6, 11 : 7)	
stable_flag_sel_lane0	5	R/W	0x0	Select the group of stable flag (0 : Vth/Tap0/Tap1/Tap2, 1 : servo/Tap3/LE/Tap4)	
adapt_fail_flag_lane0	4	R	0x0	Fail flag when max-tap0 & min-V _{th}	
stable_flag_lane0[3:0]	3:0	R	0x0	Stable flag	

Register:: L0_COEF_1 0xAB					
Name	Bits	R/W	Default	Comments	Config
eof_sel_lane0[7:0]	7:0	R/W	0x00	Select the coefficients for read-back	

Register:: L0_COEF_2 0xAC					
Name	Bits	R/W	Default	Comments	Config
eof_data_lane0[7:0]	7:0	R	0x00	Read-back the loop-coefficients	

Register:: L0_REV_1 0xAD					
Name	Bits	R/W	Default	Comments	Config
servo_overflow_flag_lane0	7	R	0x0	DC servo's coefficient overflow	
servo_underflow_flag_lane0	6	R	0x0	DC servo's coefficient underflow	
rev_1_lane0[7:0]	7:0	R/W	0x00	Reserved	

Register:: L1_DFE_EN_1 0xB0					
Name	Bits	R/W	Default	Comments	Config
clk_inv_lane1	7	R/W	0x0	inverse the symbol-rate clock in adaptation loop, 0 : positive, 1 : negative	
timer_ctrl_en_lane1	6	R/W	0x1	Enable the timer to control adaptation-loop (0 : disable, 1: timer control)	
reduce_adapt_gain_lane1[1:0]	5:4	R/W	0x0	Reduce the all adaptation-loop's gain after settling (00 : no-change, 01 : 1/2, 10 : 1/4)	
rl_det_en_lane1	3	R/W	0x1	Enable run-length detection (0 : disable, 1 : enable)	
rl_det_mode_lane1	2	R/W	0x0	Blank out case-3 symbol (0 : bypass, 1: blank out)	
rl_threshold_lane1[1:0]	1:0	R/W	0x1	The threshold of run-length detection (00 : 6, 01 : 7, 10 : 8, 11 : 9)	

Register:: L1_DFE_EN_2 0xB1					
Name	Bits	R/W	Default	Comments	Config
dfe_adapt_en_lane1[7:0]	7:0	R/W	0xFF	Enable the LE, Vth-adjust, servo-loop, or tap0~4 adaptation loop (LE_en, Vth_en, servo_en, tap4_en, tap3_en, tap2_en, tap1_en, tap0_en)	

Register:: L1_LIMIT_INIT 0xB2					
Name	Bits	R/W	Default	Comments	Config
le_min_lane1[3:0]	7:4	R/W	0xF	Minimum of LE (-0 ~ -31)	
sle_init_lane1[3:0]	3:0	R/W	0xC	Initial value of LE coefficient, effective only on mode 0/2 (bit[3:0] : -0~+31)	

Register:: L1_INIT_1 0xB3					
Name	Bits	R/W	Default	Comments	Config
le_min_lane1[4]	7	R/W	0x0	Minimum of LE (-0 ~ -31)	
le_init_lane1[4]	6	R/W	0x0	Initial value of LE coefficient effective only on mode 0/2(bit[7:0] : +0~+31)	
Init_rev1_lane1	5	R/W	0x0	Reserved	
servo_init_lane1[4:0]	4:0	R/W	0x0F	Initial value of servo-loop coefficient(bit[7:0]:+0~+31)	

Register:: L1_INIT_2 0xB4					
Name	Bits	R/W	Default	Comments	Config
init_rev2_lane1[2:0]	7:5	R/W	0x0	Reserved	
tap0_init_lane1[4:0]	4:0	R/W	0x0C	Initial value of Tap0 coefficient (bit[4:0] : +0~+31)	

Register:: L1_INIT_3 0xB5					
Name	Bits	R/W	Default	Comments	Config
init_rev3_lane1[1:0]	7:6	R/W	0x0	Reserved	
tap1_init_lane1[5:0]	5:0	R/W	0x0C	Initial value of Tap1 coefficient (bit[5:0] : -0~-64)	

Register:: L1_INIT_4
0xB6

Name	Bits	R/W	Default	Comments	Config
init_rev4_lane1[1:0]	7:6	R/W	0x0	Reserved	
tap2_init_lane1[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L1_INIT_5
0xB7

Name	Bits	R/W	Default	Comments	Config
init_rev5_lane1[1:0]	7:6	R/W	0x0	Reserved	
tap3_init_lane1[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L1_INIT_6
0xB8

Name	Bits	R/W	Default	Comments	Config
init_rev6_lane1[1:0]	7:6	R/W	0x0	Reserved	
tap4_init_lane1[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L1_INIT_7
0xB9

Name	Bits	R/W	Default	Comments	Config
init_rev7_lane1[3:0]	7:4	R/W	0x0	Reserved	
vth_init_lane1[3:0]	3:0	R/W	0x8	Initial value of V _{th} -adjust coefficient (bit[3:0] : +0~+15)	

Register:: L1_INIT_8
0xBA

Name	Bits	R/W	Default	Comments	Config
load_in_init_lane1[7:0]	7:0	R/W	0x00	Load-in the initial value from register to adaptation loop (LE, V _{th} , servo, tap4, tap3, tap2, tap1, tap0)	

Register:: L1_STABLE_FLAG
0xBB

Name	Bits	R/W	Default	Comments	Config
sf_threshold_lane1[1:0]	7:6	R/W	0x0	The total threshold of stable-flag (00 : 2, 01 : 4, 10 : 6, 11 : 7)	
stable_flag_sel_lane1	5	R/W	0x0	Select the group of stable flag (0 : V _{th} /Tap0/Tap1/Tap2, 1 : servo/Tap3/LE/Tap4)	
adapt_fail_flag_lane1	4	R	0x0	Fail flag when max-tap0 & min-V _{th}	
stable_flag_lane1[3:0]	3:0	R	0x0	Stable flag	

Register:: L1_COEF_1
0xBB

Name	Bits	R/W	Default	Comments	Config
coef_sel_lane1[7:0]	7:0	R/W	0x00	Select the coefficients for read-back	

Register:: L1_COEF_2
0xBC

Name	Bits	R/W	Default	Comments	Config
coef_data_lane1[7:0]	7:0	R	0x00	Read-back the loop coefficients	

Register:: L1_REV_1
0xBD

Name	Bits	R/W	Default	Comments	Config
servo_overflow_flag_lane1	7	R	0x0	DC-servo's coefficient overflow	
servo_underflow_flag_lane1	6	R	0x0	DC-servo's coefficient underflow	

<code>rev_1_lane1[7:0]</code>	7:0	R/W	0x00	Reserved	
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Register::L2_DFE_EN_1 0xC0					
Name	Bits	R/W	Default	Comments	Config
clk_inv_lane2	7	R/W	0x0	inverse the symbol-rate clock in adaptation loop, 0 : positive, 1 : negative	
timer_ctrl_en_lane2	6	R/W	0x1	Enable the timer to control adaptation-loop (0 : disable, 1: timer control)	
reduce_adapt_gain_lane2[1:0]	5:4	R/W	0x0	Reduce the all adaptation-loop's gain after settling (00 : no-change, 01 : 1/2, 10 : 1/4)	
rl_det_en_lane2	3	R/W	0x1	Enable run-length detection (0 : disable, 1 : enable)	
rl_det_mode_lane2	2	R/W	0x0	Blank out case-3 symbol (0 : bypass, 1: blank out)	
rl_threshold_lane2[1:0]	1:0	R/W	0x1	The threshold of run-length detection (00 : 6, 01 : 7, 10 : 8, 11 : 9)	

Register:: L2_DFE_EN_2 0xC1					
Name	Bits	R/W	Default	Comments	Config
dfe_adapt_en_lane2[7:0]	7:0	R/W	0xFF	Enable the LE, Vth-adjust, servo-loop, or tap0~4 adaptation loop (LE_en, Vth_en, servo_en, tap4_en, tap3_en, tap2_en, tap1_en, tap0_en)	

Register:: L2_LIMIT_INIT 0xC2					
Name	Bits	R/W	Default	Comments	Config
le_min_lane2[3:0]	7:4	R/W	0xF	Minimum of LE (-0 ~ -31)	
le_init_lane2[3:0]	3:0	R/W	0xC	Initial value of LE coefficient, effective only on mode 0/2 (bit[3:0] : -0~-31)	

Register:: L2_INIT_1 0xC3					
Name	Bits	R/W	Default	Comments	Config
le_min_lane2[4]	7	R/W	0x0	Mininum of LE(-0~31)	
le_init_lane2[4]	6	R/W	0x0	Initial value of LE coeffiecient,effective only on mode 0/2(-0~31)	
init_rev1_lane2	5	R/W	0x0	Reserved	
servo_init_lane2[4:0]	4:0	R/W	0x0F	Initial value of servo-loop coefficient (bit[7:0] : +0~+31)	

Register:: L2_INIT_2 0xC4					
Name	Bits	R/W	Default	Comments	Config
init_rev2_lane2[2:0]	7:5	R/W	0x0	Reserved	
tap0_init_lane2[4:0]	4:0	R/W	0x0C	Initial value of Tap0 coefficient (bit[4:0] : +0~+31)	

Register:: L2_INIT_3 0xC5					
Name	Bits	R/W	Default	Comments	Config
init_rev3_lane2[1:0]	7:6	R/W	0x0	Reserved	
tap1_init_lane2[5:0]	5:0	R/W	0x0C	Initial value of Tap1 coefficient (bit[5:0] : -0~-64)	

Register:: L2_INIT_4 0xC6					
Name	Bits	R/W	Default	Comments	Config
init_rev4_lane2[1:0]	7:6	R/W	0x0	Reserved	

tap2_init_lane2[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	
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Register::: L2_INIT_5 0xC7					
Name	Bits	R/W	Default	Comments	Config
init_rev5_lane2[1:0]	7:6	R/W	0x0	Reserved	
tap3_init_lane2[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register::: L2_INIT_6 0xC8					
Name	Bits	R/W	Default	Comments	Config
init_rev6_lane2[1:0]	7:6	R/W	0x0	Reserved	
tap4_init_lane2[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register::: L2_INIT_7 0xC9					
Name	Bits	R/W	Default	Comments	Config
init_rev7_lane2[3:0]	7:4	R/W	0x0	Reserved	
vth_init_lane2[3:0]	3:0	R/W	0x8	Initial value of V _{th} -adjust coefficient (bit[3:0] : +0~+15)	

Register::: L2_INIT_8 0xCA					
Name	Bits	R/W	Default	Comments	Config
load_in_init_lane2[7:0]	7:0	R/W	0x00	Load-in the initial value from register to adaptation loop (LE, Vth, servo, tap4, tap3, tap2, tap1, tap0)	

Register::: L2_STABLE_FLAG 0xCB					
Name	Bits	R/W	Default	Comments	Config
sf_threshold_lane2[1:0]	7:6	R/W	0x0	The total threshold of stable-flag (00 : 2, 01 : 4, 10 : 6, 11 : 7)	
stable_flag_sel_lane2	5	R/W	0x0	Select the group of stable flag (0 : Vth/Tap0/Tap1/Tap2, 1 : servo/Tap3/LE/Tap4)	
adapt_fail_flag_lane2	4	R	0x0	Fail flag when max-tap0 & min-V _{th}	
stable_flag_lane2[3:0]	3:0	R	0x0	Stable flag	

Register::: L2_COEF_1 0xCB					
Name	Bits	R/W	Default	Comments	Config
coef_sel_lane2[7:0]	7:0	R/W	0x00	Select the coefficients for read-back	

Register::: L2_COEF_2 0xCC					
Name	Bits	R/W	Default	Comments	Config
coef_data_lane2[7:0]	7:0	R	0x00	Read-back the loop coefficients	

Register::: L2_REV_1 0xCD					
Name	Bits	R/W	Default	Comments	Config
servo_overflow_flag_lane2	7	R	0x0	DC servo's coefficient overflow	
servo_underflow_flag_lane2	6	R	0x0	DC servo's coefficient underflow	
rev_1_lane2[7:0]	7:0	R/W	0x00	Reserved	

Register::: L3_DFE_EN_1 0xD0					
Name	Bits	R/W	Default	Comments	Config
clk_inv_lane3	7	R/W	0x0	inverse the symbol-rate clock in adaptation loop, 0 : positive, 1 : negative	

timer_ctrl_en_lane3	6	R/W	0x1	Enable the timer to control adaptation-loop (0 : disable, 1: timer control)	
reduce_adapt_gain_lane3[1:0]	5:4	R/W	0x0	Reduce the all adaptation-loop's gain after settling (00 : no-change, 01 : 1/2, 10 : 1/4)	
rl_det_en_lane3	3	R/W	0x1	Enable run-length detection (0 : disable, 1 : enable)	
rl_det_mode_lane3	2	R/W	0x0	Blank out case-3 symbol (0 : bypass, 1: blank out)	
rl_threshold_lane3[1:0]	1:0	R/W	0x1	The threshold of run-length detection (00 : 6, 01 : 7, 10 : 8, 11 : 9)	

Register:: L3_DFE_EN_2					0xD1
Name	Bits	R/W	Default	Comments	Config
dfe_adapt_en_lane3[7:0]	7:0	R/W	0xFF	Enable the LE, Vth-adjust, servo-loop, or tap0~4 adaptation loop (LE_en, Vth_en, servo_en, tap4_en, tap3_en, tap2_en, tap1_en, tap0_en)	

Register:: L3_LIMIT_INIT					0xD2
Name	Bits	R/W	Default	Comments	Config
le_min_lane3[3:0]	7:4	R/W	0xF	Minimum of LE (-0 ~ -31)	
le_init_lane3[3:0]	3:0	R/W	0xC	Initial value of LE coefficient, effective only on mode 0/2 (bit[3:0] : -0~-31)	

Register:: L3_INIT_1					0xD3
Name	Bits	R/W	Default	Comments	Config
le_min_lane3[4]	7	R/W	0x0	Minimum of LE (-0 ~ -31)	
le_init_lane3[4]	6	R/W	0x0	Initial value of LE coefficient, effective only on mode 0/2(-0~-31)	
init_rev1_lane3	5	R/W	0x0	Reserved	
servo_init_lane3[4:0]	4:0	R/W	0x0F	Initial value of servo-loop coefficient (bit[7:0] : +0~+31)	

Register:: L3_INIT_2					0xD4
Name	Bits	R/W	Default	Comments	Config
init_rev2_lane3[2:0]	7:5	R/W	0x0	Reserved	
tap0_init_lane3[4:0]	4:0	R/W	0x0C	Initial value of Tap0 coefficient (bit[4:0] : +0~+31)	

Register:: L3_INIT_3					0xD5
Name	Bits	R/W	Default	Comments	Config
init_rev3_lane3[1:0]	7:6	R/W	0x0	Reserved	
tap1_init_lane3[5:0]	5:0	R/W	0x0C	Initial value of Tap1 coefficient (bit[5:0] : -0~-64)	

Register:: L3_INIT_4					0xD6
Name	Bits	R/W	Default	Comments	Config
init_rev4_lane3[1:0]	7:6	R/W	0x0	Reserved	
tap2_init_lane3[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L3_INIT_5					0xD7
Name	Bits	R/W	Default	Comments	Config
init_rev5_lane3[1:0]	7:6	R/W	0x0	Reserved	

tap3_init_lane3[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	
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Register:: L3_INIT_6 0xD8					
Name	Bits	R/W	Default	Comments	Config
init_rev6_lane3[1:0]	7:6	R/W	0x0	Reserved	
tap4_init_lane3[5:0]	5:0	R/W	0x00	Initial value of Tap2 coefficient {bit[5] : sign-bit(0:+, 1:-), bit[4:0] : 0~31}	

Register:: L3_INIT_7 0xD9					
Name	Bits	R/W	Default	Comments	Config
init_rev7_lane3[3:0]	7:4	R/W	0x0	Reserved	
vth_init_lane3[3:0]	3:0	R/W	0x8	Initial value of V _{th} -adjust coefficient (bit[3:0] : +0~+15)	

Register:: L3_INIT_8 0xDA					
Name	Bits	R/W	Default	Comments	Config
load_in_init_lane3[7:0]	7:0	R/W	0x00	Load-in the initial value from register to adaptation loop (LE, Vth, servo, tap4, tap3, tap2, tap1, tap0)	

Register:: L3_STABLE_FLAG 0xDB					
Name	Bits	R/W	Default	Comments	Config
sf_threshold_lane3[1:0]	7:6	R/W	0x0	The total threshold of stable-flag (00 : 2, 01 : 4, 10 : 6, 11 : 7)	
stable_flag_sel_lane3	5	R/W	0x0	Select the group of stable flag (0 : Vth/Tap0/Tap1/Tap2, 1 : servo/Tap3/LE/Tap4)	
adapt_fail_flag_lane3	4	R	0x0	Fail flag when max-tap0 & min-V _{th}	
stable_flag_lane3[3:0]	3:0	R	0x0	Stable flag	

Register:: L3_COEF_1 0xDB					
Name	Bits	R/W	Default	Comments	Config
coef_sel_lane3[7:0]	7:0	R/W	0x00	Select the coefficients for read-back	

Register:: L3_COEF_2 0xDC					
Name	Bits	R/W	Default	Comments	Config
coef_data_lane3[7:0]	7:0	R	0x00	Read-back the loop coefficients	

Register:: L3_REV_1 0xDD					
Name	Bits	R/W	Default	Comments	Config
servo_overflow_flag_lane3	7	R	0x0	DC servo's coefficient overflow	
servo_underflow_flag_lane3	6	R	0x0	DC servo's coefficient underflow	
rev1_lane3[7:0]	7:0	R/W	0x00	Reserved	

Register:: MODE_TIMER 0xE0					
Name	Bits	R/W	Default	Comments	Config
adapt_mode[1:0]	7:6	R/W	0x2	00 : Edge-based adaptation only with LE loop 01 : Edge-based adaptation only with LE + Tap1 loop 10 : Amplitude-based adaptation with independent LE loop 11 : Amplitude-based adaptation without independent LE loop	
edge_det_mode	5	R/W	0x1	Edge lead or lag data (0 : Edge lead data, 1 : Edge lag data)	
transition_only	4	R/W	0x0	Only transition bit is effective (0 : effective on each bit, 1 : effective on transition bit)	
le_auto_reload	3	R/W	0x0	Enable auto-reload le coefficient when max-tap0 & max-le	

				(0 : disable, 1: enable)	
tap1_delay[2:0]	2:0	R/W	0x0	Delay time of tap1+LE loop after turning on tap0 ([0 1 2 3 4 6 8 12] us @ 27MHz clock)	

Register:: TIMER 0xE1					
Name	Bits	R/W	Default	Comments	Config
tap24_delay[2:0]	7:5	R/W	0x0	Delay time of tap2/3/4 after turning on tap1+LE loop ([0 1 2 4 6 8 12 16] us @ 27MHz clock)	
le_delay[2:0]	4:2	R/W	0x0	Delay time of independent LE loop after turning on tap0, effective only on mode 0/2 ([0 1 2 3 4 6 8 12] us @ 27MHz clock)	
servo_delay[1:0]	1:0	R/W	0x1	Delay time of servo-loop after turning on tap0 ([0 2 4 8] us @ 27MHz clock)	

Register:: GAIN_1 0xE2					
Name	Bits	R/W	Default	Comments	Config
tap0_gain[2:0]	7:5	R/W	0x2	Filter's gain of Tap0 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
tap1_gain[2:0]	4:2	R/W	0x4	Filter's gain of Tap1 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
sf_count[1:0]	1:0	R/W	0x0	Stable flag 累加的點數(00 : 16, 01 : 32, 10 : 64, 11 : 128)	

Register:: GAIN_2 0xE3					
Name	Bits	R/W	Default	Comments	Config
tap2_gain[2:0]	7:5	R/W	0x3	Filter's gain of Tap2 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
tap3_gain[2:0]	4:2	R/W	0x3	Filter's gain of Tap3 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
gain_rev2[1:0]	1:0	R/W	0x0	Reserved	

Register:: GAIN_3 0xE4					
Name	Bits	R/W	Default	Comments	Config
tap4_gain[2:0]	7:5	R/W	0x3	Filter's gain of Tap4 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
servo_gain[2:0]	4:2	R/W	0x3	Filter's gain of servo-loop (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
gain_rev3[1:0]	1:0	R/W	0x0	Reserved	

Register:: GAIN_4 0xE5					
Name	Bits	R/W	Default	Comments	Config
le_gain1[2:0]	7:5	R/W	0x4	Filter's gain of LE1, effective only on mode 0/2 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32)	
le_gain2[2:0]	4:2	R/W	0x1	Filter's gain of LE2, effective only on mode 2 (000 : 1/1024, 001 : 1/512,.....,101 : 1/32, 110 : 0)	
gain_rev4[1:0]	1:0	R/W	0x0	Reserved	

Register:: LIMIT_1 0xE6					
Name	Bits	R/W	Default	Comments	Config
vth_threshold[2:0]	7:5	R/W	0x7	Increase Vth's coefficient when Vth's coefficient less than the vth_threshold and Tap0's coefficient less than tap0_threshold (+0~+7)	
tap0_max[4:0]	4:0	R/W	0x16	Maximum of Tap0 (+0.5 ~ +31.5)	

Register:: LIMIT_2 0xE7					
Name	Bits	R/W	Default	Comments	Config
limit_rev2[1:0]	7:6	R/W	0x0	Reserved	
tap1_min[5:0]	5:0	R/W	0x2E	Minimum of Tap1 (-0.5 ~ -63.5)	

Register:: LIMIT_3 0xE8					
Name	Bits	R/W	Default	Comments	Config
tap2_max[4:0]	7:3	R/W	0x0A	Maximum of Tap2 (+0.5 ~ +31.5)	
tap2_min[4:2]	2:0	R/W	0x6	Minimum of Tap2 (-0.5 ~ -31.5)	

Register:: LIMIT_4 0xE9					
Name	Bits	R/W	Default	Comments	Config
tap2_min[1:0]	7:6	R/W	0x1	Minimum of Tap2 (-0.5 ~ -31.5)	
limit_rev4	5	R/W	0x0	Reserved	
tap3_max[4:0]	4:0	R/W	0x06	Maximum of Tap3 (+0.5 ~ +31.5)	

Register:: LIMIT_5 0xEA					
Name	Bits	R/W	Default	Comments	Config
tap3_min[4:0]	7:3	R/W	0x19	Minimum of Tap3 (-0.5 ~ -31.5)	
tap4_max[4:2]	2:0	R/W	0x1	Maximum of Tap4 (+0.5 ~ +31.5)	

Register:: LIMIT_6 0xEB					
Name	Bits	R/W	Default	Comments	Config
tap4_max[1:0]	7:6	R/W	0x2	Maximum of Tap4 (+0.5 ~ +31.5)	
limit_rev6	5	R/W	0x0	Reserved	
tap4_min[4:0]	4:0	R/W	0x19	Minimum of Tap4 (-0.5 ~ -31.5)	

Register:: LOOP_DIV_1 0xEC					
Name	Bits	R/W	Default	Comments	Config
servo_divisor[5:0]	7:2	R/W	0x28	Servo-loop's divider of symbol clock (2~63)	
vth_divisor[3:2]	1:0	R/W	0x1	V _{th} -adjust's divider of tap clock (1~15)	

Register:: LOOP_DIV_2 0xED					
Name	Bits	R/W	Default	Comments	Config
vth_divisor[1:0]	7:6	R/W	0x1	V _{th} -adjust's divider of tap clock (1~15)	
tap_divisor[5:0]	5:0	R/W	0x0A	Tap-loop's divider of symbol clock (2~63)	

Register:: Reserved 0xEE					
Name	Bits	R/W	Default	Comments	Config
	7:0	R/W	0x00	Reserved	

Register:: RESET_1 0xEF					
Name	Bits	R/W	Default	Comments	Config
tap0_threshold[3:0]	7:4	R/W	0xA	Increase Vth's coefficient when Vth's coefficient less than the vth_threshold and Tap0's coefficient less than tap0_threshold (+0~+15)	
dfe_adapt_rstb_lane3	3	R/W	0x0	Reset adaptation loop of lane3 (0 : reset, 1 : normal)	
dfe_adapt_rstb_lane2	2	R/W	0x0	Reset adaptation loop of lane2 (0 : reset, 1 : normal)	
dfe_adapt_rstb_lane1	1	R/W	0x0	Reset adaptation loop of lane1 (0 : reset, 1 : normal)	
dfe_adapt_rstb_lane0	0	R/W	0x0	Reset adaptation loop of lane0 (0 : reset, 1 : normal)	

Register:: COEF_1 0xF0					
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Name	Bits	R/W	Default	Comments	Config
coef_sel[7:0]	7:0	R/W	0x00	Select the coefficients for read-back	

Register:: COEF_2				0xF1	
Name	Bits	R/W	Default	Comments	Config
coef_data[7:0]	7:0	R	0x00	Read-back the loop coefficients	

Coef_Sel	Coef_data								
	[5:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
000000	VTH_COEF[3:0]								LE1_COEF[3:0]
000001	Rev	Rev	Rev	TAP0_COEF[4:0]					
000010	Rev	Rev	TAP1_COEF[5:0]						
000011	Rev	Rev	TAP2_COEF[5:0]						
Coef_Sel	Coef_data								
[5:0]	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
000000	Rev	Rev	Rev	Rev	VTH_COEF[3:0]				
000001	Rev	Rev	Rev	TAP0_COEF[4:0]					
000010	Rev	Rev	TAP1_COEF[5:0]						
000011	Rev	Rev	TAP2_COEF[5:0]						
000100	Rev	Rev	TAP3_COEF[5:0]						
000101	Rev	Rev	TAP4_COEF[5:0]						
000110	Rev	Rev	Rev	SERVO_COEF[4:0]					

ADC Histogram (Page 1E)

Register::HIST_BON_WIDTH_H 0x1EA0					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
HIST_BON_Width[11:8]	3:0	R/W	0	Horizontal Boundary width : [11:8] The Hist window register is also shared with gray pattern detection	

Register::HIST_BON_WIDTH_L 0x1EA1					
Name	bits	R/W/D	Reset State	Comments	Config
HIST_BON_Width[7:0]	7:0	R/W	0	Horizontal Boundary width : [7:0]	

Register::HIST_BON_HEIGHT_H 0x1EA2					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	R/W	0	Reserved	
HIST_BON_Height[11:8]	3:0	R/W	0	Horizontal Boundary height : [11:8]	

Register::HSIT_BON_HEIGHT_L 0x1EA3					
Name	bits	R/W/D	Reset State	Comments	Config
HIST_BON_Height[7:0]	7:0	R/W	0	Horizontal Boundary height : [7:0]	

Register::HIST_Hor_START_H 0x1EA4					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
HIST_Hor_Start[11:8]	3:0	R/W	0	Histogram Horizontal Start : [11 :8] The Hist window register is also shared with gray pattern detection	

Register::HIST_Hor_START_L 0x1EA5					
Name	bits	R/W/D	Reset State	Comments	Config
HIST_Hor_Start[7:0]	7:0	R/W	0	Histogram Horizontal Start : [7:0]	

Register::HIST_Ver_START_H 0x1EA6					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
HIST_Ver_Start[11:8]	3:0	R/W	0	Histogram Vertical Start : [11 :8]	

Register::HIST_Ver_START_L 0x1EA7					
Name	bits	R/W/D	Reset State	Comments	Config
HIST_Ver_Start[7:0]	7:0	R/W	0	Histogram Vertical Start : [7:0]	

Register::DET_ROW_H 0x1EA8					
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Name	Bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
Detect_Row[11:8]	3:0	R/W	0	Detect Row number :[11 :8] Detect which row to determine if gray level pattern or not	

Register::DET_ROW_L 0x1EA9					
Name	bits	R/W/D	Reset State	Comments	Config
Detect_Row[7:0]	7:0	R/W	0	Detect Row number :[7 :0] Detect which row to determine if gray level pattern or not	

Register::DET_COLUMN_H 0x1EAA					
Name	Bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
Detect_Column[11:8]	3:0	R/W	0	Detect Column number :[11 :8] Detect which column to determine if gray level pattern or not	

Register::DET_COLUMN_L 0x1EAB					
Name	bits	R/W/D	Reset State	Comments	Config
Detect_Column[7:0]	7:0	R/W	0	Detect Column number :[7 :0] Detect which column to determine if gray level pattern or not	

Register::START_HIST_FUNC 0x1EAC					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
Start_Test_Det	3	R/W	0	Start Histogram Func1(b):Test Pattern Detection 0:disable Test Pattern detection (default) 1:start (Hardware auto clear)	
Start_GrayLevel_Det	2	R/W	0	Start Histogram Func1(a):Gray Pattern Detection 0:disable Gray Pattern detection (default) 1:start	
Start_PQ_Jud	1	R/W	0	Start Histogram Func2 :Picture Quality Judgement Start four tones judgement 0 : Picture Quality Judgement finished (default) 1 : start Picture Quality Judgement (Hardware auto clear)	
Colu_Row_assign	0	R/W	0	1 : Detect step/A along the assigned column and row 0 : Detect step/A along the first column and first row of Window (column lose first pixel)	

Register::FUNC1_CTRL1 0x1EAD					
Name	bits	R/W/D	Reset State	Comments	Config
Decide_ifLevel_channel	7:6	R/W	0	ifGray_Level_channel: Which channel is used to decide if the pattern is gray level or not 00: R 01: G 10: B 11: Reserved	
RGB_Delta	5:3	R/W	3	RGB-Delta: Tolerance of the difference between R/G/B per pixel. If the difference of all pixels in window is less or equal to RGB-Delta, then the current frame is considered as gray pattern.	

A_Delta	2:0	R/W	2	A-Delta : Tolerance of each A_Group If both A and Step difference exceed delta at the same time, record the value in new group.	
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Register:: FUNC1_CTRL2					0x1EAE
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7	--		Reserved	
Ref_ifUse_AVG	6	R/W	1	0:Reference value always refers to the first pixel of A 1:Reference value will update to the average of the first four pixels per step	
Step_Delta	5:3	R/W	2	Step-Delta: Tolerance of each Step_Group If both A and Step difference exceed delta at the same time, record the value in new group.	
Step_In_Delta	2:0	R/W	3	Step-inside-Delta: The difference between reference value and current pixel over Step-inside-Delta is considered as next step The reference value is considered as the first pixel of A If bit6=1, the reference value will update to the average of the first four pixel.	

Register:: FUNC1_CTRL3					0x1EAF
Name	bits	R/W/D	Reset State	Comments	Config
Group_Counter THD	7:3	R/W	8	One Counter of Group1,2,3 exceed this THD, GrayLevl Pattern flag=1	
A_min_Value	2:0	R/W	4	A_min_Value Only record the A_value which is greater than this threshold	

Register:: FUNC1_CTRL4					0x1EB0
Name	bits	R/W/D	Reset State	Comments	Config
overRGB_counter	7:0	R/W	0	OverRGB_counter: if RGB variance exceed RGB-delta pixel number over counter, then gray pattern fail	

Register::FUNC1_RESULT1					0x1EB1
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:3	--		Reserved	
Gray_Det_Result	2	R/W/D	0	Gray Pattern Detection Result: 0: is not gray pattern 1: is gray pattern	hw_clr
Mono_Det_Result	1	R	0	Mono pattern Detection Result: Both row and column find A is close to width/height of Window (The difference is within A-Delta) 0: not mono gray pattern 1: is mono gray pattern	
GrayLevel_Det_Result	0	R	0	Gray Level pattern Detection Result: At least one of three A/step Groups Counter over THD 0: not gray level pattern 1 :is gray level pattern	

Register::FUNC1_RESULT2	0x1EB2
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Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:5	--		Reserved	
Window_sft_Dir	4:3	R/W		Direction of the histogram window shift direction: 00: Horizontal and increasing gray code downward ↓ 01: Horizontal and increasing gray code upward ↑ 10: Vertical and increasing gray code to the right → 11: Vertical and increasing gray code to the right ← The histogram window shift according to this direction	
Reserved	2	--		Reserved	
GrayLevel_Dir	1:0	R	0	Direction of the gray level pattern arrangement: 00: Horizontal and increasing gray code downward ↓ 01: Horizontal and increasing gray code upward ↑ 10: Vertical and increasing gray code to the right → 11: Vertical and increasing gray code to the right ← The histogram window shift according to this direction	

Register::MONO_REF_VALUE 0x1EB3					
Name	bits	R/W/D	Reset State	Comments	Config
Mono_Ref_Value	7:0	R		Reference Value (only for Mono Pattern)	

Register::STEP_H 0x1EB4					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:3	--		Reserved	
Step_Group1_Val[8]	2	R		Step_Group1 Value: [8]	
Step_Group2_Val[8]	1	R		Step_Group2 Value: [8]	
Step_Group3_Val[8]	0	R		Step_Group3 Value: [8]	

Register::STEP_1 0x1EB5					
Name	bits	R/W/D	Reset State	Comments	Config
Step_Group1_Val[7:0]	7:0	R		Step_Group1 Value: [7:0]	

Register::STEP_2 0x1EB6					
Name	bits	R/W/D	Reset State	Comments	Config
Step_Group2_Val[7:0]	7:0	R		Step_Group2 Value: [7:0]	

Register::STEP_3 0x1EB7					
Name	bits	R/W/D	Reset State	Comments	Config
Step_Group3_Val[7:0]	7:0	R		Step_Group3 Value: [7:0]	

Register::A_1_H 0x1EB8					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	

A_Group1_Val[11:8]	3:0	R	0	A_Group1 Value[11:8]	
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Register::A_1_L 0x1EB9					
Name	bits	R/W/D	Reset State	Comments	Config
A_Group1_Val[7:0]	7:0	R	0	A_Group1 Value[7:0]	

Register::A_2_H 0x1EBA					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
A_Group2_Val[11:8]	3:0	R		A_Group2 Value[11:8]	

Register::A_2_L 0x1EBB					
Name	bits	R/W/D	Reset State	Comments	Config
A_Group2_Val[7:0]	7:0	R		A_Group2 Value[7:0]	

Register::A_3_H 0x1EBC					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
A_Group3_Val[11:8]	3:0	R		A_Group3 Value[11:8]	

Register::A_3_L 0x1EBD					
Name	bits	R/W/D	Reset State	Comments	Config
A_Group3_Val[7:0]	7:0	R		A_Group3 Value[7:0]	

Register::COUNTER_1 0x1EBE					
Name	bits	R/W/D	Reset State	Comments	Config
Group1_Counter	7:0	R		Number of members in Group1	

Register::COUNTER_2 0x1EBF					
Name	bits	R/W/D	Reset State	Comments	Config
Group2_Counter	7:0	R		Number of members in Group2	

Register::COUNTER_3 0x1EC0					
Name	bits	R/W/D	Reset State	Comments	Config
Group3_Counter	7:0	R		Number of members in Group3	

Register::FUNC2_CTRL1 0x1EC1					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6			Reserved	
Tone_Num_RGB_Sel	5:4	R/W	3	Select which channel return Tone Number : 00:R 01:G 10:B 11:Auto switch R/G/B channel to count PQ 00,01,10 is for test mode.	

				If 00, only count R channel PQ and 0x1EC1~0x1EC8 show R channel result. If 11, the PQ function auto switch R/G/B channel. After finished R/G/B counting, 0x1EAC[1]=0	
Window_Shift_time	3:0	R/W	0	Histogram window shift time	

Register:: FUNC2_CTRL2 0x1EC2					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--		Reserved	,,
Main_Tone_STD[13:8]	5:0	R/W	0	Water level of Histogram Main Tone : [13 :8] The count start from STD number, any tone count over 14bit get one point Ex. Noise < 10% and total window has $127*127=16129$ WaterLevel= $2^{14} - 16129*0.9$	

Register:: FUNC2_CTRL3 0x1EC3					
Name	bits	R/W/D	Reset State	Comments	Config
Main_Tone_STD[7:0]	7:0	R/W	0	Water level of Histogram Main Tone : [7:0] The count start from STD number, any tone count over 14bit get one point	

Register::FUNC2_CTRL4 0x1EC4					
Name	bits	R/W/D	Reset State	Comments	Config
IfUse_Min_Tone_Val	7	R/W	0	If use min tone to count Histogram	
HIST_Min_Tone_Val	6:0	R/W	0	Histogram min tone value The Histogram count the above 4 tones, the min value is only used in Factory mode.	

Register::SHIFT_A_H 0x1EC5					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
Shift_A_Val[11:8]	3:0	R/W	0	Shift A Value[11:8]	

Register::SHIFT_A_L 0x1EC6					
Name	bits	R/W/D	Reset State	Comments	Config
Shift_A_Val[7:0]	7:0	R/W	0	Shift A Value[7:0]	

Register:: TONE1_NUM_H 0x1EC7					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--		Reserved	
TONE1_Num[13:8]	5:0	R		Number of Histogram Tone1 : [13 :8]	

Register:: TONE1_NUM_L 0x1EC8					
Name	bits	R/W/D	Reset State	Comments	Config
TONE1_Num[7:0]	7:0	R		Number of Histogram Tone1 : [7 :0]	

Register:: TONE2_NUM_H 0x1EC9					
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Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--		Reserved	
TONE2_Num[13:8]	5:0	R		Number of Histogram Tone2 : [13 :8]	

Register:: TONE2_NUM_L 0x1ECA					
Name	bits	R/W/D	Reset State	Comments	Config
TONE2_Num[7:0]	7:0	R		Number of Histogram Tone2 : [7 :0]	

Register:: TONE3_NUM_H 0x1ECB					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--		Reserved	
TONE3_Num[13:8]	5:0	R		Number of Histogram Tone3 : [13 :8]	

Register:: TONE3_NUM_L 0x1ECC					
Name	bits	R/W/D	Reset State	Comments	Config
TONE3_Num[7:0]	7:0	R		Number of Histogram Tone3 : [7 :0]	

Register:: TONE4_NUM_H 0x1ECD					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:6	--		Reserved	
TONE4_Num[13:8]	5:0	R		Number of Histogram Tone4 : [13 :8]	

Register:: TONE4_NUM_L 0x1ECE					
Name	bits	R/W/D	Reset State	Comments	Config
TONE4_Num[7:0]	7:0	R		Number of Histogram Tone4 : [7 :0]	

Register::HIST_SCORE1 0x1ECF					
Name	bits	R/W/D	Reset State	Comments	Config
Reserved	7:4	--		Reserved	
HIST_Score_R	3:0	R		The total score of R channel	

Register::HIST_SCORE2 0x1ED0					
Name	bits	R/W/D	Reset State	Comments	Config
HIST_Score_G	7:4	R		The total score of G channel	
HIST_Score_B	3:0	R		The total score of B channel	

Register::RSV_DUMMY_1ECD 0x1ED1					
Name	bits	R/W/D	Reset State	Comments	Config
RSV_DUMMY_1ECD	7:0	--		Reserved to 0	

Register::PWM01_LINE_DELAY_MSB 0xA0					
Name	Bits	R/W	Default	Comments	Config
PWM1_Line_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM0_Line_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register::PWM0_LINE_DELAY_LSB 0xA1					
Name	Bits	R/W	Default	Comments	Config
PWM0_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register::PWM1_LINE_DELAY_LSB 0xA2					
Name	Bits	R/W	Default	Comments	Config
PWM1_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register::PWM23_LINE_DELAY_MSB 0xA3					
Name	Bits	R/W	Default	Comments	Config
PWM3_Line_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM2_Line_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register::PWM2_LINE_DELAY_LSB 0xA4					
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Name	Bits	R/W	Default	Comments	Config
PWM2_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register:::PWM3_LINE_DELAY_LSB				0xA5	
Name	Bits	R/W	Default	Comments	Config
PWM3_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register:::PWM45_LINE_DELAY_MSB				0xA6	
Name	Bits	R/W	Default	Comments	Config
PWM5_Line_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM4_Line_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register:::PWM4_LINE_DELAY_LSB				0xA7	
Name	Bits	R/W	Default	Comments	Config
PWM4_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register:::PWM5_LINE_DELAY_LSB				0xA8	
Name	Bits	R/W	Default	Comments	Config
PWM5_Line_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no line delay 1: delay 1 line 2: delay 2 line ...	

Register:::PWM01_PIXEL_DELAY_MSB				0xA9	
Name	Bits	R/W	Default	Comments	Config
PWM1_Pixel_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM0_Pixel_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register:::PWM0_PIXEL_DELAY_LSB				0xAA	
Name	Bits	R/W	Default	Comments	Config

PWM0_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay 1: delay 1 pixel 2: delay 2 pixel ...	
-----------------------	-----	-----	---	---	--

Register:::PWM1_PIXEL_DELAY_LSB					0xAB
Name	Bits	R/W	Default	Comments	Config
PWM1_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay 1: delay 1 pixel 2: delay 2 pixel ...	

Register:::PWM23_PIXEL_DELAY_MSB					0xAC
Name	Bits	R/W	Default	Comments	Config
PWM3_Pixel_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM2_Pixel_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register:::PWM2_PIXEL_DELAY_LSB					0xAD
Name	Bits	R/W	Default	Comments	Config
PWM2_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay 1: delay 1 pixel 2: delay 2 pixel ...	

Register:::PWM3_PIXEL_DELAY_LSB					0xAE
Name	Bits	R/W	Default	Comments	Config
PWM3_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay 1: delay 1 pixel 2: delay 2 pixel ...	

Register:::PWM45_PIXEL_DELAY_MSB					0xAF
Name	Bits	R/W	Default	Comments	Config
PWM5_Pixel_Delay[11:8]	7:4	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	
PWM4_Pixel_Delay[11:8]	3:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on	

Register:::PWM4_PIXEL_DELAY_LSB					0xB0
Name	Bits	R/W	Default	Comments	Config
PWM4_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay	

				1: delay 1 pixel 2: delay 2 pixel ...	
--	--	--	--	---	--

Register:::PWM5_PIXEL_DELAY_LSB 0xB1				
Name	Bits	R/W	Default	Comments
PWM5_Pixel_Delay[7:0]	7:0	R/W	0	Only effect when VS_RST and CK_SEL_HS are both on 0: no pixel delay 1: delay 1 pixel 2: delay 2 pixel ...

Register:::PWM_SEL_DCLK 0xB2				
Name	Bits	R/W	Default	Comments
PWM_Sel_Dclk_Dummy	7:6	R/W	0	Dummy
PWM5_Sel_Dclk_en	5	R/W	0	PWM5 Select Dclk enable 0: reference 0xFF3A[5] 1: select Dclk as PWM5 input source clk
PWM4_Sel_Dclk_en	4	R/W	0	PWM4 Select Dclk enable 0: reference 0xFF3A[4] 1: select Dclk as PWM4 input source clk
PWM3_Sel_Dclk_en	3	R/W	0	PWM3 Select Dclk enable 0: reference 0xFF3A[3] 1: select Dclk as PWM3 input source clk
PWM2_Sel_Dclk_en	2	R/W	0	PWM2 Select Dclk enable 0: reference 0xFF3A[2] 1: select Dclk as PWM2 input source clk
PWM1_Sel_Dclk_en	1	R/W	0	PWM1 Select Dclk enable 0: reference 0xFF3A[1] 1: select Dclk as PWM1 input source clk
PWM0_Sel_Dclk_en	0	R/W	0	PWM0 Select Dclk enable 0: reference 0xFF3A[0] 1: select Dclk as PWM0 input source clk

Register:::PWM_HS_MASK 0xB3				
Name	Bits	R/W	Default	Comments
PWM_HS_Mask_Dummy	7:6	R/W	0	Dummy
PWM5_HS_MASK_en	5	R/W	0	PWM5 Mask HS Enable 0: Disable 1: Enable (The number of HS masked after VS is PWM5_Line_Delay[11:0])
PWM4_HS_MASK_en	4	R/W	0	PWM4 Mask HS Enable 0: Disable 1: Enable (The number of HS masked after VS is PWM4_Line_Delay[11:0])
PWM3_HS_MASK_en	3	R/W	0	PWM3 Mask HS Enable 0: Disable 1: Enable (The number of HS masked after VS is PWM3_Line_Delay[11:0])
PWM2_HS_MASK_en	2	R/W	0	PWM2 Mask HS Enable 0: Disable

				1: Enable (The number of HS masked after VS is PWM2_Line_Delay[11:0])	
PWM1_HS_MASK_en	1	R/W	0	PWM1 Mask HS Enable 0: Disable 1: Enable (The number of HS masked after VS is PWM1_Line_Delay[11:0])	
PWM0_HS_MASK_en	0	R/W	0	PWM0 Mask HS Enable 0: Disable 1: Enable (The number of HS masked after VS is PWM0_Line_Delay[11:0])	

Embedded OSD

Addressing and Accessing Register

ADDRESS	BIT							
	7	6	5	4	3	2	1	0
High Byte	-	-	-	-	A12	-	-	-
Med Byte	C3	C2	C1	C0	A11	A10	A9	A8
Low Byte	A7	A6	A5	A4	A3	A2	A1	A0

Figure 4. Addressing and Accessing Registers

Date	BIT							
Byte 0	D7	D6	D5	D4	D3	D2	D1	D0
Byte 1	D7	D6	D5	D4	D3	D2	D1	D0
Byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Figure 2. Data Registers

High Byte, Med Byte, and Low Byte means the registers OSD_SCRAMBLE(CR93), OSD_ADDR_MSB(CR90), and OSD_ADDR_LSB(CR91) respectively.

All kind of registers can be controlled and accessed by these 2 bytes, and each address contains 3-byte data, details are described as follows:

Write mode: [A15:A14] select which byte to write

-00: Byte 0 -01:Byte 1 -10: Byte 2 -11: All

*All data are sorted by these three Bytes (Byte0~Byte2)

[A13] Auto Load (Double Buffer)

[A12] Address indicator

-0: Window and frame control registers.

-1: Font Select and font map SRAM

[A12:A0] Address mapping

- Font Select and font map SRAM address: 000~1A9F1ABF 6.67k6.848k*3byte

- Frame control register address: 000~0xx (**Latch**)

- Window control register address: 100~1xx (**Latch**)

* Selection of SRAM address or Latch address selection is determined by A12!

Example:

Bit [15:14]=00

-All data followed are written to byte0 and address increases.

Byte0 → Byte0 → Byte0... (Address will auto increase)

Bit [15:14]=01

-All data followed are written to byte1 and address increases.

Byte1 → Byte1 → Byte1... (Address will auto increase)

Bit [15:14] =11

- Address will be increased after each 3-byte data written.

Byte0 → Byte1 → Byte2 → Byte0 → Byte1 → Byte2... (Address will auto increase)

Window control registers

- Windows all support shadow/border/3D button/3D function
- Window0, 5, 6, 7, 8, 9 support gradient functions.
- Window2, 3, 4 support grid functions
- Window 0, 1, 2, 3, 4, 4-1~4-8, 5, 6, 7, 8, 9 start/end resolution are 1line(pixel)
- All window start and end position include the **special effect (border/shadow/3D button)** been assigned
- Font comes after windows by 10 pixels, so you should compensate 10 pixels on windows to meet font position

Window 0 Shadow/Border/Gradient

Address: 100h

Byte 0

Bit	Mode	Function
7	W	Window 0 shadow color index in 64-color LUT [4]
6	W	Window 0 border color index in 64-color LUT [4]
5:3	W	Window 0 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 0 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 0 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 0 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient

0	W	Enable Blue Color Gradient
---	---	----------------------------

Window 0 start position
Address: 101h

Byte 0

Bit	Mode	Function
7:4	W	Window 0 horizontal start[11:8]
3:0	W	Window 0 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 horizontal start[7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical start [7:0]

Window 0 end position
Address: 102h

Byte 0

Bit	Mode	Function
7:4	W	Window 0 horizontal end [11:8]
3:0	W	Window 0 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 0 vertical end [7:0]

Window 0 control
Address: 103h

Byte 0

Bit	Mode	Function
7	W	Window 0 shadow color index in 64-color LUT [5]
6	W	Window 0 border color index in 64-color LUT [5]
5	W	Window 0 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 150 for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2	W	Window 0 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension:

		0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively
--	--	---

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 0 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 0 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 0 Enable 0: Disable 1: Enable

Window 1 Shadow/Border/Gradient

Address: 104h

Byte 0

Bit	Mode	Function
7	W	Window 1 shadow color index in 64-color LUT [4]
6	W	Window 1 border color index in 64-color LUT [4]
5:3	W	Window 1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 1 shadow/border height in line unit

		000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness
--	--	---

Byte 1

Bit	Mode	Function
7:4	W	Window 1 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 1 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1 start position

Address: 105h

Byte 0

Bit	Mode	Function
7:4	W	Window 1 horizontal start [11:8]
3:0	W	Window 1 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 1 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical start [7:0]

Window 1 end position

Address: 106h

Byte 0

Bit	Mode	Function
7:4	W	Window 1 horizontal end [11:8]
3:0	W	Window 1 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 1 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 1 vertical end [7:0]

Window 1 control

Address: 107h

Byte 0

Bit	Mode	Function
7	W	Window 1 shadow color index in 64-color LUT [5]
6	W	Window 1 border color index in 64-color LUT [5]
5	W	Window 1 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 1 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)

1:0	--	Reserved
-----	----	----------

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 1 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 1 Enable 0: Disable 1: Enable

Window 2 Shadow/Border/Gradient

Address: 108h

Byte 0

Bit	Mode	Function
7	W	Window 2 shadow color index in 64-color LUT [4]
6	W	Window 2 border color index in 64-color LUT [4]
5:3	W	Window 2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 2 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 2 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2 start position
Address: 109h

Byte 0

Bit	Mode	Function
7:4	W	Window 2 horizontal start [11:8]
3:0	W	Window 2 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 2 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical start [7:0]

Window 2 end position
Address: 10Ah

Byte 0

Bit	Mode	Function
7:4	W	Window 2 horizontal end [11:8]
3:0	W	Window 2 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 2 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 2 vertical end [7:0]

Window 2 control
Address: 10Bh

Byte 0

Bit	Mode	Function
7	W	Window 2 shadow color index in 64-color LUT [5]
6	W	Window 2 border color index in 64-color LUT [5]
5	W	Window 2 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 2 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 2 color index in 64-color LUT [4:0]

Byte 2 default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved

4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 2 Enable 0: Disable 1: Enable

Window 3 Shadow/Border/Gradient

Address: 10Ch

Byte 0

Bit	Mode	Function
7	W	Window 3 shadow color index in 64-color LUT [4]
6	W	Window 3 border color index in 64-color LUT [4]
5:3	W	Window 3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 3 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 3 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 3 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3 start position

Address: 10Dh

Byte 0

Bit	Mode	Function
7:4	W	Window 3 horizontal start [11:8]
3:0	W	Window 3 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 3 horizontal start [7:0]

Byte 2

Bit	Mode	Function

7:0	W	Window 3 vertical start [7:0]
-----	---	-------------------------------

Window 3 end position
Address: 10Eh

Byte 0

Bit	Mode	Function
7:4	W	Window 3 horizontal end [11:8]
3:0	W	Window 3 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 3 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 3 vertical end [7:0]

Window 3 control
Address: 10Fh

Byte 0

Bit	Mode	Function
7	W	Window 3 shadow color index in 64-color LUT [5]
6	W	Window 3 border color index in 64-color LUT [5]
5	W	Window 3 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 3 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 3 color index in 64-color LUT [4:0]

Byte 2 default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 3 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved

		111: Border
0	W	Window 3 Enable 0: Disable 1: Enable

Window 4 Shadow/Border/Gradient

Address: 110h

Byte 0

Bit	Mode	Function
7	W	Window 4 shadow color index in 64-color LUT [4]
6	W	Window 4 border color index in 64-color LUT [4]
5:3	W	Window 4 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/ bottom border color
3:0	W	Window 4 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4 start position

Address: 111h

Byte 0

Bit	Mode	Function
7:4	W	Window 4 horizontal start [11:8]
3:0	W	Window 4 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical start [7:0]

Window 4 end position

Address: 112h

Byte 0

Bit	Mode	Function
7:4	W	Window 4 horizontal end [11:8]

3:0	W	Window 4 vertical end [11:8]
-----	---	------------------------------

Byte 1

Bit	Mode	Function
7:0	W	Window 4 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4 vertical end [7:0]

Window 4 control

Address: 113h

Byte 0

Bit	Mode	Function
7	W	Window 4 shadow color index in 64-color LUT [5]
6	W	Window 4 border color index in 64-color LUT [5]
5	W	Window 4 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1:0	--	Reserved

Byte 1

Bit	Mode	Function
7:4	--	Reserved
3:0	W	Window 4 color index in 64-color LUT [3:0]

Byte 2 default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4 Enable 0: Disable 1: Enable

Window 5 Shadow/Border/Gradient

Address: 114h

Byte 0

Bit	Mode	Function
7	W	Window 5 shadow color index in 64-color LUT [4]
6	W	Window 5 border color index in 64-color LUT [4]
5:3	W	Window 5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 5 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 5 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 5 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 5 start position

Address: 115h

Byte 0

Bit	Mode	Function
7:4	W	Window 5 horizontal start [11:8]
3:0	W	Window 5 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical start [7:0]

Window 5 end position

Address: 116h

Byte 0

Bit	Mode	Function
7:4	W	Window 5 horizontal end [11:8]
3:0	W	Window 5 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 5 vertical end [7:0]

Window 5 control

Address: 117h

Byte 0

Bit	Mode	Function
7	W	Window 5 shadow color index in 64-color LUT [5]
6	W	Window 5 border color index in 64-color LUT [5]
5	W	Window 5 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15A for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2	W	Window 5 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension: 0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 5 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function

		0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 5 Enable 0: Disable 1: Enable

Window 6 Shadow/Border/Gradient

Address: 118h

Byte 0

Bit	Mode	Function
7	W	Window 6 shadow color index in 64-color LUT [4]
6	W	Window 6 border color index in 64-color LUT [4]
5:3	W	Window 6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 6 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 6 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/ bottom border color
3:0	W	Window 6 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity

		0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 6 start position
Address: 119h

Byte 0

Bit	Mode	Function
7:4	W	Window 6 horizontal start [11:8]
3:0	W	Window 6 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 6 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical start [7:0]

Window 6 end position
Address: 11Ah

Byte 0

Bit	Mode	Function
7:4	W	Window 6 horizontal end [11:8]
3:0	W	Window 6 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 6 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 6 vertical end [7:0]

Window 6 control
Address: 11Bh

Byte 0

Bit	Mode	Function
7	W	Window 6 shadow color index in 64-color LUT [5]
6	W	Window 6 border color index in 64-color LUT [5]
5	W	Window 6 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15C for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1)

		0: disable 1: enable
2	W	Window 6 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension: 0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 6 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 6 Enable 0: Disable 1: Enable

Window 7 Shadow/Border/Gradient

Address: 11Ch

Byte 0

Bit	Mode	Function
7	W	Window 7 shadow color index in 64-color LUT [4]
6	W	Window 7 border color index in 64-color LUT [4]
5:3	W	Window 7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 7 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 7 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 7 start position
Address: 11Dh

Byte 0

Bit	Mode	Function
7:4	W	Window 7 horizontal start [11:8]
3:0	W	Window 7 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 7 horizontal start [7:0]

Byte 2

Bit	Mode	Function

7:0	W	Window 7 vertical start [7:0]
-----	---	-------------------------------

Window 7 end position
Address: 11Eh

Byte 0

Bit	Mode	Function
7:4	W	Window 7 horizontal end [11:8]
3:0	W	Window 7 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 7 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 7 vertical end [7:0]

Window 7 control
Address: 11Fh

Byte 0

Bit	Mode	Function
7	W	Window 7 shadow color index in 64-color LUT [5]
6	W	Window 7 border color index in 64-color LUT [5]
5	W	Window 7 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 15E for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2	W	Window 7 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension: 0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 7 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
-----	------	----------

7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 7 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 7 Enable 0: Disable 1: Enable

Window 8 Shadow/Border/Gradient

Address: 120h

Byte 0

Bit	Mode	Function
7	W	Window 8 shadow color index in 64-color LUT [4]
6	W	Window 8 border color index in 64-color LUT [4]
5:3	W	Window 8 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 8 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 8 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 8 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity

		0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 8 start position
Address: 121h

Byte 0

Bit	Mode	Function
7:4	W	Window 8 horizontal start [11:8]
3:0	W	Window 8 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 8 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 8 vertical start [7:0]

Window 8 end position
Address: 122h

Byte 0

Bit	Mode	Function
7:4	W	Window 8 horizontal end [11:8]
3:0	W	Window 8 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 8 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 8 vertical end [7:0]

Window 8 control
Address: 123h

Byte 0

Bit	Mode	Function
7	W	Window 8 shadow color index in 64-color LUT [5]
6	W	Window 8 border color index in 64-color LUT [5]
5	W	Window 8 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 160 for saturated color setting)

		0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2	W	Window 8 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension: 0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient
4:0	W	Window 8 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 8 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 8 Enable 0: Disable 1: Enable

Note: Chessboard function and gradient function cannot enable simultaneously

Window 9 Shadow/Border/Gradient

Address: 124h

Byte 0

Bit	Mode	Function
7	W	Window 9 shadow color index in 64-color LUT [4]
6	W	Window 9 border color index in 64-color LUT [4]
5:3	W	Window 9 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 9 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

PS: This is for non-rotary, rotate 270, rotate 90 and 180.

Byte 1

Bit	Mode	Function
7:4	W	Window 9 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 9 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7	W	R Gradient Polarity 0: Decrease 1: Increase
6	W	G Gradient Polarity 0: Decrease 1: Increase
5	W	B Gradient Polarity 0: Decrease 1: Increase
4:3	W	Gradient level 00: 1 step per level 01: Repeat 2 step per level 10: Repeat 3 step per level 11: Repeat 4 step per level
2	W	Enable Red Color Gradient
1	W	Enable Green Color Gradient
0	W	Enable Blue Color Gradient

Window 9 start position

Address: 125h

Byte 0

Bit	Mode	Function
7:4	W	Window 9 horizontal start [11:8]
3:0	W	Window 9 vertical start [11:8]

Byte 1

Bit	Mode	Function

7:0	W	Window 9 horizontal start [7:0]
Byte 2		
Bit	Mode	Function
7:0	W	Window 9 vertical start [7:0]

Window 9 end position
Address: 126h

Byte 0

Bit	Mode	Function
7:4	W	Window 9 horizontal end [11:8]
3:0	W	Window 9 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 9 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 9 vertical end [7:0]

Window 9 control
Address: 127h

Byte 0

Bit	Mode	Function
7	W	Window 9 shadow color index in 64-color LUT [5]
6	W	Window 9 border color index in 64-color LUT [5]
5	W	Window 9 color index in 64-color LUT [5]
4	W	Saturated color mode for gradient (refer to ADDR 162 for saturated color setting) 0: disable 1: enable
3	W	Reversed color mode for gradient (valid while [4] is 1) 0: disable 1: enable
2	W	Window 9 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	--	Reserved
0	W	Gradient level extension: 0: R/G/B channel use the same 8-level 1: R/G/B channel have 256-level respectively

Byte 1

Bit	Mode	Function
7:5	W	111: 7 level per gradient 110: 6 level per gradient 101: 5 level per gradient 100: 4 level per gradient 011: 3 level per gradient 010: 2 level per gradient 001: 1 level per gradient 000: 8 level per gradient

4:0	W	Window 9 color index in 64-color LUT [4:0]
Byte 2		default: 00h
Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6	W	Gradient function 0: Disable 1: Enable
5	W	Gradient direction 0: Horizontal 1: Vertical
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 9 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 9 Enable 0: Disable 1: Enable

Note: Chessboard function and gradient function cannot enable simultaneously

Window 4-1 Shadow/Border/Chessboard

Address: 200h

Byte 0

Bit	Mode	Function
7	W	Window 4-1 shadow color index in 64-color LUT [4]
6	W	Window 4-1 border color index in 64-color LUT [4]
5:3	W	Window 4-1 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-1 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-1 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-1 start position
Address: 201h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-1 horizontal start [11:8]
3:0	W	Window 4-1 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-1 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-1 vertical start [7:0]

Window 4-1 end position
Address: 202h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-1 horizontal end [11:8]
3:0	W	Window 4-1 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-1 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-1 vertical end [7:0]

Window 4-1 control
Address: 203h

Byte 0

Bit	Mode	Function
7	W	Window 4-1 shadow color index in 64-color LUT [5]
6	W	Window 4-1 border color index in 64-color LUT [5]
5	W	Window 4-1 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-1 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-1 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-1 color index in 64-color LUT [4:0]

Byte 2 default: 00h

Bit	Mode	Function
7	W	Blend function

		0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-1 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-1 Enable 0: Disable 1: Enable

Window 4-2 Shadow/Border/Chessboard
Address: 204h

Byte 0

Bit	Mode	Function
7	W	Window 4-2 shadow color index in 64-color LUT [4]
6	W	Window 4-2 border color index in 64-color LUT [4]
5:3	W	Window 4-2 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-2 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-2 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-2 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-2 start position
Address: 205h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-2 horizontal start [11:8]
3:0	W	Window 4-2 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-2 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-2 vertical start [7:0]

Window 4-2 end position
Address: 206h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-2 horizontal end [11:8]
3:0	W	Window 4-2 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-2 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-2 vertical end [7:0]

Window 4-2 control
Address: 207h

Byte 0

Bit	Mode	Function
7	W	Window 4-2 shadow color index in 64-color LUT [5]
6	W	Window 4-2 border color index in 64-color LUT [5]
5	W	Window 4-2 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-2 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-2 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-2 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-2 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4

		100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-2 Enable 0: Disable 1: Enable

Window 4-3 Shadow/Border/Chessboard
Address: 208h

Byte 0

Bit	Mode	Function
7	W	Window 4-3 shadow color index in 64-color LUT [4]
6	W	Window 4-3 border color index in 64-color LUT [4]
5:3	W	Window 4-3 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-3 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-3 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-3 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-3 start position
Address: 209h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-3 horizontal start [11:8]
3:0	W	Window 4-3 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-3 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-3 vertical start [7:0]

Window 4-3 end position
Address: 20Ah

Byte 0

Bit	Mode	Function
7:4	W	Window 4-3 horizontal end [11:8]
3:0	W	Window 4-3 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-3 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-3 vertical end [7:0]

Window 4-3 control
Address: 20Bh

Byte 0

Bit	Mode	Function
7	W	Window 4-3 shadow color index in 64-color LUT [5]
6	W	Window 4-3 border color index in 64-color LUT [5]
5	W	Window 4-3 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-3 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-3 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-3 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-3 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-3 Enable 0: Disable 1: Enable

Window 4-4 Shadow/Border/Chessboard
Address: 20Ch

Byte 0

Bit	Mode	Function
7	W	Window 4-4 shadow color index in 64-color LUT [4]
6	W	Window 4-4 border color index in 64-color LUT [4]
5:3	W	Window 4-4 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-4 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-4 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-4 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-4 start position
Address: 20Dh
Byte 0

Bit	Mode	Function
7:4	W	Window 4-4 horizontal start [11:8]
3:0	W	Window 4-4 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-4 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-4 vertical start [7:0]

Window 4-4 end position
Address: 20Eh
Byte 0

Bit	Mode	Function
7:4	W	Window 4-4 horizontal end [11:8]
3:0	W	Window 4-4 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-4 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-4 vertical end [7:0]

Window 4-4 control
Address: 20Fh

Byte 0

Bit	Mode	Function
7	W	Window 4-4 shadow color index in 64-color LUT [5]
6	W	Window 4-4 border color index in 64-color LUT [5]
5	W	Window 4-4 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-4 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-4 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-4 color index in 64-color LUT [4:0]

Byte 2

Bit	Mode	Function	default: 00h
7	W	Blend function 0: Disable 1: Enable	
6:5	W	Reserved	
4	W	Shadow/Border/3D button 0: Disable 1: Enable	
3:1	W	Window 4-4 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border	
0	W	Window 4-4 Enable 0: Disable 1: Enable	

Window 4-5 Shadow/Border/Chessboard
Address: 210h

Byte 0

Bit	Mode	Function
7	W	Window 4-5 shadow color index in 64-color LUT [4]
6	W	Window 4-5 border color index in 64-color LUT [4]
5:3	W	Window 4-5 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-5 shadow/border height in line unit 000~111: 1 ~ 8 line

		It must be the same as bit [5:3] for 3D button thickness
--	--	--

Byte 1

Bit	Mode	Function
7:4	W	Window 4-5 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-5 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-5 start position
Address: 211h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-5 horizontal start [11:8]
3:0	W	Window 4-5 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-5 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-5 vertical start [7:0]

Window 4-5 end position
Address: 212h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-5 horizontal end [11:8]
3:0	W	Window 4-5 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-5 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-5 vertical end [7:0]

Window 4-5 control
Address: 213h

Byte 0

Bit	Mode	Function
7	W	Window 4-5 shadow color index in 64-color LUT [5]
6	W	Window 4-5 border color index in 64-color LUT [5]
5	W	Window 4-5 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-5 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-5 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-5 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-5 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-5 Enable 0: Disable 1: Enable

Window 4-6 Shadow/Border/Chessboard
Address: 214h

Byte 0

Bit	Mode	Function
7	W	Window 4-6 shadow color index in 64-color LUT [4]
6	W	Window 4-6 border color index in 64-color LUT [4]
5:3	W	Window 4-6 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel

2:0	W	Window 1 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness
-----	---	---

Byte 1

Bit	Mode	Function
7:4	W	Window 4-6 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-6 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-6 start position

Address: 215h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-6 horizontal start [11:8]
3:0	W	Window 4-6 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-6 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-6 vertical start [7:0]

Window 4-6 end position

Address: 216h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-6 horizontal end [11:8]
3:0	W	Window 4-6 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-6 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-6 vertical end [7:0]

Window 4-6 control

Address: 217h

Byte 0

Bit	Mode	Function
7	W	Window 4-6 shadow color index in 64-color LUT [5]
6	W	Window 4-6 border color index in 64-color LUT [5]
5	W	Window 4-6 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-6 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00)

		1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-6 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-6 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-6 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-6 Enable 0: Disable 1: Enable

Window 4-7 Shadow/Border/Chessboard**Address: 218h**

Byte 0

Bit	Mode	Function
7	W	Window 4-7 shadow color index in 64-color LUT [4]
6	W	Window 4-7 border color index in 64-color LUT [4]
5:3	W	Window 4-7 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-7 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-7 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-7 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-7 start position
Address: 219h

Byte 0

Bit	Mode	Function
7:4	W	Window 4-7 horizontal start [11:8]
3:0	W	Window 4-7 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-7 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-7 vertical start [7:0]

Window 4-7 end position
Address: 21Ah

Byte 0

Bit	Mode	Function
7:4	W	Window 4-7 horizontal end [11:8]
3:0	W	Window 4-7 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-7 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-7 vertical end [7:0]

Window 4-7 control
Address: 21Bh

Byte 0

Bit	Mode	Function
7	W	Window 4-7 shadow color index in 64-color LUT [5]
6	W	Window 4-7 border color index in 64-color LUT [5]
5	W	Window 4-7 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-7 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-7 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-7 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-7 Type 000: Shadow Type 1 001: Shadow Type 2 010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-7 Enable 0: Disable 1: Enable

Window 4-8 Shadow/Border/Chessboard
Address: 21Ch

Byte 0

Bit	Mode	Function
7	W	Window 4-8 shadow color index in 64-color LUT [4]
6	W	Window 4-8 border color index in 64-color LUT [4]
5:3	W	Window 4-8 shadow/border width or 3D button thickness in pixel unit 000~111: 1 ~ 8 pixel
2:0	W	Window 4-8 shadow/border height in line unit 000~111: 1 ~ 8 line It must be the same as bit [5:3] for 3D button thickness

Byte 1

Bit	Mode	Function
7:4	W	Window 4-8 shadow color index in 64-color LUT [3:0] For 3D window, it is the left-top/bottom border color
3:0	W	Window 4-8 border color index in 64-color LUT [3:0] For 3D window, it is the right-bottom/top border color

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-8 start position
Address: 21Dh

Byte 0

Bit	Mode	Function
7:4	W	Window 4-8 horizontal start [11:8]
3:0	W	Window 4-8 vertical start [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-8 horizontal start [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-8 vertical start [7:0]

Window 4-8 end position
Address: 21Eh

Byte 0

Bit	Mode	Function
7:4	W	Window 4-8 horizontal end [11:8]
3:0	W	Window 4-8 vertical end [11:8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-8 horizontal end [7:0]

Byte 2

Bit	Mode	Function
7:0	W	Window 4-8 vertical end [7:0]

Window 4-8 control
Address: 21Fh

Byte 0

Bit	Mode	Function
7	W	Window 4-8 shadow color index in 64-color LUT [5]
6	W	Window 4-8 border color index in 64-color LUT [5]
5	W	Window 4-8 color index in 64-color LUT [5]
4:3	--	Reserved
2	W	Window 4-8 reference OSD delay select: 0: reference the first OSD delay values (frame_ctrl_00) 1: reference the second OSD delay values (frame_ctrl_01)
1	W	Window 4-8 Border Priority 0: lower than font 1: higher than font
0	--	Reserved

Byte 1

Bit	Mode	Function
7:5	--	Reserved
4:0	W	Window 4-8 color index in 64-color LUT [4:0]

Byte 2

default: 00h

Bit	Mode	Function
7	W	Blend function 0: Disable 1: Enable
6:5	W	Reserved
4	W	Shadow/Border/3D button 0: Disable 1: Enable
3:1	W	Window 4-8 Type 000: Shadow Type 1 001: Shadow Type 2

		010: Shadow Type3 011: Shadow Type 4 100: 3D Button Type 1 101: 3D Button Type 2 110: Reserved 111: Border
0	W	Window 4-8 Enable 0: Disable 1: Enable

Window Advanced Control**Window 0****Address: 174h**

Byte 0

Bit	Mode	Function
7:0	W	RED gradient level

Byte 1

Bit	Mode	Function
7:0	W	Green gradient level

Byte 2

Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 175h ~ Address 176h are reserved

Address: 177h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 0 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1

Address 17Bh ~ Address 17Dh are reserved

Address: 17Eh

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 1 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2**Address: 182h**

Byte 0

Bit	Mode	Function
7:0	W	Reserved

7:0	W	Reserved
-----	---	----------

Byte 1

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
-----	---	----------

Byte 2

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
-----	---	----------

Address: 183h

Byte 0

Bit	Mode	Function
-----	------	----------

7:6	W	Window 2 grid line width 00~11: 1~4 pixels
-----	---	---

5:0	W	Window 2 grid line color index in 64-colot LUT
-----	---	--

Byte 1

Bit	Mode	Function
-----	------	----------

7	W	Horizontal grid line enable
---	---	-----------------------------

6	W	Vertical grid line enable
---	---	---------------------------

5:0	W	Window 2 grid line offset (unit: pixel)
-----	---	---

Byte 2

Bit	Mode	Function
-----	------	----------

7:0	W	Window 2 grid line pitch [7:0] (unit: um)
-----	---	---

Address: 184h

Byte 0

Bit	Mode	Function
-----	------	----------

7:1	W	Window 2 grid line pitch [14:8]
-----	---	---------------------------------

0	W	Grid function enable
---	---	----------------------

Address: 185h

Byte 0

Bit	Mode	Function
-----	------	----------

7:1	W	Reserved
-----	---	----------

0	W	Window 2 rotation function enable
---	---	-----------------------------------

Byte 1

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
-----	---	----------

Byte 2

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
-----	---	----------

Window 3
Address: 189h

Byte 0

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
-----	---	----------

Byte 1

Bit	Mode	Function
-----	------	----------

7:0	W	Reserved
Byte 2		
Bit	Mode	Function
7:0	W	Reserved

Address: 18Ah

Byte 0

Bit	Mode	Function
7:6	W	Window 3 grid line width 00~11: 1~4 pixels
5:0	W	Window 3 grid line color index in 64-colot LUT

Byte 1

Bit	Mode	Function
7	W	Horizontal grid line enable
6	W	Vertical grid line enable
5:0	W	Window 3 grid line offset (unit: pixel)

Byte 2

Bit	Mode	Function
7:0	W	Window 3 grid line pitch [7:0] (unit: um)

Address: 18Bh

Byte 0

Bit	Mode	Function
7:1	W	Window 3 grid line pitch [14:8]
0	W	Grid function enable

Address: 18Ch

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 3 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4
Address: 190h

Byte 0

Bit	Mode	Function
7:0	W	Reserved

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Address: 191h

Byte 0

Bit	Mode	Function
7:6	W	Window 4 grid line width 00~11: 1~4 pixels
5:0	W	Window 4 grid line color index in 64-color LUT

Byte 1

Bit	Mode	Function
7	W	Horizontal grid line enable
6	W	Vertical grid line enable
5:0	W	Window 4 grid line offset (unit: pixel)

Byte 2

Bit	Mode	Function
7:0	W	Window 4 grid line pitch [7:0] (unit: um)

Address: 192h

Byte 0

Bit	Mode	Function
7:1	W	Window 4 grid line pitch [14:8]
0	W	Grid function enable

Address: 193h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 5
Address: 197h

Byte 0

Bit	Mode	Function
7:0	W	RED gradient level

Byte 1

Bit	Mode	Function
7:0	W	Green gradient level

Byte 2

Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 198h ~ Address 199h are reserved

Address: 19Ah

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 5 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 6
Address: 19Eh

Byte 0

Bit	Mode	Function
7:0	W	RED gradient level

Byte 1

Bit	Mode	Function
7:0	W	Green gradient level

Byte 2

Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 19Fh ~ Address 1A0h are reserved

Address: 1A1h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 6 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 7
Address: 1A5h

Byte 0

Bit	Mode	Function
7:0	W	RED gradient level

Byte 1

Bit	Mode	Function
7:0	W	Green gradient level

Byte 2

Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 1A6h ~ Address 1A7h are reserved

Address: 1A8h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 7 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 8

Address: 1ACh

Byte 0

Bit	Mode	Function
7:0	W	RED gradient level

Byte 1

Bit	Mode	Function
7:0	W	Green gradient level

Byte 2

Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 1ADh ~ Address 1AEh are reserved

Address: 1AFh

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 8 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 9

Address: 1B3h

Byte 0

Bit	Mode	Function
-----	------	----------

7:0	W	RED gradient level
Byte 1		
Bit	Mode	Function
7:0	W	Green gradient level
Byte 2		
Bit	Mode	Function
7:0	W	Blue gradient level

Note: These three bytes are valid only when gradient level extension bit is enabled

Address 1B4h ~ Address 1B5h are reserved

Address: 1B6h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 9 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-1

Address 1BAh ~ Address 1BCh are reserved

Address: 1BDh

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-1 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-2

Address 1C1h ~ Address 1C3h are reserved

Address: 1C4h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-2 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-3

Address 1C8h ~ Address 1CAh are reserved

Address: 1CBh

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-3 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-4

Address 1CFh ~ Address 1D1h are reserved

Address: 1D2h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-4 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-5

Address 1D6h ~ Address 1D8h are reserved

Address: 1D9h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-5 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-6

Address 1DDh ~ Address 1DFh are reserved

Address: 1E0h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-6 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-7

Address 1E4h ~ Address 1E6h are reserved

Address: 1E7h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-7 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-8

Address 1EBh ~ Address 1EDh are reserved

Address: 1EEh

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-8 rotation function enable

Byte 1

Bit	Mode	Function
7:0	W	Reserved

Byte 2

Bit	Mode	Function
7:0	W	Reserved

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Window 3D Control

Window 0

Address: 250h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 0 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 0 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 250h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 1

Address: 254h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 1 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 1 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 254h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 2
Address: 258h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 2 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 2 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 258h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 3
Address: 25Ch

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 3 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 3 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 25Ch Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4
Address: 260h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 260h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 5**Address: 264h**

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 5 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 5 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 264h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 6**Address: 268h**

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 6 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 6 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 268h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 7**Address: 26Ch**

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 7 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Reserved

7:0	W	Window 7 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 26Ch Byte1 is written)
-----	---	---

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 8
Address: 270h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 8 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 8 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 270h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 9
Address: 274h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 9 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 9 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 274h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-1
Address: 278h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-1 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function

7:0	W	Window 4-1 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 278h Byte1 is written)
-----	---	---

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-2
Address: 27Ch

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-2 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-2 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 27Ch Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-3
Address: 280h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-3 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-3 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 280h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-4
Address: 284h

Byte 0

Bit	Mode	Function

7:1	W	Reserved
0	W	Window 4-4 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-4 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 284h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-5
Address: 288h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-5 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-5 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 288h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-6
Address: 28Ch

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-6 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-6 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 28Ch Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-7
Address: 290h

Byte 0

Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-7 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-7 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 290h Byte1 is written)

Byte 2

Bit	Mode	Function
7:0	W	Reserved

Window 4-8
Address: 294h

Byte 0

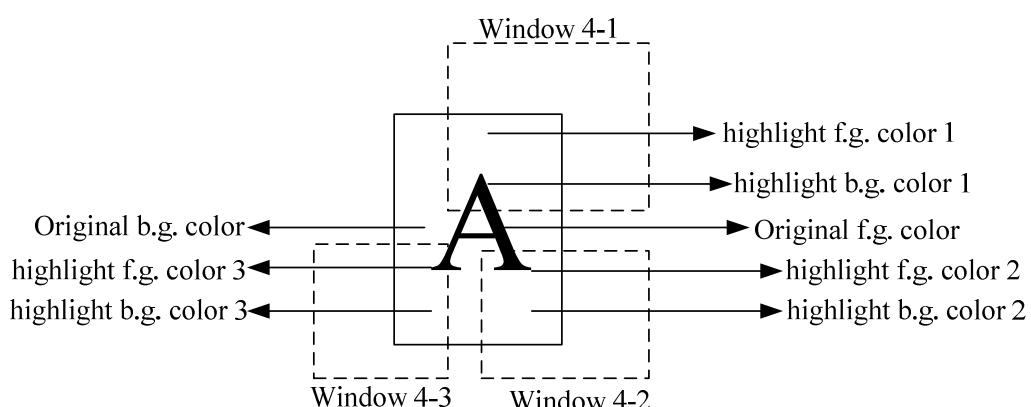
Bit	Mode	Function
7:1	W	Reserved
0	W	Window 4-8 shift value between OSDs of two eyes [8]

Byte 1

Bit	Mode	Function
7:0	W	Window 4-8 shift value between OSDs of two eyes [7:0] The shift value has its own double-buffer (only valid when address 294h Byte1 is written)

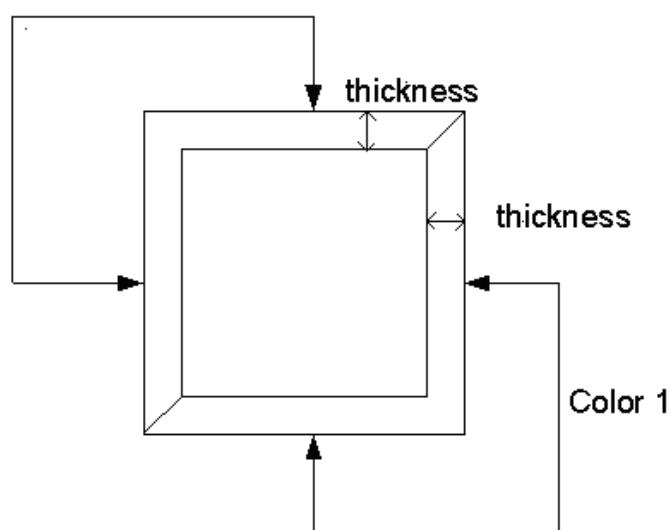
Byte 2

Bit	Mode	Function
7:0	W	Reserved

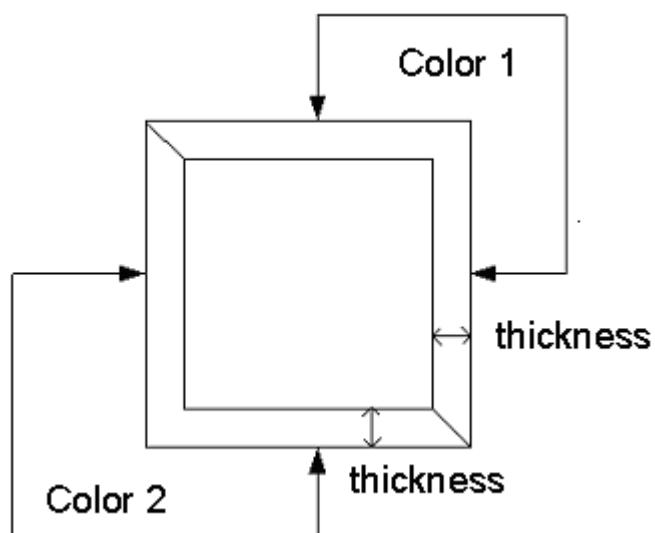


Highlight function of window4-1, window4-2 and window4-3

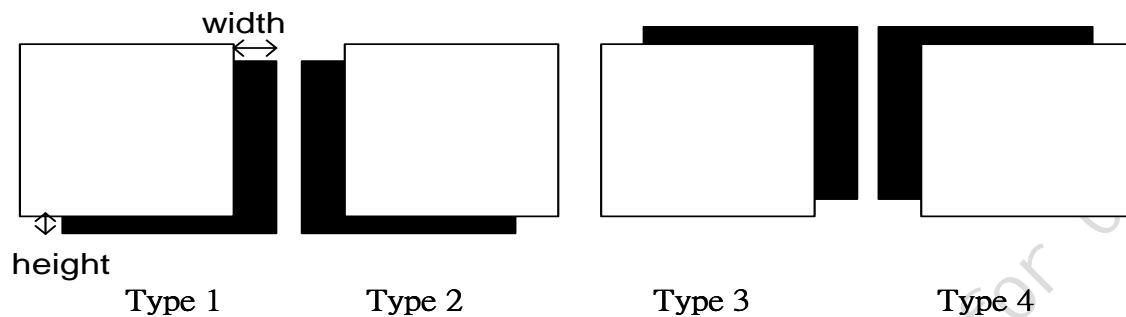
Color 2



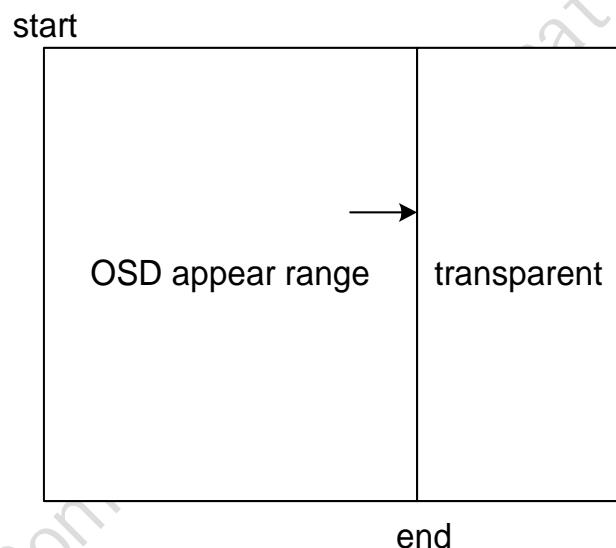
3D Button Type 1



3D Button Type 2



Shadow in all direction



Window mask fade/in out function

Frame control registers

Address: 000h

Byte 0

Bit	Mode	Function
7:0	R/W	First Vertical Delay [10:3] The bits define the vertical starting address. Total 2048 step unit: 1 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	R/W	First Horizontal Delay [9:2] The bits define the horizontal starting address. When address 0x002 bit[0] 0: Total 1024 step unit:4 pixels (minimum should set 2) 1: Total 4096 step unit:1 pixels (minimum should set 8)

Byte 2

default: xxxx_xxx0b

Bit	Mode	Function
7:6	R/W	First Horizontal Delay bit [1:0]
5:3	R/W	First Vertical Delay [2:0]
2:1	R/W	Display zone, for smaller character width 00: middle 01: left 10: right 11: reserved
0	R/W	OSD enable 0: OSD circuit is inactivated 1: OSD circuit is activated

- When OSD is disabled, Double Width (address 0x003 Byte1[1]) must be disabled to save power.
- These three bytes have their own double-buffer (only valid when address 000h Byte2 is written).

Address: 001h

Byte 0

Bit	Mode	Function
7:0	R/W	Second Vertical Delay [10:3] The bits define the vertical starting address. Total 2048 step unit: 1 line

Vertical delay minimum should set 1

Byte 1

Bit	Mode	Function
7:0	R/W	Second Horizontal Delay [9:2] The bits define the horizontal starting address. When address 0x002 bit[0] 0: Total 1024 step unit:4 pixels (minimum should set 2)

		1: Total 4096 step unit:1 pixels (minimumu should set 8) default: xxxx_xxx0b
Byte 2		
Bit	Mode	Function
7:6	R/W	Second Horizontal Delay bit [1:0]
5:3	R/W	Second Vertical Delay [2:0]
2:0	--	reserved

- These three bytes have their own double-buffer (only valid when address 001h Byte2 is written).

Address: 002h

Byte 0		Default: 00h
Bit	Mode	Function
7:5	--	reserved
4	R/W	Horizontal delay step unit 0: 4 pixels (default) 1: 1 pixels
3:2	R/W	First Horizontal Delay bit[11:10] (valid only when address 0x002 bit[4] is 1)
1:0	R/W	Second Horizontal Delay bit[11:10] (valid only when address 0x002 bit[4] is 1)

Byte 1		Default: 00h
Bit	Mode	Function
7:4	--	reserved
3	R/W	win7 mask option 0: mask all windows and fonts 1: mask all transparent fonts
2	R/W	4-bit font background 0: reference 4-bit font byte2 bit[1:0] (default) 1: reference 4-bit font byte0 bit[3:0]
1	R/W	Window 4 priority 0: lower than font 1: higher than font
0	R/W	Window 3 priority 0: lower than font 1: higher than font

Byte 2		Default: 00h
Bit	Mode	Function
7	R/W	Window 2 priority 0: lower than font 1: higher than font
6	R/W	Window 9 priority 0: lower than font 1: higher than font
5	R/W	Window 8 priority 0: lower than font 1: higher than font

4	R/W	blending type 2 match color 0: match blending type 2 color bit[3:0] 1: match blending type 2 color bit[5:0]
3:2	R/W	Blending color from 64-color LUT [5:4] (blending type 2)
1:0	R/W	Char shadow/border color [5:4]

Address: 003h

Bit	Mode	Function	Default: 00h
7	R/W	Specific color blending (blending type 2) 0: Disable 1: Enable	
6:5	R/W	Window 7special function 00: disable 01: blending (blending type 3) 10: window 7 mask region appear 11: window 7 mask region transparent	
4	R/W	OSD vertical start input signal source select 0: Select DVS as OSD VSYNC input 1: Select ENA as OSD VSYNC input	
3:0	R/W	Blending color from 64-color LUT [3:0] (blending type 2)	

Bit	Mode	Function	Default: 00h
7:4	R/W	Char shadow/border color [3:0]	
3:2	R/W	Alpha blending type (blending type 1) 00: Disable alpha blending 01: Only window blending 10: All blending 11: Window and Character background blending	
1	R/W	Double width enable (For all OSD including windows and characters) 0: Normal 1: Double	
0	R/W	Double Height enable (For all OSD including windows and characters) 0: Normal 1: Double	

Total blending area = blending type1 area + blending type 2 area + blending type 3 area

Bit	Mode	Function	Default: 00h
7:6	R/W	Font downloaded swap control 0x: No swap 10: CCW 11: CW	
5	R	Buffer Empty 0: Empty 1: Not Empty	
4	R	Buffer Valid 0: Done 1: Buffer is writing to SDRAM	
3	R/W	Reset Buffer	

		Write 1 to reset and auto-clear after finished.
2	R/W	<p>Hardware Rotation Enable 0: Disable 1: Enable (Default) OSD compression function must be enabled simultaneously.</p>
1	R/W	<p>Global Blinking Enable 0: Disable 1: Enable</p>
0	R/W	<p>Rotation 0: Normal (data latch 24 bit per 24 bit) 1: Rotation (data latch 18 bit per 24 bit)</p>

Bit	7	6	5	4	3	2	1	0
Firmware	A	B	C	D	E	F	G	H
CW	A	E	B	F	C	G	D	H
CCW	E	A	F	B	G	C	H	D

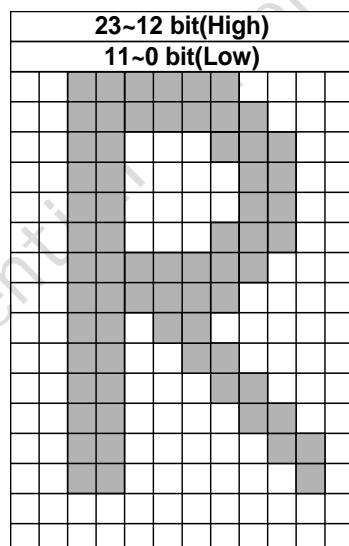
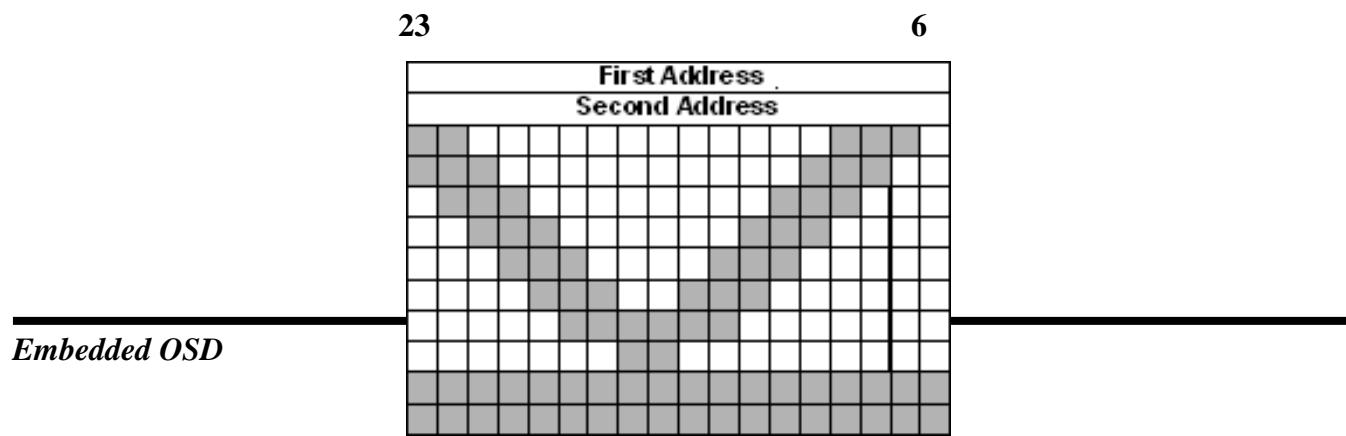


Figure 3 Non-rotated memory alignments



Embedded OSD

Figure 4 Rotated memory alignments**Base address offset****Address: 004h**

Byte 0

Bit	Mode	Function
7:0	R/W	Font Select Base Address[7:0]

Byte 1

Bit	Mode	Function
7:4	R/W	Font Select Base Address[11:8]
3:0	R/W	Font Base Address[3:0]

Byte 2

Bit	Mode	Function
7:0	R/W	Font Base Address[11:4]

When OSD Special Function for POP-ON is enabled (OSD[008]), Font Select Base Address here will not be effective.

OSD Compression**Address: 005h**

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 0
3:0	R/W	4-bit value for VLC code 100

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1010
3:0	R/W	4-bit value for VLC code 1011

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1100
3:0	R/W	4-bit value for VLC code 1101 0

Address: 006h

Byte 0

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1101 1
3:0	R/W	4-bit value for VLC code 1110 0

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1110 10
3:0	R/W	4-bit value for VLC code 1110 11

Byte 2

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 00
3:0	R/W	4-bit value for VLC code 1111 01

Address: 007h

Byte 0

Bit	Mode	Function
7:0	R/W	

7:4	R/W	4-bit value for VLC code 1111 100
3:0	R/W	4-bit value for VLC code 1111 101

Byte 1

Bit	Mode	Function
7:4	R/W	4-bit value for VLC code 1111 110
3:0	R/W	4-bit value for VLC code 1111 1110

Byte 2

default: xxxx_x0000b

Bit	Mode	Function
7:3	--	reserved
2	R/W	Write 3-byte decoded-data into SRAM each time for acceleration 0: disable 1: enable active when compression and hardware rotation function are both enabled.
1	R/W	Decide to decode which kind of data 0: decode compressed data 1: decode non-compressed data
0	R/W	OSD compression (4bit/symbol, VLC code 1111_1111 represents the end of data) (only for SRAM) 0: disable 1: enable

Note:

1. If enable OSD compression or auto load (double buffer), only one byte can be read after writing address at 0x90, 0x91.
2. For OSD compression, MSB 4 bits of original byte is first transferred to corresponding VLC code, and then LSB 4 bits is transferred. VLC code is placed from LSB to MSB of compression font. For example, 4-bit value for VLC code 1100 is 4'b0101, and 4-bit value for VLC code 100 is 4'b0001. Original data 0x15 is transferred to compression x0011001.
3. OSD double buffer and compression can't be enabled simultaneously.
4. When power-down mode or lack of crystal clock, OSD compression font can't be written.
5. After OSD enable, it is better to delay 1 DVS to start writing OSD compression data.
6. While decoding non-compressed data, it is necessary to reset compression function while decode is done.
Because this is the only way to reset compression circuit and ready for next decode job
7. ADDR007 Byte2 bit[2] is designed to accelerate the speed of writing compression/rotation data into SRAM. When the bit is enabled, 3-byte data will be written to SRAM for each cycle and it is supposed to be used while **compression** and **hardware rotation function** are both enabled. Besides, the result of the acceleration will have the best performance while the burst write mode is enabled at the same time. However the burst write setting should be constrained by the two conditions as following:
 - (1) Time of MCU write cycle > 18 x (Tm2pll/2)
 - (2) Time of MCU write cycle > ((4 x (Tm2pll/2) + 9 x TDCLK) x 9) / 7

OSD Special Function

Address: 008h

Byte 0

Default: 0x00

Bit	Mode	Function
7	R/W	OSD Special Function Enable 0: Disable 1: Enable
6	R/W	OSD Special Function Select (Effective only when Bit[7]=1) 0: ROLL-UP 1: POP-ON
5	R/W	OSD Vertical Boundary Function Enable 0: Disable 1: Enable

4	R/W	Reserved to 0
3	R/W	OSD 2 font function 0: disable (row & font select command refer to the FRAM ADDR 004 1: enable (row command of font A refer to the ADDR 008 byte 1 row command of font B refer to the ADDR 008 byte 2 font select command of font A refer to the ADDR 009 FS0 font select command of font B refer to the ADDR 009 FS1)
2	R/W	Font A reference OSD delay select: 0: reference first OSD delay values (frame_ctrl_00) 1: reference second OSD delay values (frame_ctrl_01)
1	R/W	Font B reference OSD delay select: 0: reference first OSD delay values (frame_ctrl_00) 1: reference second OSD delay values (frame_ctrl_01)
0	R/W	Display Base Select (Effective only when Bit[7:6]=11`b) 0: Base 0 1: Base 1

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 0 [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	Row Command Base 1 [7:0]

Address: 009h

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	Font Select Base 0 [11:8]
3:0	R/W	Font Select Base 1 [11:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	Font Select Base 0 [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	Font Select Base 1 [7:0] (Not effective when ROLL-UP)

Address: 00Ah

Byte 0 Default: 0x00

Bit	Mode	Function
7	R/W	Reserved
6:4	R/W	OSD Vertical Upper Boundary [10:8]
3	R/W	Reserved
2:0	R/W	OSD Vertical Lower Boundary [10:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Upper Boundary [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	OSD Vertical Lower Boundary [7:0]

Address: 00Bh

Byte 0 Default: 0x00

Bit	Mode	Function
7	R/W	Font Base Address[12]
6	R/W	Window 6 Special Blending Function 0: OFF 1: ON
5:4	R/W	Blending Type of Window 7 00: NO Blending for both F/B 01: NO Blending for Foreground 10: NO Blending for Background 11: Both Blending for F/B
3:2	R/W	Blending Type of Window 6 00: NO Blending for both F/B 01: NO Blending for Foreground 10: NO Blending for Background 11: Both Blending for F/B
1:0	--	Reserved

Byte 1 Default: 0x00

Bit	Mode	Function
7	R/W	2-bit font char select offset [7]
6:0	R/W	2-bit font char select offset [6:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	--	Reserved

Address: 00Ch

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	FONT A horizontal delay [11:8]
3:0	R/W	FONT A vertical delay [11:8]

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT A horizontal delay [7:0]

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT A vertical delay [7:0]

Address: 00Dh

Byte 0 Default: 0x00

Bit	Mode	Function
7:4	R/W	FONT B horizontal delay [11:8] (valid only while 2 font function enabled)
3:0	R/W	FONT B vertical delay [11:8] (valid only while 2 font function enabled)

Byte 1 Default: 0x00

Bit	Mode	Function
7:0	R/W	FONT B horizontal delay [7:0] (valid only while 2 font function enabled)

Byte 2 Default: 0x00

Bit	Mode	Function
7:0	--	Reserved

7:0	R/W	FONT B vertical delay [7:0] (valid only while 2 font function enabled)
-----	-----	--

Address: 00Eh

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved
6	R/W	Highlight function for window4-1 0: Disable (default) 1: Enable
5:0	R/W	Foreground color1 for highlight

Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color1 for highlight

Note: Background color1[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color1 for highlight

Address: 00Fh

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved
6	R/W	Highlight function for window4-2 0: Disable (default) 1: Enable
5:0	R/W	Foreground color2 for highlight

Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color2 for highlight

Note: Background color2[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color2 for highlight

Address: 010h

Byte 0 default: x0xx_xxxx

Bit	Mode	Function
7	--	Reserved
6	R/W	Highlight function for window4-3 0: Disable (default) 1: Enable

5:0	R/W	Foreground color3 for highlight
-----	-----	---------------------------------

Byte 1

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Background color3for highlight

Note: Background color3[3:0]=4'b0000 is special for transparent

Byte 2

Bit	Mode	Function
7	--	Reserved
6	--	Reserved
5:0	R/W	Character border/shadow color3 for highlight

Note: 1. This highlight function only supports 1-bit font & blank.

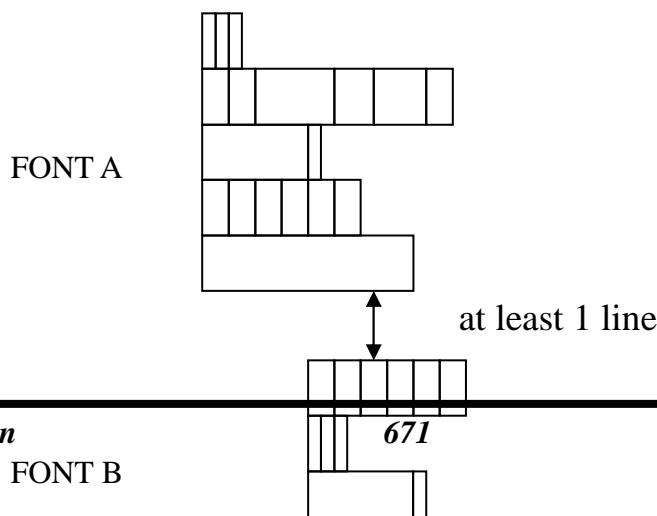
2. If highlight function on, the color of blank will become foreground color.

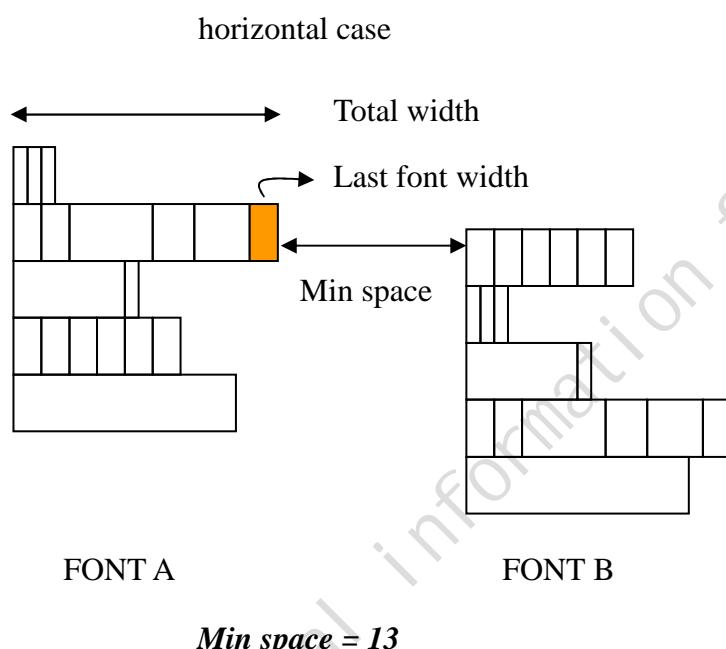
3. The priority of these three windows: window4-3 > window4-2 >window4-1. If these three windows are overlapped, the highlight color of foreground, background and character border/shadow would be only displayed the setting of window4-3.

Note:

1. When OSD Special Function for POP-ON is enabled, Font Select Base Address in OSD[004] will not be effective anymore.
2. When OSD Vertical Boundary Function is enabled, OSD image above upper boundary and below lower boundary will be invisible.
3. When ROLL-UP function is enabled, OSD will always start from the row-command pointed by Base0, and after the row-command pointed by Base1 has been dealt with, the next row-command will be the first one in OSD SRAM. Row-command processing will terminate in the row-command before the one pointed by Base0. (For example, R1 is pointed by Base0, and R5 is pointed by Base1. OSD will show R1 as the first row, followed by R2, R3, R4, R5, and R0 as last row.)
4. When POP-ON function is enabled, OSD will start from the row command pointed by the base selected as display base(selected by OSD[008][0.0]), and terminate when end-command is encountered. That is, all row-command will be separated into two non-overlay subset which is enclosed by the row-command pointed by base and end-command.
5. While 2 font function is enabled (selected by OSD [008][0.3]), FONT A & FONT B can't be overlapped
6. While 2 font function is enabled (selected by OSD [008][0.3]), for vertical case, lines between of FONT A & FONTB must be larger than 1
7. While 2 font function is enabled (selected by OSD [008][0.3]), for horizontal case, pixels between of FONT A & FONT B must follow the rules as following:

Vertical case





Write-Protection Function & Bit Swap Function

Address: 011h

Byte 0

Bit	Mode	Function
7:6	--	Reserved
5	R/W	Blank Command Byte2-Bit[5:4] Enable/Disable 0: Enable 1: Disable
4	R/W	SRAM read function when osd off:

		0: Disable (default) 1: Enable When function is on, need to send 2 times' read command , the 2nd data to be read out is the right value.
3	R/W	2-bit font character command byte0 bit[4]/byte1 bit[7] swap function: 0: Disable (default) 1: Enable 2-bit font character command extend character select: 0: Disable (default) Compatible with RL6086~RL6192 1: Enable Compatible with RL6048/RL6049
2:1	R/W	Byte selection control for write-protection function: 00: byte 0 01: byte 1 10: byte 2 11: reserved
0	R/W	Write-protection function for font SRAM when osd on: 0: Disable (default) 1: Enable

Byte 1

Bit	Mode	Function
7	R/W	Bit[7] write-protection: 0: Disable (default) 1: Enable
6	R/W	Bit[6] write-protection: 0: Disable (default) 1: Enable
5	R/W	Bit[5] write-protection: 0: Disable (default) 1: Enable
4	R/W	Bit[4] write-protection: 0: Disable (default) 1: Enable
3	R/W	Bit[3] write-protection: 0: Disable (default) 1: Enable
2	R/W	Bit[2] write-protection: 0: Disable (default) 1: Enable
1	R/W	Bit[1] write-protection: 0: Disable (default) 1: Enable
0	R/W	Bit[0] write-protection: 0: Disable (default) 1: Enable

Byte 2

Bit	Mode	Function
7:0	--	Reserved

Grid function
Address: 012h

Byte 0

Bit	Mode	Function
7	--	Reserved
6:4	R/W	Horizontal panel pitch[10:8] The interval between pixels (unit: um)
3	--	Reserved
2:0	R/W	Vertical panel pitch[10:8] The interval between pixels (unit: um)

Byte 1

Bit	Mode	Function
7:0	R/W	Horizontal panel pitch[7:0]

Byte 2

Bit	Mode	Function
7:0	R/W	Vertical panel pitch[7:0]

OSD rotation function & 3D function
Address: 013h

Byte 0

Bit	Mode	Function
7:4	R/W	First OSD length [11:8]
3:0	R/W	First OSD width [11:8]

Byte 1

Bit	Mode	Function
7:0	R/W	First OSD length [7:0]

Byte 2

Bit	Mode	Function
7:0	R/W	First OSD width [7:0]

Address: 014h

Byte 0

Bit	Mode	Function
7:4	R/W	Second OSD length [11:8]
3:0	R/W	Second OSD width [11:8]

Byte 1

Bit	Mode	Function
7:0	R/W	Second OSD length [7:0]

Byte 2

Bit	Mode	Function
7:0	R/W	Second OSD width [7:0]

Address: 015h

Byte 0 default: xxxx_xxx0

Bit	Mode	Function
7:0	R/W	row total number

Byte 1 default: xxxx_xxx0

Bit	Mode	Function
-----	------	----------

7:0	R/W	Font A row total number
Byte 2		
Bit	Mode	Function
7:0	R/W	Font B row total number

Address: 016h

Byte 0 default: xxxx_xxx0

Bit	Mode	Function
7:5	R/W	Reserved
4	R/W	OSD auto rotation direction 0: CCW 1: CW
3	R/W	Enable font map library rotation
2	R/W	Enable FONT_A row and character command remapping (valid only when OSD auto rotation function is enabled)
1	R/W	Enable FONT_B row and character command remapping (valid only when OSD auto rotation function is enabled)
0	R/W	OSD auto rotation function

Byte 1 default: xxxx_xxx0

Bit	Mode	Function
7:0	--	Reserved

Byte 2

Bit	Mode	Function
7:0	R/W	Reserved

Address: 017h

Byte 0 default: xxxx_xxx0

Bit	Mode	Function
7:3	--	Reserved
2	R/W	When 3D mode enable: 0: Lframe follows the registers setting, Shift the R frame 1: Rframe follows the registers setting, Shift the L frame
1	R/W	3D output mode: 0: L/R switches by DVS 1: L/R switches by DHS
0	R/W	3D OSD enable

Byte 1 default: xxxx_xxx0

Bit	Mode	Function
7:0	--	Reserved

Byte 2

Bit	Mode	Function
7:0	--	Reserved

When we download the font, we have to set the Frame control 003h byte2 [7:6]

] to set the method of hardware bit swap. If the OSD is Counter-Clock-Wise rotated, we have to set to 0x01 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “7 5 3 1 6 4 2 0” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). If it is Clock-Wise rotated, we have to set to 0x10 (the 8 bits of every byte of font SRAM downloaded by firmware will be in a sequence of “6 4 2 0 7 5 3 1” (from MSB to LSB) and should be rearranged to “7 6 5 4 3 2 1 0” by hardware). After we finish the downloading or if we don't have to rotate the OSD, we have to set it to 0x00.

Row Command

Byte 0

Bit	Mode	Function
7	W	1: Row Start Command 0: OSD End Command Each row must start with row-command, last word of OSD map must be end-command
6	R/W	VBI OSD function enable (not valid while rotation enabled) 0: normal OSD function as usual 1: support VBI OSD functions like underline, B/F separated blink and 512 fonts select
5	W	1-bit font selection 0: font select from 0-511 1: font select from 512-1023
4:2	W	Character border/shadow 000: None 001: Border 100: Shadow (left-top) 101: Shadow (left-bottom) 110: Shadow (right-top) 111: Shadow (right-bottom)
1	W	Double character width 0: x1 1: x2
0	W	Double character height 0: x1 1: x2

Byte 1

Bit	Mode	Function
7:3	W	Row height (1~32)
2:0	W	Column space 0~7 pixel column space When Char is doubled, so is column space.

Notice:

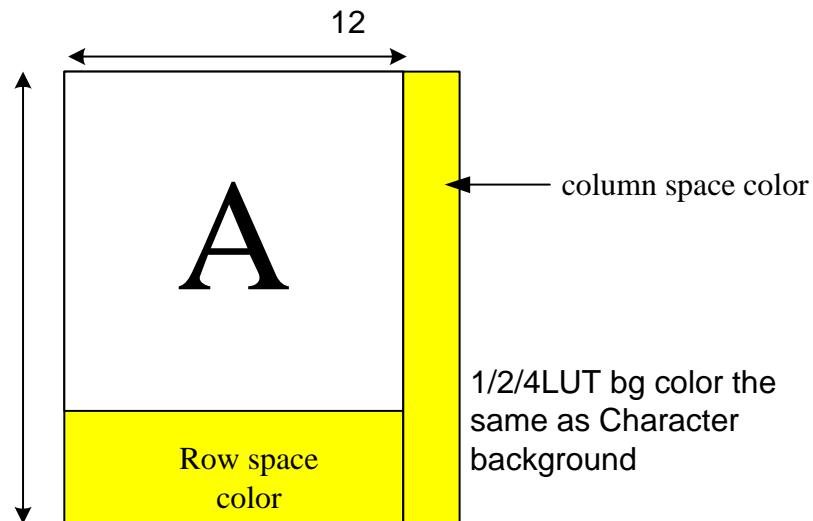
When character height/width is doubled, the row height/column space definition also twice. If the row height is larger than character height, the effect is just like space between rows. If it is smaller than character height, it will drop last several bottom line of character.

When using 1/2/4LUT font, column space and font smaller than row height, the color of column space and row space is the same as font background color, ~~only 4 bit true color font mode, the color is transparent~~

Byte 2

Bit	Mode	Function

7:0	W	Row length	unit: font base
-----	---	------------	-----------------



Character Command (For blank)

Byte 0

Bit	Mode	Function
7	W	0
6	W	Blinking effect 0: Disable 1: Enable
5:4	W	01
3:2	W	reserved
1:0	W	Blank font types 00: blank font 01: align 10: 3D mark 11: reserved

Byte 1

Bit	Mode	Function
7:0	W	When byte0-bit[1:0] is 00: Blank pixel length (at least 3 pixels, and can't exceed 255 pixels) 01: reserved 10: font shift value between two eyes (only valid in 3D mode) 11: reserved

Byte 2

Bit	Mode	Function
7:6	W	Reserved
5:4	W	Blank color – select one of 64-color LUT [5:4]
3:0	W	Blank color – select one of 64-color LUT [3:0] (0 is special for transparent)

Character Command (For 1-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	Use combined with [5:4]
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	<p>{[7], [5:4]}</p> <p>(Font type 000: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 0-255 When Row command Byte 0[5] is 1 Font select from 512-767 Color palette from 16-31 001: Blank 010: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 256-511 When Row command Byte 0[5] is 1 Font select from 768-1023 Color palette from 0-15 011: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 256-511 When Row command Byte 0[5] is 1 Font select from 768-1023 Color palette from 16-31 100: 1-bit RAM Font When Row command Byte 0[5] is 0 Font select from 0-255 When Row command Byte 0[5] is 1 Font select from 512-767 Color palette from 0-15 101: 4-bit RAM Font Font select from 0-255 Color palette from 0-63 110: 2-bit RAM Font Font select from 0-254 (with Frame Ctrl register 00B byte1 [6:0]) Color palette from 0-15 111: 2-bit RAM Font Font select from 0-254 (with Frame Ctrl register 00B byte1 [6:0]) Color palette from 16-31)</p>
	W	VBI OSD disable: Character width (only for 1-pixel font, doubled when specifying double-width in Row/Blank command register) For 12x18 font:

		0100: 4-pixel 0101: 5-pixel 0110: 6-pixel 0111: 7-pixel 1000: 8-pixel 1001: 9-pixel 1010: 10-pixel 1011: 11-pixel 1100: 12-pixel For 18x12 Font (rotated) 0000: 4-pixel 0001: 5-pixel 0010: 6-pixel 0011: 7-pixel 0100: 8-pixel 0101: 9-pixel 0110: 10-pixel 0111: 11-pixel 1000: 12-pixel 1001: 13-pixel 1010: 14-pixel 1011: 15-pixel 1100: 16-pixel 1101: 17-pixel 1110: 18-pixel 1111: 36-pixel VBI OSD enable: While VBI OSD enable, 1 bit font will be NO rotated and 12-pixel fonts always. Then the [3:0] setting will be as following: [3]: character select[8] support 512 font while VBI OSD enable [2]: additional blinking effect {[6], [2]} 00: NO blink for both F/B 01: Only blink for Foreground 10: Only blink for Background 11: Both blink for F/B [1]: Underline enable underline will be at 17th & 18th line and got the same color with foreground [0]: Reserved
--	--	---

When using border/shadow/ effect, the width of the 1-bit font should at least 6 pixel.

Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

Byte 2

Bit	Mode	Function
7:4	W	Foreground color Select one of 16-color from color LUT
3:0	W	Background color Select one of 16-color from color LUT (0 is special for transparent)

Character command (For 2-bit RAM Font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	MSB of Foreground color 11, Background 00
5	W	1
4	W	When 2-bit font extend character select (frame control 0x011h byte0 bit[3]) is disabled (default): 0: color palette 0-15 1: color palette 16-31

		When 2-bit font extend character select (frame control 0x011h byte0 bit[3]) is enabled: MSB of Foreground color 10, Foreground 01
3:1	W	Foreground color 11 Select one of 8 color from color LUT Add Byte0 [6] as MSB for 16-color LUT.
0	W	Background color 00 Bit[2] Select one of 8 color from color LUT

Byte 1

Bit	Mode	Function
7	W	When 2-bit font extend character select (frame control 0x011h byte0 bit[3]) is disabled (default): MSB of Foreground color 10, Foreground 01 When 2-bit font extend character select (frame control 0x011h byte0 bit[3]) is enabled: Character Select [7]
6:0	W	Character Select [6:0]

Byte 2

Bit	Mode	Function
7:6	W	Background color 00 Bit[1:0] Select one of 8 color from color LUT While 0 is special for transparent Add Byte0 [6] as MSB for 16-color LUT. Once we fill 0000 or 1000(MSB follow Byte0[6]), BG appears transparent.
5:3	W	Foreground color 10 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.
2:0	W	Foreground color 01 Select one of 8 color from color LUT Add Byte0 [4] as MSB for 16-color LUT.

Character command (For 4-bit RAM font)

Byte 0

Bit	Mode	Function
7	W	1
6	W	Character Blinking effect 0: Disable 1: Enable
5:4	W	01 (Font type 00: 1-bit RAM Font 01: 4-bit RAM Font 1x: 2-bit RAM Font)
3:0	W	(for Byte1[7]=0) select one color from 16-color LUT as background When address 002h byte1[2] is 0: When byte0[3:0] =0000 means transparent When byte0[3:0]!=0000, byte2[1:0] determine the color

		1: byte0[3:0] determine the color
--	--	-----------------------------------

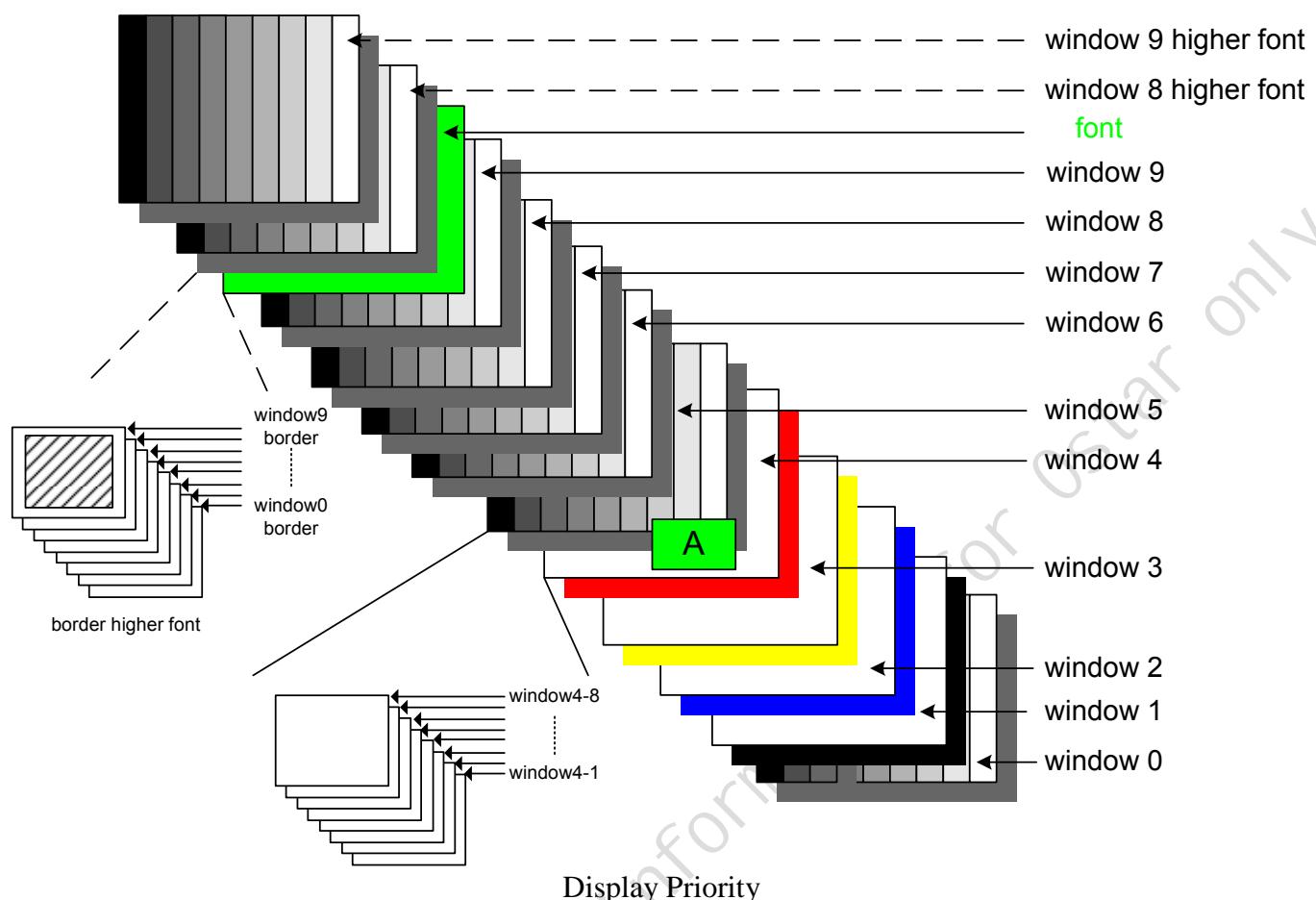
Byte 1

Bit	Mode	Function
7:0	W	Character Select [7:0]

- When 4-bit look-up table mode , color of column space is the same as background.
- When 4-bit look-up table mode and pixel value is 0000, and byte0[3:0]=0000 means transparent.
- ~~When true color mode and pixel value is 0000 , it is transparent~~

Byte 2

Bit	Mode	Function
7:6	W	Color select 12 13 14 15 00: color select 12 13 14 15 01: color select 28 29 30 31 10: color select 44 45 46 47 11: color select 60 61 62 63
5:4	W	Color select 8 9 10 11 00: color select 8 9 10 11 01: color select 24 25 26 27 10: color select 40 41 42 43 11: color select 56 57 58 59
3:2	W	Color select 4 5 6 7 00: color select 4 5 6 7 01: color select 20 21 22 23 10: color select 36 37 38 39 11: color select 52 53 54 55
1:0	W	Color select 0 1 2 3 00: color select 0 1 2 3 01: color select 16 17 18 19 10: color select 32 33 34 35 11: color select 48 49 50 51 When address 002h byte1[2] is 0: byte2[1:0] determine the background color (color select 0) 1: byte0[3:0] determine the background color (color select 0)

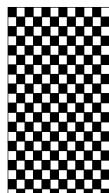


We have six windows with gradient and twelve windows without gradient, the window priority is as above, character should be always on the top layer of the window.

Pattern gen.

Use OSD to replace display pattern generator.

Chess Board: make a font as below



If we want to fill to the full 1280x1024 screen with character, we need 1280*1024 pixels. Required character is:

Using 12*18 font

$$1280/12 = 106.7 \rightarrow 107$$

$$1024/18 = 56.9 \rightarrow 57$$

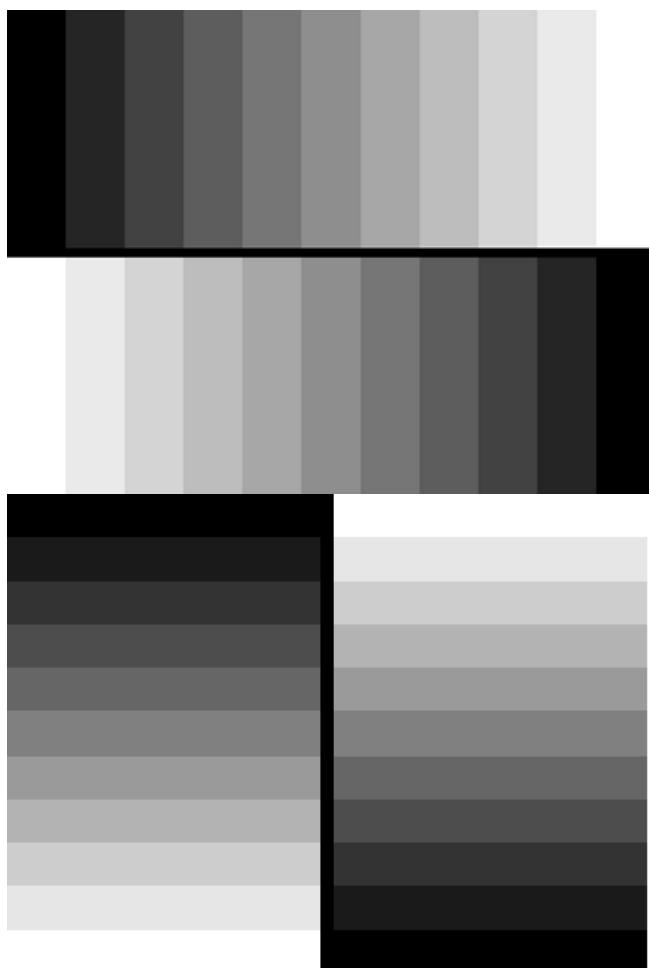
$$107*57 = 6099 \text{ character}$$

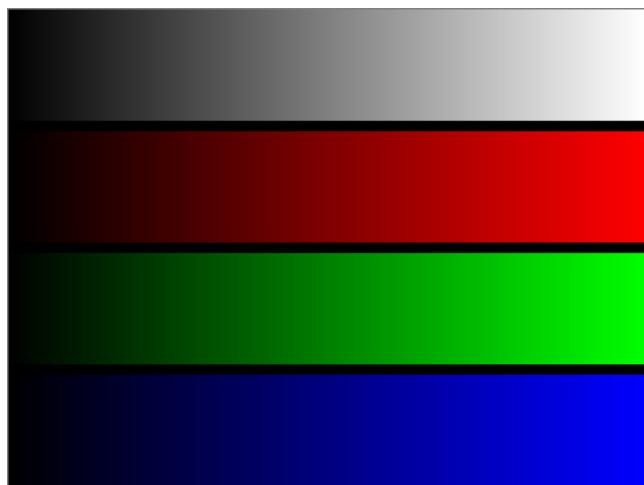
The required number of character map is larger than RAM size. We must turn on double width or double height function to reduce the half of character map.

So the basic unit to chessboard is 2x2 pixel. You can use larger chessboard instead of 2x2 pixels unit, such as 4x4 and so on.

Gray level

We can display 256 gray level by gradient window, 8 and 16 gray level by character map. 32 and 64 gray level is not supported.





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6. Electric Specification

DC Characteristics

Table 1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerant)	V _{IN}	-1		5	V
Supply Voltage	PVCC	3.14	3.3	3.47	V
	VCCK	1.14	1.2	1.26	V
Electrostatic Discharge	V _{ESD}			±2.5	kV
Latch-Up	I _{LA}			±100	mA
Ambient Operating Temperature	T _A	0		70	°C
Storage temperature (plastic)	T _{STG}	-55		125	°C
Thermal Resistance (Junction to case thermal resistance)	θ _{JC}			10	°C/W
Thermal Resistance (Junction to Air)	θ _{JA}			32	°C/W
Junction Acceptable Temperature	T _j			125	°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset pulse period	Trst-en ¹	1120			ns
Power on reset period	Tpor-rst ²	146.5			ms

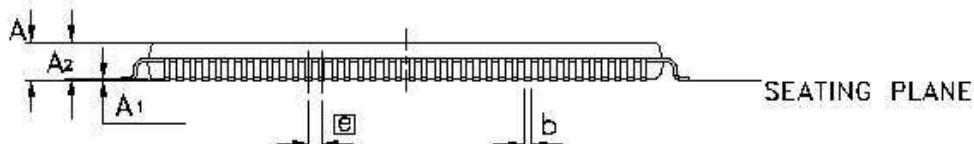
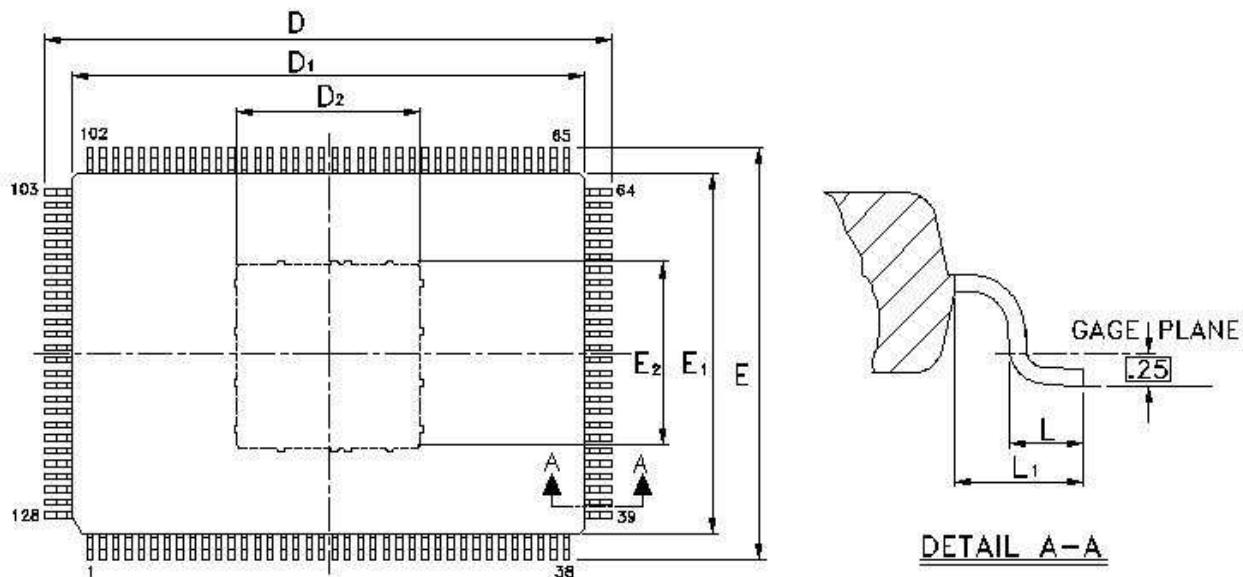
1. 16 * x'tal_cycle(1/14.3Mhz)

2. 65536*32*Xtal_cycle(1/14.3Mhz)

7. Mechanical Specification

128 Pin Package (LQFP)

Thermal Enhance Low Profile Plastic Quad Flat Package 128 Leads 14x20mm² Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A ₁	0.05	—	0.15	0.002	—	0.006
A ₂	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D	22.00BSC			0.866BSC		
D ₁	20.00BSC			0.787BSC		
E	16.00BSC			0.630BSC		
E ₁	14.00BSC			0.551BSC		
D ₂ /E ₂	6.48	6.73	6.98	0.255	0.265	0.275
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MS-26.