

HAO CHEN

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RESEARCH INTERESTS

Electronic Design Automation, Physical Design, Logic Synthesis, Formal Methods, Combinatorial Optimization.

EDUCATION

- | | |
|-------------------|---|
| 08/2019 – Present | The University of Texas at Austin , Austin, TX
Ph.D. Student in Electrical and Computer Engineering (GPA: 4.0/4.0)
Advisor: Dr. David Z. Pan |
| 09/2014 – 01/2019 | National Taiwan University (NTU) , Tapei, Taiwan
B.S.E. in Electrical Engineering (GPA: 3.75/4.0) |

WORK EXPERIENCE

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|-------------------|---|
| 07/2017 – 08/2017 | IC Compiler - RDL Routing Team, Synopsys Inc. , Taipei, Taiwan
R&D Intern (Mentor: Kai-Shun Hu) <ul style="list-style-type: none">– Proposed and implemented an algorithm on <i>Routing Pattern Optimization Improvement</i>; up to 93% of bend count reduction is achieved. The algorithm has been merged into the product code base.– Proposed an algorithm on X-architecture Steiner-tree construction. |
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RESEARCH EXPERIENCE

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| 08/2019 – Present | UT Design Automation Laboratory (UTDA) , UT ECE, Austin, TX
Graduate Research Assistant (Advisor: Dr. David Z. Pan) <ul style="list-style-type: none">– Researched on the Machine Generated Analog IC Layout System (MAGICAL) project of the DARPA IDEA Program, mainly responsible for the routing engine. [J2, C5, C4]– Research on matching constraint extraction for analog circuits with machine learning. [C8]– Taped-out an ADC with state-of-the-art performance under TSMC 40nm technology with fully automatically generated layout. [C7] |
| 09/2017 – 01/2019 | Applied Logic and Computation Laboratory , NTU EE, Taipei, Taiwan
Research Assistant (Advisor: Dr. Jie-Hong R. Jiang) <ul style="list-style-type: none">– Researched on <i>Threshold Logic Synthesis and Optimization</i> for modern circuit design.– Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks. [C3] |
| 02/2017 – 01/2019 | Electronic Design Automation Laboratory , NTU EE, Taipei, Taiwan
Research Assistant (Advisor: Dr. Yao-Wen Chang) <ul style="list-style-type: none">– Proposed an algorithm on Obstacle-Aware On-Track Bus Routing based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours. [J1, C2]– Designed an algorithm on Initial Detailed Routing; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest. [C1] |

PUBLICATIONS

Journal Articles

- [J3] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Nan Sun, and David Z. Pan, “[Challenges and Opportunities Toward Fully Automated Analog Layout Design](#),” in *Journal of Semiconductors (JoS)*, 2020. (* equal contribution) (Invited, **featured on cover**)
- [J2] **Hao Chen***, Mingjie Liu*, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan, “[MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII](#),” in *IEEE Design and Test (D&T)*, 2020. (* equal contribution) (Invited)
- [J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

Conference Papers

- [C8] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks,” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, Jul. 11–15, 2021. (accepted)
- [C7] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun, and David Z. Pan, “MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s $\Delta\Sigma$ ADC,” in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, USA, Apr. 25–28, 2021. (* equal contribution) (accepted)
- [C6] Keren Zhu, Mingjie Liu, **Hao Chen**, Zheng Zhao, and David Z. Pan, “[Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network](#),” in *Proc. ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, Nov. 16–20, 2020.
- [C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “[Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020.
- [C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “[Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020. (**Best Paper Award Nomination from track**)
- [C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, “[Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.
- [C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.
- [C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, “[A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5–8, 2018.

HONORS & AWARDS

2019–2021	Cockrell School of Engineering Fellowship , The University of Texas at Austin.
2018–2019	Outstanding Performance Scholarship , National Taiwan University.
2018	3rd Place , IEEE/ACM ICCAD CAD Contest - Problem A.
2018	Top 10 , IEEE/ACM ICCAD CAD Contest - Problem B.
2018	3rd Place , ACM ISPD Initial Detailed Routing Contest.

SKILLS

Programming:	C/C++, Java, Python, Verilog, \LaTeX , Linux System
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys Hspice, Synopsys PrimeTime
Deep Learning Toolkits:	Pytorch, Tensorflow, Keras

PROFESSIONAL SERVICES

Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD’20)
- ACM/IEEE Design Automation Conference (DAC’21)