Hao Chen

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Research Interests

Electronic Design Automation, Physical Design, Logic Synthesis, Formal Methods, Automated Reasoning, Combinatorial Optimization.

Education

08/2019 – Present
The University of Texas at Austin, Austin, TX
Ph.D. in Electrical and Computer Engineering (GPA: 4.0/4.0)
Advisor: Prof. David Z. Pan

09/2014 – 01/2019
National Taiwan University (NTU), Taipei, Taiwan
B.S.E. in Electrical Engineering (GPA: 3.75/4.0)

Experience

05/2021 – Present
NVIDIA Corp. (Design Automation Research Group), Austin, TX
Research Intern (Manager: Dr. Mark H. Ren)

- Developed an automatic layout flow with novel place-and-route algorithms for analog/mixed-signal circuits under TSMC 5nm technology. [C13]
- Proposed placement algorithms with comprehensive analog-specific constraints supported using satisfiability modulo theories (SMT) and matching-aware routing methods. [C12]

08/2019 – Present
UT Design Automation Laboratory (UTDA), UT ECE, Austin, TX
Graduate Research Assistant (Advisor: Prof. David Z. Pan)

- Researched on the **Machine Generated Analog IC Layout System (MAGICAL)** project of the DARPA IDEA Program, mainly responsible for the routing engine. [J4, J2, C5, C4]
- Research on matching constraint extraction for analog circuits with machine learning. [C8]
- Taped-out chips with state-of-the-art performance under TSMC 40nm technology with fully automatically generated layout. [C9, C7]

09/2017 – 01/2019
Applied Logic and Computation Laboratory, NTU EE, Taipei, Taiwan
Research Assistant (Advisor: Prof. Jie-Hong R. Jiang)

- Researched on *Threshold Logic Synthesis and Optimization* for modern circuit design.
- Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks. [C3]

02/2017 – 01/2019
Electronic Design Automation Laboratory, NTU EE, Taipei, Taiwan
Research Assistant (Advisor: Prof. Yao-Wen Chang)

- Proposed an algorithm on **Obstacle-Aware On-Track Bus Routing** based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours. [J1, C2]
- Designed an algorithm on **Initial Detailed Routing**; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest. [C1]

07/2017 – 08/2017
Synopsys Inc. (IC Compiler II - RDL Routing Team), Taipei, Taiwan
Research Intern (Manager: Kai-Shun Hu)

- Proposed and implemented an algorithm on *Routing Pattern Optimization Improvement*; up to 93% of bend count reduction is achieved. The algorithm has been merged into the product code base.
- Proposed an algorithm on X-architecture Steiner-tree construction.

Honors & Awards

2022–2023	**NVIDIA Graduate Fellowship**, NVIDIA Corporation.
2019–2023	**Cockrell School of Engineering Graduate Fellowship**, The University of Texas at Austin.
2019	**2019 Outstanding Performance Scholarship**, National Taiwan University.
2018	**2018 Outstanding Performance Scholarship**, National Taiwan University.
2018	**3rd Place, 2018 CAD Contest- Problem A**, IEEE/ACM ICCAD.
2018	**Top 10, 2018 CAD Contest- Problem B**, IEEE/ACM ICCAD.
2018	**3rd Place, 2018 Initial Detailed Routing Contest**, ACM ISPD.

Publications

Journal Articles

[J4] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, "Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System," in *IEEE Trans. Circuit and Systems II (TCAS-II)*, 2022. (* equal contribution) **(Invited)**

[J3] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Nan Sun, and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," in *Journal of Semiconductors (JoS)*, 2020. (* equal contribution) **(Invited, featured on cover)**

[J2] **Hao Chen***, Mingjie Liu*, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," in *IEEE Design and Test (D&T)*, 2020. (* equal contribution) **(Invited)**

[J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

Conference Papers

[C13] **Hao Chen**, Walker J. Turner, Sanquan Song, Keren Zhu, George F. Kokai, Brian Zimmer, C. Thomas Gray, Brucek Khailany, David Z. Pan, and Haoxing Ren, "AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies," in *Proc. ACM International Conference on Physical Design (ISPD)*, Virtual Event, Canada, Mar. 27–30, 2022. **(Invited)**

[C12] **Hao Chen**, Walker J. Turner, David Z. Pan, and Haoxing Ren, "Routability-Aware Placement for Advanced FinFET Mixed-Signal Circuits using Satisfiability Modulo Theories," in *Proc. IEEE/ACM Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, Mar. 14–23, 2022.

[C11] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, "Automating Analog Constraint Extraction: From Heuristics to Learning," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022. **(Invited)**

[C10] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, "Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022.

[C9] Mingjie Liu, Xiyuan Tang, Keren Zhu, **Hao Chen**, Nan Sun, and David Z. Pan, "OpenSAR: An Open Source Automated End-to-end SAR ADC Compiler," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 01–04, 2021.

[C8] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, Jul. 11–15, 2021.

[C7] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun, and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s $\Delta\Sigma$ ADC," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, USA, Apr. 25–28, 2021. (* equal contribution)

[C6] Keren Zhu, Mingjie Liu, **Hao Chen**, Zheng Zhao, and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," in *Proc. ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, Nov. 16–20, 2020.

[C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020.

[C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020. (**Best Paper Award Nomination from Track**)

[C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, "Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.

[C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.

[C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, "A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5–8, 2018.

Skills

Programming:	C++, C, Java, Python, Tcl, Verilog, LaTeX, Linux System
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys IC Compiler II
Deep Learning Toolkits:	Pytorch, Tensorflow, Keras

Related Courses

- EE382M: VLSI Physical Design Automation — Prof. David Z. Pan
- EE382M: VLSI CAD and Optimization — Prof. David Z. Pan
- EE382M: VLSI I — Prof. Jacob A. Abraham
- EE382M: Verification of Digital Systems — Prof. Jacob A. Abraham
- EE382M: Analog Integrated Circuit Design — Prof. Nan Sun
- EE381V: Combinatorial Optimization — Prof. Constantine Caramanis
- EE381V: Unconventional Computation — Prof. David Soloveichik
- ECE382N: High-Speed Computer Arithmetic I — Prof. Earl E. Swartzlander
- CS389L: Automated Logical Reasoning — Prof. Isil Dillig

Professional Services

Reviewer/Second Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD'20, 21, 22)
- ACM/IEEE Design Automation Conference (DAC'21, 22)