HAO CHEN

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Research Interests

- VLSI Computer-Aided Design, Physical Design, Logic Synthesis, Design for Manufacturing/Reliability, Computational Models, Combinatorial Optimization.

Education

- **The University of Texas at Austin** *Austin, TX*
  Ph.D. student, Department of Electrical and Computer Engineering *Aug. 2019 - Present*
  - **Advisor**: Prof. David Z. Pan
- **National Taiwan University** *Taipei, Taiwan*
  B.S., Department of Electrical Engineering *Sep. 2014 - Jan. 2019*
  - **GPA**: Overall - 3.76/4.0; Major - 3.85/4.0; Last 2 Years - 3.95/4.0.
  - **Coursework**: Physical Design for Nanometer ICs*, Logic Synthesis and Verification*, Convex Optimization*, Machine Learning*, Operating System*, Algorithms (*graduate-level courses).

Work Experience

- **The UT Design Automation Laboratory (UTDA)** *Austin, TX*
  Research Assistant (Advisor: Prof. David Z. Pan) *Aug. 2019 - Present*
  - Researched on the **DARPA Machine Generated Analog IC Layout System (MAGICAL)** project.
- **Applied Logic and Computation Laboratory** *Taipei, Taiwan*
  Undergraduate Research Assistant (Advisor: Prof. Jie-Hong R. Jiang) *Sep. 2017 - Jan. 2019*
  - Researched **Threshold Logic Synthesis and Optimization** for modern circuit design.
  - Proposed a brand-new data structure for efficient threshold logic function representation.
  - Designed a threshold logic network optimization algorithm that minimized the interconnections in the network; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks.
- **Electronic Design Automation Laboratory** *Taipei, Taiwan*
  Undergraduate Research Assistant (Advisor: Prof. Yao-Wen Chang) *Feb. 2017 - Jan. 2019*
  - Focused on placement and routing optimization problems and techniques for advanced VLSI Design.
  - Proposed an algorithm on **Obstacle-Aware On-Track Bus Routing** based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours.
  - Designed an algorithm on **Initial Detailed Routing**; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest.
- **Synopsys Inc.** *Taipei, Taiwan*
  R&D Intern, RDL Group, IC Compiler team *Jul. 2017 - Aug. 2017*
  - Invited to give a presentation on algorithms at 2017 Synopsys Shanghai InnoDay based on my outstanding internship performance.
  - Proposed and implemented an algorithm on **Routing Pattern Optimization Improvement**; up to 93% of bend count reduction is achieved.
  - Proposed and implemented an algorithm on **Obstacle-Avoiding X-architecture Steiner Tree Construction**.

Publications

Conference Papers

[C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, "Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis," in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *Proc. of ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, "A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides," in *Proc. of IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5-8, 2018.

Honors & Awards

- 2019 **Cockrell School of Engineering Fellowship**, The University of Texas at Austin.
- 2018 **Outstanding Performance Scholarship**, National Taiwan University.
- 2018 **3rd Place**, IEEE/ACM ICCAD CAD Contest - Problem A.
- 2018 **Top 10**, IEEE/ACM ICCAD CAD Contest - Problem B.
- 2018 **3rd Place**, ACM ISPD Initial Detailed Routing Contest.

Skills

- **Programming**: C/C++, Python, Java, LaTeX, Linux System.
- **EDA**: Cadence Innovus.
- **Languages**: Mandarin (native), Taiwanese (native), English (fluent).

Selected Projects

- **ThreABC**: A system for threshold logic synthesis and optimization integrated on Berkeley ABC. *Sep. 2018*
  - Supplied transformation between threshold logic network and AIG network.
  - Provided a fast threshold logic optimizing operation to reduce the interconnects of threshold networks.
- **LuLuBus**: A multithreaded topology-matching on-track bus router considering DRC constraints. *Sep. 2018*
  - Performed bus routing with topology constraints on complex track configuration.
  - Produced routing results with few design rule violations.
- **LuLuEC**: A smart name mapping program for VLSI design written in python. *Aug. 2018*
  - Won the top-3 award in 2018 ICCAD CAD Contest - Problem A.
- **LuLuRoute**: A multithreaded detailed router considering several industrial DRC constraints. *Mar. 2018*
  - Outperformed the top-3 routers in 2018 ISPD Contest.
  - Supported the standard LEF/DEF file format used in industry.
  - Enabled multithread routing for runtime improvement.
- **ABC-1Sub**: A 1-input resubstitution finder implemented in Berkeley ABC system. *Dec. 2017*
  - Wrote a procedure in ABC to find for each gate in a circuit all 1-input resubstitution candidates.
- **XSteiner**: A fast multi-layer X-architecture Steiner tree router with obstacle awareness. *Jun. 2017*
  - Supported multi-layer Steiner tree construction avoiding octagonal obstacles.
  - Constructed Steiner trees with 45 and 135 degree routing segments for further wirelength minimization.
- **F-Legalizer**: A fast standard cell placement legalizer handling several design constraints. *May. 2017*
  - Generated high-quality legalization results efficiently using the Abacus dynamic programming algorithm.
- **B*-FP**: A circuit floorplanner based on B*-Tree and fast-SA algorithm. *Apr. 2017*
  - Generated floorplan results with fixed-outline constraint.
  - Provided circuit visualization through GNU plot.
- **FM-Partition**: A circuit partitioner based on FM algorithm. *Mar. 2017*
- **FRAIG**: A AIG logic network optimization framework using SAT solver. *Jan. 2016*