

# HAO CHEN

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## RESEARCH INTERESTS

Design Automation for Analog Circuits, VLSI Physical Design, Logic Synthesis, Formal Methods, Combinatorial Optimization.

## EDUCATION

08/2019 – Present	<p>Ph.D. Student in Electrical and Computer Engineering <b>The University of Texas at Austin</b>, Austin, TX Advisor: Dr. David Z. Pan</p> <ul style="list-style-type: none"><li>– Courses: VLSI Physical Design Automation, Verification of Digital System, VLSI I, Analog IC Design.</li></ul>
09/2014 – 01/2019	<p>B.S.E. in Electrical Engineering <b>National Taiwan University (NTU)</b>, Tapei, Taiwan</p> <ul style="list-style-type: none"><li>– Courses: Physical Design for Nanometer ICs<sup>†</sup>, Logic Synthesis and Verification<sup>†</sup>, Convex Optimization<sup>†</sup>, Machine Learning<sup>†</sup>, Operating System<sup>†</sup>, Algorithms (<sup>†</sup> graduate-level courses).</li></ul>

## WORK EXPERIENCE

07/2017 – 08/2017	<p><b>IC Compiler - RDL Routing Team, Synopsys Inc.</b>, Taipei, Taiwan R&amp;D Intern (Mentor: Kai-Shun Hu)</p> <ul style="list-style-type: none"><li>– Proposed and implemented an algorithm on <i>Routing Pattern Optimization Improvement</i>; up to 93% of bend count reduction is achieved.</li></ul>
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## RESEARCH EXPERIENCE

08/2019 – Present	<p><b>UT Design Automation Laboratory (UTDA)</b>, UT ECE, Austin, TX Graduate Research Assistant (Advisor: Dr. David Z. Pan)</p> <ul style="list-style-type: none"><li>– Researched on the <b>Machine Generated Analog IC Layout System (MAGICAL)</b> project of the DARPA IDEA Program, mainly responsible for the routing engine.</li></ul>
09/2017 – 01/2019	<p><b>Applied Logic and Computation Laboratory</b>, NTU EE, Taipei, Taiwan Undergraduate Research Assistant (Advisor: Dr. Jie-Hong R. Jiang)</p> <ul style="list-style-type: none"><li>– Researched on <i>Threshold Logic Synthesis and Optimization</i> for modern circuit design.</li><li>– Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks.</li></ul>
02/2017 – 01/2019	<p><b>Electronic Design Automation Laboratory</b>, NTU EE, Taipei, Taiwan Undergraduate Research Assistant (Advisor: Dr. Yao-Wen Chang)</p> <ul style="list-style-type: none"><li>– Proposed an algorithm on <b>Obstacle-Aware On-Track Bus Routing</b> based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours.</li><li>– Designed an algorithm on <b>Initial Detailed Routing</b>; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest.</li></ul>

## PUBLICATIONS

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### Journal Articles

- [J3] **Hao Chen\***, Mingjie Liu\*, Keren Zhu\*, Xiyuan Tang\*, Nan Sun, and David Z. Pan, “Challenges and Opportunities Toward Fully Automated Analog Layout Design”, in *Journal of Semiconductors (JoS)*, 2020. (\* alphabetical order)
- [J2] **Hao Chen\***, Mingjie Liu\*, Biying Xu\*, Keren Zhu\*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan, “MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII”, in *IEEE Design and Test (D&T)*, 2020. (\* alphabetical order)
- [J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

### Conference Papers

- [C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits”, in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020.
- [C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow”, in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020.
- [C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, “[Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.
- [C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.
- [C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, “[A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5-8, 2018.

## HONORS & AWARDS

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2019	<b>Cockrell School of Engineering Fellowship</b> , The University of Texas at Austin.
2019, 2018	<b>Outstanding Performance Scholarship</b> , National Taiwan University.
2018	<b>3<sup>rd</sup> Place</b> , IEEE/ACM ICCAD CAD Contest - Problem A.
2018	<b>Top 10</b> , IEEE/ACM ICCAD CAD Contest - Problem B.
2018	<b>3<sup>rd</sup> Place</b> , ACM ISPD Initial Detailed Routing Contest.

## SKILLS

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Programming:	C/C++, Python, Java, Verilog, $\text{\LaTeX}$ , Linux System.
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys Hspice, Synopsys PrimeTime.
Languages:	Mandarin (native), Taiwanese (native), English (fluent).