

# HAO CHEN

📍 2501 Speedway, EER 4.852, Austin, TX, 78712

☎ +1 (360) 712-5252 ✉ haoc@utexas.edu 🏠 baloneymath.github.io 🔗 linkedin.com/in/hao9chen

## RESEARCH INTERESTS

Electronic Design Automation, Physical Design, Automated Reasoning, Machine Learning and Reinforcement Learning for EDA.

## EDUCATION

- |                      |   |
|----------------------|---|
| 08/2019 –<br>12/2023 | <b>The University of Texas at Austin</b> , Austin, TX<br>Ph.D. in Electrical and Computer Engineering (GPA: 4.0/4.0)<br>Advisor: Prof. David Z. Pan |
| 09/2014 –<br>01/2019 | <b>National Taiwan University (NTU)</b> , Tapei, Taiwan<br>B.S.E. in Electrical Engineering (GPA: 3.75/4.0)   |

## EXPERIENCE

- |                      |  |
|----------------------|--|
| 05/2021 –<br>Present | <b>NVIDIA Corp. (Design Automation Research Group)</b> , Austin, TX<br>Research Intern (Manager: Dr. Mark H. Ren) <ul style="list-style-type: none"><li>- Developed an automatic layout flow with novel place-and-route algorithms for analog/mixed-signal circuits under TSMC 5nm technology. [C13]</li><li>- Proposed placement algorithms with comprehensive analog-specific constraints supported using satisfiability modulo theories (SMT) and matching-aware routing methods. [C12]</li><li>- Reinforcement learning assisted detailed routing for full custom circuits.</li></ul>  |
| 08/2019 –<br>Present | <b>UT Design Automation Laboratory (UTDA)</b> , UT ECE, Austin, TX<br>Graduate Research Assistant (Advisor: Prof. David Z. Pan) <ul style="list-style-type: none"><li>- Researched on the <b>Machine Generated Analog IC Layout System (MAGICAL)</b> project of the DARPA IDEA Program, mainly responsible for the routing engine. [J4, J2, C5, C4]</li><li>- Research on matching constraint extraction for analog circuits with machine learning. [C8]</li><li>- Taped-out chips with state-of-the-art performance under TSMC 40nm technology with fully automatically generated layout. [C9, C7]</li></ul>                      |
| 09/2017 –<br>01/2019 | <b>Applied Logic and Computation Laboratory</b> , NTU EE, Taipei, Taiwan<br>Research Assistant (Advisor: Prof. Jie-Hong R. Jiang) <ul style="list-style-type: none"><li>- Researched on <i>Threshold Logic Synthesis and Optimization</i> for modern circuit design.</li><li>- Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks. [C3]</li></ul>  |
| 02/2017 –<br>01/2019 | <b>Electronic Design Automation Laboratory</b> , NTU EE, Taipei, Taiwan<br>Research Assistant (Advisor: Prof. Yao-Wen Chang) <ul style="list-style-type: none"><li>- Proposed an algorithm on <b>Obstacle-Aware On-Track Bus Routing</b> based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours. [J1, C2]</li><li>- Designed an algorithm on <b>Initial Detailed Routing</b>; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest. [C1]</li></ul> |
| 07/2017 –<br>08/2017 | <b>Synopsys Inc. (IC Compiler II - RDL Routing Team)</b> , Taipei, Taiwan<br>Research Intern (Manager: Kai-Shun Hu) <ul style="list-style-type: none"><li>- Proposed and implemented an algorithm on <i>Routing Pattern Optimization Improvement</i>; up to 93% of bend count reduction is achieved. The algorithm has been merged into the product code base.</li><li>- Proposed an algorithm on X-architecture Steiner-tree construction.</li></ul>  |

## HONORS & AWARDS

---

2022–2023	<b>NVIDIA Graduate Fellowship</b> , NVIDIA Corporation.
2019–2023	<b>Cockrell School of Engineering Graduate Fellowship</b> , The University of Texas at Austin.
2019	<b>2019 Outstanding Performance Scholarship</b> , National Taiwan University.
2018	<b>2018 Outstanding Performance Scholarship</b> , National Taiwan University.
2018	<b>3<sup>rd</sup> Place, 2018 CAD Contest- Problem A</b> , IEEE/ACM ICCAD.
2018	<b>Top 10, 2018 CAD Contest- Problem B</b> , IEEE/ACM ICCAD.
2018	<b>3<sup>rd</sup> Place, 2018 Initial Detailed Routing Contest</b> , ACM ISPD.

## PUBLICATIONS

---

### Journal Articles

- [J4] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, “Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System,” in *IEEE Trans. Circuit and Systems II (TCAS-II)*, 2022. (\* equal contribution) (Invited)
- [J3] **Hao Chen\***, Mingjie Liu\*, Xiyuan Tang\*, Keren Zhu\*, Nan Sun, and David Z. Pan, “[Challenges and Opportunities Toward Fully Automated Analog Layout Design](#),” in *Journal of Semiconductors (JoS)*, 2020. (\* equal contribution) (Invited, featured on cover)
- [J2] **Hao Chen\***, Mingjie Liu\*, Biying Xu\*, Keren Zhu\*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan, “[MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII](#),” in *IEEE Design and Test (D&T)*, 2020. (\* equal contribution) (Invited)
- [J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

### Conference Papers

- [C14] Keren Zhu, **Hao Chen**, Walker J. Turner, George F. Kokai, Po-Hsuan Wei, David Z. Pan, and Haoxing Ren, “TAG: Learning Circuit Spatial Embedding From Layouts,” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Oct. 30–Nov. 3, 2022. (accepted)
- [C13] **Hao Chen**, Walker J. Turner, Sanquan Song, Keren Zhu, George F. Kokai, Brian Zimmer, C. Thomas Gray, Brucek Khailany, David Z. Pan, and Haoxing Ren, “[AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies](#),” in *Proc. ACM International Conference on Physical Design (ISPD)*, Virtual Event, Canada, Mar. 27–30, 2022. (Invited)
- [C12] **Hao Chen**, Walker J. Turner, David Z. Pan, and Haoxing Ren, “Routability-Aware Placement for Advanced FinFET Mixed-Signal Circuits using Satisfiability Modulo Theories,” in *Proc. IEEE/ACM Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, Mar. 14–23, 2022.
- [C11] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, “[Automating Analog Constraint Extraction: From Heuristics to Learning](#),” in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022. (Invited)
- [C10] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, “[Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits](#),” in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022.
- [C9] Mingjie Liu, Xiyuan Tang, Keren Zhu, **Hao Chen**, Nan Sun, and David Z. Pan, “[OpenSAR: An Open Source Automated End-to-end SAR ADC Compiler](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 01–04, 2021.
- [C8] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “[Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, Jul. 11–15, 2021.
- [C7] **Hao Chen\***, Mingjie Liu\*, Xiyuan Tang\*, Keren Zhu\*, Abhishek Mukherjee, Nan Sun, and David Z. Pan, “[MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s  \$\Delta\Sigma\$  ADC](#),” in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, USA, Apr. 25–28, 2021. (\* equal contribution)
- [C6] Keren Zhu, Mingjie Liu, **Hao Chen**, Zheng Zhao, and David Z. Pan, “[Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network](#),” in *Proc. ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, Nov. 16–20, 2020.

- [C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “[Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020.
- [C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “[Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020. (**Best Paper Award Nomination from Track**)
- [C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, “[Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.
- [C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.
- [C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, “[A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5–8, 2018.

## SKILLS

---

Programming:	C++, C, Python, Java, Tcl, Verilog, Git
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys IC Compiler II
Deep Learning Toolkits:	PyTorch, Tensorflow
Optimization Toolkits:	JAX, OR-Tools (CP-SAT), Z3 (SMT), Gurobi (MILP)
Languages:	Mandarin (native), Taiwanese (native), English (full professional).

## RELATED COURSES

---

• EE382M: VLSI Physical Design Automation	Prof. David Z. Pan
• EE382M: VLSI CAD and Optimization	Prof. David Z. Pan
• EE382M: VLSI I	Prof. Jacob A. Abraham
• EE382M: Verification of Digital Systems	Prof. Jacob A. Abraham
• EE382M: Analog Integrated Circuit Design	Prof. Nan Sun
• EE381V: Combinatorial Optimization	Prof. Constantine Caramanis
• EE381V: Unconventional Computation	Prof. David Soloveichik
• ECE382N: High-Speed Computer Arithmetic I	Prof. Earl E. Swartzlander
• CS389L: Automated Logical Reasoning	Prof. Isil Dillig

## PROFESSIONAL SERVICES

---

### Reviewer/Secondary Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD’20, 21, 22)
- ACM/IEEE Design Automation Conference (DAC’21, 22)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD’22)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS’22)