

HAO CHEN

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RESEARCH INTERESTS

Design Automation for Analog Circuits, VLSI Physical Design, Logic Synthesis, Formal Methods, Combinatorial Optimization.

EDUCATION

08/2019 – Present	The University of Texas at Austin , Austin, TX Ph.D. Student in Electrical and Computer Engineering Advisor: Dr. David Z. Pan <ul style="list-style-type: none">– Courses: VLSI Physical Design Automation, Verification of Digital System, VLSI I, Analog IC Design.
09/2014 – 01/2019	National Taiwan University (NTU) , Tapei, Taiwan B.S.E. in Electrical Engineering <ul style="list-style-type: none">– Courses: Physical Design for Nanometer ICs[†], Logic Synthesis and Verification[†], Convex Optimization[†], Machine Learning[†], Operating System[†], Algorithms ([†] graduate-level courses).

WORK EXPERIENCE

07/2017 – 08/2017	IC Compiler - RDL Routing Team, Synopsys Inc. , Taipei, Taiwan R&D Intern (Mentor: Kai-Shun Hu) <ul style="list-style-type: none">– Proposed and implemented an algorithm on <i>Routing Pattern Optimization Improvement</i>; up to 93% of bend count reduction is achieved.
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RESEARCH EXPERIENCE

08/2019 – Present	UT Design Automation Laboratory (UTDA) , UT ECE, Austin, TX Graduate Research Assistant (Advisor: Dr. David Z. Pan) <ul style="list-style-type: none">– Researched on the Machine Generated Analog IC Layout System (MAGICAL) project of the DARPA IDEA Program, mainly responsible for the routing engine.
09/2017 – 01/2019	Applied Logic and Computation Laboratory , NTU EE, Taipei, Taiwan Undergraduate Research Assistant (Advisor: Dr. Jie-Hong R. Jiang) <ul style="list-style-type: none">– Researched on <i>Threshold Logic Synthesis and Optimization</i> for modern circuit design.– Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks.
02/2017 – 01/2019	Electronic Design Automation Laboratory , NTU EE, Taipei, Taiwan Undergraduate Research Assistant (Advisor: Dr. Yao-Wen Chang) <ul style="list-style-type: none">– Proposed an algorithm on Obstacle-Aware On-Track Bus Routing based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours.– Designed an algorithm on Initial Detailed Routing; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest.

PUBLICATIONS

Journal Articles

- [J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

Conference Papers

- [C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits,” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020. (accepted)
- [C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, “Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow,” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020. (accepted)
- [C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, “[Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.
- [C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, “[A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing](#),” in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.
- [C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, “[A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides](#),” in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5-8, 2018.

HONORS & AWARDS

2019	Cockrell School of Engineering Fellowship , The University of Texas at Austin.
2019, 2018	Outstanding Performance Scholarship , National Taiwan University.
2018	3rd Place , IEEE/ACM ICCAD CAD Contest - Problem A.
2018	Top 10 , IEEE/ACM ICCAD CAD Contest - Problem B.
2018	3rd Place , ACM ISPD Initial Detailed Routing Contest.

SKILLS

Programming: C/C++, Python, Java, Verilog, \LaTeX , Linux System.
EDA Tools: Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys Hspice, Synopsys PrimeTime.
Languages: Mandarin (native), Taiwanese (native), English (fluent).

SELECTED PROJECTS

- MAGICAL [C5, C4]:** The DARPA IDEA Machine Generated Analog IC Layout System program.
– Developed an complete routing system for analog/mixed-signal circuits layout.
– Taped-out a complex high performance ADC under TSMC 40nm technology with fully automatically generated layout.
- ThreABC [C3]:** A system for threshold logic synthesis and optimization integrated on Berkeley ABC.
– Supplied transformation between threshold logic network and AIG network.
– Provided a fast threshold logic optimizing operation to reduce the interconnects of threshold networks.
- LuLuBus [J1, C2]:** A multithreaded topology-matching on-track bus router considering DRC constraints.
– Performed bus routing with topology constraints on complex track configuration.
– Produced routing results with few design rule violations.
- LuLuRoute [C1]:** A multithreaded ASIC detailed router considering several industrial DRC constraints.
– Outperformed the top-3 routers in 2018 ISPD Contest.
– Supported the standard LEF/DEF file format used in industry.
– Enabled multithread routing for runtime improvement.