Hao Chen

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Research Interests

Electronic Design Automation, Physical Design, Automated Reasoning, Machine Learning and Reinforcement Learning for EDA.

Education

08/2019 – 05/2023 | **The University of Texas at Austin**, Austin, TX
Ph.D. in Electrical and Computer Engineering
Advisor: Dr. David Z. Pan

09/2014 – 01/2019 | **National Taiwan University (NTU)**, Tapei, Taiwan
B.S. in Electrical Engineering

Experience

06/2023 – Present | **X Development LLC** *Mountain View, CA*
Software Engineer
- Invent and prototype novel optimization techniques to break VLSI design hierarchies and impact chip design

10/2022 – 05/2023 | **X Development LLC** *Mountain View, CA*
Ph.D. Resident, Electronic Design Automation
- Implemented prototypes in electronic design automation using high-performance computing methods.

05/2021 – 09/2022 | **NVIDIA Corporation** *Austin, TX*
Research Intern, Design Automation Research
- Developed an automatic layout flow with novel place-and-route algorithms for analog/mixed-signal circuits under TSMC 5nm technology. [C13]
- Proposed placement algorithms with comprehensive analog-specific constraints supported using satisfiability modulo theories (SMT) and matching-aware routing methods. [C12]
- Detailed routing pattern optimization for full custom circuits using reinforcement learning and graph neural networks.

08/2019 – Present | **UT Design Automation Laboratory (UTDA)**, UT ECE *Austin, TX*
Graduate Research Assistant (Advisor: Dr. David Z. Pan)
- Researched on the **Machine Generated Analog IC Layout System (MAGICAL)** project of the DARPA IDEA Program, mainly responsible for the routing engine. [J4, J2, C5, C4]
- Research on matching constraint extraction for analog circuits with machine learning. [C8]
- Taped-out chips with state-of-the-art performance under TSMC 40nm technology with fully automatically generated layout. [C9, C7]

07/2017 – 08/2017 | **Synopsys Inc.** *Taipei, Taiwan*
Research Intern, IC Compiler II - RDL Routing Team
- Proposed and implemented an algorithm on *Routing Pattern Optimization Improvement* for routing wires bend reduction.
- Proposed an algorithm on X-architecture Steiner-tree construction.

Honors & Awards

2022–2023 | **NVIDIA Graduate Fellowship**, NVIDIA Corporation.
2019–2023 | **Cockrell School of Engineering Graduate Fellowship**, The University of Texas at Austin.
2019 | **2019 Outstanding Performance Scholarship**, National Taiwan University.
2018 | **2018 Outstanding Performance Scholarship**, National Taiwan University.
2018 | **3rd Place, 2018 CAD Contest- Problem A**, IEEE/ACM ICCAD.
2018 | **Top 10, 2018 CAD Contest- Problem B**, IEEE/ACM ICCAD.
2018 | **3rd Place, 2018 Initial Detailed Routing Contest**, ACM ISPD.

Publications

Book Chapters

[B2] Steven M. Burns, **Hao Chen**, Tonmoy Dhar, Ramesh Harjani, Jiang Hu, Nibedita Karmokar, Kishor Kunal, Yaguang Li, Yishuang Lin, Mingjie Liu, Meghna Madhusudan, Parijat Mukherjee, David Z. Pan, Jitesh Poojary, S. Ramprasath, Sachin S. Sapatnekar, Arvind K. Sharma, Wenbin Xu, Soner Yaldiz, and Keren Zhu, "Machine Learning Applications in Electronic Design Automation," Springer, 2022. (alphebetical order)

[B1] Mohamed B. Alawieh, Ahmet F. Budak, **Hao Chen**, Mingjie Liu, David Z. Pan, Wei Shi, Xiyuan Tang, Shuhan Zhang, and Keren Zhu, "CAD for Analog/Mixed-Signal Integrated Circuits," in *Advances in Semiconductor Technologies: Selected Topics Beyond Conventional CMOS*, Wiley-IEEE Press., 2022. (alphebetical order)

Journal Articles

[J6] Mingjie Liu, Xiyuan Tang, Keren Zhu, **Hao Chen**, Nan Sun, and David Z. Pan "1MS/s and 80MS/s SAR ADCs in 40nm CMOS with End-to-End Compilation," in *IEEE Solid-State Circuits Letters (SSC-L)*, 2023.

[J5] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, "Hierarchical Analog and Mixed-Signal Circuit Placement Considering System Signal Flow," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2023.

[J4] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, "Tutorial and Perspectives on MAGICAL: A Silicon-Proven Open-Source Analog IC Layout System," in *IEEE Trans. Circuit and Systems II (TCAS-II)*, 2022. **(Invited)**

[J3] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Nan Sun, and David Z. Pan, "Challenges and Opportunities Toward Fully Automated Analog Layout Design," in *Journal of Semiconductors (JoS)*, 2020. (* equal contribution) **(Invited, featured on cover)**

[J2] **Hao Chen***, Mingjie Liu*, Biying Xu*, Keren Zhu*, Xiyuan Tang, Shaolan Li, Yibo Lin, Nan Sun, and David Z. Pan, "MAGICAL: An Open-Source Fully Automated Analog IC Layout System from Netlist to GDSII," in *IEEE Design and Test (D&T)*, 2020. (* equal contribution) **(Invited)**

[J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

Conference Papers

[C17] Ahmet F. Budak, Keren Zhu, **Hao Chen**, Souradip Poddar, Linran Zhao, Yaoyao Jia, and David Z. Pan, "Joint Optimization of Sizing and Layout for AMS Designs: Challenges and Opportunities," in *Proc. ACM International Conference on Physical Design (ISPD)*, Virtual Event, USA, Mar. 26–29, 2023.

[C16] **Hao Chen**, Kai-Chieh Hsu, Walker J. Turner, Po-Hsuan Wei, Keren Zhu, David Z. Pan, and Haoxing Ren, "Reinforcement Learning Guided Detailed Routing for Custom Circuits," in *Proc. ACM International Conference on Physical Design (ISPD)*, Virtual Event, USA, Mar. 26–29, 2023.

[C15] Haoxing Ren, Siddhartha Nath, Yanqing Zhang, **Hao Chen**, and Mingjie Liu, "Why are Graph Neural Networks Effective for EDA Problems?" in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Oct. 30–Nov. 3, 2022. **(Invited)**

[C14] Keren Zhu, **Hao Chen**, Walker J. Turner, George F. Kokai, Po-Hsuan Wei, David Z. Pan, and Haoxing Ren, "TAG: Learning Circuit Spatial Embedding From Layouts," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Oct. 30–Nov. 3, 2022.

[C13] **Hao Chen**, Walker J. Turner, Sanquan Song, Keren Zhu, George F. Kokai, Brian Zimmer, C. Thomas Gray, Brucek Khailany, David Z. Pan, and Haoxing Ren, "AutoCRAFT: Layout Automation for Custom Circuits in Advanced FinFET Technologies," in *Proc. ACM International Conference on Physical Design (ISPD)*, Virtual Event, Canada, Mar. 27–30, 2022. **(Invited)**

[C12] **Hao Chen**, Walker J. Turner, David Z. Pan, and Haoxing Ren, "Routability-Aware Placement for Advanced FinFET Mixed-Signal Circuits using Satisfiability Modulo Theories," in *Proc. IEEE/ACM Design, Automation and Test in Europe (DATE)*, Antwerp, Belgium, Mar. 14–23, 2022.

[C11] Keren Zhu, **Hao Chen**, Mingjie Liu, and David Z. Pan, "Automating Analog Constraint Extraction: From Heuristics to Learning," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022. **(Invited)**

[C10] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Wei Shi, Nan Sun, and David Z. Pan, "Generative-Adversarial-Network-Guided Well-Aware Placement for Analog Circuits," in *Proc. IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Virtual Event, Taiwan, Jan. 17–20, 2022.

[C9] Mingjie Liu, Xiyuan Tang, Keren Zhu, **Hao Chen**, Nan Sun, and David Z. Pan, "OpenSAR: An Open Source Automated End-to-end SAR ADC Compiler," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 01–04, 2021.

[C8] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Universal Symmetry Constraint Extraction for Analog and Mixed-Signal Circuits with Graph Neural Networks," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, Jul. 11–15, 2021.

[C7] **Hao Chen***, Mingjie Liu*, Xiyuan Tang*, Keren Zhu*, Abhishek Mukherjee, Nan Sun, and David Z. Pan, "MAGICAL 1.0: An Open-Source Fully-Automated AMS Layout Synthesis Framework Verified With a 40-nm 1GS/s $\Delta\Sigma$ ADC," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, Virtual Event, USA, Apr. 25–28, 2021. (* equal contribution)

[C6] Keren Zhu, Mingjie Liu, **Hao Chen**, Zheng Zhao, and David Z. Pan, "Exploring Logic Optimizations with Reinforcement Learning and Graph Convolutional Network," in *Proc. ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Virtual Event, Iceland, Nov. 16–20, 2020.

[C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020.

[C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Virtual Event, USA, Nov. 2–5, 2020. (**Best Paper Award Nomination from Track**)

[C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, "Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.

[C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2–6, 2019.

[C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, "A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5–8, 2018.

Skills

Programming:	C++, C, Python, Java, Tcl, Verilog
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys IC Compiler II
Deep Learning Toolkits:	PyTorch, Tensorflow
Optimization Toolkits:	OR-Tools, Z3, JAX
Languages:	Mandarin (native), Taiwanese (native), English (full professional)

Professional Services

Reviewer/Secondary Reviewer

- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD'20, 21, 22)
- ACM/IEEE Design Automation Conference (DAC'21, 22, 23)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD'22)
- ACM/IEEE Workshop on Machine Learning for CAD (MLCAD'22)
- IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS'22)
- Integration - The VLSI Journal (VLSIJ'22)