Hao Chen

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Research Interests

Design Automation for Analog Circuits, VLSI Physical Design, Logic Synthesis, Formal Methods, Combinatorial Optimization.

Education

08/2019 – Present
Ph.D. Student in Electrical and Computer Engineering
The University of Texas at Austin, Austin, TX
Advisor: Dr. David Z. Pan
- Courses: VLSI Physical Design Automation, Verification of Digital System, VLSI I, Analog IC Design.

09/2014 – 01/2019
B.S.E. in Electrical Engineering
National Taiwan University (NTU), Tapei, Taiwan
- Courses: Physical Design for Nanometer ICs†, Logic Synthesis and Verification†, Convex Optimization†, Machine Learning†, Operating System†, Algorithms († graduate-level courses).

Work Experience

07/2017 - 08/2017
IC Compiler - RDL Routing Team, Synopsys Inc., Taipei, Taiwan
R&D Intern (Mentor: Kai-Shun Hu)
- Proposed and implemented an algorithm on *Routing Pattern Optimization Improvement*; up to 93% of bend count reduction is achieved.

Research Experience

08/2019 – Present
UT Design Automation Laboratory (UTDA), UT ECE, Austin, TX
Graduate Research Assistant (Advisor: Dr. David Z. Pan)
- Researched on the **Machine Generated Analog IC Layout System (MAGICAL)** project of the DARPA IDEA Program, mainly responsible for the routing engine.

09/2017 – 01/2019
Applied Logic and Computation Laboratory, NTU EE, Taipei, Taiwan
Undergraduate Research Assistant (Advisor: Dr. Jie-Hong R. Jiang)
- Researched on *Threshold Logic Synthesis and Optimization* for modern circuit design.
- Proposed threshold logic network interconnect optimization algorithm using an efficient threshold logic function representation data structure; up to 10% interconnection and 14% weight/threshold value reduction achieved over highly optimized threshold logic networks.

02/2017 – 01/2019
Electronic Design Automation Laboratory, NTU EE, Taipei, Taiwan
Undergraduate Research Assistant (Advisor: Dr. Yao-Wen Chang)
- Proposed an algorithm on **Obstacle-Aware On-Track Bus Routing** based on directed acyclic graph; outperformed the winning teams in the 2018 ICCAD Contest, where the top-3 routers result in 145%, 158%, 420% higher costs than ours.
- Designed an algorithm on **Initial Detailed Routing**; in particular 23% reduction of routing cost was obtained compared with the first place router in the 2018 ISPD Contest.

Publications

Journal Articles

[J1] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2020.

Conference Papers

[C5] **Hao Chen**, Keren Zhu, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Toward Silicon-Proven Detailed Routing for Analog and Mixed-Signal Circuits", in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020. (accepted)

[C4] Keren Zhu, **Hao Chen**, Mingjie Liu, Xiyuan Tang, Nan Sun, and David Z. Pan, "Effective Analog/Mixed-Signal Circuit Placement Considering System Signal Flow", in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 2-5, 2020. (accepted)

[C3] **Hao Chen**, Shao-Chun Hung, and Jie-Hong R. Jiang, "Disjoint-Support Decomposition and Extraction for Interconnect-Driven Threshold Logic Synthesis," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C2] Chen-Hao Hsu, Shao-Chun Hung, **Hao Chen**, Fan-Keng Sun, and Yao-Wen Chang, "A DAG-Based Algorithm for Obstacle-Aware Topology-Matching On-Track Bus Routing," in *Proc. ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, Jun. 2-6, 2019.

[C1] Fan-Keng Sun, **Hao Chen**, Ching-Yu Chen, Chen-Hao Hsu, and Yao-Wen Chang, "A Multithreaded Initial Detailed Routing Algorithm Considering Global Routing Guides," in *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Diego, CA, Nov. 5-8, 2018.

Honors & Awards

2019	**Cockrell School of Engineering Fellowship**, The University of Texas at Austin.
2019, 2018	**Outstanding Performance Scholarship**, National Taiwan University.
2018	**3rd Place**, IEEE/ACM ICCAD CAD Contest - Problem A.
2018	**Top 10**, IEEE/ACM ICCAD CAD Contest - Problem B.
2018	**3rd Place**, ACM ISPD Initial Detailed Routing Contest.

Skills

Programming:	C/C++, Python, Java, Verilog, LaTeX, Linux System.
EDA Tools:	Cadence Virtuoso, Cadence Innovus, Cadence ADE, Synopsys Hspice, Synopsys PrimeTime.
Languages:	Mandarin (native), Taiwanese (native), English (fluent).