Programmable CMOS/Memristor Threshold Logic

Ligang Gao, Fabien Alibart, and Dmitri B. Strukov

***Abstract*—This paper proposes a hybrid CMOS/memristor implementation of a programmable threshold logic gate. In this gate, memristive devices implement ratioed diode-resistor logic, while CMOS circuitry is used for signal amplification and inversion. Due to the excellent scaling prospects and nonvolatile analog memory of memristive devices, the proposed threshold logic is in-field configurable and potentially very compact. The concept is experimentally verified by implementing a 4-input symmetric linear threshold gate with an integrated circuit CMOS flip-flop, silicon diodes, and Ag/a-Si/Pt memristive devices.**

***Index Terms*—Memristor, neural networks, programmable circuits, solid-state electrolyte memory, threshold logic.**

I. Introduction

THE development of high-performance threshold logic would benefit a number of important applications in computing, from microprocessors to bio-inspired information processing [1]. To be specific, let us focus on a particular type of threshold logic—a linear threshold gate (LTG), whose transfer function for N-input gate is defined as

$$f(x_1, \ldots x_n) = \begin{cases} 1, & \text{if } \sum_{i=1}^{N} w_i x_i \geq T \\ 0, & \text{otherwise} \end{cases} \quad (1)$$

where x_i is a Boolean input variable, w_i is an integer weight of the corresponding input i, and the threshold T is an integer number [2]. A special case of LTG is symmetric LTG with identical weights for different inputs [1], [3]. N-input symmetric LTG can implement a maximum of N nontrivial Boolean functions $f^{(k)}\ (x_1, x_2, \ldots, x_N)$ defined by $w_1^{(k)} = w_2^{(k)} = \cdots = w_N^{(k)} = 1$ and $T^{(k)} = k$, i.e.,

$$f^{(k)}(x_1, \ldots x_N) = \begin{cases} 1, & \text{if} \sum_{i=1}^{N} x_i \geq k \\ 0, & \text{otherwise} \end{cases} \quad (2)$$

where $k = 1, 2, \ldots, N$. By dividing the inequality in (2) by k, the alternative definition for the symmetric LTG (which is also used in the paper) is given by $w_1^{(k)} = w_2^{(k)} = \cdots = w_N^{(k)} = 1/k$ and $T^{(k)} = 1$.

LTG is a universal gate and much more powerful than similar fan-in single NAND or NOR gates. A recent study indicates up to 2× reduction on average (and even up to 5× for some) in the gate count for representative benchmark circuits implemented with LTGs, as compared to traditional logic synthesis [4]. This is an example of why LTGs have been a popular choice for the implementation of computer arithmetic circuits [5], [6]. However, these gates have been historically more commonly applied in artificial neural networks, due to their similarity in functionality with that of biological neurons [1], and also conventional signal and image processing due to efficient implementation of weighted filters [7]. For instance, one of the earliest concepts in artificial neural networks—the McCullough–Pitts perceptron [8]—can be implemented with a single LTG.

Various implementations of LTGs have been investigated, and some are even used today in commercial products [1]. Most common implementations are based on pseudo-nMOS, output-wired inverters, and floating-gate and switch capacitor logic styles, whereas less conventional ones utilize nontraditional device technologies such as single electron transistors and negative differential resistance devices. In most cases the weights are fixed and cannot be changed in-field, but some LTG implementations are employing digitally stored weights (which incurs a rather large penalty), and perhaps only a hybrid technology approach based on CMOS and floating gate transistors relies on programming analog weights directly into the gate [9].[1] The in-field reconfiguration of the LTG's weights is a very desirable feature for most of the applications, and in this paper we present an alternative solution for programmable LTGs based on hybrid-circuit technology. The potential advantages over the floating-gate approach and a comparison to another memristor-based threshold gate concept [10]–[13] are discussed in Section IV.

The key element of the proposed hybrid CMOS/memristor circuits[2] is a resistance-switching "memristive" [14]–[16] device—see, e.g., reviews of such devices and their applications

Manuscript received March 19, 2012; accepted June 26, 2012. Date of publication January 18, 2013; date of current version March 6, 2013. This work was supported by the National Science Foundation under Grant CCF-1017579 and by the Air Force Office of Scientific Research under MURI grant FA9550-12-1-0038. The review of this paper was arranged by Associate Editor S. D. Cotofana.

The authors are with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: lggao@ece.ucsb.edu; alibart@ece.ucsb.edu; strukov@ece.ucsb.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TNANO.2013.2241075

[1]The technique of achieving LTG by replicating normal/complimentary inputs of a fixed majority gate, which is a symmetric LTG with fixed weights, is also not attractive due to its large area overhead.

[2]According to the original definition [14], [15], the more appropriate name would be "CMOS/memristive-device circuit" because the resistance switching devices considered in this work are not pure memristors because of nonlinear $I-V$ characteristics and hence they belong to a more general class of memristive devices. However, such a name is in line with the recent suggestion from the same authors [16], which is to use the term "memristor" in a much broader sense.

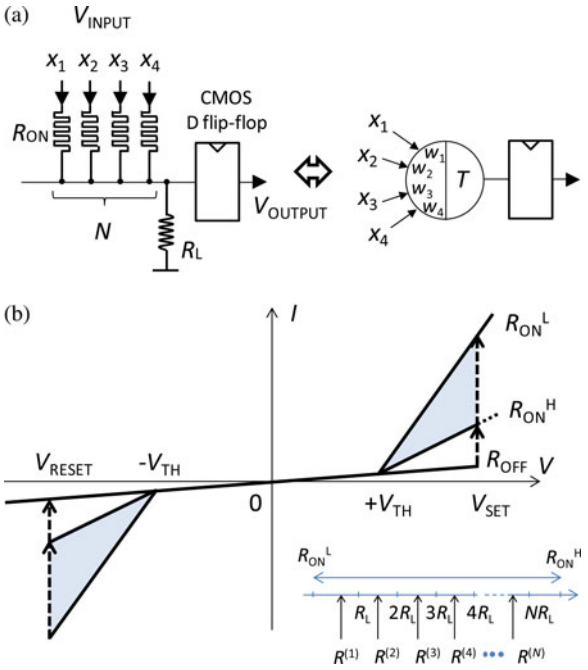

Fig. 1. (a) Main idea of a LTG implemented with memristors and CMOS D flip-flop. (b) $I-V$ characteristics of memristive devices (schematically represented). The shaded area on panel (b) shows the range of possible intermediate states utilized for the implementation of the threshold gate.

in [17]–[21]. In the simplest case, a memristive device consists of an active thin film layer of some material sandwiched between two metal electrodes. The device's footprint is determined by the overlap area of two electrodes and, therefore, limited only by the electrode's dimensions. Application of a relatively large electrical stress (voltage or current) across electrodes changes the resistivity ("memory state") of the thin film material. The memory state of properly engineered devices is nonvolatile and could be read without disturbing it with a smaller (as compared to a write) electrical stress. For many devices, the resistance can be changed continuously so that the memory state is essentially analog, which enables many prospective applications [20]–[24].

II. CMOS/Memristor Threshold Gate

A. General Case

Memristive devices are well suited for implementing weights in the proposed threshold logic circuits [see Fig. 1(a)]. In particular, let us consider diode-like memristive devices with a strongly suppressed current below the effective threshold $V_{\rm TH}$ (e.g., due to an additional layer added in the device stack) and linear conductance above such a threshold with a configurable slope (differential conductance) $1/R$ [see Fig. 1(b)]. Here we assume that the slope can be configured to any value between $1/R_{\rm ON}^L$ and $1/R_{\rm ON}^H$, so that

$$1/R_{\rm ON}^H \le 1/R \le 1/R_{\rm ON}^L. \tag{3}$$

Such particular $I-V$ of the memristive device simplifies the implementation of the configurable ratioed diode-resistor logic (DRL) [see Fig. 1(a)], which is comprised of several (N) memristive devices connected in parallel to a single pull-down resistor R_L.[3] To suppress leakage currents between inputs of the gate, operating voltage is chosen from the condition

$$V_{\rm TH} < V_{\rm DD} < 2V_{\rm TH}. \tag{4}$$

Neglecting leakage currents below $V_{\rm TH}$, i.e., currents via $R_{\rm OFF}$ resistance [Fig. 1(b)], the output voltage of ratioed DRL always ranges from 0 to $V_{\rm DD}-V_{\rm TH}$ and is equal half of that value when

$$\sum_{i=1}^{N} x_i \frac{1}{R_i} = \frac{1}{R_L}. \tag{5}$$

Generally, the DRL is connected to a CMOS gate so that the voltage swing is restored (and possibly inverted) and the output of the CMOS gate is used to drive the inputs of other logic gates. In principle, a simple CMOS inverter would be sufficient for that purpose, although we chose D-flip-flop because of its effectiveness for high-throughput pipelined circuits [3], [25]. Assuming that the CMOS gate is designed to restore a signal to $V_{\rm DD}$ (logical "1"), if the input voltage is larger than $(V_{\rm DD}-V_{\rm TH})/2$ and otherwise to 0 (logical "0"), the combined circuit [see Fig. 1(a)] implements the LTG defined by (1), where $w_i = 1/R_i$ and $T = 1/R_L$. Note that the noninteger (rational) weights and the threshold could always be converted to the integer numbers required by the original definition of LTG by multiplying both sides of the inequality in (1) by the appropriate constants.

B. Symmetric LTG

The effect of the dynamic range of memristive devices (i.e., the ratio $R_{\rm ON}^H/R_{\rm ON}^L$) on the number of different Boolean functions which the N-input LTG can implement, the choice of optimal R_L, and the weights of the memristive devices for a particular Boolean function are best investigated using a symmetric LTG. For symmetric LTG weights, $w^{(k)} = 1/R^{(k)}$ and R_L must satisfy the following pair of conditions:

$$(k-1)R_L < R^{(k)} < k\,R_L. \tag{6}$$

The inset of Fig. 1(b) shows the possible spectrum of $R^{(k)}$ with respect to R_L given by (6). In order to implement all N Boolean functions with a symmetric LTG, the $[R_L, NR_L]$ range should fit within a physically permitted range $[R_{\rm ON}^L, R_{\rm ON}^H]$; therefore [4]

$$R_{\rm ON}^H/R_{\rm ON}^L = N. \tag{7}$$

[3]The same circuit can also be implemented with memristive devices having nonlinear $I-V$ over the whole range of applied voltages, though in this case the analysis is less straightforward.

[4]In principle, a simpler design of a symmetric LTG is possible, with fixed weights and load resistor implemented with a memristive device. However, such implementation is less suitable for circuit integration (e.g., in the context of CMOL FPGA circuits, in which weights must be configurable—see discussion below) and, moreover, cannot be used to implement more general case LTGs. Nevertheless, having both R_L and weights implemented with memristive devices may allow flexibility in choosing the optimal value of R_L to relax (6).

When $R^H_{\rm ON}/R^L_{\rm ON} \approx N$, the value R_L could be chosen close to $R^L_{\rm ON}$, e.g.,

$$R_L = R^L_{\rm ON} + (R^H_{\rm ON} - R^L_{\rm ON})/N. \quad (8)$$

Finally, for a particular threshold function $k > 1$ and fixed R_L, the best choice of $R^{(k)}$ is dictated by the largest voltage margins, i.e., from (6)

$$R^{(k)} \approx R_L[k(k-1)]^{0.5}. \quad (9)$$

III. Experimental Demonstration

The proposed LTG is experimentally demonstrated using Ag/a-Si/Pt memristive devices. The memristive device consists of a top Ag electrode, the a-Si layer, and Pt as the bottom electrode. An evaporated Ti/Pt bottom electrode (5 nm/35 nm) is patterned by the standard optical lithography technique on a Si/SiO_2 substrate (500 μm/200 nm, respectively) at a rate of 0.1 nm/s. A 40-nm a-Si active layer is then deposited by a plasma-enhanced chemical vapor deposition at 300 °C and a pressure of 600 mT, using SiH_4 (2% in He). The orthogonal top electrode is defined by a lift-off step. An Ag/Au electrode (50 nm/25 nm) is evaporated on top of the a-Si active layer. After deposition, the device is annealed at 450 °C in a high-vacuum condition (10^{-8}T) to diffuse the Ag to a-Si film.

Fig. 2(a) shows a typical *I–V* characteristic, with multiple resistance states achieved by controlling sweeping voltage during the reset process (negative polarity), or by controlling the current compliance during the set process (positive polarity). In order to characterize switching dynamics for Ag/a-Si/Pt devices, pulse protocol measurements are employed [24]. For Ag/a-Si/Pt devices, application of voltage biases in the range $|V| \leq V_{\rm SW} = 0.3$ V was found to have a negligible effect on the resistance state, even for relatively long stress times [see Fig. 2(b), (c)]; however, the switching rate grows rapidly with the applied voltages $|V| > V_{\rm SW}$. This is in agreement with the experimentally observed (and theoretically predicted [26]) exponential dependence of the switching dynamics on the applied voltage.

The switching behavior is similar to previously reported results for TiO_{2-x} devices by our group [24]. The poor apparent ON/OFF current ratio, in comparison to other devices reported in the literature, is due to the requirement of keeping the device in the ohmic regime in all dynamic ranges. The linear ON state is likely due to metallic filament(s) bridging two electrodes, while modulation of the state is attributed to the changes in the radius (and shape) of the filament(s). In particular, Ag/a-Si/Pt devices can be programmed to have any linear resistance state between $R^L_{\rm ON} = 0.5$ KΩ and $R^H_{\rm ON} = 10$ KΩ. Note that the device can be also programmed to higher resistance states (with the most extreme one corresponding to the OFF state), but these states are nonlinear.

For the purpose of demonstration, the voltage threshold $V_{\rm TH}$ in the Ag/a-Si/Pt device is implemented with two external Si diodes connected in anti-parallel fashion (see inset of Fig. 3). Note that PN diodes might not provide sufficient current density for a completely integrated solution, and so a more practical approach would be the integration of the MIM structure [27] or the ovonic threshold switch [28] in the device stack. In fact,

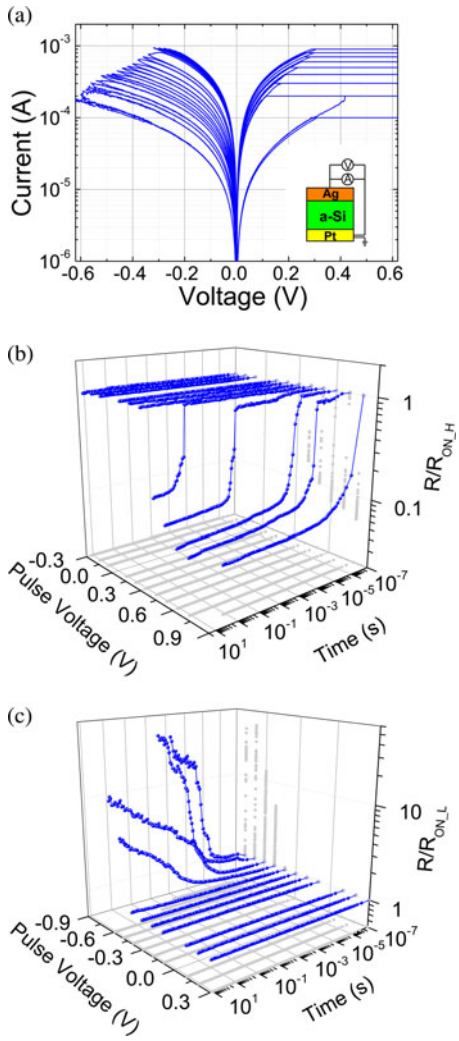

Fig. 2. $I-V$ and switching dynamics for an Ag/a-Si/Pt device. (a) Typical $I-V$s are obtained with triangular voltage sweeps with approriate current complience. (b) Gradual set and (c) reset of the resistance state measured at 100 mV and normalized to initial state as a function of applied voltage pulses with variable amplitude and duration.

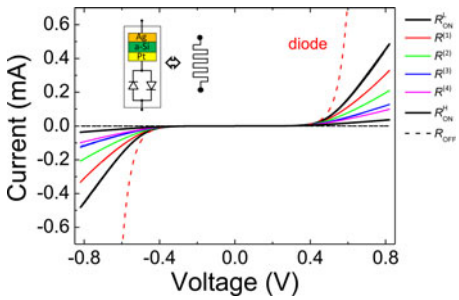

Fig. 3. Measured $I-V$ characteristics of an Ag/a-Si/Pt device in series with anti-parallelly connected Si diodes. The red, green, blue, and magenta colors show four particular intermediate states, with differential conductance (weights) $w^{(1)} = 1.2$ mS, $w^{(2)} = 0.7$ mS, $w^{(3)} = 0.4$ mS, and $w^{(4)} = 0.3$ mS, respectively, and two extreme linear ON states (i.e., $R^H_{\rm ON}$ and $R^L_{\rm ON}$) and OFF states are shown in black. The inset is a schematic representation of the device structure. Note that the figure does not show set and reset transitions, which happen at $|V| > 0.82$ V for the combined device.

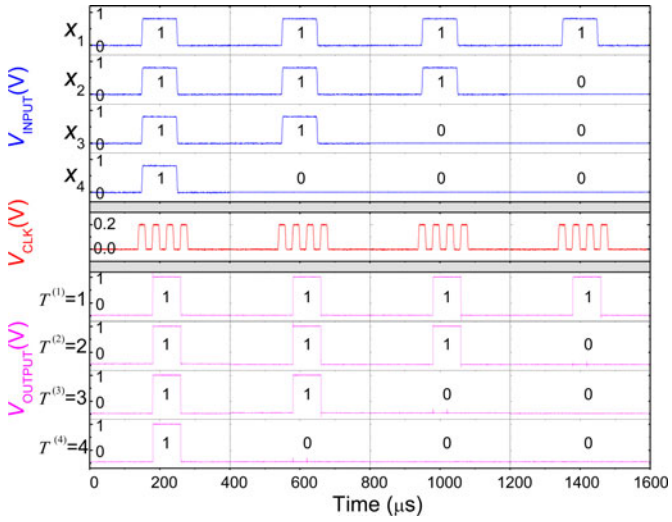

Fig. 4. Experimental demonstration of a symmetric 4-input linear threshold logic gate operation. The bottom part of the figure shows output voltage for the LTG with $w = 1$ and four different programmed thresholds ($T^{(1)} = 1$, $T^{(2)} = 2$, $T^{(3)} = 3$, and $T^{(4)} = 4$), which are implemented with the corresponding weights shown in Fig. 3, for the four different combinations of the inputs shown at the top of the figure. All voltage levels are normalized with respect to actual supply/clock voltages ($V_{\rm DD}^{\rm FF} = 1$ V, $V_{\rm SS}^{\rm FF} = -0.43$ V, $V_{\rm CLK} = 0.2$ V, and $V_{\rm INPUT} = 0.82$ V, and $R_L = 2$ kΩ).

the integration of the high current density selector device with the memristor is being actively investigated in the context of memory circuits [29].

A measured *I–V* for the combined device stack (see Fig. 3) is very similar to the ideal piecewise *I–V* shown in Fig. 1(b), with $V_{\rm TH} \approx 0.52$ V and switching voltage $V_{\rm SET} = -V_{\rm RESET} = V_{\rm TH} + V_{\rm SW} \approx 0.82$ V. In particular, Fig. 3 shows four values of $R^{(k)}$ used for the demonstration of a 4-input symmetric LTG (see Fig. 4), selected according to the approach discussed in the previous section. Memristive devices are programmed with a high-precision variation-tolerant tuning algorithm [24].

To increase voltage margins, the largest permissible voltage $V_{\rm DD} = 0.82$ V (which does not modify the state of memristive devices during the logic operation) is applied to the input of the ratioed DRL. The threshold of the integrated circuit D-flip-flop is set to $(V_{\rm DD} - V_{\rm TH})/2 = 0.15$ V by choosing the appropriate power supply voltages $V_{\rm DD}^{\rm FF} = 1$ V and $V_{\rm SS}^{\rm FF} = -0.43$ V. With such a choice of power supply, the output of the D-flip-flop is different from the inputs applied to the gate. For a fully integrated solution, the D-flip-flop must be redesigned to allow for compatible output and input voltages.

IV. Discussion and Summary

The ionic nature of the memory mechanism for memristive devices [17]–[20] enables much better scaling prospects, and hence a much denser and more potent LTG implementation of the proposed gate than those based on floating-gate transistor approaches [9]. The latter could not provide analog properties when aggressively scaled. For example, the number of electrons on a floating gate ($\delta 16$) is already a limiting factor for the number of memory levels it can supply for sub-20-nm channel length NAND flash memory devices.

The concept also compares favorably with the other CMOS/memristor circuits proposed earlier. The proposed implementation in this paper does not rely on changing the state of memristive devices during the logic operation, which makes it more robust as compared to approaches suggested in [10] and [13]. In addition, each memristive device in the suggested threshold logic in [10]–[12] is served by a CMOS-based current mirror circuit, which comes with considerable overhead and is probably unsuitable for the most promising crossbar architectures. However, this is not an issue in our proposed concept. Memristive devices might be integrated into crossbar circuits which are patterned above the CMOS layer (e.g., similar to the proposed (3-D) CMOL concepts [18], [26]), so that the area of the threshold gate will be mostly determined by the CMOS flip-flop, with some minor additional circuitry required for programming the memristive devices.

In fact, it should be clear that the functionality of CMOL-based digital logic [18], [25], [30], [31] will be enriched by implementing LTG cells. Particularly for these circuits the memristive device would serve two purposes. Configuring memristive devices to the $R_{\rm ON}^{H} \le R \le R_{\rm ON}{}^{L}$ resistance state would set the logic gate functionality and at the same time provide gate interconnect. The gates would be electrically disconnected by setting the corresponding memristive device to an $R_{\rm OFF}$ resistance state. The implementation of the LTG in CMOL-based pattern matching circuits [25], [30], [32] might be especially rewarding since it would enable the efficient implementation of approximate pattern matching.

The fact that the voltage margins decrease linearly with N for the proposed threshold gate implementation might not necessarily decrease the speed of operation, because occasional errors might be tolerated in many applications [33], [34] including high fan-in pattern matching operations [25], [30], [32]. At least in CMOL-based logic gate fan-in might be programmed in-field so that whenever highly reliable logic gates are required low fan-in gates can be utilized and appropriate mixture of different grade reliability gates could be selected according to the specific application needs.

In summary, we propose and experimentally demonstrate a programmable CMOS/memristor LTG. The gate is potentially very compact and suited for hybrid crossbar circuit implementation with prospective applications in signal, image, and bio-inspired signal processing.

References

[1] V. Beiu, J. M. Quintana, and M. J. Avedillo, "VLSI implementations of threshold logic: A comprehensive survey," *IEEE Trans. Neural Netw.*, vol. 14, no. 5, pp. 1217–1243, Sep. 2003.

[2] S. Muroga, *Threshold Logic and its Applications*. Hoboken, NJ, USA: Wiley, 1972.

[3] M. Padure, S. Cotofana, and S. Vassiliadis, "Design and experimental results of a CMOS flip-flop featuring embedded threshold logic," in *Proc. ISCAS*, Bangkok, Thailand, May 2003, pp. 253–256.

[4] R. Zhang, P. Gupta, L. Zhong, and N. K. Jha, "Synthesis and optimization of threshold logic networks with application to nanotechnologies," in *Proc. DATE'04*, Paris, France, Feb. 2004, pp. 904–909.

[5] Y. Leblebici, H. Özdemir, A. Kepkep, and U. Çilingiroglu, "A compact high-speed (31, 5) parallel counter circuit based on capacitive threshold logic gates," *IEEE J. Solid-State Circuits*, vol. 31, no. 8, pp. 1177–1183, Aug. 1996.

[6] P. Celinski, S. Cotofana, and D. Abbott, "A-DELTA: A 64-bit high speed, compact, hybrid dynamic-CMOS/threshold-logic adder," in *Proc. IWANN*, Menorca, Spain, Jun. 2003, pp. 73–80.

[7] O. Yli-Harja, J. Astola, and Y. Neuvo, "Analysis of the properties of median and weighted median filters using threshold logic and stack filter representation," *IEEE Trans. Signal Process.*, vol. 39, no. 2, pp. 395–410, Feb. 1991.

[8] W. McCulloch and W. Pitts, "A logical calculus of the ideas immanent in nervous activity," *Bulletin Math. Biophys.*, vol. 7, pp. 115–133, 1943.

[9] V. Bohossian, P. Hasler, and J. Bruck, "Programmable neural logic," *IEEE Trans. Compon. Packag. Manuf. Technol. Part B*, vol. 21, no. 4, pp. 346–351, Nov. 1998.

[10] J. Rajendran, H. Manem, and G. S. Rose, "NDR based threshold logic fabric with memristive synapses," in *Proc. IEEE Nano*, Genoa, Italy, Jul. 2009, pp. 725–728.

[11] J. Rajendran, H. Manem, R. Karri, and G. S. Rose, "Memristor based programmable threshold logic array," in *Proc. Nanoarch*, Anaheim, CA, USA, Jun. 2010, pp. 5–10.

[12] G. S. Rose, J. Rajendran, H. Manem, R. Karri, and R. E. Pino, "Leveraging memristive systems in the construction of digital logic circuits," *Proc. IEEE*, vol. 100, no. 6, pp. 2033–2049, Jun. 2012.

[13] S. Kvatinsky, N. Wald, G. Satat, A. Kolodny, U. C. Weiser, and E. G. Friedman, "MRL: Memristor ratioed logic," in *Proc. Int. Cellular Nanoscale Netw. Appl.*, 2012, pp. 1–6.

[14] L. O. Chua, "Memristor: The missing circuit element," *IEEE Trans. Circuit Theory*, vol. 18, no. 5, pp. 507–519, Sep. 1971.

[15] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*,, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[16] L. O. Chua, "Resistance switching memories are memristors," *Appl. Phys. A*, vol. 102, pp. 765–783, 2011.

[17] R. Waser, R. Dittman, G. Staikov, and K. Szot, "Redox-based resistive switching memories—nanoionic mechanisms, prospects, and challenges," *Adv. Mater.*, vol. 21, pp. 2632–2663, 2009.

[18] K. K. Likharev, "Hybrid CMOS/nanoelectronic circuits: Opportunities and challenges," *J. Nanoelectron. Optoelectron.*, vol. 3, pp. 203–230, 2008.

[19] D. B. Strukov and H. Kohlstedt, "Resistive switching phenomena in thin films: Materials, devices and applications," *MRS Bulletin*, vol. 37, no. 02, pp. 108–114, 2012.

[20] K. Eshraghian, O. Kavehei, K. R. Cho, J. M. Chappell, A. Iqbal, S. F. Al-Sarawi, and D. Abbott, "Memristive device fundamentals and modeling: Applications to circuits and systems simulation," *Proc. IEEE*, vol. 100, no. 6, pp. 1991–2007, Jun. 2012.

[21] Y. V. Pershin and M. Di Ventra, "Practical approach to programmable analog circuits with memristors," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 57, no. 8, pp. 1857–1864, Aug. 2010.

[22] S. Shin, K. Kim, and S. M. Kang, "Memristor applications for programmable analog ICs," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 266–274, Mar. 2011.

[23] D. B. Strukov, "Smart connections," *Nature*, vol. 476, pp. 403–405, 2011.

[24] F. Alibart, L. Gao, B. Hoskins, and D. B. Strukov, "High-precision tuning of state for memristive devices by adaptable variation-tolerant algorithm," *Nanotechnology*, vol. 23, art. 074201, 2012.

[25] F. Alibart, T. Sherwood, and D. B. Strukov, "Hybrid CMOS/nanodevice circuits for high throughput pattern matching applications," in *Proc. AHS'11*, San Diego, CA, Jun. 2011, pp. 279–286.

[26] D. B. Strukov and R. S. Williams, "Four-dimensional address topology for circuits with stacked multilayer crossbar arrays," *Proc. National Academy Sci.*, vol. 106, pp. 20155–20158, 2009.

[27] E. William Cowell III, N. Alimardani, C. C. Knutson, J. F. Conley Jr., D. A. Keszler, B. J. Gibbons, and J. F. Wager, "Advancing MIM electronics: Amorphous metal electrodes," *Adv. Mater.*, vol. 23, no. 1, pp. 74–78, Jan. 2011.

[28] D. C. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K. W. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, and G. Spadini, "A stackable cross point phase change memory," in *Proc. Tech. Dig. IEDM Tech. Dig.*, 2009, pp. 617–620.

[29] International Technology Roadmap for Semiconductors [Online]. Available: http://www.itrs.net, 2011

[30] D. B. Strukov, "Hybrid CMOS/nanodevice circuits with tightly integrated memory and logic functionality," in *Proc. Nanotech'11*, vol. 2, Boston, MA, USA, Jun. 2011, pp. 9–12.

[31] D. B. Strukov and A. Mishchenko, "Monolithically stackable hybrid FPGA," in *Proc. Design Autom. Test Europe*, Dresden, Germany, Mar. 2010, pp. 661–666.

[32] A. Madhavan and D. B. Strukov, "Mapping of image and network processing tasks on high-throughput CMOL FPGA circuits," in *Proc. VLSI-SoC'12*, 2012, pp. 82–87.

[33] H. Esmaeilzadeh, A. Sampson, M. Ringenburg, L. Ceze, D. Grossman, and D. Burger, "Adressing dark silicon challenges with disciplined approximate computing," in *Proc. 4th Workshop Energy-Efficient Design*, 2012, pp. 1–2.

[34] J. Sartori, J. Sloan, and R. Kumar, "Stochastic computing: Embracing errors in architecture and design of processors and applications," in *Proc. CASES*, 2011, pp. 135–144.