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Energy Efficient Reconfigurable Threshold Logic Circuit with Spintronic Devices

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ABSTRACT A Threshold Logic Gate (TLG) performs weighted summation of multiple binary inputs and compares the summation with a threshold. Different logic functions can be implemented by reconfiguring the weights and threshold of the same TLG circuit. This paper introduces a novel design of reconfigurable Spintronic Threshold Logic Gate (STLG), which employs spintronic weight devices to perform current-mode weighted summation of binary inputs, whereas, the low voltage fast switching spintronic threshold device carries out the threshold operation in an energy efficient manner. The proposed STLG operates at a small terminal voltage of 50 mV, resulting in ultra-low energy consumption. A bottom-up cross-layer simulation framework is developed to synthesize and map large scale digital logic functions to the proposed STLG circuits. The simulation results of ISCAS-85 benchmarks show that the proposed STLG based reconfigurable logic hardware can achieve two orders lower Energy-Delay Product (EDP) compared with state-of-the-art CMOS Field Programmable Gate Arrays (FPGA), and smaller EDP compared to large scale Memristive Threshold Logic (MTL) based FPGA. Moreover, the ultra-low programming energy of spintronic weight device also leads to three orders lower reconfiguration energy of STLG compared to MTL design.

INDEX TERMS Magnetic domain wall strip, reconfigurable logic, threshold logic, magnetic tunnel junction, spintronic

I. INTRODUCTION

A Threshold Logic Gate (TLG) essentially constitutes of summation of weighted inputs, followed by a threshold operation as shown in Figure 1, where IN_i's are multiple binary inputs to a TLG, W_i's are scalar weights with which the corresponding inputs are multiplied and θ is the threshold [1]. W_i is a real number, which can be either positive or negative. Hence, depending upon the input combination, the summation can yield either a positive or a negative value, result of which is determined by a thresholding function. The same TLG circuit can implement different logic functions by reconfiguring the weights, threshold, or both. The threshold logic can be potentially applied to neuromorphic computing, signal processing, reconfigurable logic, image processing, pattern recognition, fast switching memory and control systems [2], [3].

A. RELATED WORK

In previous research works, threshold logic gates have been implemented in Complementary Metal-Oxide Semiconductor (CMOS) and other bulk semiconductor technologies, such as CMOS look-up-tables (LUT) [4], single electron transistors [5], monostable-Bistable logic elements [6], resonant tunneling diode [7] and capacitor based TLG [8]. Such hardware implementations suffer from power, delay and area overhead, which limits the wide application of threshold logic. Recent discovery of nanoscale memristor, whose multilevel or analog resistance can be programmed with an applied electric field, has led to proposal of energy-efficient Memristive Threshold Logic (MTL) [4], [9]. Such memristive TLG typically employ crossbar array to perform analog summation of binary input voltage signals (acting as weighing), and the thresholding operation can be implemented using current mirrors [4], voltage comparator [9] or spintronic devices [10]. Compared with CMOS LUT based TLG design, such MTL can potentially provide two orders lower energy consumption and higher area density [4], [10]. However, due to the intrinsic high energy consumption and long programming delay of memristor (AgCh [9], TiO_2 [4]), the memristor based TLG suffers from high power and long delay in reconfiguration operation, thereby eschewing the benefits of reconfigurable logic computing. Beyond that, nanomagnetic logic is also adopted in the

threshold logic gate circuit design, which utilizes the magnetization switching behavior under focalized magnetic field [11]. It is desirable to explore other emerging nano-devices that can be potentially employed as multilevel or analog weights required in TLG with similar or better computation energy efficiency, and more importantly, with ultra-low energy and fast reconfiguration operation.

Recent experiments on spintronic devices have demonstrated high speed switching ($\sim$ 1 ns) of nanoscale magnets with small spin polarized currents ($\sim 10^{11}$ A/m^2) due to spin-transfer torque (STT) [12], [13]. Together with other characteristics, including non-volatility, zero leakage current, compatibility with CMOS fabrication technology and high integration density, spintronic devices have been explored to design compact, high performance, low power memory [3], Boolean logic [10], [14]–[16], analog and neuromorphic computing [3], [17]–[19].

B. TECHNICAL CONTRIBUTION

In this work, a Spintronic Weight Device (SWD) based on magnetic domain wall strip and Magnetic Tunnel Junction (MTJ) is introduced. The continuous conductance of SWD can be programmed using a small current ($\sim 30\,\mu$A) pulse within 2 ns, which makes SWD an energy efficient device candidate to implement multilevel or analog weight of TLG. We then propose an ultra-low voltage ($\sim$ 50 mV) Spintronic Threshold Logic Gate (STLG) design that employs SWD to perform current mode weighted summation of binary inputs, while the low voltage spintronic threshold device (STD) carries out the threshold operation in an energy efficient manner. The proposed STLG operates at an ultra-low terminal voltage of $\sim$50 mV, resulting in ultra-low energy consumption. A bottom-up cross-layer simulation framework is also developed to synthesize and map large scale digital logic functions to the proposed STLG-based FPGA. Performance (including defect tolerance, energy, delay, area, EDP) comparison between the proposed STLG, MTL, Capacitive Threshold Logic (CTL) and LUT-based FPGAs are provided using ISCAS-85 benchmarking circuits. It shows that the proposed STLG based reconfigurable logic hardware can achieve two orders lower EDP compared with LUT-based FPGA, and smaller EDP in comparison with large scale MTL based FPGA. Moreover, the ultra-low programming energy of spintronic weight device also leads to three orders lower reconfiguration energy of STLG, compared with MTL design. In summary, the novelty and contributions of our work lie in applying such compact and energy efficient spintronic devices in ultra-low voltage and low energy hybrid spin-CMOS threshold logic design, which spans from device to architecture abstraction levels. The integration of peripheral ultra-low voltage ($\sim$50 mV) CMOS circuits and ultra-low current ($\sim 30\,\mu$A) spintronic devices lead to orders of performance improvement.

The technical contributions of our work are summarized as follows:

1) Ultra-low voltage and low energy reconfigurable spintronic threshold logic gate and spintronic threshold logic network (STLN) circuit are proposed based on spintronic weight device and spintronic threshold device with energy efficient computation and reconfiguration operations.
2) A reconfiguration circuit for spintronic weight device array is proposed to map the preset weight value to the corresponding spintronic weight device conductance of a STLG.
3) Circuit-level pipelining technique is proposed to maximize the STLG-based FPGA throughput.
4) A bottom-up cross-layer simulation framework is developed to synthesize any Boolean logic netlist and map synthesized netlist into the proposed spintronic threshold logic network. Performance evaluation (including defect tolerance, energy, delay, area, EDP) of the proposed Spintronic Threshold Logic Network with ISCAS-85 benchmarks is conducted and further compared with other CMOS and memristor based counterparts.

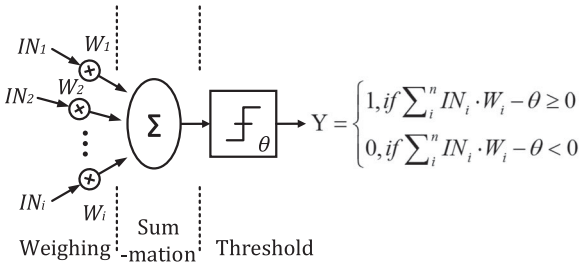

FIGURE 1. A schematic representation of Threshold Logic Gate (TLG) and its mathematical expression.

For clarification, this paper is the extended version of our previously published work [20], in which the initial spintronic threshold logic gate circuit was proposed, corresponding to contribution 1). While, the remaining three technical contributions are newly added.

The rest of this paper is organized as follows. In Section II, we describe the magnetic domain wall device including the device structure and circuit model of the proposed reconfigurable spintronic weight device, and spintronic threshold device for the thresholding function in TLG. The proposed circuit design of spintronic threshold logic gate is presented in Section III. Section IV introduces the simulation framework from device level through circuit level to the architecture level. Taking advantage of our simulation framework, we evaluate and optimize the performance of STLG-based FPGA in Section V. Finally, the conclusion is drawn in Section VI.

II. MAGNETIC DOMAIN WALL DEVICE

A TLG can be divided into three steps, i.e., weighing, summation and thresholding as shown in Figure 1. In this section, we present the device structure and operation of the Spintronic Weight Device and Spintronic Threshold Device. SWD has a reconfigurable continuous conductance range, which can be employed to implement the first step of (i.e., weighting) a TLG, while the STD can implement the compact current-mode thresholding function in TLG design.

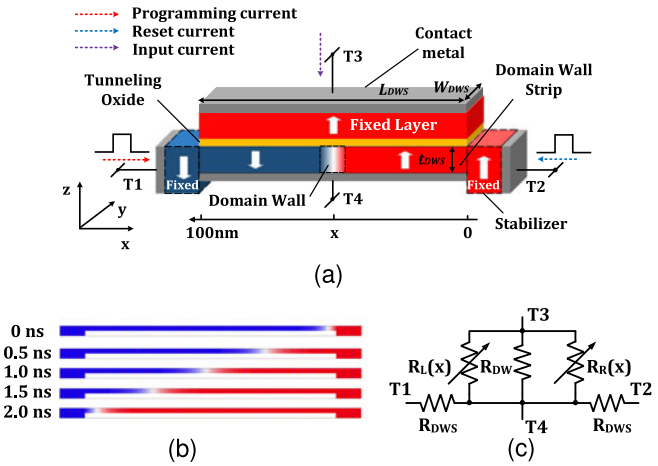

FIGURE 2. (a) Spintronic weight device structure, (b) Micromagnetic simulation of domain wall motion with 8.5 × 10^11 A/m^2 (c) SPICE model of spintronic weight device.

A. SPINTRONIC WEIGHT DEVICE

As shown in Figure 2, the SWD is based on a composite four-terminal device structure comprising a magnetic Domain Wall Strip (DWS) and a Magnetic Tunnel Junction. A MTJ consists of two ferromagnetic layers with a tunneling oxide (MgO) barrier sandwiched between them. The free ferromagnetic layer (domain wall strip) is laterally connected to two anti-parallel fixed magnetic domains between terminal 1 (T1) and terminal 2 (T2) [17], [21], [22]. The transition area between these two domains is called *Domain Wall* (DW). The larger thickness at the edges is used to stabilize the domain wall at an intermediate position within the domain wall strip [22]. Recent experiments demonstrate that the steady Domain Wall Motion (DWM) can be induced using current injection along the magnetic nano-strip [13], [23]. For example, in Figure 2, when the electrons are injected into T1 or T2, they become spin-polarized and exert a Spin-Transfer Torque on the domain wall. If STT is large enough to overcome the pinning field, it leads to steady domain wall motion (towards T1 in this case). The authors in [13] demonstrate steady domain wall motion critical current density of $\sim 6 \times 10^{11}$ A/m^2 and ~ 60 m/s domain wall velocity for 20 nm-wide magnetic nano-strips. In general, the application of current induced domain wall motion faces the problem of stable control due to domain wall structural change, bidirectional displacements, thermal effect of Joule heating, stochastic nature and the intrinsic pinning effect [24]–[26]. The reduction of critical current density to depin domain wall from a pinning site can largely solve those problems. A small domain wall motion critical current density in the range of 10^{11} A/m^2 was demonstrated experimentally in a scaled magnetic nano-strip with Perpendicular Magnetic Anisotropy (PMA) [13]. The relative smaller critical current density of scaled PMA device comes from smaller domain wall length and lower hard-axis anisotropy [24], [26]. In this work, the domain wall strip dimension $L_{DWS} \times W_{DWS} \times t_{DWS}$ of SWD, shown in Figure 2, is $100 \times 20 \times 2$ nm^3 respectively. A Neel type DW is formed

TABLE 1. SWD and STD device parameters.

Symbol	Quantity	Value
α	Damping coefficient	0.02
K_u	Uniaxial anisotropy	3.5×10^5 J/m^3
M_s	Saturation magnetization	6.8×10^5 A/m
A_ex	Exchange stiffness	1.1×10^{-11} J/m
P	Polarization	0.6
t_{MgO}	MgO thickness of SWD	1.1 nm
$(L \cdot W \cdot t)_{DWS,swd}$	DWS dimension of SWD	$100 \times 20 \times 2$ nm^3
$(L \cdot W)_{MTJ,swd}$	MTJ dimension of SWD	100×20 nm^2
$(L \cdot W \cdot t)_{DWS,std}$	DWS dimension of STD	$50 \times 20 \times 2$ nm^3
$(L \cdot W)_{DWS,std}$	MTJ dimension of STD	20×20 nm^2
$(L \cdot W \cdot t)_{sta}$	stabilizer dimension	$10 \times 20 \times 4$ nm^3

because of the small strip width (20 nm) [16]. The domain wall length is ~ 17 nm, derived from $L_{DW} = \pi\sqrt{A_{ex}/K_u}$ based on our device parameters listed in Table 1.

The SWD device can be treated as a four-terminal device with lateral and vertical current paths. For the lateral path (T1 to T2, $\pm x$ direction), T1 forms the input programming port, assuming T2 is supplied with a constant voltage. The domain wall can be moved along the x-axis depending on the lateral current pulse magnitude, direction and duration [13], [23], leading to a continuous resistance/conductance change of the MTJ in the vertical direction. The transient micromagnetic simulation plot of the domain wall motion implemented in OOMMF [27] is shown in Figure 2, where a 0.5 ns current pulse with magnitude of 8.5×10^{11}A/m^2 is applied from T1 to T2. It can be seen that domain wall moves to the left (along the direction of electron flow) with a speed of ~ 50 m/s. The magnetization dynamics of domain wall strip are simulated based on Landau-Lifshitz-Gilbert (LLG) equation with current induced STT, which will be explained in details in Section IV-A. The device parameters used in the simulation are listed in Table 1. We benchmarked the micromagnetic simulation with the experimental data in [13] (the same nano-strip width of 20 nm is fabricated) and it shows a good match as shown in Figure 3(a).

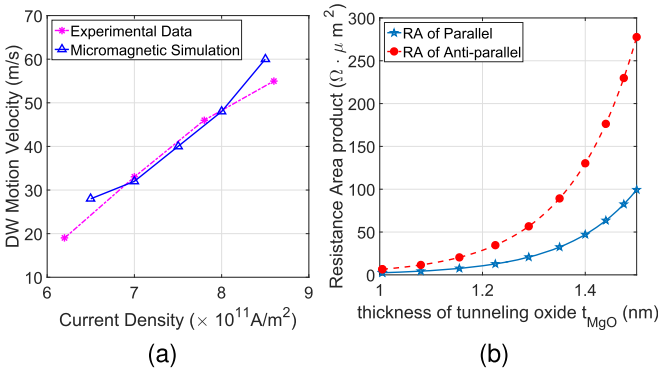

FIGURE 3. (a) Simulated domain wall motion velocity versus lateral current density, showing a good match with experimental data reported in [13]. (b) Resistance-area product versus the thickness of tunneling oxide in AP and P state (with constant voltage of 50 mV).

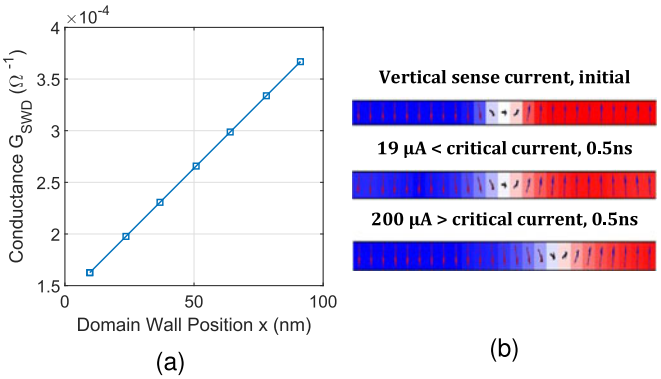

FIGURE 4. (a) SWD conductance versus domain wall position in the domain wall strip (b) micromagnetic simulation of SWD domain wall strip with different vertical sense current.

The vertical path (from T3 to T4, z direction) is used for sensing the position of domain wall in terms of MTJ vertical conductance. The MTJ conductance is a function of voltage, tunneling oxide thickness (t_{MgO}) and the angle between domain wall strip and fixed layer magnetization. The atomistic level simulation framework based on Non-Equilibrium Greens Function (NEGF) formalism [28] is used to evaluate the MTJ resistance, which will be explained in Section IV-A. In order to simulate the device with CMOS interface circuits in HSPICE, as shown in Figure 2(c), SWD is modeled as three parallel MTJs with variable conductance depending on domain wall positions which can be described as

$$G_L(x) = (W_{DWS} \times (L_{DWS} - x - 0.5 \cdot L_{DW}))/RA_{AP} \quad (1)$$

$$G_R(x) = (W_{DWS} \times (x - 0.5 \cdot L_{DW}))/RA_P \quad (2)$$

$$G_{DW} = (W_{DWS} \times L_{DW})/RA_{DW}, \quad (3)$$

where, G_L, G_{DW} and G_R are respectively the vertical conductance of left anti-parallel, domain wall and right parallel equivalent MTJ conductance; x is domain wall position (midpoint), L_{DW} is the domain wall length, RA_{AP}, RA_{DW} and RA_P are respectively MTJ Resistance-Area product (RA) for anti-parallel, DW and parallel configurations obtained in the NEGF-based MTJ model [28]. Figure 3(b) shows the MTJ Resistance-Area (RA) product versus MgO thickness in Anti-Parallel (AP) and Parallel (P) state (with constant voltage of 50 mV). It shows that RA exponentially increases with the increase of tunnel oxide thickness (with the device parameters listed in Table 1). The optimization of MgO thickness will be discussed in following section. The conductance of the SWD can then be computed as

$$G_{SWD} = G_L + G_{DW} + G_R. \quad (4)$$

Figure 4(a) shows the SWD conductance is linearly proportional to the domain wall positions in the domain wall strip (with $t_{MgO} = 1.1$ nm). Thus, this device can be employed as weights at the inputs of a TLG by programming to a specific conductance. Based on our micromagnetic simulation, the conductance of SWD can be programmed from minimum to maximum using a $30\,\mu\text{A} - 2$ ns current pulse, which leads to low reconfiguration energy of TLG design with spintronic devices.

The authors in [21] have experimentally shown that the vertical current may also shift domain wall when the current density is above a critical value because of the out-of-plane (field-like) STT. Domain wall position displacement is what we want to avoid in this design due to that domain wall position essentially encodes the weight (i.e., SWD conductance) of a TLG. Based on the micromagnetic simulation for vertical current injection, the vertical critical current density to depin the domain wall was found to be $\sim 5 \times 10^{10}$ A/m^2 (equivalent current as $\sim 100\,\mu$A), which is close to experimental results in [21]. Thus, the largest allowed voltage difference across the SWD in the vertical direction is ~ 260 mV. In order to keep a good amount of sensing margin, such sense voltage is set to be ~ 50 mV (explained later in Section III-A), which corresponds to a maximum of $\sim 19\,\mu$A vertical sensing current. From the micromagnetic simulation shown in Figure 4(b), the domain wall position is stable when the vertical sensing current is $19\,\mu$A, while it is not when the applied current is $200\,\mu$A that is larger than the critical current.

B. SPINTRONIC THRESHOLD DEVICE

In this section we present a Spintronic Threshold Device based on magnetic domain wall strip. Such STD design will serve as the third step of a TLG, which is a thresholding function.

The device structure for the STD is shown in Figure 5(a). As the device dimension stated in Table 1, it constitutes of a thin (2 nm) and short (50 nm) magnetic domain wall strip connecting two anti-parallel fixed magnetic domains. The magnetization of domain wall strip can be written anti-parallel to the fixed layer by injecting a current (larger than critical current) along it from T1 to T2 and vice verse [10], [13]. A fixed small magnet and domain wall strip beneath it form a MTJ to sense the magnetization of domain wall strip. Unlike in SWD, the fixed layer of sense MTJ in STD is very small (20 nm × 20 nm). The resistance states are binary, i.e., either high (AP) or low (P). Thus, the STD can detect the polarity of current flow at its input node, acting as an ultra-low voltage and compact current comparator that can be employed in the design of current-mode TLG.

The threshold of STD, i.e., the minimum current magnitude required to switch the domain wall strip magnetization (move domain wall from one end to the other end), is determined by the critical current density and domain wall velocity. Based on our micromagnetic simulation and device dimension as shown in Figure 5(b) and Table 1, the STD intrinsic threshold (I_{th}) is $\sim 30\,\mu$A for 1 ns switching, corresponding to domain wall velocity of ~ 50 m/s. Figure 5(e) describes domain wall strip magnetization switch corresponding to the applied current pulse (1 ns). A hysteresis can be observed due to domain wall motion critical current density. In this work, a reset operation is required to relocate the

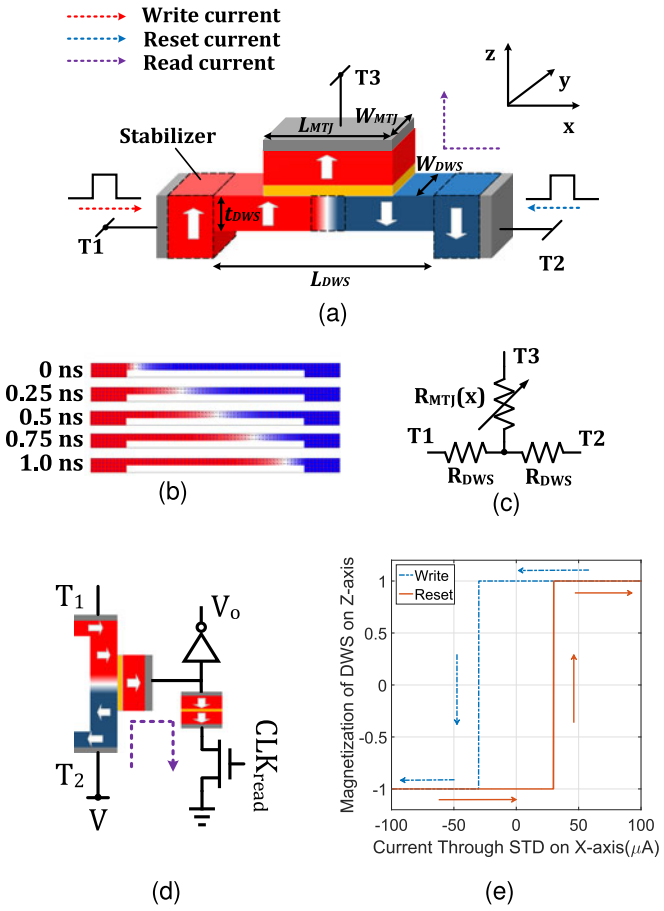

FIGURE 5. (a) Spintronic threshold device structure. (b) Micro-magnetic simulation result of domain wall motion with 30 μA input current. (c) Behavior SPICE model of STD. (d) STD sense circuit. (e) STD transfer function of write and reset.

domain wall to T2 side. Recently, application of spin orbital coupling has been explored for reducing the critical current and increasing domain wall motion velocity [29], [30]. The threshold current can be further reduced to less than 10 μA.

The effective resistance of the MTJ formed between domain wall strip and fixed layer (T3 side) is smaller when they have the same magnetization and vice verse. The ratio of two resistances is defined in terms of Tunneling Magneto Resistance ratio (TMR). As shown in Figure 5(d), STD forms a voltage divider with a fixed reference MTJ to sense the resistance state. Static current in the voltage divider can be minimized by increasing the MTJ oxide thickness. For 1 ns clock cycle, the oxide thickness in this work is chosen to be 1.5 nm that results in a total power dissipation of $\sim 1\,\mu$W for the sensing circuit (including the clocking power). The sense current can be further reduced to less than 1 μA by increasing the oxide thickness [10]. Note that in the detection circuit, the transient current with short duration (1 ns) and low magnitude ($\sim 2\,\mu$A) flows from T2 to T3, which will not disturb the domain wall position.

In summary, the circuit in Figure 5(d) can implement a compact current mode thresholding function in TLG design. Next, we will describe circuit design for combining the SWD and STD to implement an ultra-low power reconfigurable spintronic threshold logic gate.

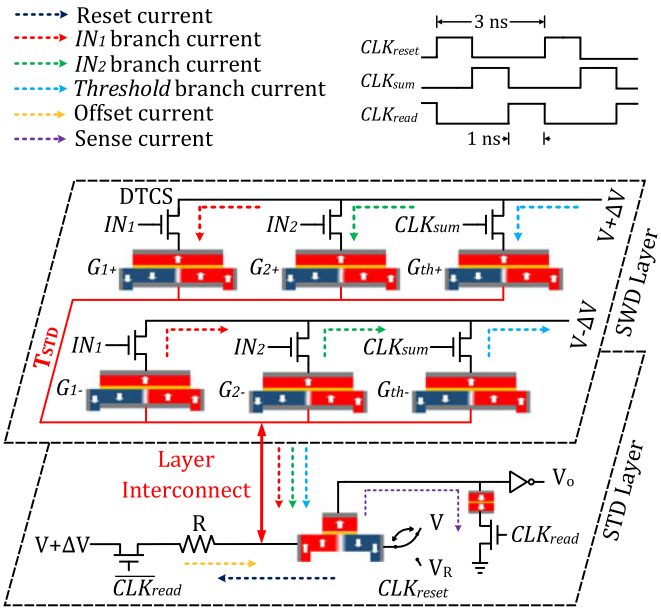

FIGURE 6. Schematic representation of a two fan-in Threshold Logic Gate (TLG) and clock timing diagram.

III. SPINTRONIC THRESHOLD LOGIC GATE AND RECONFIGURATION CIRCUIT

In this section, we explain the circuit realization of Spintronic Threshold Logic Gate and the corresponding reconfiguration circuit. Our proposed STLG can be divided into SWD layer, layer interconnect and STD layer, which accomplishes weighing, summation and thresholding operations respectively. SWD is evenly distributed as an array on the SWD layer. We propose a reconfiguration circuit to achieve precise domain wall relocation. A two fan-in STLG is taken as an example to clarify the design. Larger number of fan-ins can also be implemented using the same principle which is analyzed in Sections IV-A and V.

A. SPINTRONIC THRESHOLD LOGIC GATE

Figure 6 depicts the circuit realization of a single STLG. In order to realize large scale Spintronic Threshold Logic Network and for the convenience of SWD reconfiguration, the STLG is designed as multilayer arrays (SWD layer and STD layer) with layer interconnect. The SWD layer is employed to perform current-mode weighting function of binary inputs (first step of STLG). Then the interconnect across SWD and STD layers implements the current summation (second step). Finally, the low voltage fast switching STD layer carries out the thresholding operation (third step) in an energy efficient manner.

In SWD layer, SWD conductance can be configured to a specific value (corresponding resistance values are listed in Table 3) for different Boolean functions. Since the weights and threshold of a TLG can be either positive or negative, two SWDs are combined as one *weight unit* to represent one

weight value. In order to have a precise control of domain wall pinning/depinning operation and good thermal stability, N_{level} number of artificial trapping necks (such as notches) could be manufactured within the magnetic domain wall strip to obtain N_{level} discrete SWD vertical conductance levels [31]. We define ΔG as the SWD vertical conductance difference when domain wall moves to the next neighboring trapping sites. Thus the conductance of SWD can be expressed as

$$G_{SWD} = G_{min} + k \times \Delta G, \quad k \in [0, N_{level} - 1], \tag{5}$$

where G_{min} is the minimum conductance of SWD, and k is an integer. For a two fan-in STLG shown in Figure 6, the conductance difference of two SWDs (G_{i+} and G_{i-}) in the same column jointly represent the corresponding weight (W_i) of input-i (IN_i), which is $W_i = (G_{i+} - G_{i-})/\Delta G$ mathematically. In this case, weight unit can be configured to positive ($G_{i+} > G_{i-}$), negative ($G_{i+} < G_{i-}$) or zero ($G_{i+} = G_{i-}$). Note that, the SWDs in the most right column are combined as the weight unit (W_{th}) for threshold value θ in TLG expression (Figure 1). We define $W_{th} = -\theta$ and the TLG function is rewritten as

$$V_o = sign\left(\sum_{1}^{n} IN_i \cdot W_i + CLK_{sum} \cdot W_{th}\right), \tag{6}$$

where IN_i is binary signal, and the clock signal (CLK_{sum}) is always high during the computation of STLG. Next, we will map this mathematical expression into our proposed STLG circuit.

The proposed TLG is controlled by a three-phase (CLK_{reset}, CLK_{sum}, and CLK_{read}) Clock with 3 ns period, and each phase is 1 ns (Timing diagram of clock signals are shown in in Figure 6). Although a TLG operation can be separated into weighting, summation and thresholding, in the circuit, all these three steps are accomplished in computation phase (CLK_{sum}). STD reset and driving the next stage STLG operations are completed during reset phase (CLK_{reset}) and read phase (CLK_{read}) respectively. For this section, we only focus on the computation phase of STLG (CLK_{sum}), while other phases will be discussed in Section IV-B.

During the computation phase, the input signal (IN_i) is received through CMOS transistors that act as Deep Triode region Current Sources (DTCS) [10]. The source terminals of DTCS are wired to a potential of $V + \Delta V$ for positive SWD (G_{i+} and G_{th+}), and $V - \Delta V$ for negative SWD (G_{i-} and G_{th-}), where ΔV can be ~ 50 mV. As shown in Figure 6, the RHS of STD is connected to DC voltage V, when CLK_{reset} is low. The static current therefore flows across a small terminal voltage of ΔV, resulting in small static power consumption. Moreover, the dynamic power dissipation is enormously reduced due to ultra-small voltage swing as well. Due to the small resistance of magneto metallic STD and DTCS, the current contributed by each weigh unit is approximated to be $IN_i \cdot \Delta V \cdot (G_{i+} - G_{i-})$. The current out of each weight unit can be either positive ($G_{i+} > G_{i-}$ & $IN_i = 1$), negative ($G_{i+} < G_{i-}$ & $IN_i = 1$) or zero ($G_{i+} = G_{i-}$ or $IN_i = 0$). Thus the positive or negative weights of each input is encoded as the conductance difference of G_{i+} and G_{i-}. Moreover, an additional offset current (I_{offset}) is required for the weighted summation current to overcome the STD intrinsic threshold (explained in Section II-B). Hence, the total current through STD (I_{STD}) and the output of STD sense circuit can be expressed as

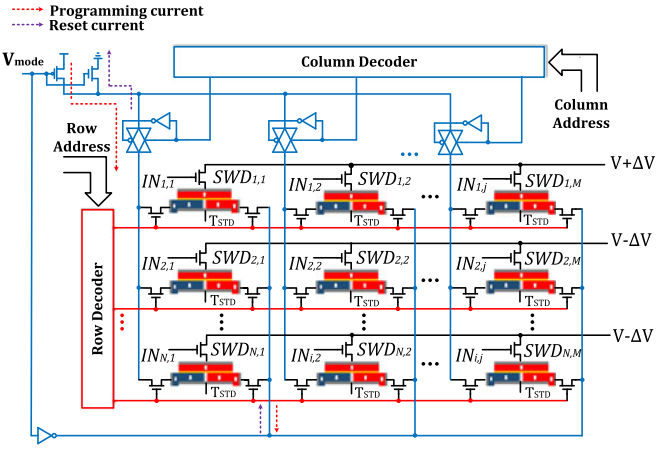

FIGURE 7. The configuration circuit for SWD array layer. Row and Column decoder used to choose specific SWD device. V_{mode} is used to switch between configuration and reset operation.

$$I_{STD} = \left(\sum_{1}^{n} IN_i \cdot \Delta V \cdot (G_{i+} - G_{i-}) + \Delta V \cdot (G_{th+} - G_{th-})\right) + I_{offset} \tag{7}$$

$$V_o = \begin{cases} 1, & I_{STD} \geq I_{th} \\ 0, & I_{STD} < I_{th} \end{cases}, \tag{8}$$

where I_{offset} equals to the STD intrinsic threshold (I_{th}). When the I_{STD} is no less than the threshold, which displaces the domain wall from RHS to LHS, STD sense circuit outputs 1, otherwise it outputs 0. The output (V_o) of STD sense circuit associated with each TLG, in turn, drives the fan-out of STLG. Due to the non-volatility of STD, the proposed STLG design can be easily extended to realize a pipelined architecture without inserting CMOS latches, which will be discussed in Section V.

B. WEIGHT AND THRESHOLD RECONFIGURATION CIRCUIT

In order to realize the reconfiguration of STLG, we also propose a weight and threshold reconfiguration circuit, which is shown in Figure 7. SWDs are evenly distributed on the SWD layer as an $N \times M$ dimension array. The configuration circuit is shared by the entire SWD layer through using row and column decoders to program a specific SWD. For instance, in order to configure $SWD_{i,j}$, the column and row decoders are fed with row address i and column address j. A mode selection signal (V_{mode}) is used to switch between configuration and reset. The reconfiguration circuit start programming $SWD_{i,j}$ in the following sequence. First, V_{mode} is set to low

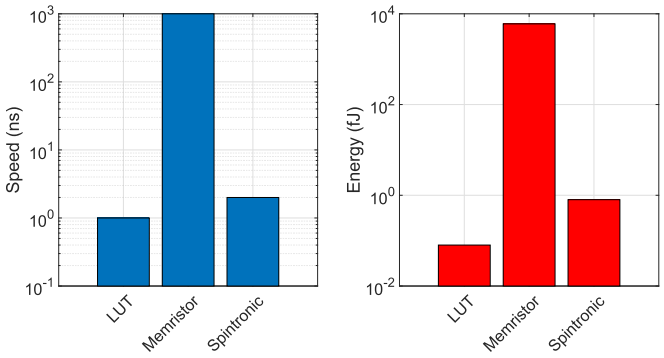

FIGURE 8. The configuration speed and energy dissipation for LUT, memristor and spintronic device.

(reset mode) and a reset current follows through SWD and replace the domain wall back to initial position. Next, V_{mode} is set to high (configuration mode) to program the domain wall to specific position with corresponding pulse width.

Compared with MTL [4], [9], programming the SWD conductance is much more energy efficient and faster, which greatly reduces the energy consumption of SWD array reconfiguration. In this work, we define the reconfiguration energy as the averaged energy of programming the weight from minimum to maximum and from maximum to minimum. For LUT based TLG, it is the averaged energy of writing 0 and 1. For Ag-Ch memristor, authors in [9] used 0.3 V $\sim 1\,\mu$s and 0.6 V $\sim 1\,\mu$s voltage pulses to program memristance between 10 to 100 KΩ. While in spintronic weight device, a $30\,\mu$A ~ 2 ns current pulse can move the DW from one end to the other, thus programming the weight from minimum to maximum, vice verse. Figure 8 presents the reconfiguration speed and energy consumption of LUT, memristor (Ag-Ch [9]) and SWD. It can be seen that the CMOS LUT consumes least energy and has the fastest programming speed. SWD reconfiguration energy and delay are slightly larger than CMOS LUT, however, it is almost three orders lower in energy consumption and three orders faster in programming speed compared with memristor (Ag-Ch).

IV. SIMULATION FRAMEWORK AND RESULT

In order to evaluate the performance of the proposed STLG, we come up with a simulation framework as shown in Figure 9. The bottom to up simulation framework can be divided into device level, circuit level and logic synthesis & architecture level. For device level simulation, we benchmark the domain wall motion dynamics with experimental data [13] utilizing Object Oriented MicroMagnetic Framework (OOMMF) [27]. The MTJ (constituted of domain wall strip, tunneling oxide layer and fixed ferromagnetic layer) is modeled in Verilog-A, using NEGF-LLG solution for spin to charge interface. For the circuit level simulation, 45 nm North Carolina State University (NCSU) Product Development Kit (PDK) library [32] is used in SPICE to verify the proposed design, and acquire the performance (Energy dissipation and defect tolerance)

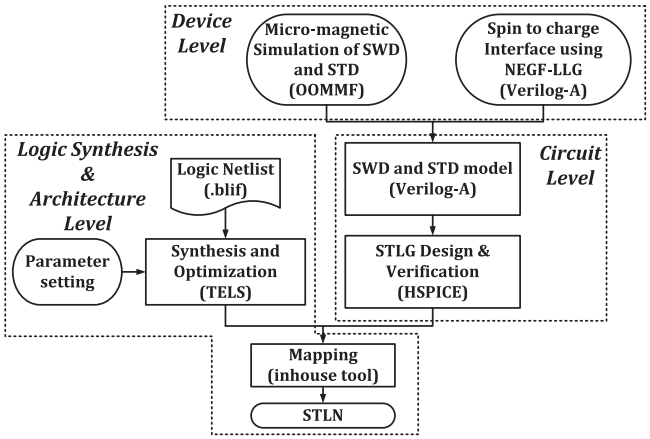

FIGURE 9. The simulation framework for proposed STLG.

of STLG. Furthermore, we take the advantage of TELS [33][1] to implement the logic synthesis, which generates the threshold logic netlists with corresponding weight and threshold values from any input logic functions. Different parameters can be set during the logic synthesis, such as fan-in restriction and defect tolerance. Subsequently, the synthesized threshold logic network (TLN) are mapped to our spintronic TLN by configuring the corresponding SWD conductance values. The details of each level are given in the following sections respectively.

A. DEVICE LEVEL

The magnetization dynamics $\vec{m}$ of domain wall strip are simulated by solving the Landau-Lifshitz-Gilbert (LLG) equation with current induced spin-transfer torque as shown below [3]

$$\frac{\partial \vec{m}}{\partial t} = -|\gamma|(\vec{m} \times \vec{H}_{eff}) - \alpha\left(\vec{m} \times \frac{\partial \vec{m}}{\partial t}\right) - \frac{I_s}{qN_{sx}}\frac{\partial \vec{m}}{\partial x} + \xi\frac{I_s}{qN_{sx}}\vec{m} \times \frac{\partial \vec{m}}{\partial x}, \tag{9}$$

where $\vec{H}_{eff}$ is the effective magnetic field, and α is Gilbert's damping coefficient. $N_{sx} = M_s A/\mu_B$ is the number of spins per domain along the x-direction with A is the cross-sectional area through which current flows, M_s is saturation magnetization, and μ_B is Bohr magneton. Also, the spin polarized current $I_s = PI$, where P is the spin polarization of the conduction electrons. The first two terms are the usual precession and damping terms. The third term describes the local tracking of conduction electrons to local magnetization (adiabatic torque) and the forth term is a phenomenological non-adiabatic spin-transfer term whose strength is described by ξ. Based on the device parameters shown in Table 1, the micromagnetic simulation result shown in Figure 3(a) illustrates a good match with experimental data.

[1]The ThrEshold Logic Synthesizer (TELS) can be download from NANOHUB at https://nanohub.org/resources/3353.

TABLE 2. Weight of Boolean functions.

Function	Weight				Function	Weight			
	A	B	C	Threshold		A	B	C	Threshold
AB	2	2	-	−3	A+B	2	2	-	−1
ABC	1	1	1	−3	A+B+C	1	1	1	−1
AB+BC+CA	1	1	1	−2	A+BC	2	1	1	−2
AB+AC	2	1	1	−3					

As previously shown in Figure 3(b), the MTJ Resistance-Area product versus t_{MgO} curve is obtained based on an experiment benchmarked NEGF compact model from [34], [35]

$$RA_{MTJ,AP/P} = A/(e^{c_1 t_{MgO}+c_2} V_{MTJ}^2 + e^{c_3 t_{MgO}+c_4}), \qquad (10)$$

where A is the cross-sectional area of tunneling oxide, V_{MTJ} is the voltage applied on the fixed layer and domain wall strip of SWD. $c_{1\sim4}$ are fitting constants, which are different for anti-parallel and parallel state. The obtained MTJ resistance-area product values for anti-parallel and parallel states are used to model SWD and STD in our verilog-A circuit model described in earlier section.

B. CIRCUIT LEVEL

In this section, we discuss circuit level simulation results and performance of the proposed STLG. Besides, the performance comparison with other TLG implementations, such as CMOS LUT, CTL and MTL [4] is also presented. In this work, we use 45 nm NCSU PDK to evaluate our STLG in SPICE circuit simulation environment.

Any Boolean function can be implemented using a single TLG or Threshold Logic Network (TLN) by reconfiguring their weights, thresholds or both. In this section, several two fan-in and three fan-in linearly separable Boolean functions [36] are employed to demonstrate the functionality and performance of the proposed design. Large scale benchmarks (ISCAS-85) will be discussed in next section. Table 2 lists few samples of TLG Boolean functions with their mathematical weights and threshold. As we discussed in Section III-A, the weight of threshold is the negative value of threshold ($W_{th} = -\theta$). For example, an AND Boolean function ($F = A \cdot B$) can be implemented using a single TLG with (2, 2) as input weights and three as threshold. The same circuit can also implement an OR Boolean function (A+B) by just reconfiguring the threshold to 1 as shown in Table 2. From Table 2, it can be seen that only three discrete levels are required for the weights and threshold values. Since the weight W_i is encoded as $(G_{i+} - G_{i-})/\Delta G$ in our proposed design, four discrete conductance levels of SWD are sufficient in this application.

Table 3 lists the corresponding SWD resistance configurations for Boolean functions listed in Table 2, which are used in HSPICE simulation. Figure 10 depicts the transient simulation result of STLG implementing two-input AND and OR Boolean functions. A three-phase (CLK_{reset}, CLK_{sum} and CLK_{read}) clock with 3 ns period is used in the circuit simulation. The first clock

TABLE 3. The corresponding SWD resistance configuration and energy of different boolean functions.

Function	A+ ($K\Omega$)	A- ($K\Omega$)	B+ ($K\Omega$)	B- ($K\Omega$)	C+ ($K\Omega$)	C- ($K\Omega$)	th+ ($K\Omega$)	th- ($K\Omega$)	Energy (fJ)
AB	3.355	6.229	3.355	6.229	-	-	6.229	2.726	6.57
A+B	3.355	6.229	3.355	6.229	-	-	6.229	4.361	6.29
ABC	4.361	6.229	4.361	6.229	4.361	6.229	6.229	2.726	6.88
A+B+C	4.361	6.229	4.361	6.229	4.361	6.229	6.229	4.361	6.61
AB+BC+CA	4.361	6.229	4.361	6.229	4.361	6.229	6.229	3.355	6.75
A+BC	3.335	6.229	4.361	6.229	4.361	6.229	6.229	3.355	6.82
AB+AC	3.335	6.229	4.361	6.229	4.361	6.229	6.229	2.726	6.95

phase CLK_{reset}, is used to reset the STD. As described in Section III-A, a reset operation is required before the weighted summation current modifying the domain wall position of STD. When the CLK_{reset} is high, the right side terminal of STD is connected to potential V_R (which is about $V + 2\Delta V$). Thus, a $-32\,\mu$A current is applied at the input terminal of STD (T_{STD}), leading to shift of domain wall to the right end of domain wall strip, where the sense MTJ of STD is in parallel state. Then, CLK_{sum} is on, the input voltages are applied onto the corresponding DTCS transistors and the net current flowing into the STD is determined by the weighted summation of inputs (discussed in Section III-A). As shown in Figure 5(e), when the interconnect current (I_{STD}) is greater than the STD intrinsic threshold current (30 μA), domain wall is moved to the LHS

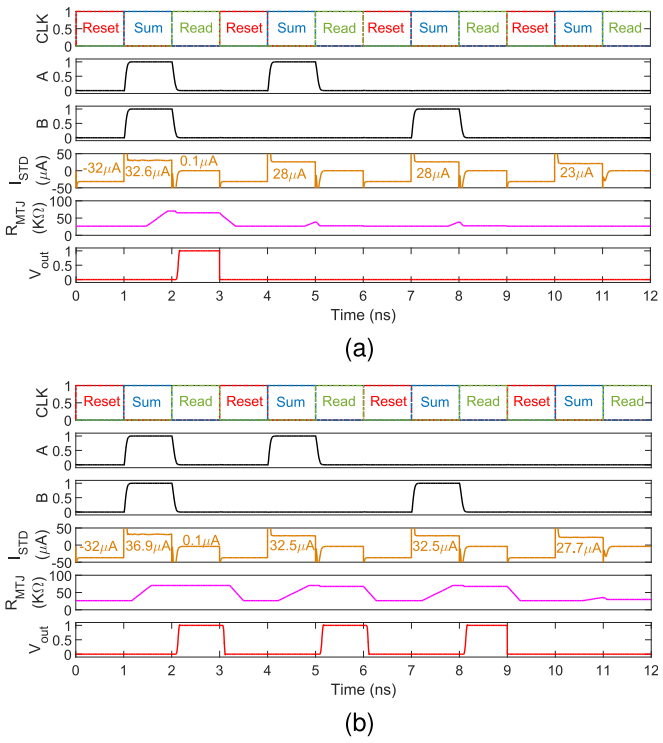

FIGURE 10. HSPICE transient simulation result of STLG implementing (a) AND and (b) OR functions. In the CLK timing diagram, red (CLK_{reset}), blue (CLK_{sum}) and green (CLK_{read}) waveform represent reset, computation and read phase respectively. When the $I_{STD} \geq 30\,\mu$A during computation phase, V_{out} outputs 1 at the following read phase, otherwise output is 0.

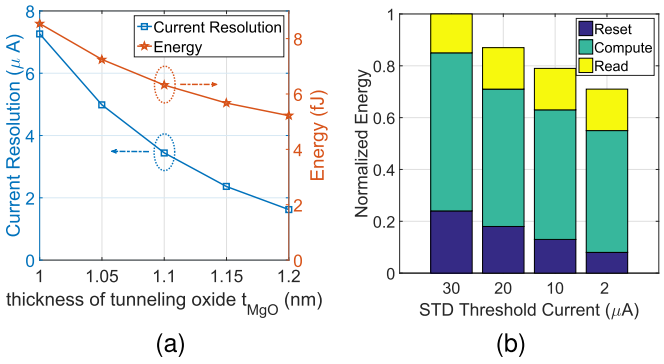

FIGURE 11. For two fan-in OR Boolean function: (a) Energy and current resolution trade-off w.r.t SWD tunnel oxide thickness, (b) normalized energy versus different STD threshold current.

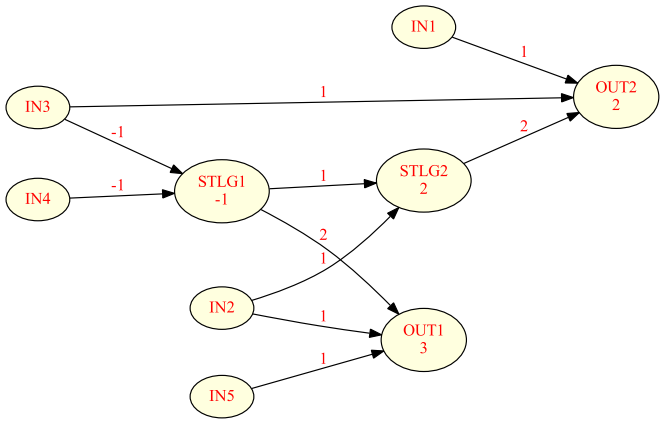

FIGURE 12. Synthesized four fan-in ISCAS-85 C17 threshold logic network.

while sense MTJ is in anti-parallel state, otherwise domain wall does not relocate and the sense MTJ remains in parallel state (initial state). For input A and B with combination values of $(11, 10, 01, 00)$, the corresponding net current flowing into STD is $(32.6, 28, 28, 23\,\mu A)$ and $(36.9, 32.5, 32.5, 27.7\,\mu A)$ for AND and OR Boolean functions respectively (also labeled in Figure 10). Since the threshold current of STD is $\sim 30\,\mu A$, it can be seen in Figure 10 that the sense MTJ resistance (R_{MTJ}) is (high, low, low, low) and (high, high, high, low) respectively. When the third phase CLK_{read} is on, the STD sense circuit read the state of MTJ and sends the binary voltage output to next TLG through an inverter.

The energy consumption of each Boolean function is also shown in Table 3. Based on the simulation, such energy consumption highly depends on the tunnel oxide thickness (t_{MgO}) of SWD under the same clock frequency. In Section III-A, we explained that the current going out of each weight unit equals to $IN_i \cdot \Delta V \cdot (G_{i+} - G_{i-})$, where V_i is binary value (0 or 1), $\Delta V = 50$ mV and $G_{i+} - G_{i-}$ represents the corresponding weight value. It can be seen that the current flowing through SWD, thus energy consumption, depends on the conductance range of SWD. Based on the NEGF-MTJ model and the simulation results shown in Figure 3(b), the conductance range is mainly determined by the tunnel oxide thickness (t_{MgO}) in an exponential manner with the same voltage (50 mV). Larger tunnel oxide thickness (i.e., smaller conductance range) is preferred for minimizing the energy consumption. However, the *current resolution* (I_{unit}), defined as the minimum current difference between different weights, is inversely proportional to the tunnel oxide thickness. It is important to maintain a relative large current resolution in TLG design to clearly identify different input current levels to STD, thus avoid the erroneous computation result. Large I_{unit} can be helpful to overcome the process variations on the circuits and improve the defect tolerance. For example, if $t_{MgO} = 1.2$ nm, the resistance-area product is $10.58\,\Omega\mu m^2$, the corresponding four SWD resistance states are $(12.26, 8.77, 6.83, 5.59)$ KΩ and the I_{unit} is $1.6\,\mu A$. If $t_{MgO} = 1.1$ nm, the resistance-area product is $5.85\,\Omega\mu m^2$, the corresponding four SWD resistance states are $(2.73, 3.34, 4.36, 6.23)$ KΩ and the I_{unit} is $3.5\,\mu A$. It can be seen that the later current resolution is $2\times$ larger with a 21 percent energy consumption increase. Figure 11(a) shows the energy and current resolution versus SWD tunneling oxide thickness for STLG implementing OR Boolean function. It is a trade-off between the current resolution (i.e., defect tolerance) and energy consumption.

The energy consumption of proposed STLG also depends on the STD threshold current. The smaller of required threshold current, the lower energy consumption of STLG as shown in Figure 11(b). It is due to the reduction of required net current from the input weights. Recently, application of spin orbital coupling has been explored for reducing the required current for a given speed of domain wall motion by an order of magnitude [29], [30]. Thus, it is possible to reduce the STD threshold current to be less than $10\,\mu A$ and further reduce the energy consumption of STLG.

C. LOGIC SYNTHESIS AND ARCHITECTURE LEVEL

The architecture level simulation framework is described in Figure 9. First of all, a logic netlist in Berkeley Logic Interchange Format (.blif) is fed into ThrEshold Logic Synthesizer (TELS) to obtain synthesized Threshold Logic Network (TLN) with weight, threshold, connection and stage information [33]. Meanwhile, parameters such as fan-in restriction and defect tolerance are set up during the synthesis. Figure 12 presents the synthesized ISCAS-85 C17 TLN as an example. The nodes without inputs are primary input (PI) nodes, and each node (expect PI) represents one TLG. The connections between two nodes are fan-ins and fan-outs. The numbers labeled on the connections are weights, and threshold weight is labeled inside the node. Moreover, the nodes in the same column are of one stage, whereas the column only consists of PIs does not count as one stage. All the STLGs in same stage are operating synchronously. In this work, any Boolean function can be synthesized into threshold logic network and further implemented by our proposed spintronic threshold logic network through configuring the spintronic weight device conductance. An inhouse mapping tool, as described in Algorithm 1, takes the synthesized threshold logic network netlist generated from TELS [33] as input and maps to our proposed spintronic threshold logic network circuits. This

process mainly involves mapping weights $W_{i,j,k}$ to the corresponding conductance values $G_{i,j,k}+$ and $G_{i,j,k}-$ of spintronic weight devices with mapping algorithm described in Algorithm 1. Performance metrics of spintronic threshold logic gate are extracted from circuit level simulation in HSPICE in Section IV-B. The performance of mapped STLN is introduced in the next section.

Algorithm 1. Spintronic Weight Device Mapping Algorithm for Spintronic Threshold Logic Network

Input: $W_{i,j,k} \leftarrow$ weight value of ith input for threshold logic gate j in stage k (Extracted from TELS output file);
$SWD_{min}, SWD_{max} \leftarrow$ Indicating the conductance range of SWD;

Output: $G_{i,j,k}+, G_{i,j,k}- \leftarrow$ conductance values of SWDs corresponding to $W_{i,j,k}$;
Initialisation :
$W_{max} \leftarrow$ find the maximum value of $W_{i,j,k}$;
$N_{level} = W_{max} + 1 \leftarrow$ Number of conductance levels of SWD;
$\Delta G = (SWD_{max} - SWD_{min})/(N_{level} - 1) \leftarrow$ conductance step length;
LOOP Process
for Each threshold logic gate **do**
  if $W_{i,j,k} > 0$ **then**
    $G_{i,j,k}+ = SWD_{min} + W_{i,j,k} \cdot \Delta G$;
    $G_{i,k,k}- = SWD_{min}$;
  else if $W_{i,j,k} < 0$ **then**
    $G_{i,j,k}+ = SWD_{min}$;
    $G_{i,j,k}- = SWD_{min} + |W_{i,j,k}| \cdot \Delta G$;
  end if
end for
return $G_{i,j,k}+, G_{i,j,k}-$

V. PERFORMANCE ANALYSIS AND OPTIMIZATION OF SPINTRONIC THRESHOLD LOGIC NETWORK

A. DEFECT TOLERANCE

Different from the memristance drift phenomenon occurred in MTL [4], the conductance of SWD will not drift during computation of STLG, since the vertical current through SWD is much smaller than the domain wall displacement critical current. Moreover, the artificial trapping neck [31] is also designed into the SWD to further enhance the stability of domain wall strip. Nevertheless, the process variation of SWDs might disturb the functionality of STLG, which comes from the edge roughness of magnetic nano-strip and the thickness variations of tunneling oxide (MgO) [37]. The thickness variation of t_{MgO} leads to the deviation of Resistance-Area product of SWD, and magnetic nano-strip shape variation causes area variation between SWDs. Both of them result in the conductance variation of SWDs, which might cause erroneous STLG outputs.

As the mathematical expression of TLG described in equation (7), the output of STLG is 1 when the current summation

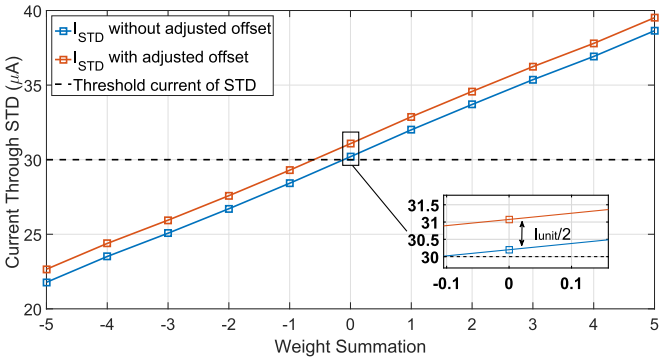

FIGURE 13. Current through STD (I_{STD}) versus weighted summation of STLG's inputs. A four fan-in STLG with SWD of five levels is used as example here. Offset current is shifted by $I_{unit}/2$ to improve the defect tolerance.

(I_{STD}) is larger than or equivalent to STD's intrinsic threshold. It has a much higher probability to detect an erroneous output when the weighted summation current is equal or close to the threshold current due to device variation or noise. A countermeasure to increase variation and noise tolerance near threshold is introduced in TELS synthesis tool[33] by modifying the threshold during the synthesis as shown below

$$Y = \begin{cases} 1, & if \ \sum_i^n IN_i \cdot W_i - \theta \geq \delta_{on} \\ 0, & if \ \sum_i^n IN_i \cdot W_i - \theta \leq -\delta_{off} \end{cases}, \qquad (11)$$

where δ_{on} and δ_{off} is default to be 0 and 1 respectively. By setting δ_{on} and δ_{off} to be positive numbers, it avoids the cases that the weighted summation is equal or close to the threshold during synthesis, thus achieving better defect tolerance. Ideally, better defect tolerance is expected by increasing the δ_{on} and δ_{off} values. However, based on our simulation, it will also largely increase the required number of conductance levels (N_{level}) of SWD and the total number of STLGs for the same logic function, which reduces the current resolution and increases the total energy. In this work, we use the default δ_{on} and δ_{off} values during synthesis, but employ a circuit technique to increase the defect tolerance. As shown in Figure 13, the offset current is increased by half current resolution ($I_{unit}/2$). It is equivalent to set both δ_{on} and δ_{off} to be 0.5, which can not be done in logic synthesis. Shifting the offset current avoids the cases that the weighted summation current is close to threshold, which guarantee at least half of current resolution as a noise margin. The detailed variation analysis employing such technique is discussed later by Monte Carlo simulation.

The average Error Rate (ER) is related to current resolution, weight configuration (different Boolean functions), input value and number of fan-ins. In order to evaluate the ER for different Boolean functions listed in Table 2, we run a Monte Carlo simulation with a Gaussian distributed variation ($3\sigma = 0\% \sim 70\%$) added on SWD conductance. Twenty equidistant samples of conductance variation between 0 and 70 percent are chosen, and for each variation sample we run 2,000 times with all possible input combinations. The simulation result is shown in Figure 14. It can be seen that no

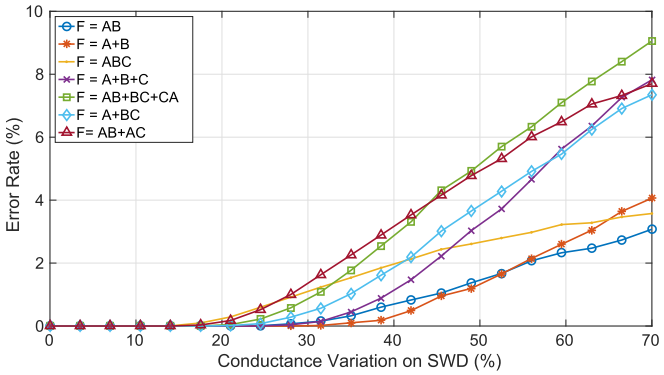

FIGURE 14. The average Error Rate (ER) of different Boolean functions versus conductance variation of SWD.

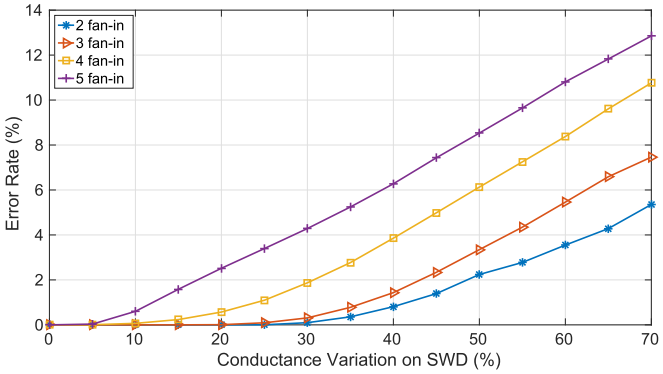

FIGURE 15. The average Error Rate (ER) of different number of fan-ins versus conductance variation of SWD for ISCAS-85 C432 STLN.

errors are observed if the conductance variation is smaller than 20 percent and the average ER of different Boolean functions increases with larger SWD conductance variation. As explained earlier, when the computed I_{STD} is closer to the STD intrinsic threshold, it is easier to detect an erroneous output. For instance, both $F = ABC$ and $F = AB + BC + CA$ are implemented by three fan-in STLG, whose current resolution is same. The ratio of weighted summation is 0 or -1 of eight input combinations ($000 \sim 111$) are 50 and 75 percent for $F = ABC$ and $F = AB + BC + CA$ respectively. Thus, the average ER of $F = AB + BC + CA$ is higher than the average ER of $F = ABC$.

The STLN with higher fan-in number is demonstrated to be less variation tolerant as shown in Figure 15. Note that, when using the default σ_{on} and σ_{off}, N_{level} of different fan-in restricted (2, 3, 4 and 5 fan-ins) STLN is (3, 4, 5 and 6) respectively. As shown in the figure, the average error rates of two fan-in and three fan-in restricted STLN are almost zero until the maximum possible conductance variation is 30 percent, which shows better defect tolerance than higher fan-in number STLN. Since current resolution I_{unit} is inversely proportional to the number of SWD conductance levels (N_{level}), smaller fan-in restriction has better defect tolerance.

The thermal noise of components are mainly contributed by the transistors at input terminals and the STD because of their small resistance value. The circuit level thermal noise can be described by $\bar{I_n^2} = 4KTf/R$ [38], where K is the Boltzmann constant, which is 1.38×10^{-23} J/K, R is the resistance of component and f is the frequency of STLG, which is 1/3 GHz in our design. Thus, the root mean square of noise current I_{rms} (σ) at STD is about 0.43 μA at $T = 300$ K in a four fan-in STLG. For the I_{STD} curve with adjusted offset shown in Figure 13, when the weighted summation is 0 or -1 (close to the threshold boundary), the margin between I_{STD} and threshold current ($\sim 1\ \mu$A) is about $2 \times I_{rms}$, the corresponding output Error Rate is 4.6 percent [39]. Choosing smaller N_{level}, thus larger current resolution, will avoid erroneous output from thermal noise as well. For example, I_{unit} is 2.8 μA when N_{level} is 4, where the margin between I_{STD} and threshold current is about $3.3 \times I_{rms}$, the corresponding ER is further reduced to 0.10 percent.

B. DELAY

The network delay comparison of ISCAS-85 benchmarks using LUT, CTL, MTL and STLG are listed in the Table 4. The delay of STLG is calculated as $t_{reset} + N_{stage} \times t_{sum} + t_{read}$, where t_{reset}, t_{sum}, and t_{read} are the pulse width (1 ns) of reset clock, computation clock and read clock respectively. N_{stage} is the number of stages of STLN. As shown in the Table 4, delay of benchmarks using STLG is about 4$\times$ better than CTL, similar as MTL, but worse than LUT method.

TABLE 4. Delay of ISCAS-85 benchmarks, and comparison between four Fan-In LUT, CTL, MTL and STLG.

Benchmark	LUT (ns) [4]	CTL (ns) [4]	MTL (ns) [4]	STLG (ns)		with pipeline Reduction over (%)		
				without pipeline	with pipeline	LUT	CTL	MTL
C17	1.05	9.47	2.99	5	3	−185.71	68.32	−0.33
C432	10.1	114	20.23	17	3	70.30	97.37	85.17
C499	8.18	110.1	13.90	15	3	63.33	97.28	78.42
C880	8.4	109.02	15.28	19	3	64.29	97.25	80.37
C1355	9.95	102.96	17.33	22	3	69.85	97.09	82.69
C1908	11.55	138.74	21.42	26	3	74.03	97.84	85.99
C2670	6.93	82.43	12.30	21	3	56.71	96.36	75.61
C3540	15.25	188.52	25.95	31	3	80.33	98.41	88.44
C5315	13.93	150.51	24.32	24	3	78.46	98.01	87.66
C6288	62.4	356.53	105.03	118	3	95.19	99.16	97.14
C7552	12.68	273.91	21.88	31	3	76.34	98.90	86.29

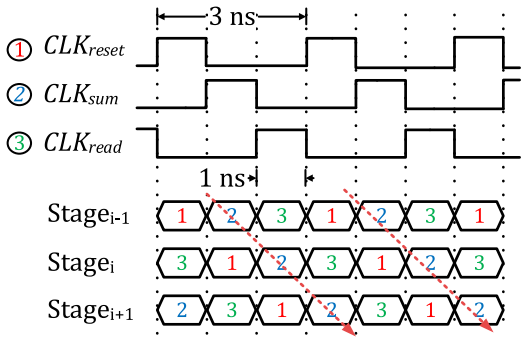

FIGURE 16. **Timing diagram for STLN with pipelining technique.**

For the sake of achieving faster speed and higher throughput, STLN can be designed using pipeline technique, which is described in the Figure 16. Without any additional clock control circuit, the fully pipelined design can be realized by alternately apply three clock signals on neighboring stages. Because of the non-volatility of STD, no extra CMOS registers are required to implement pipelining technique. The fully pipelined design can enormously increase our STLG's throughput to one output set per 3 ns, which leads to equivalent 3 ns delay for all benchmarks. However, it is necessary to insert additional buffers between two STLGs, if the subsequent STLG does not locate at next neighboring stage. As shown in Figure 17(b), since IN3 input node was directly connected to OUT2 in stage 3 (as displayed in Figure 12), two Domain Wall Buffer (DWB1 and DWB2) are inserted into stage 1 and 2 respectively. The proposed DWB circuit is

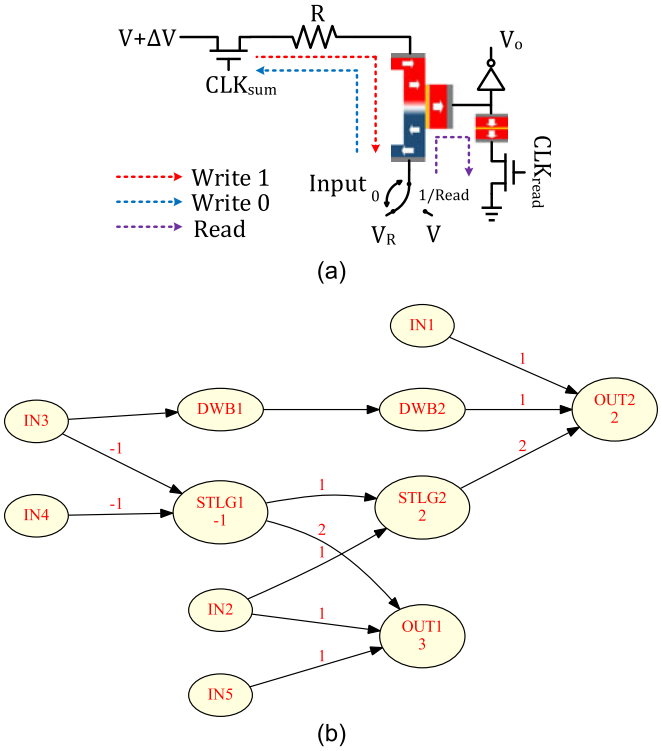

FIGURE 17. **(a) Domain Wall Buffer (DWB) circuit designed for pipeline architecture (b) C17 STLN with buffer.**

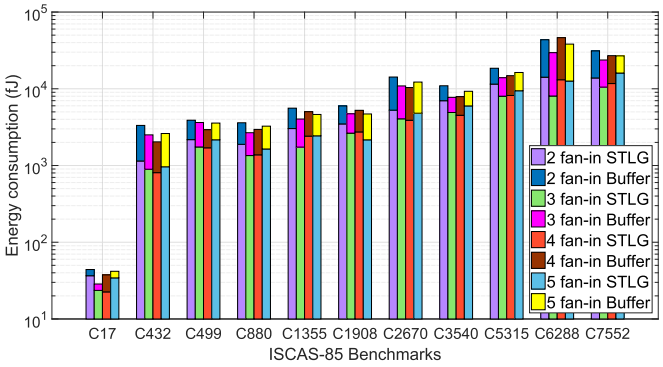

FIGURE 18. **Energy dissipation of ISCAS-85 benchmarks for different fan-in restriction STLNs.**

shown in Figure 17(a). Different from STLG, the DWB only has two operations: write and read corresponding to CLK_{sum} and CLK_{read}. When the CLK_{sum} is high, the input switch selects different voltage to introduce current of opposite direction, thus the new data bit will cover the original data and stored at STD. The sense circuit is same as it in the STD (Section III-A). In order to reduce the energy consumption, there is no reset operation applied on our proposed buffer. Since the sense circuit only works after the write operation, removing reset clock would not disturb the functionality and pipeline implementation of our design.

The benchmarks with fully-pipelined architecture shows average 49.37, 95.09, and 77.04 percent delay reduction over LUT, CTL and MTL correspondingly. In general, the larger scale STLN shows better delay performance with pipeline architecture.

C. ENERGY

The Energy dissipation of ISCAS-85 benchmarks with different fan-ins are displayed in Figure 18. Generally, for all benchmarks, it shows a good amount energy reduction when increasing the fan-in restriction from two fan-in to three or four fan-in. However, when improving the fan-in restriction, the percentage of functions that are threshold functions significantly reduces, which leads to increased number of STLGs, thus higher energy dissipation of entire STLN [33]. The energy dissipation of single inserted buffer is about 2.5 fJ, which is much smaller than the energy consumed by STLG, as shown in Table 3. However, due to the large amount of buffer, the energy consumption of buffers is larger than that of STLGs in some benchmarks, which further diminish the advantage of increasing fan-in. In general, it can be seen that the energy consumption is optimized when the fan-in number is set to be 3 or 4. We also compared energy consumption of our proposed STLG with LUT, CTL and MTL [4]. As listed in Table 5, the energy consumption of ISCAS-85 benchmarks using STLG with or without pipeline shows average 86 and 93 percent energy reduction over LUT respectively. STLG with pipeline shows average 47 percent energy reduction over CTL, but when design STLG in pipelining technique, the STLG consumes more energy than CTL

TABLE 5. Energy disspation of ISCAS-85 benchmarks, and comparison between four Fan-In LUT, CTL, MTL and STLG.

Benchmark	LUT (fJ) [4]	CTL (fJ) [4]	MTL (fJ) [4]	STLG (fJ)	
				without pipeline	with pipeline
C17	71.46	49.7	6.3	22.53	37.53
C432	17,362.56	1,781.7	217.37	807.03	2,034.53
C499	33,795.57	4,153.9	465.32	1,700.48	2,927.98
C880	26,394.41	2,837.5	344.84	1,377.26	2,954.76
C1355	56,284.24	4,589.9	524.01	2,416.01	5,026.01
C1908	56,930.13	4,046.6	499.05	2,738.94	5,241.44
C2670	45,734.83	5,595.9	707.46	3,888.98	10,383.98
C3540	14,8281.6	8,544.8	1,095.05	4,515.07	7,905.07
C5315	250,892.01	14,918	1,876.49	8,177.26	14,834.76
C6288	2,030,231.42	20,775.3	2,492.94	13,112.58	46,347.58
C7552	315,929.35	21,701.9	2,627.22	11,698.12	27,043.12

TABLE 6. Transistor count of ISCAS-85 benchmarks, and comparison between four Fan-In LUT, CTL, MTL and STLG.

Benchmark	LUT [4]	CTL [4]	MTL [4]	STLG	
				without pipeline	with pipeline
C17	504	182	182	56	80
C432	12,726	4,680	3,510	1,974	3,938
C499	30,492	9,516	9,386	4,116	6,080
C880	23,184	7,930	6,266	3,276	5,800
C1355	41,958	12,038	11,388	6,132	10,308
C1908	36,540	10,556	9,074	6,482	10,486
C2670	49,014	14,872	12,714	9,758	20,150
C3540	72,072	24,466	18,798	10,752	16,176
C5315	133,560	39,962	32,110	20,832	31,484
C6288	241,164	63,986	63,934	34,188	87,364
C7552	184,590	58,630	48,516	31,010	55,562

due to large amount of inserted DWBs. Compared with MTL, our proposed STLG does not show a better energy performance, but they are still in the same order. Unlike MTL as a combinational logic gate, the proposed STLG is controlled by a three-phase clock signal and it requires reset operation for each computation.

D. AREA

The number of transistors for a N fan-in STLG is $2 \times (N + 1) + 4$, thus the four fan-in STLG consists of 14 transistors. Each inserted buffer comprises four transistors, which is much less than the STLG. Therefore, total amount of transistor count is $14 \times N_{STLG} + 4 \times N_{buffer}$, where N_{STLG} is the number of STLG and N_{buffer} is the number of buffers inserted to implement pipeline. However, due to the large amount of buffers inserted, the transistor count increases correspondingly. For instance, the N_{STLG} of four fan-in restricted ISCAS C5315, which is a 9-bit Arithmetic Logic Unit (ALU), is 1,488. The corresponding N_{buffer} is 2,663, which is larger than the logic gate. As shown in Figure 19, the number of transistor count of four fan-in is larger than that of two fan-in for C6288 benchmark. That's because C6288 is a 16×16 multiplier, which constitutes of large amount of full and half adders. The XOR ($A \oplus B$) function used in full and half adders is not linearly separable, thus increasing fan-in will not lower the N_{STLG} used for STLN [4]. Since the synthesized STLN is obtained from TELS. Further transistor count reduction can be targeted by re-designing the synthesis algorithm.

The transistor count comparison between LUT, CTL, MTL and STLG is displayed in Table 6. Note that, the chip area is dominated by the CMOS transistors. The MTJs will not increase the chip area using CMOS-magnet 3D integration technology [40]. The STLG without pipeline architecture shows greatly less amount transistor count than all the other three methods, which makes STLG (without pipeline) better option for high chip density design. The pipeline architecture sacrifices this benefit for higher throughput, but it still needs much less transistors than LUT. A solution to reduce the transistor count is to employ partial run-time reconfiguration technique [41], [42]. Such technique can be easily adopted to our proposed design due to high speed and low energy dissipation of SWD configuration and the non-volatility of STD. It is promising to be employed in Software Defined Radio (SDR) [43], field testing, remote sensors and other adaptive applications [44]. In SDR, most radio usage are dominated by standby operations, the zero idle power dissipation of our proposed non-volatile STLG-based FPGA makes it promising to achieve orders better energy efficiency and high chip area density.

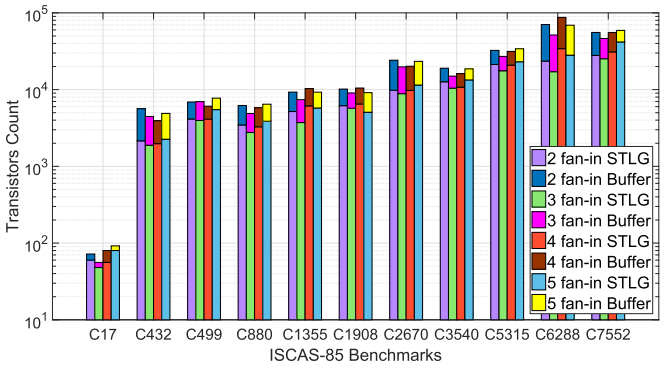

FIGURE 19. Transistor count with different number of fan-in restrictions of ISCAS-85.

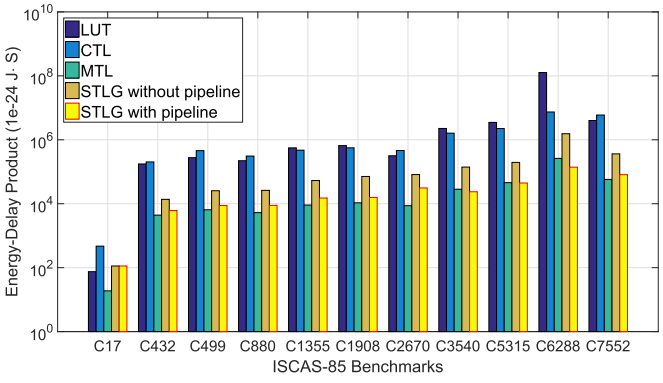

FIGURE 20. EDP of ISCAS-85 benchmarks using four fan-in LUT, CTL, MTL, STLN with or without pipeline technique.

E. ENERGY-DELAY PRODUCT

Figure 20 depicts the energy-delay product (EDP) of ISCAS-85 benchmarks using LUT, CTL MTL and STLN with or without pipeline technique. The EDP of STLN without pipelining technique shows average 75 and 88 percent reduction over LUT and CTL respectively, and the pipelined STLN further pushes this result to 80 and 95 percent. MTL shows about 4× better EDP than STLN without pipeline mainly due to its lower energy dissipation. However, the EDP of STLN drastically decreases after employing pipeline architecture. For the smaller scale benchmarks from C17 to C2670, MTL shows slightly better EDP. While, the EDP of pipelined STLN becomes smaller in larger scale benchmarks (such as C3540, C5315 and C6288) due to the constant 3 ns delay. For benchmark C6288, the EDP of STLN is only 50 percent of MTL. In summary, our proposed pipelined STLN shows better EDP performance over other three implementation methods for large scale threshold logic networks.

VI. CONCLUSION

In this paper, we propose a spintronic weight device that can jointly work with spintronic threshold device to design spintronic threshold logic gate. Ultra-low energy is achieved due to low voltage (50 mV), low current computing facilitated by the proposed design. Moreover, the spintronic weight device also leads to low power and fast speed in reconfiguration operation of the proposed design. Compared with reconfigurable MTL design, the proposed STLG consumes three orders lower reconfiguration energy. A reconfiguration circuit is also presented to realize precise SWDs programming. Besides, the simulation framework is designed to evaluate the performance of mapped spintronic threshold logic network, where it shows average 49.37, 95.09, and 77.04 percent delay reduction over LUT, CTL and MTL utilizing pipelining technique. In the large scale benchmarks, our proposed STLN shows a trend of better energy delay product compared with MTL. In summary, the flexibility and outstanding performance of spintronic threshold logic gate will open a new door for future post-CMOS, ultra-low energy reconfigurable computing era.

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