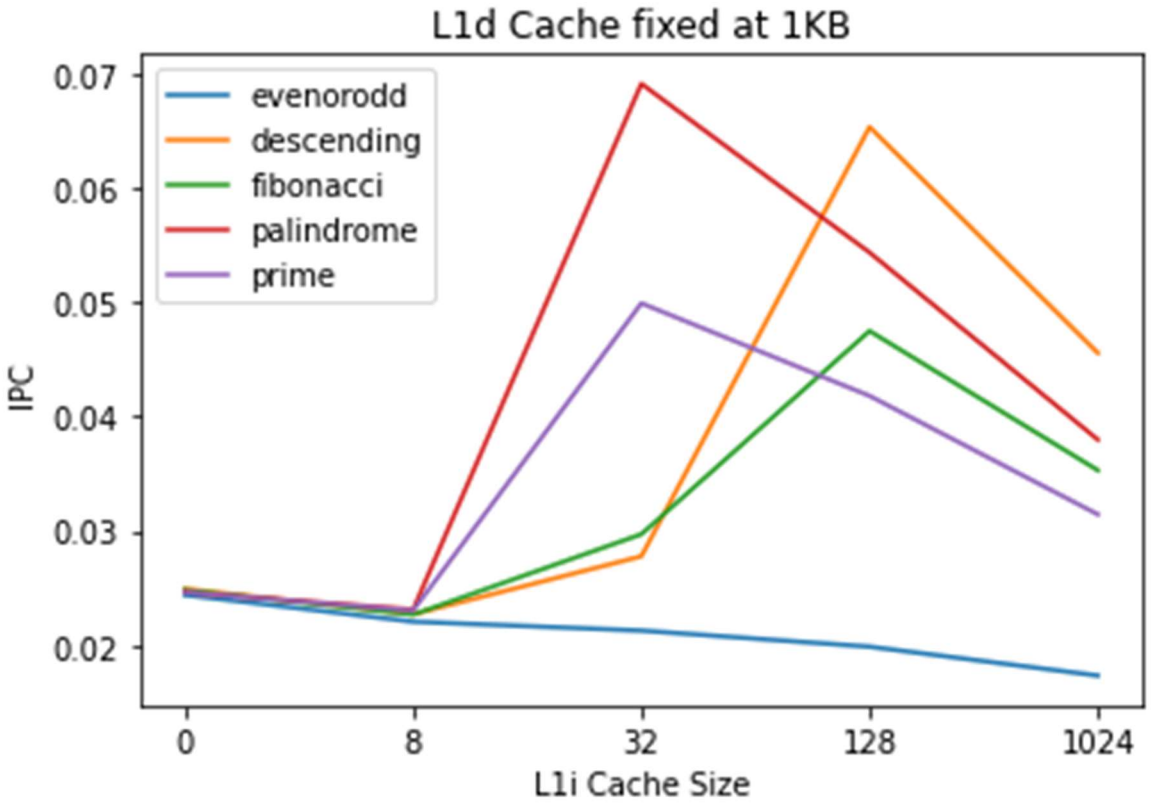
CS 311 - Computer Architecture Lab

Assignment 6: Caches

180010008, 180020024, 180010019

- The size of the **L1d-cache** fixed at 1kB →

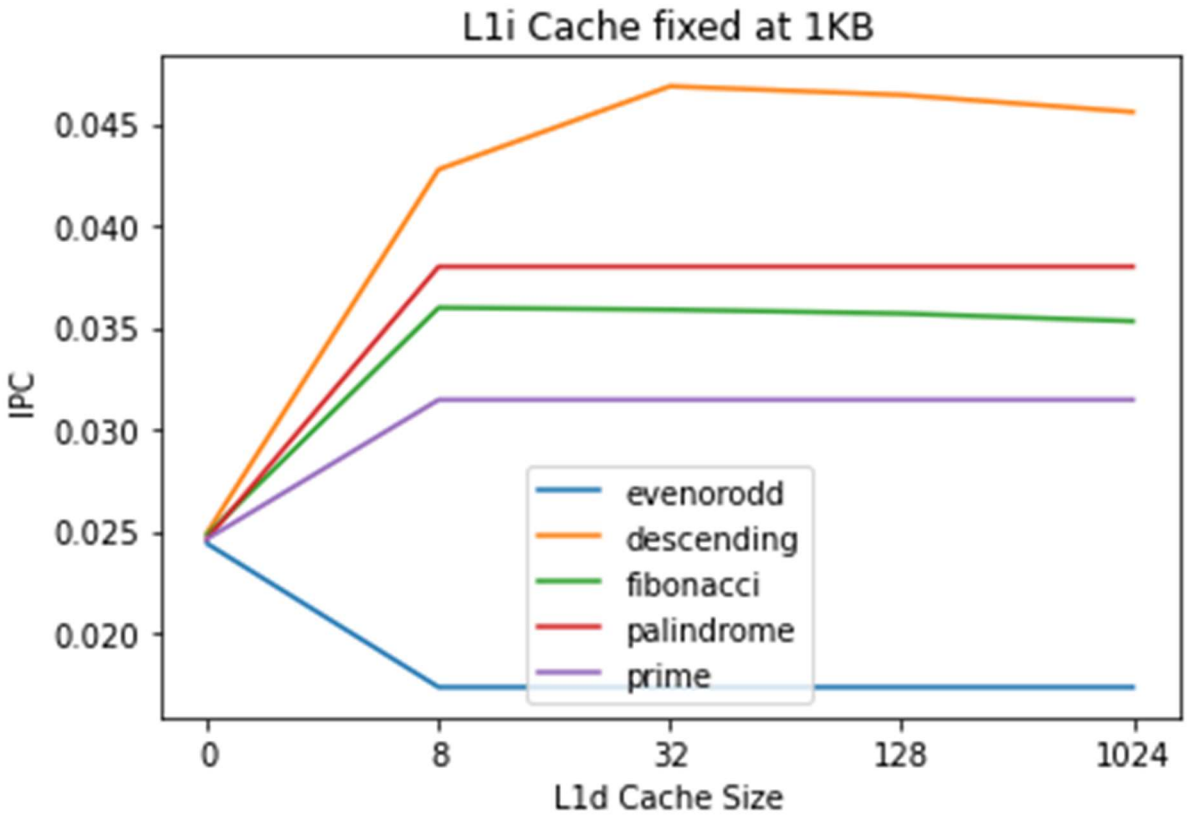
Size of L1i-cache	Without Cache	8B	32B	128B	1024B
evenorodd	0.02439024	0.022058824	0.02127660	0.019867550	0.017341040
descending	0.02493179	0.022703242	0.02777778	0.065353625	0.045585115
fibonacci	0.02482679	0.022672456	0.02970923	0.047498737	0.035311796
palindrome	0.02462620	0.023121387	0.06913580	0.054368930	0.037991860
prime	0.02463054	0.023035230	0.04992658	0.041820418	0.031452358



As L1i cache size increases, latency also increases, and so does the hit rate. There will be an optimum size of L1i cache where IPC is maximum.

- The size of the **L1i-cache** fixed at 1kB →

Size of L1d-cache	Without Cache	8B	32B	128B	1024B
evenorodd	0.02439024	0.017341040	0.017341040	0.017341040	0.017341040
descending	0.02493179	0.042765085	0.046848927	0.046419940	0.045585115
fibonacci	0.02482679	0.035973977	0.035877860	0.035687167	0.035311796
palindrome	0.02462620	0.037991860	0.037991860	0.037991860	0.037991860
prime	0.02463054	0.031452358	0.031452358	0.031452358	0.031452358



Here also the latency increases with increment in cache size and hit rate also increases. There will be an optimum size of L1d cache where IPC is maximum.