CoolSiC™ totem-pole PFC design guide and power loss modeling

About this document

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Scope and purpose

This document is a design guide for a CoolSiC™ power factor correction (PFC) totem-pole converter, including:

- Equations for design and power losses
- Selection guide for semiconductor devices and passive components
- 3300 W design example with calculated and experimental results

Intended audience

This document is intended for design engineers who want to design CoolSiC™ CCM totem-pole PFC converters.

Table of contents

1 Introduction

Front-end AC-DC rectifiers (**Figure 1**) contain a PFC front-end stage that regulates the bus voltage to a DC value (~400 V), followed by a DC-DC stage that steps down the bus voltage and provides a galvanically isolated and regulated DC output (e.g., 12 V or 48 V). This document discusses the PFC stage in high-power applications such as telecom and data center server power supplies.

PFC shapes the input current of the power supply to be in synchronization with the mains voltage, in order to maximize the real power drawn from the mains. In a perfect PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics.

Boost-derived topologies are the most common for PFC. SiC-based totem-pole PFC proves to be a winning topology in terms of efficiency and power density. This document illustrates the benefits of SiC-based totem-pole PFC and introduces its analysis and design methodology, including equations for power loss estimation, a selection guide for semiconductor devices and passive components, and a design example with experimental results.

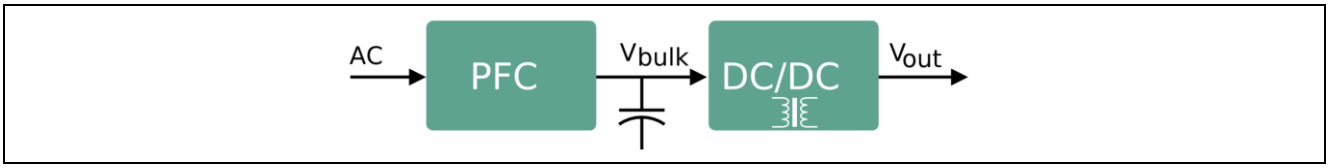


Figure 1 AC-DC rectifier

The following is a quick overview of the classic boost PFC vs. SiC totem pole PFC.

1.1 Classic boost PFC

A classic boost converter (**Figure 2**) is the most popular topology used in PFC applications. The key boost converter waveforms are shown on the right-hand side. Since the input voltage to the boost is a rectified sinusoidal voltage, varying from zero to the sinusoidal peak voltage, the duty cycle also varies with the input voltage variation across the line cycle. The line current shown in **Figure 2** is conducted throught two diodes of the rectifier bridge at all times, and this causes significant conduction loss, especially at higher power and low-line conditions.

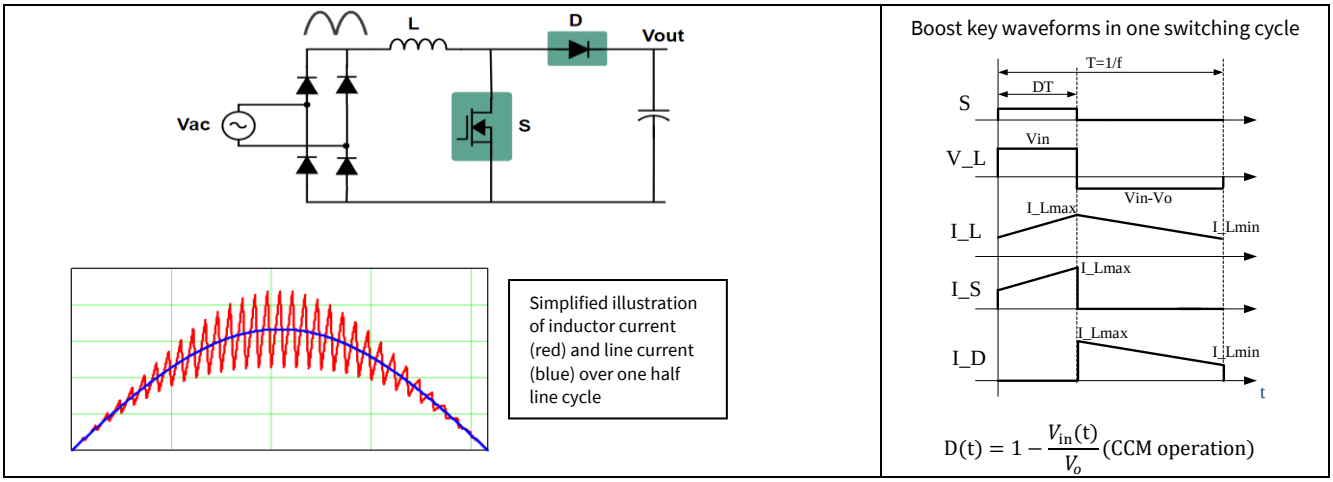


Figure 2 Structure and key waveforms of a boost converter

1.2 Bridgeless totem-pole PFC

Figure 3 shows the totem-pole PFC topology. Its main benefit compared to the classic boost PFC is that it is a bridgeless circuit, meaning that it doesn't include a rectifier diode bridge at its input. Therefore, the associated rectifier bridge losses are eliminated, leading to higher efficiency and power density.

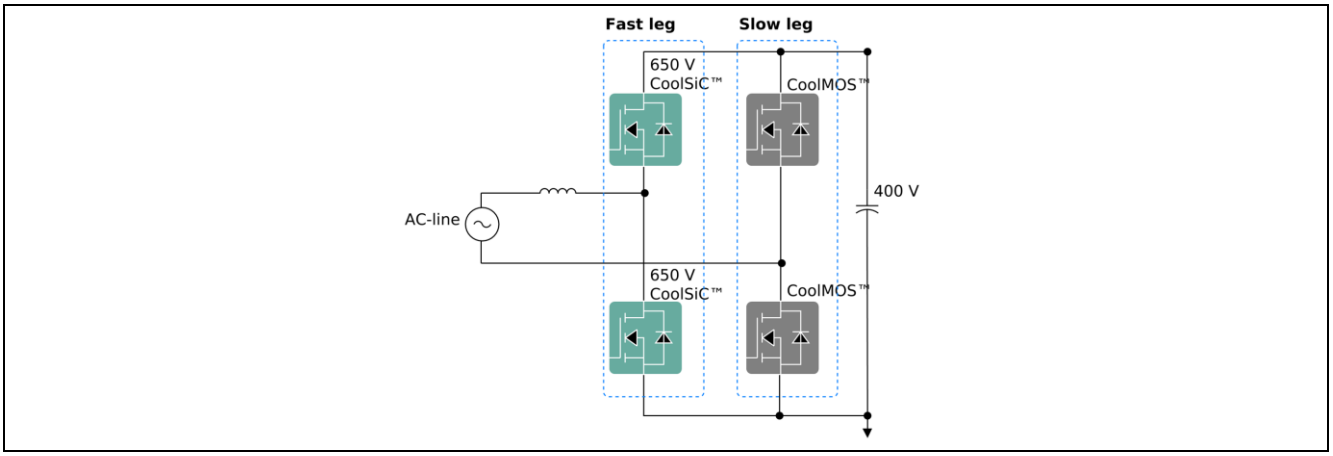
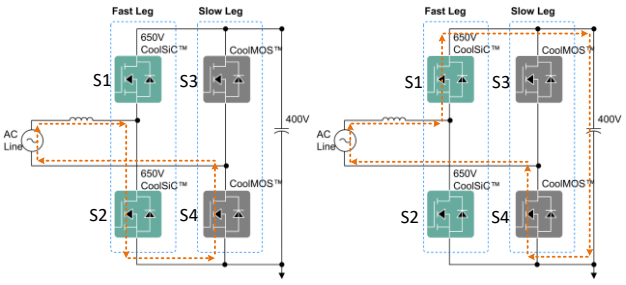
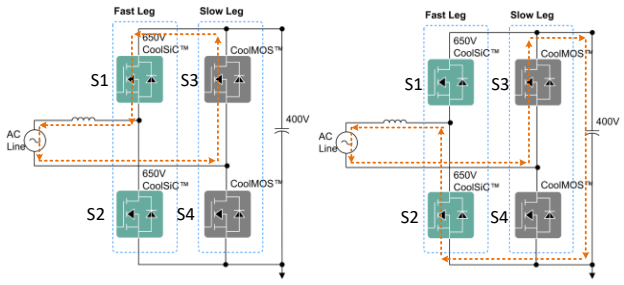


Figure 3 Structure for totem-pole PFC power stage

Table 1 shows the operational modes of the totem pole during the positive and negative halves of the AC-line cycle. Two switches (fast leg) run at high switching frequency with the function of the boost switch and rectifier switch, while the other two switches (slow leg) run at line frequency with the function of line rectifier.

Table 1 Operational totem-pole modes during positive and negative halves of the AC-line cycle

Positive AC voltage half line	Negative AC voltage half line
S1: Switching as synchronous switch S2: Switching as control switch S3: Off S4: On	S1: Switching as control switch S2: Switching as synchronous switch S3: On S4: Off
	

2 CCM totem-pole PFC benefits

2.1 Efficiency

CoolSiC™ has a unique benefit of a very low body diode reverse recovery, which makes it an enabling device for totem-pole PFC topology, because the switch is working as a main PFC switch in one half of the line cycle and then as a synchronous switch in the following half line cycle, as shown in **Table 1**. A CoolMOS™ body diode is not suitable for such operation because its body diode has a high reverse recovery charge.

To illustrate the CoolSiC™ efficiency benefit, **Figure 4** shows a breakdown of main power losses at 50 percent load and high-line condition. This example breakdown belongs to a 3300 W PFC design using classic PFC boost with CoolMOS™ vs. totem-pole PFC with CoolSiC™.

Although the two CoolSiC™ switches have lower loss compared to the combined boost CoolMOS™ and diodes, the more obvious benefit of totem-pole PFC is the saved diode bridge loss, which has a significant share of total losses as seen in the classic boost PFC case.

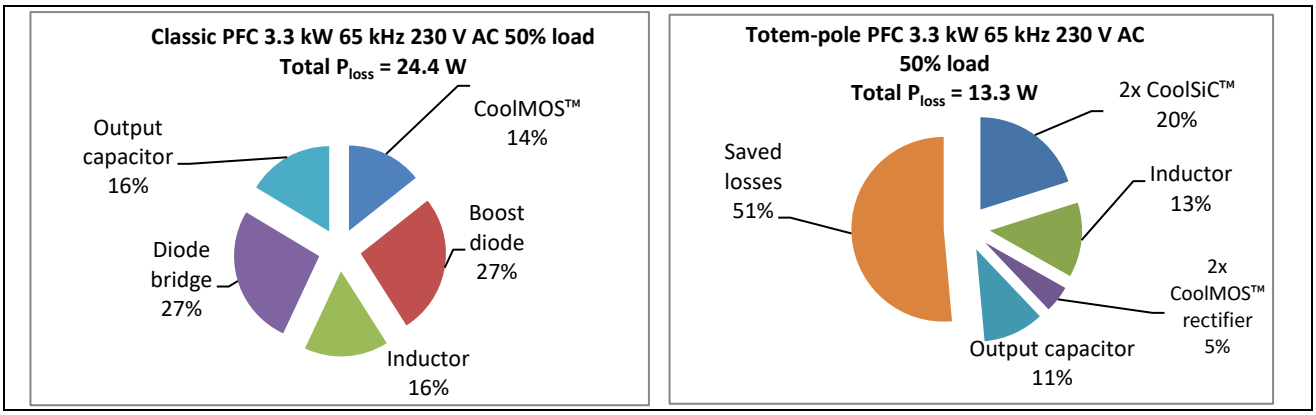


Figure 4 Breakdown of power losses: classic boost PFC vs. totem pole PFC

2.2 Power density

A multi-domain/objective optimization simulation calculates the maximum attainable efficiency vs. power density based on the limits of technological parameters. **Figure 5** shows the trade-off limit curve (Pareto front) of a multi-objective, i.e., efficiency and power density design optimizations for classic boost PFC and totem pole PFC. It clearly shows the maximum possible efficiency benefit of the totem pole compared to the classic boost PFC for the same power density; furthermore, the totem pole can reach higher density limits at a higher efficiency compared to the classic boost PFC.

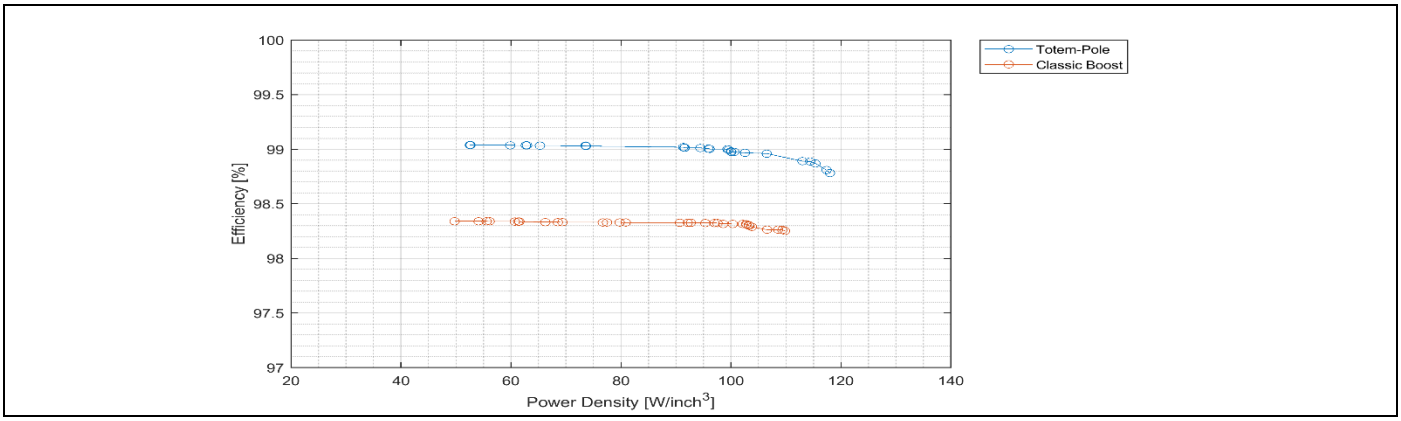


Figure 5 Pareto chart efficiency and power density, for classic boost PFC vs. totem pole PFC

3 CCM totem pole PFC power stage design

This section details the converter design and power loss equations for the CCM totem-pole PFC. The design example specifications listed in **Table 2** will be used for all of the equation calculations. Since the converter is designed to deliver full power at the high-line 230 V AC, and power is derated at low-line voltage, all design equations and power losses will be calculated using the high-line voltage condition, unless it is necessary to also consider the low-line condition.

Table 2 Specifications of the power stage

Input voltage	176 to 265 V AC 50/60 Hz
Output voltage	400 V
Maximum power steady-state	3300 W at 230 V AC
Switching frequency	65 kHz
Inductor current ripple	15 percent at full load
Output voltage 120 Hz ripple	20 V_{p-p}
Hold-up time	10 ms at $V_{o.min}$ = 340 V

3.1 PFC inductor

The PFC inductor value and its maximum current are determined based on the specified maximum inductor current ripple, as shown below:

$$L = \frac{1}{\%Ripple} \cdot \frac{{V_{ac}}^2}{P_o}\left(1 - \frac{\sqrt{2} \cdot V_{ac}}{V_o}\right) \cdot T = \frac{1}{15\%} \cdot \frac{(230V)^2}{3300W}\left(1 - \frac{\sqrt{2} \cdot 230V}{400V}\right) \cdot \frac{1}{65 \cdot 10^3 Hz} = 307\ \mu H \quad \text{Eq. 1}$$

$$I_{L.max} = \frac{\sqrt{2} \cdot P_o}{V_{ac}} \cdot \left(1 + \frac{\%Ripple}{2}\right) = \frac{\sqrt{2} \cdot 3300W}{230V} \cdot \left(1 + \frac{0.15}{2}\right) = 21.8\ A \quad \text{Eq. 2}$$

A swinging choke has an inductance value that is inversely proportional to its operating current. AmoFlux, Kool Mu and High Flux are different powder core materials from Magnetics Inc.; for example, they can deliver good power factor, THDi and EMI performance, due to the high inductance at lower current (or DC bias).

In this design, a 60 µ permeability High Flux core from Magnetics Inc. is used, EQH3626E060L174 with 60 turns. The DC resistance is about 35 mΩ, and the inductance ranges from 518 µH at no load dropping to about 295 µH at 230 V AC and full load, which is close to the desired value calculated above in Eq. 1. Inductor saturation current must be rated as greater than $I_{L.max}$, to survive line and load transients.

Since the inductance value varies across the line and load range, and also across the line cycle, it would be more accurate to model the inductance value as a function of V_{in}, P_o and t, to better estimate the switching currents and losses. This specific inductor design was modeled as shown in **Figure 6** as a function of power (P_o) and time (t) across the line cycle, using the equations Eq. 3 to Eq. 6, below:

$$I(t, Po) = \frac{P_o \cdot \sqrt{2}}{V_{ac}} \cdot sin(2\pi \cdot f_{line} \cdot \mathrm{t}) \quad \text{Eq. 3}$$

$$H(t, Po) = \left|\frac{0.4 \cdot \pi \cdot N \cdot I_L(t, Po)}{l_e\ (cm)}\right| \quad \text{Eq. 4}$$

$$\mu_{eff}(t, Po) = \frac{1}{a + b \cdot H(t, Po)^c} \cdot \frac{\mu_i}{100} \quad \text{Eq. 5}$$

(where a = 0.01 $b = 1.583 \cdot 10^{-8}$ c = 2.572 for High Flux EQ cores)

$$L(t,Po) = \frac{0.4 \cdot \pi \cdot N^2 \cdot \mu_{eff}(t,Po) \cdot A_e(in\ cm^2)}{l_e\ (cm)}$$ Eq. 6

$Inductor\ cross\ section\ area\ A_e = 181\ mm^2$

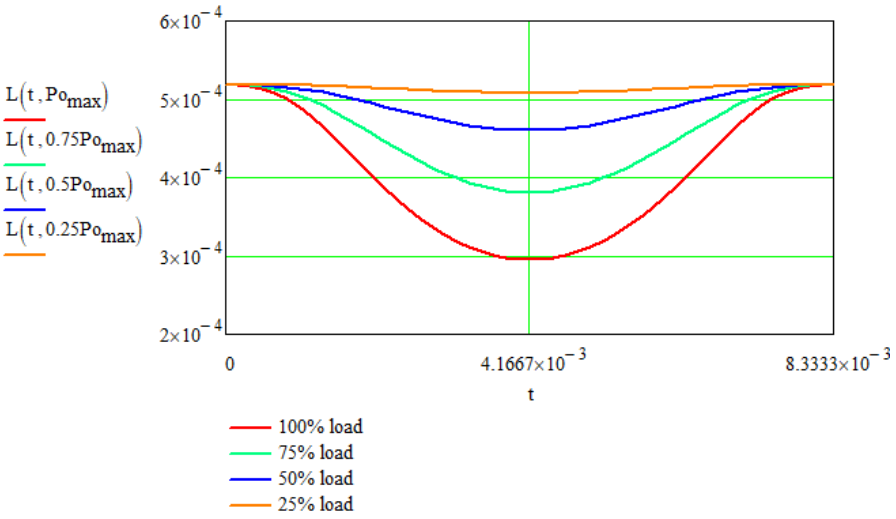


Figure 6 Inductor value across half line cycle at different load currents

3.1.1 Inductor copper loss

The inductor RMS current and the corresponding copper loss are:

$$I_{L.rms} \cong I_{in.rms} = \frac{P_o}{V_{ac}} = \frac{3300\ W}{230\ V} = 11.7\ A$$ Eq. 7

$$P_{L.cond} = {I_{L.rms}}^2 \cdot DCR = (11.74\ A)^2 \cdot 0.035\ \Omega = 4.8\ W$$ Eq. 8

3.1.2 Inductor core losses

At high-line, core losses are far from the sinusoidal shape (**Figure 7**), so it is necessary to model the core loss across the line cycle as a function of time, and then integrate it to obtain the average loss. The following set of equations can be used in Mathcad® or other tools:

$$I_{L.max}(t) = \frac{P_o \cdot \sqrt{2}}{V_{ac}} \cdot sin(2\pi \cdot f_{line} \cdot t)\left(1 + \frac{\%Ripple}{2}\right), \quad H_{max}(t) = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.max}(t)}{l_e\ (cm)}$$ Eq. 9

$$I_{L.min}(t) = \frac{P_o \cdot \sqrt{2}}{V_{ac}} \cdot sin(2\pi \cdot f_{line} \cdot t)\left(1 - \frac{\%Ripple}{2}\right), \quad H_{min}(t) = \frac{0.4 \cdot \pi \cdot N \cdot I_{L.min}(t)}{l_e\ (cm)}$$ Eq. 10

$$B = \left(\frac{a + b \cdot H + c \cdot H^2}{1 + d \cdot H + e \cdot H^2}\right)^x$$ Eq. 11

*a=4.7128*10-2 b=1.715*10-2 c=7.430*10-4 d=7.138*10-2 e=4.824*10-4 x=1.631 (for High Flux EQ Cores)*

$$B_{max}(t) = \left(\frac{a + b \cdot H_{max}(t) + c \cdot H_{max}(t)^2}{1 + d \cdot H_{max}(t) + e \cdot H_{max}(t)^2}\right)^x, \quad B_{min}(t) = \left(\frac{a + b \cdot H_{min}(t) + c \cdot H_{min}(t)^2}{1 + d \cdot H_{min}(t) + e \cdot H_{min}(t)^2}\right)^x$$ Eq. 12

Where [B] = Tesla (T), [H] = Oersteds (Oe)

$$\Delta B(t) = \frac{B_{max}(t) - B_{min}(t)}{2}$$ Eq. 13

$$P_{core}(t) = a \cdot \Delta B(t)^b \cdot \left(\frac{f}{10^3}\right)^c \cdot V_e \cdot 10^{-6}$$ Eq. 14

a=47.8 b=2.2 c=1.64 (for High Flux EQ cores)

Average core loss across the line cycle is:

$$P_{core.av} = f_{line} \cdot \int_0^{1/f_{line}} P_{core}(t)\, dt \quad = 1.3W$$ Eq. 15

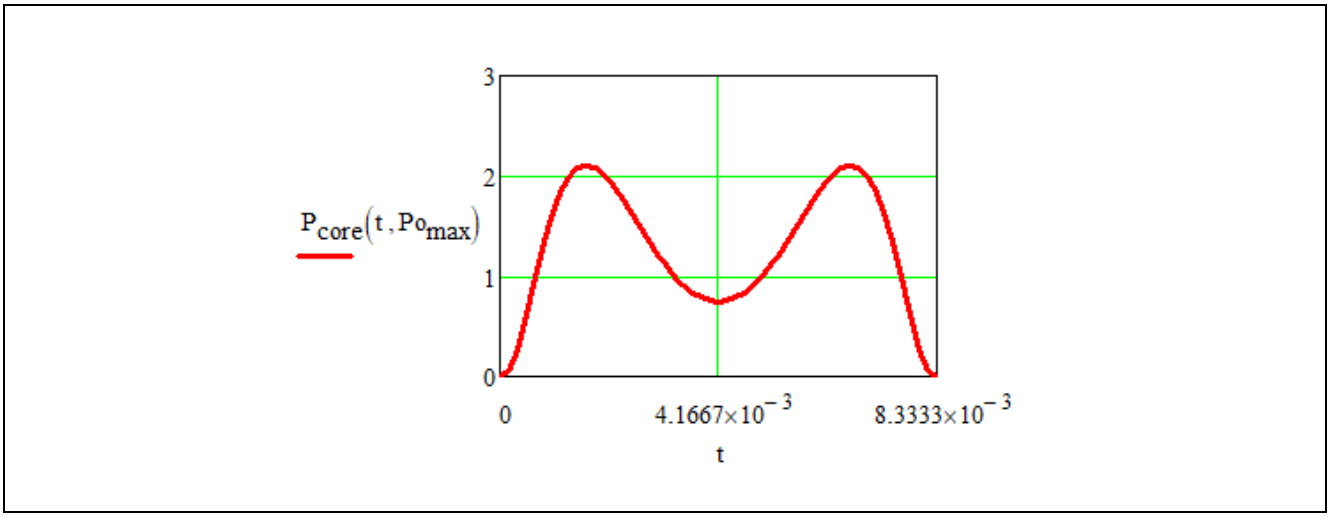


Figure 7 Inductor core loss across across half line cycle at full load

3.2 CoolSiC™ features

CoolSiC™ MOSFETs offer significantly better figures-of-merit (FOM) and key characteristics, which enables new topologies with higher density and efficiency compared to silicon superjunction MOSFETs.

- **Reverse-recovery charge Q_{rr}:** The reverse recovery performance of CoolSiC™ is a major advantage compared to Si transistors. 600 V Si power transistors have intrinsic body diode structures with a large reverse recovery charge and associated peak current. It is so large that superjunction is generally not applied to topologies or control strategies that include repetitive reverse recovery requirements, for example hard-switching half-bridge. CoolSiC™ transistors have very low Q_{rr}. Because of this, CoolSiC™ enables a whole new class of topologies that, for the first time, can effectively and efficiently improve performance. One example is the totem-pole PFC.

- **$R_{DS(on)}$ temperature coefficient:** The change of on-state resistance ($R_{DS(on)}$) with the temperature differs between the technologies (**Figure 8**). CoolSiC™ exhibits the lowest increase of $R_{DS(on)}$ over temperature, which makes it the prime choice for high-current applications in hard-switched topologies, such as in the totem-pole PFC stage.

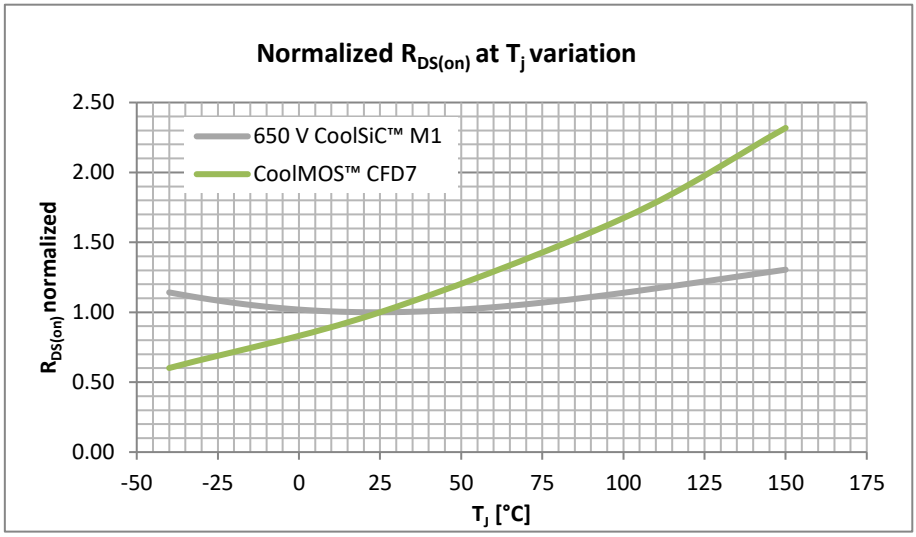


Figure 8 **Comparison of temperature dependency of the on-state resistance for the different semiconductor technologies**

- **Output charge Q_{oss}:** Traditional Si superjunction 600 V power transistors have a very non-linear output charge characteristic. As V_{DS} is increased from 0 V to about 25 V, the charge increases rapidly at a steep slope. Then suddenly the slope flattens out, and the charge only increases a small additional amount as V_{DS} is further increased all the way to 400 V or more. CoolSiC™ has a mostly linear characteristic, and the overall charge is much lower (**Figure 9**). This offers a significant benefit in both soft-switching and hard-switching applications. Lower Q_{OSS} shortens the dead time needed for zero voltage switching (ZVS) and enables higher frequency in the LLC resonant stage, and reduces the hard commutation losses in the CCM totem-pole stage.

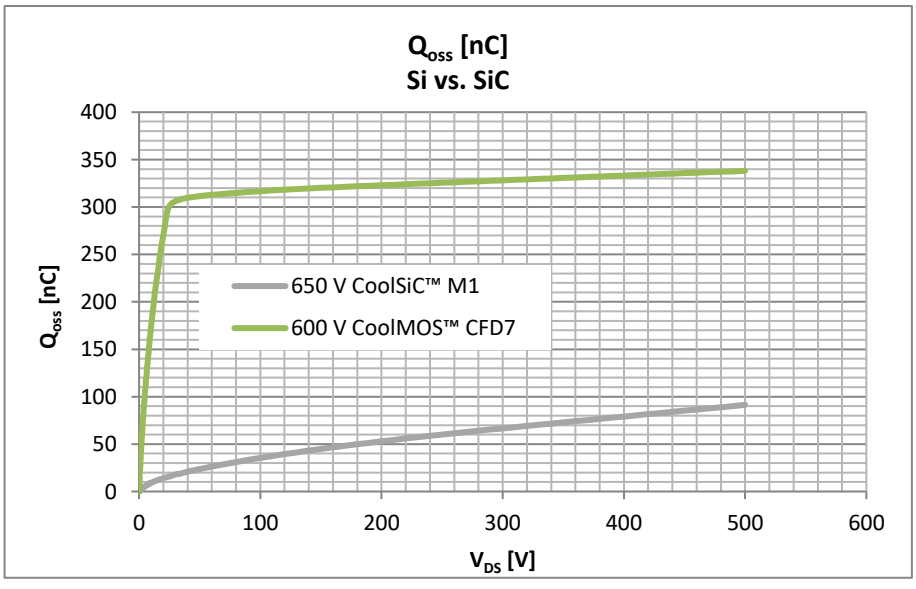


Figure 9 **Voltage dependency of parasitic output charge (Q_{oss}) for different semiconductor technologies**

- **Gate charge Q_g:** Gate charge affects how quickly the transistor can be switched on and off, and how frequently – as in the power required to operate the gate drive circuit at high frequencies. Low gate charge is a desired characteristic in power transistors. Again, comparing CoolSiC™ to Si MOSFETs, CoolSiC™ has about half the Q_g compared to superjunction.

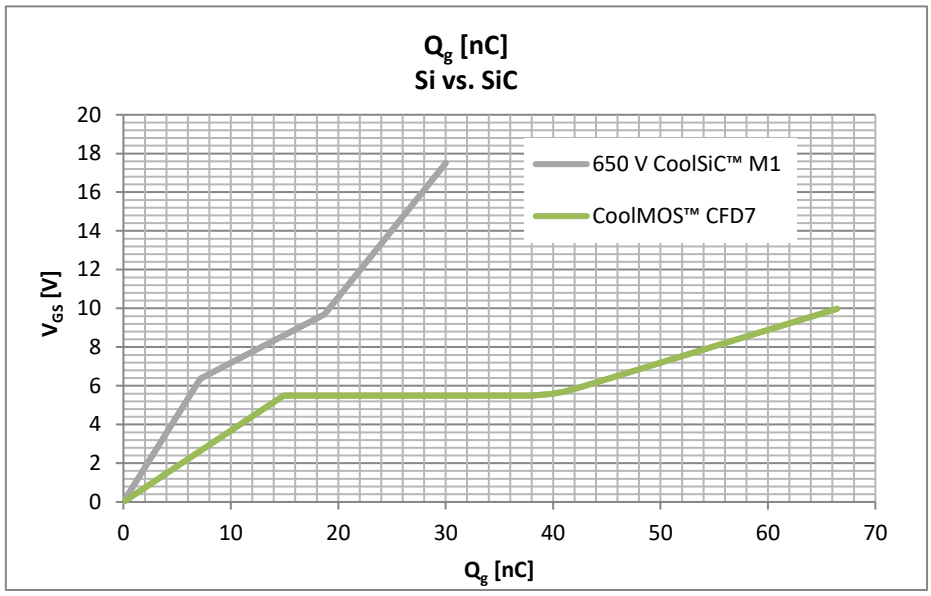


Figure 10 Gate charge for different semiconductor technologies

3.3 650 V CoolSiC™ M1 optimum $R_{DS(on)}$ selection charts

Selection of the optimum on-state resistance of a CoolSiC™ MOSFET is based on balancing the switching losses and conduction losses of the device at a targeted load point. This can be done by modeling all losses in a software tool such as Mathcad® by evaluating different values of the on-state resistance. This requires few iterations and entry of several parameters from the datasheet of each part.

An alternative and easier approach is to use CoolSiC™ selection charts. **Figure 11** shows the selection chart for $R_{DS(on)}$ optimized at half load for designs targeting the highest peak efficiency, while **Figure 12** is for $R_{DS(on)}$ optimized at full load for designs targeting best thermal performance at full load.

The following is a guide to how to use these CoolSiC™ $R_{DS(on)}$ selection charts.

We can use the specifications in **Table 1** as a design example:

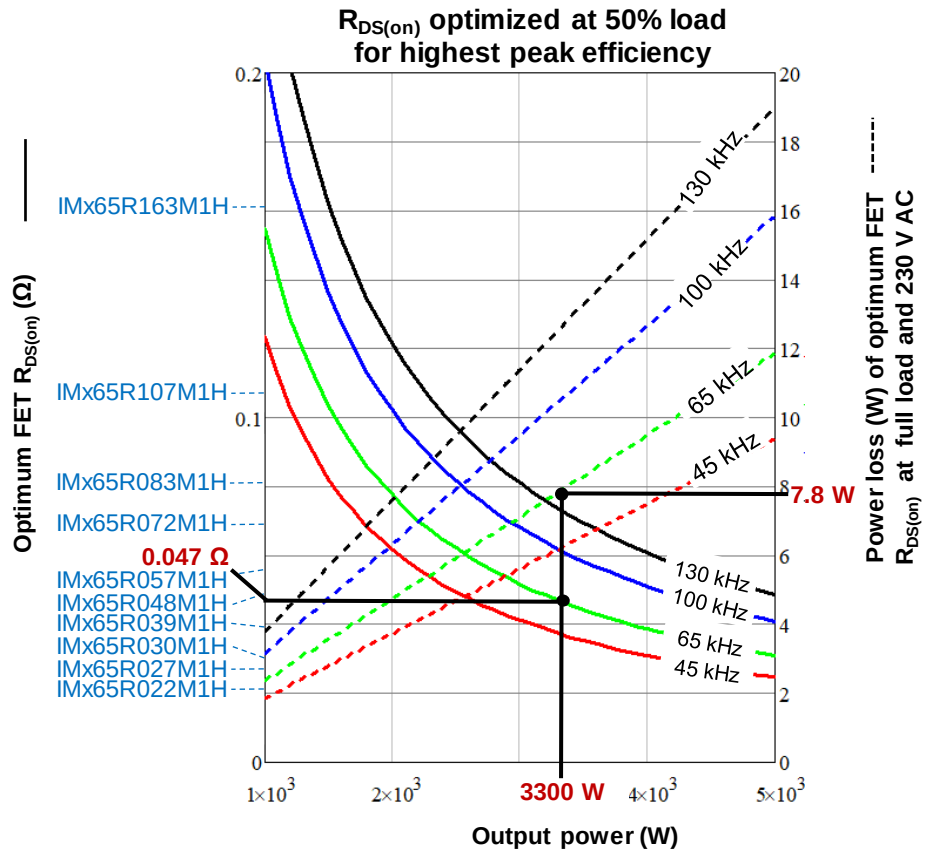
Design requirements: P_o = 3300 W, f = 65 kHz; peak efficiency at half load is critical.

- Step 1: Find the correct chart – **Figure 11** shows the chart for $R_{DS(on)}$ optimized at half load.
- Step 2: Find the 65 kHz curves (green curves in this example).
- Step3: Mark the 3300 W on the x-axis.
- Step 3: Find the 3300 W intersection with the solid green line for the 65 kHz, read the left-side y-axis, we find that 0.047 Ω is the optimum $R_{DS(on)}$ for CoolSiC™, then we may choose IMx65R048M1H for example.
- Step 4: Find the 3300 W intersection with the dashed green line for the 65 kHz, read the right-side y-axis, we find that the 0.047 Ω will result in 7.8 W power loss at full load and 230 V AC.

If the same example is applied in **Figure 12**, where $R_{DS(on)}$ is optimized at full load, then we can find that 0.024 Ω is optimal and will result in 5.8 W power loss at full load and 230 V AC.

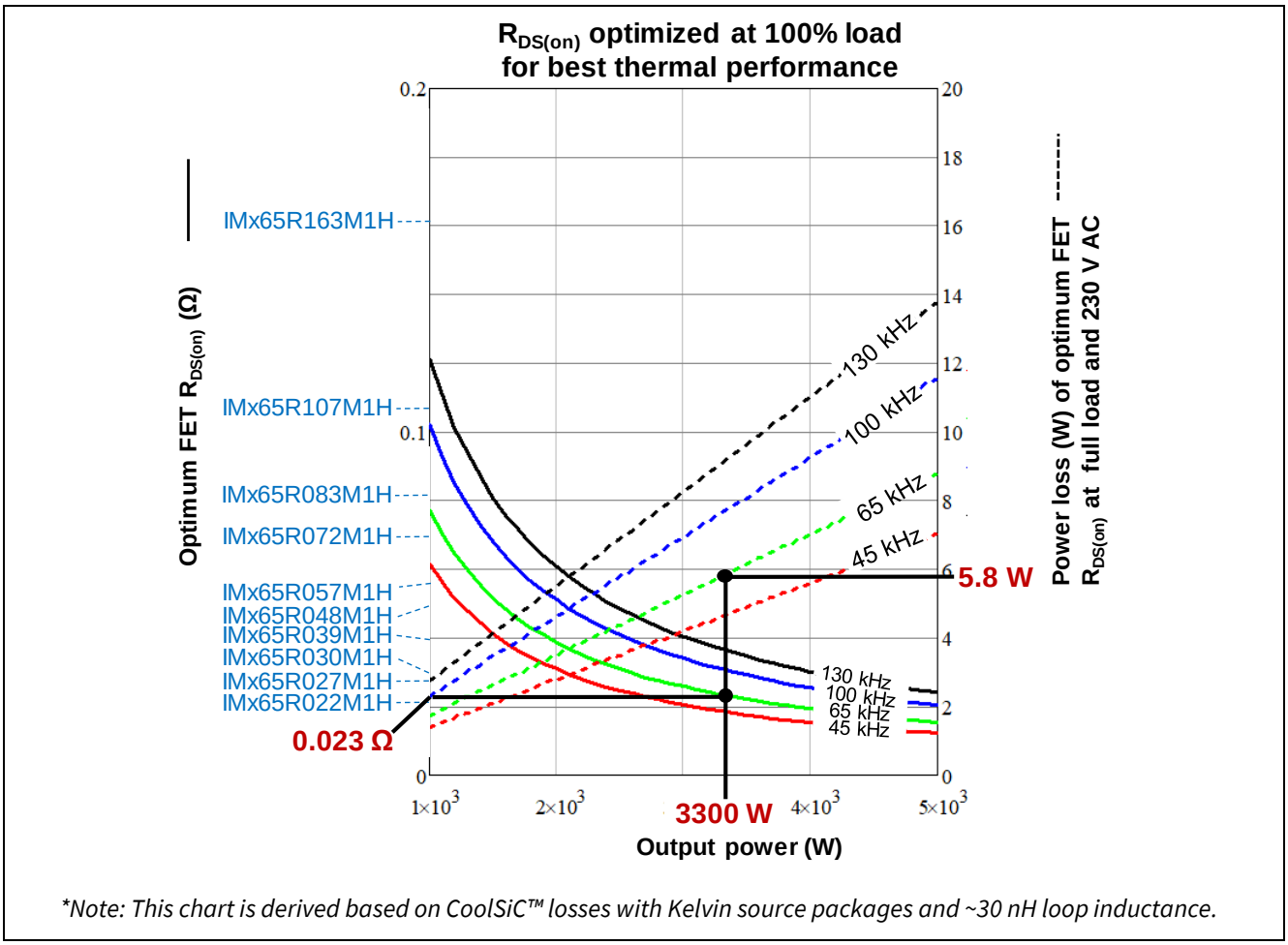
Therefore, to balance the peak efficiency optimal $R_{DS(on)}$ and the best thermal optimal $R_{DS(on)}$ mentioned above, the designer may choose an $R_{DS(on)}$ value between the two values mentioned above.

This design is focused on peak efficiency at half load, hence it uses a 0.048 Ω CoolSiC™ for the fast leg, and the following section shows the detailed loss analysis.



**Note: This chart is derived based on CoolSiC™ losses with Kelvin source packages and ~30 nH loop inductance.*

Figure 11 650 V CoolSiC™ M1 optimum $R_{DS(on)}$ selection chart at half load, with example



Note: This chart is derived based on CoolSiC™ losses with Kelvin source packages and ~30 nH loop inductance.

Figure 12 650 V CoolSiC™ M1 optimum $R_{DS(on)}$ selection chart at full load

3.4 CoolSiC™ power losses

Across the 60 Hz line cycle, each CoolSiC™ works as a boost switch for a half line cycle, then as a boost rectifier for the following half line cycle, so we need to calculate the loss in both operational modes then average them to find the total loss per device across the full 60 Hz line cycle, as follows.

3.4.1 CoolSiC™ losses during operation as a boost switch

RMS current of a boost switch can be calculated by the following equation, and consequently the conduction loss can be obtained as:

$$I_{S.rms} = \frac{P_o}{V_{ac}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{ac}}{3 \cdot \pi \cdot V_o}} = \frac{3300\ W}{230\ V} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot 230V}{3 \cdot \pi \cdot 400V}} = 8\ A \quad \text{Eq. 16}$$

$$P_{S.cond} = {I_{S.rms}}^2 \cdot R_{on(125℃)} = (8A)^2 \cdot (0.048\Omega \cdot 1.2) = 3.7\ W \quad \text{Eq. 17}$$

$$where\ R_{on(125℃)} = 1.2 \cdot R_{on(25℃)}$$

For switching turn-on and turn-off losses, the typical equations used for calculating switching times and losses become inaccurate in fast-switching CoolSiC™ , due to the high di/dt effects associated with package and PCB parasitics. Therefore, characterization of turn-on and turn-off losses in an experimental setup would be more realistic, as shown in **Figure 13**.

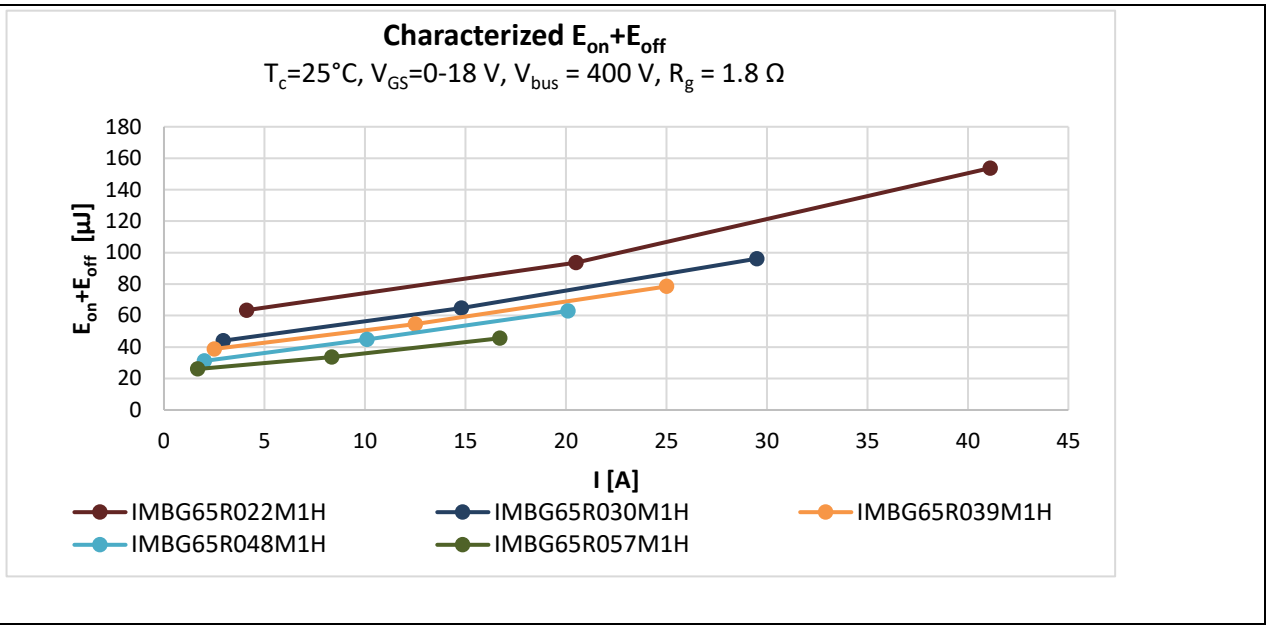


Figure 13 Characterized E_{on} + E_{off} switching losses for different $R_{DS(on)}$

In order to facilitate the usage of the characterized $E_{on/off}$ data in power loss modeling, an averaged fitted formula based on characterization of different $R_{DS(on)}$ of CoolSiC™ FETs was derived as shown in Eq. 18, and **Figure 14** shows a plot of the fitted E_{on} + E_{off} vs. switching current for different $R_{DS(on)}$ values.

$$E_{on,off} = 1.85 \cdot I + 1.24/RDS_{on} \quad \text{Eq. 18}$$

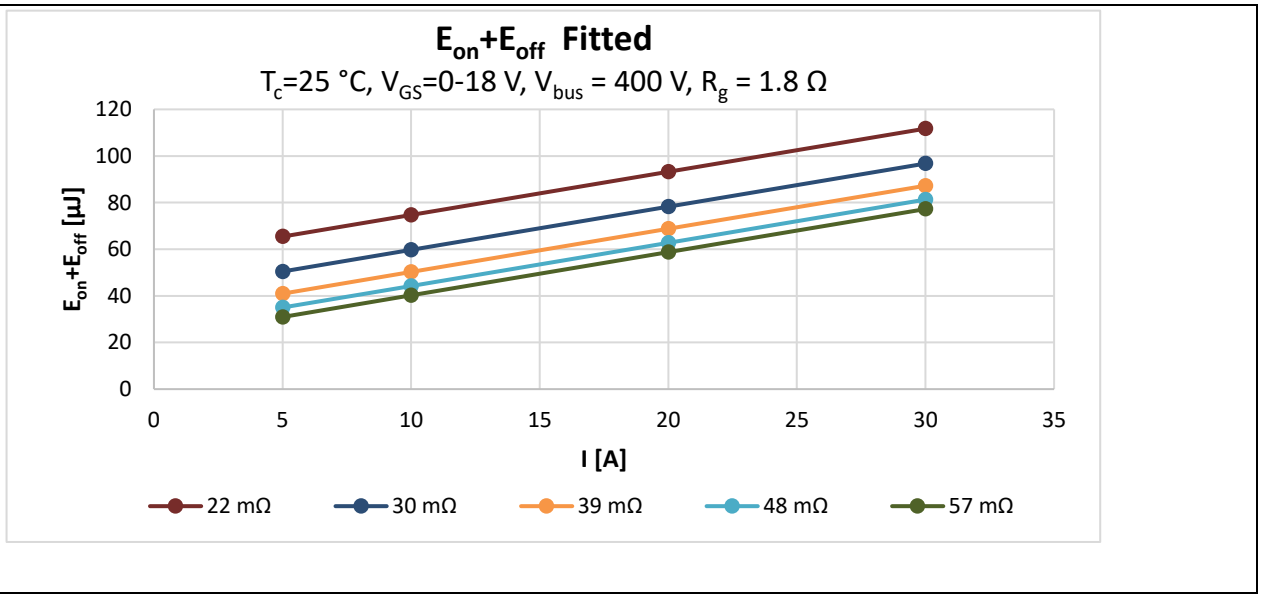


Figure 14 Fitted equation E_{on} + E_{off} switching losses for different $R_{DS(on)}$

Since the switching current in a PFC application varies across the AC-line cycle, the average inductor current can be used to calculate the average switching losses across the AC-line cycle.

The average input current is given as:

$$I_{L.avg} = \frac{P_o}{V_{ac}} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = \frac{3300\ W}{230\ V} \cdot \frac{2 \cdot \sqrt{2}}{\pi} = 12.9\ A \quad \text{Eq. 19}$$

Using Eq. 18 for the average inductor current and $R_{DS(on)}$ of 48 mΩ, E_{on} + E_{off} is:

$$E_{on,off} = (1.85 \cdot I + \frac{1.24}{RDS_{on}})\ \mu J = 1.85 \cdot 12.9 + \frac{1.24}{0.048} = 49.7\ \mu J$$ Eq. 20

Turn-on and turn-off switching loss:

$$P_{S.sw} = E_{on,off} \cdot f = 49.7 \mu J \cdot 65 \cdot 10^3 Hz = 3.2\ W$$ Eq. 21

Gate drive loss:

$$P_{S.g} = V_g \cdot Q_g \cdot f = 18\ V \cdot 33nC \cdot 65 \cdot 10^3 Hz = 0.04\ W$$ Eq. 22

Total loss during the boost switch mode (half line cycle):

$$P_{S.total} = P_{S.cond} + P_{S.sw} + P_{S.g} = 6.9\ W$$ Eq. 23

3.4.2 CoolSiC™ losses during operation as a boost rectifier

The switch operation as a rectifier will mainly have conduction loss, body diode conduction loss and gate drive loss. The body diode reverse recovery loss occurs in the other FET and is already included in the E_{on} loss characterized in the previous section.

Conduction loss when the channel is turned on can be calculated by the following equations:

$$I_{R.rms} = \frac{P_o}{V_{ac}} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{ac}}{3 \cdot \pi \cdot V_o}} = \frac{3300\ W}{230\ V} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot 230V}{3 \cdot \pi \cdot 400V}} = 11.9\ A$$ Eq. 24

$$P_{R.cond} = I_{S.rms}^2 \cdot R_{on(125°C)} = (11.9\text{A})^2 \cdot (0.048\Omega \cdot 1.2) = 8.2\ W$$ Eq. 25

$$where\ R_{on(125°C)} = 1.2 \cdot R_{on(25°C)}$$

When the channel is turned off, the CoolSiC™ body diode carries the current during the dead times. Typically the associated body diode conduction loss is small; however, in higher switching frequency applications, the dead time percentage of the switching period becomes higher, and its associated power loss becomes noticeable.

The average inductor current $I_{L.avg}$ = 12.9 A (Eq. 19) passes through the body diode voltage drop (V_{SD}) during the dead times before turn-on and after turn-off. V_{SD} is equal to ~3.5 V at I_{SD} = 12.9 A, therefore the reverse conduction loss can be calculated as:

$$P_{R.reverse.cond} = 2 \cdot I_{L.avg} \cdot V_{SD} \cdot DeadTime \cdot f = 2 \cdot 12.9A \cdot 3.5V \cdot 100ns \cdot 65kHz = 0.59\text{W}$$ Eq. 26

Gate drive loss is defined as:

$$P_{S.g} = V_g \cdot Q_g \cdot f = 18\ V \cdot 33nC \cdot 65 \cdot 10^3 Hz = 0.04\ W$$ Eq. 27

Total loss during the rectifier switch mode (half line cycle):

$$P_{R.total} = P_{R.cond} + P_{R.g} + PR.reverse.cond = 8.8\ W$$ Eq. 28

Total CoolSiC™ loss across a full line cycle:

$$P_{CoolSiC.total} = \frac{P_{S.total} + P_{R.total}}{2} = 7.9W$$ Eq. 29

3.5 Line rectifier MOSFET

The line rectifier chosen is CoolMOS™ IPW60R017C7. Each rectifier MOSFET conducts for a half line cycle to carry the line current, and only conduction loss is considered since it operates at line frequency.

RMS current and conduction loss are:

$$I_{CoolMOS.rms} = \frac{P_o}{V_{ac}} \cdot \sqrt{0.5} = \frac{3300\ W}{230\ V} \cdot \sqrt{0.5} = 10.1A \quad \text{Eq. 30}$$

$$P_{CoolMOS.cond} = {I_{CoolMOS.rms}}^2 \cdot R_{on(80℃)} = (5.8\ A)^2 \cdot 0.015\ \Omega \cdot 1.5 = 2.3\ W \quad \text{Eq. 31}$$

$$where\ R_{on(80℃)} = 1.5 \cdot R_{on,typ(25℃)}$$

3.6 Output capacitor

The output capacitor is sized to meet both the hold-up time and the low-frequency voltage ripple requirements. The capacitor value is selected to have the larger value between the two equations below:

$$C_o \geq \frac{2 \cdot P_o \cdot t_{hold}}{{V_o}^2 - {V_{o.min}}^2} = \frac{2 \cdot 3300W \cdot 10 \cdot 10^{-3} sec}{(400V)^2 - (340V)^2} = 1486\ \mu F \quad \text{Eq. 32}$$

$$C_o \geq \frac{P_o}{2 \cdot \pi \cdot f_{line} \cdot \Delta V_o \cdot V_o} = \frac{3300W}{2 \cdot \pi \cdot 60Hz \cdot 20V \cdot 400V} = 1094\ \mu F \quad \text{Eq. 33}$$

$$\rightarrow C_o = max\ (1486\ \mu F\ , 1094\ \mu F) = 1486\ \ \mu F$$

In this design we used four parallel 470 µF capacitors, with dissipation factor (tan δ) of 0.2, and consequently the capacitor ESR loss is obtained as:

$$ESR = \frac{DF}{2 \cdot \pi \cdot f \cdot C_o} = \frac{0.2}{2 \cdot \pi \cdot 120Hz \cdot (4 \cdot 470\ \mu F)} = 0.141\ \Omega \quad \text{Eq. 34}$$

The capacitor RMS current and power loss across the line cycle can be calculated by the following equations:

$$I_{Co.rms} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot {P_o}^2}{3 \cdot \pi \cdot V_{ac} \cdot V_o} - \frac{{P_o}^2}{{V_o}^2}} = \sqrt{\frac{8 \cdot \sqrt{2} \cdot (3300\ W)^2}{3 \cdot \pi \cdot 230V \cdot 400\ V} - \frac{(3300\ W)^2}{(400\ V)^2}} = 8.6\ A \quad \text{Eq. 35}$$

$$P_{Co} = {I_{Co.rms}}^2 \cdot ESR = (8.6A)^2 \cdot 0.141\ \Omega = 10.4\ W \quad \text{Eq. 36}$$

4 Experimental and modeling results

The design example discussed in this document was modeled in Mathcad®. All of the power loss equations were written as a function of the output power in order to be able to plot an estimated efficiency curve across the output power range as shown in **Figure 15** (left). The experimental efficiency curve of this design example (evaluation board) is shown in **Figure 15** (right).

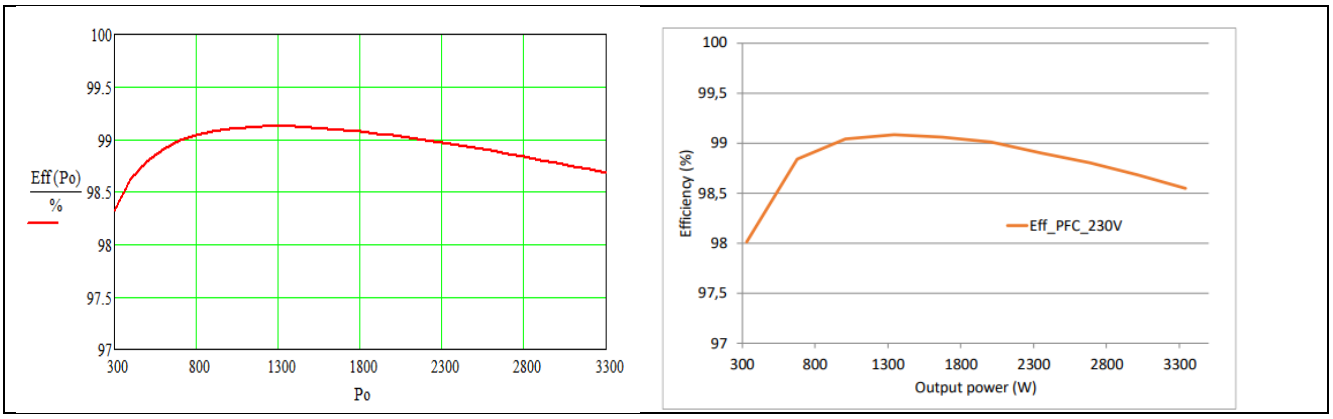


Figure 15 Calculated efficiency (left) vs. experimental efficiency (right) at 230 V AC

Figure 16 shows a breakdown of the main power losses at 230 V AC, 50 percent and 100 percent load condition.

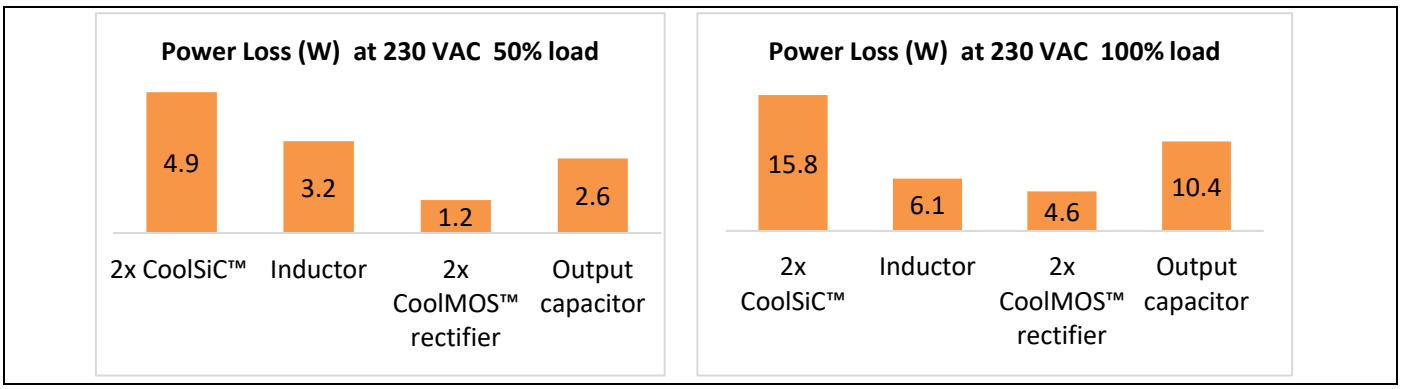


Figure 16 Breakdown of main power losses at 50 percent and 100 percent load conditions

Figure 17 shows the CoolSIC™ conduction vs. switching losses (for two FETs) at 50 percent and 100 percent load conditions.

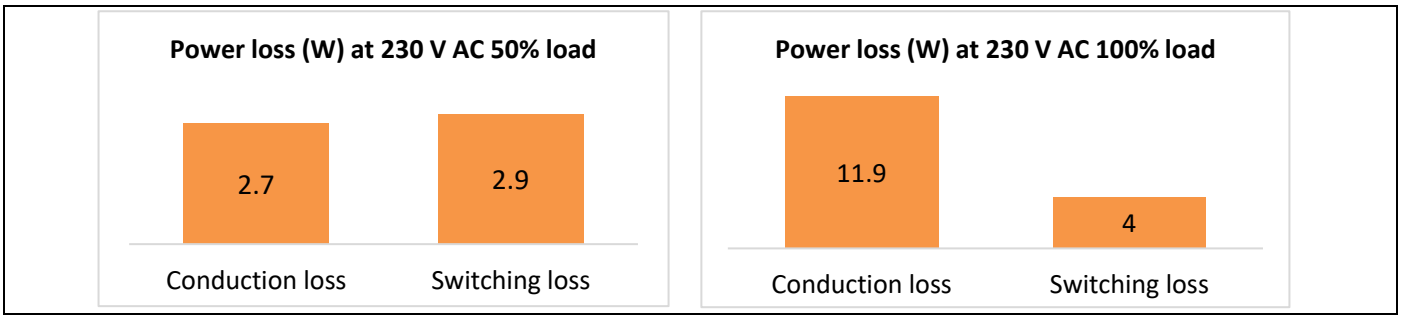


Figure 17 CoolSiC™ conduction vs. switching losses (for two FETs) at 50 percent and 100 percent load conditions

5 Board design

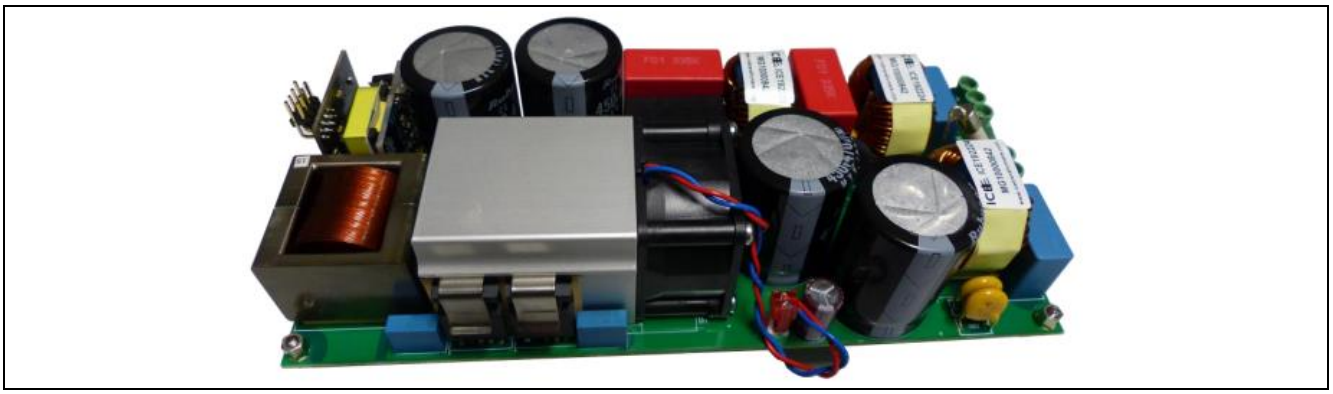


Figure 18 Evaluation board EVAL_3K3W_TP_PFC_SIC

5.1 Schematics

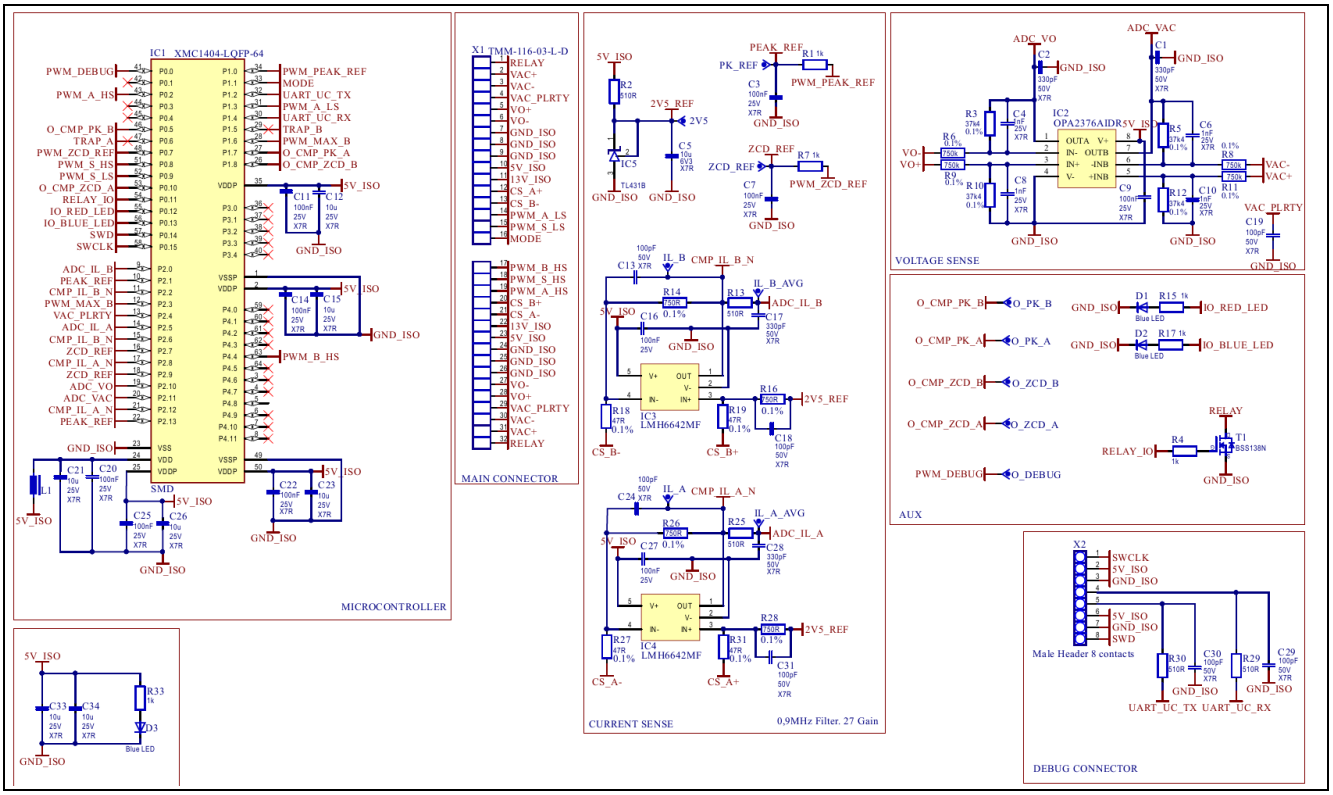


Figure 19 Control board schematic

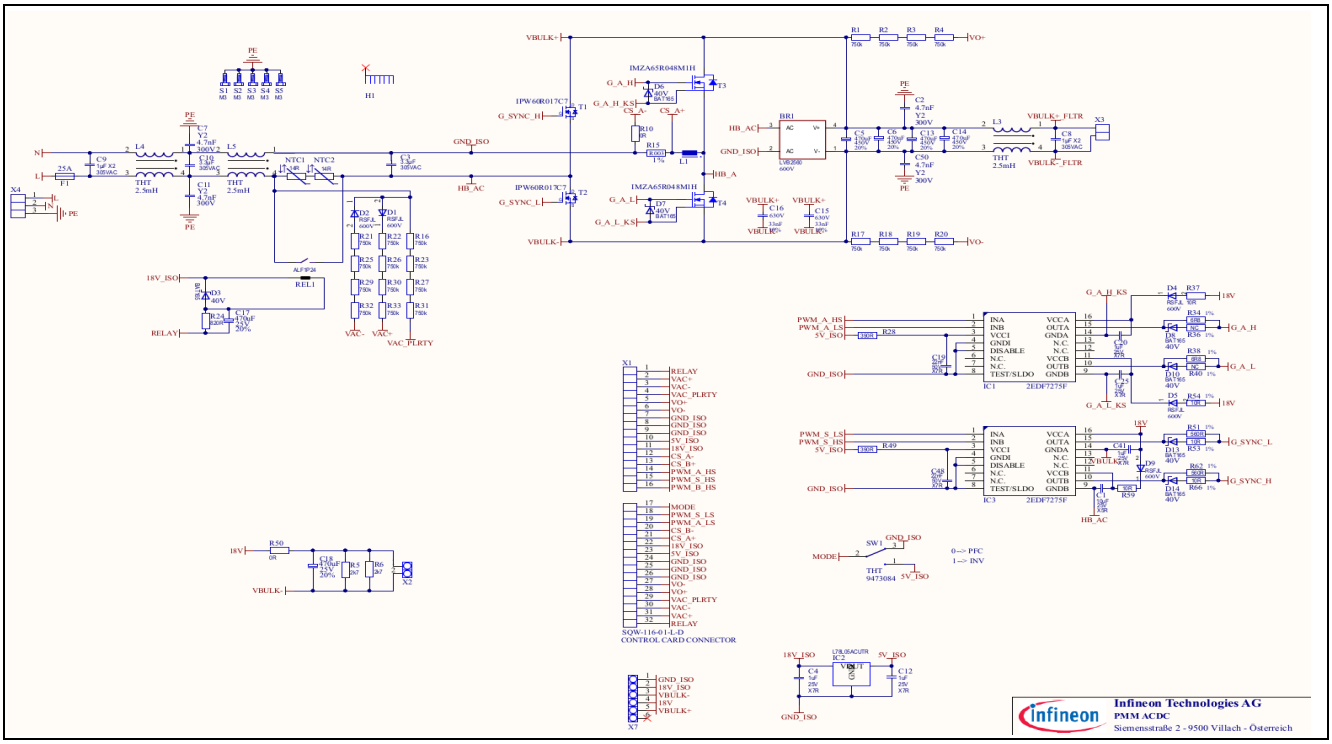


Figure 20 Main board schematic

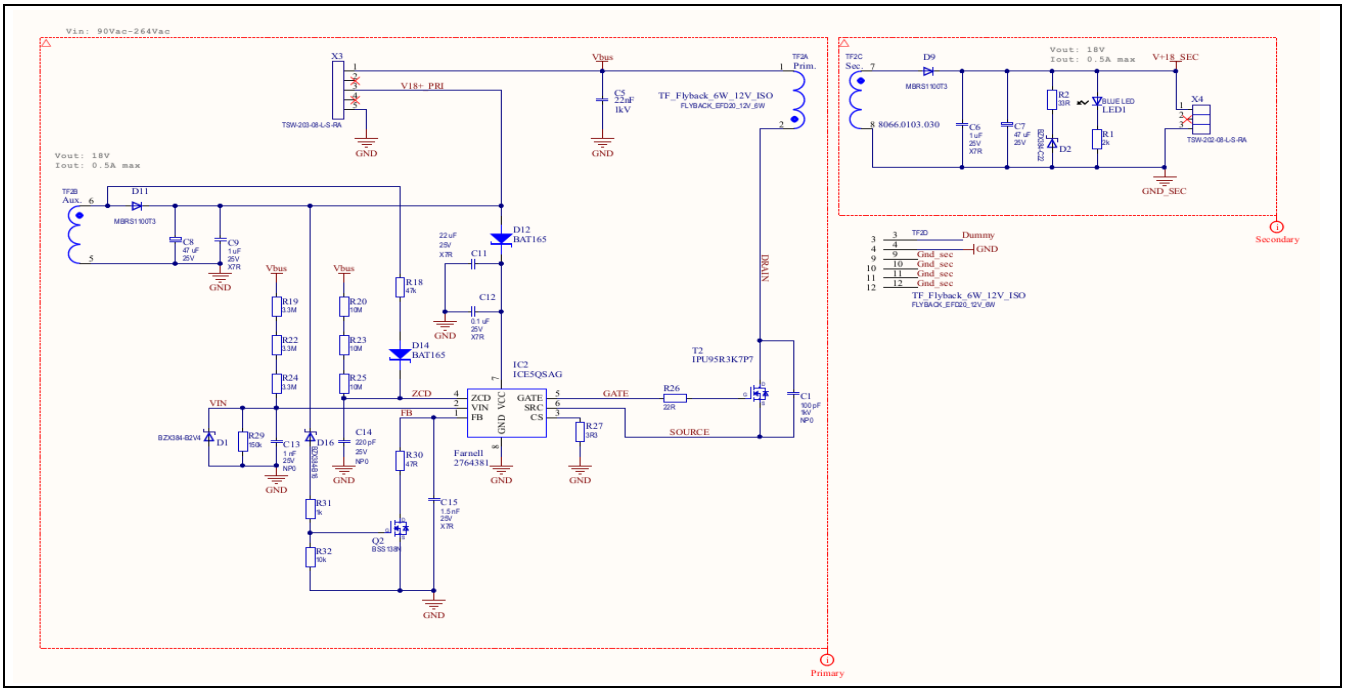


Figure 21 Bias board schematic

More details on the board design and bill of materials are available in the “3300 W CCM bi-directional totem pole with 650 V CoolSiC™ and XMC™” application note **[1]**.

References

[1] Infineon Technologies AG: *3300 W CCM bi-directional totem pole with 650 V CoolSiC™ and XMC™;* **Available online**

[2] Infineon Technologies AG: *PFC boost converter design guide*; **Available online**

[3] Infineon Technologies AG: *CoolGaN™ totem-pole PFC design guide and power loss modeling*; **Available online**

[4] Magnetics®: *Magnetics Powder Core Catalog 2020*; **Available online**

Symbols used in formulas

Table 3 Symbols used in formulas

V AC	Input voltage
V_o	Output voltage
P_o	Output power
f	Switching frequency
T	Switching time period
f_{line}	Line frequency
L	Filter inductor
%Ripple	Inductor current ripple percentage of input current
DC_R	Inductor DC resistance
$R_{on(125C)}$	MOSFET on-resistance at 125°C
Q_g	MOSFET total gate charge
R_g	MOSFET gate resistance
ESR	Output capacitor resistance
t_{hold}	Hold-up time
$V_{o.min}$	Hold-up minimum output voltage
ΔV_{out}	Output voltage ripple

Revision History

Document revision	Date	Description of changes
V 1.0	2023-02-14	Initial release

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Edition 2023-02-14
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_2212_PL52_2301_194003

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