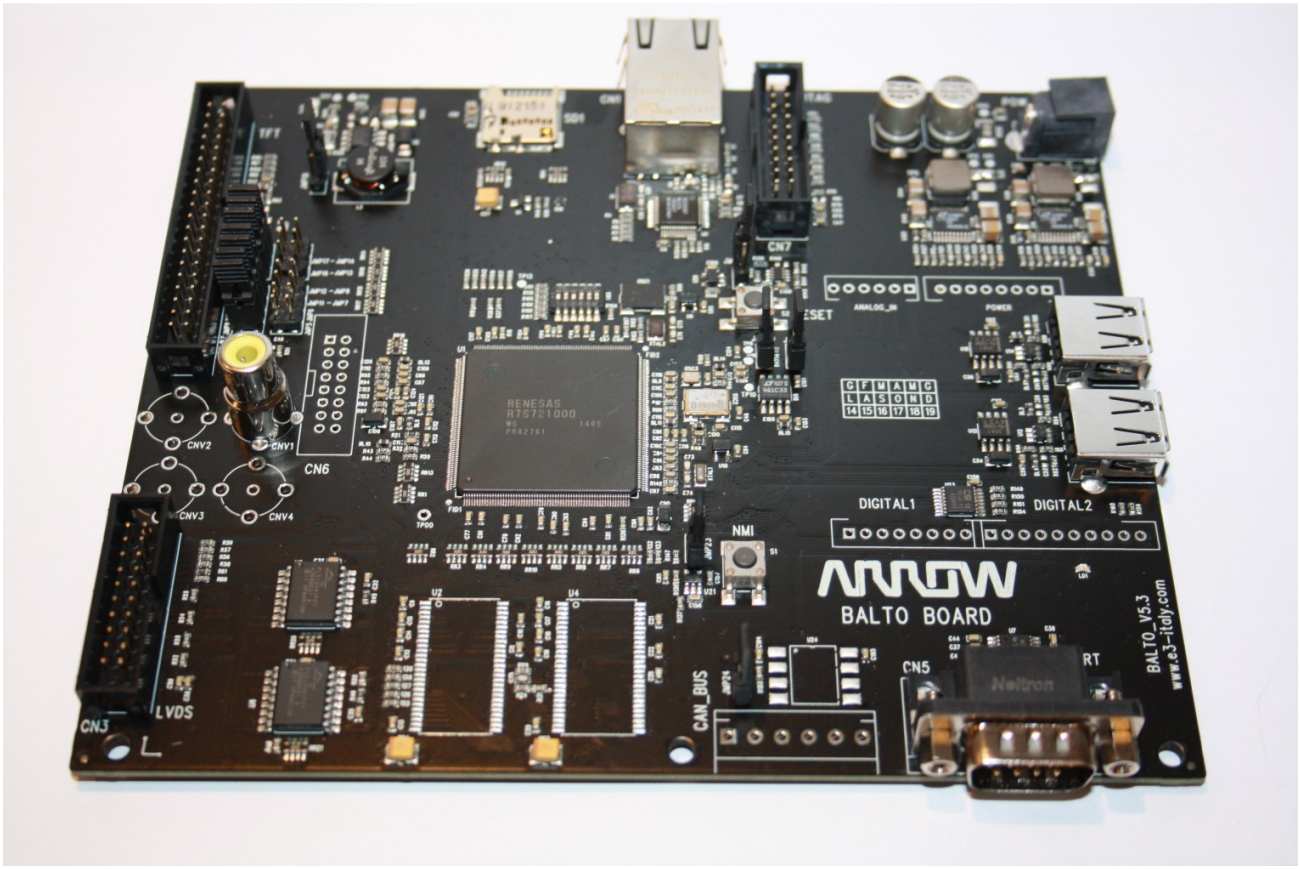
BALTO BOARD



Five Years Out

Hardware Manual

INDEX

1. Overview

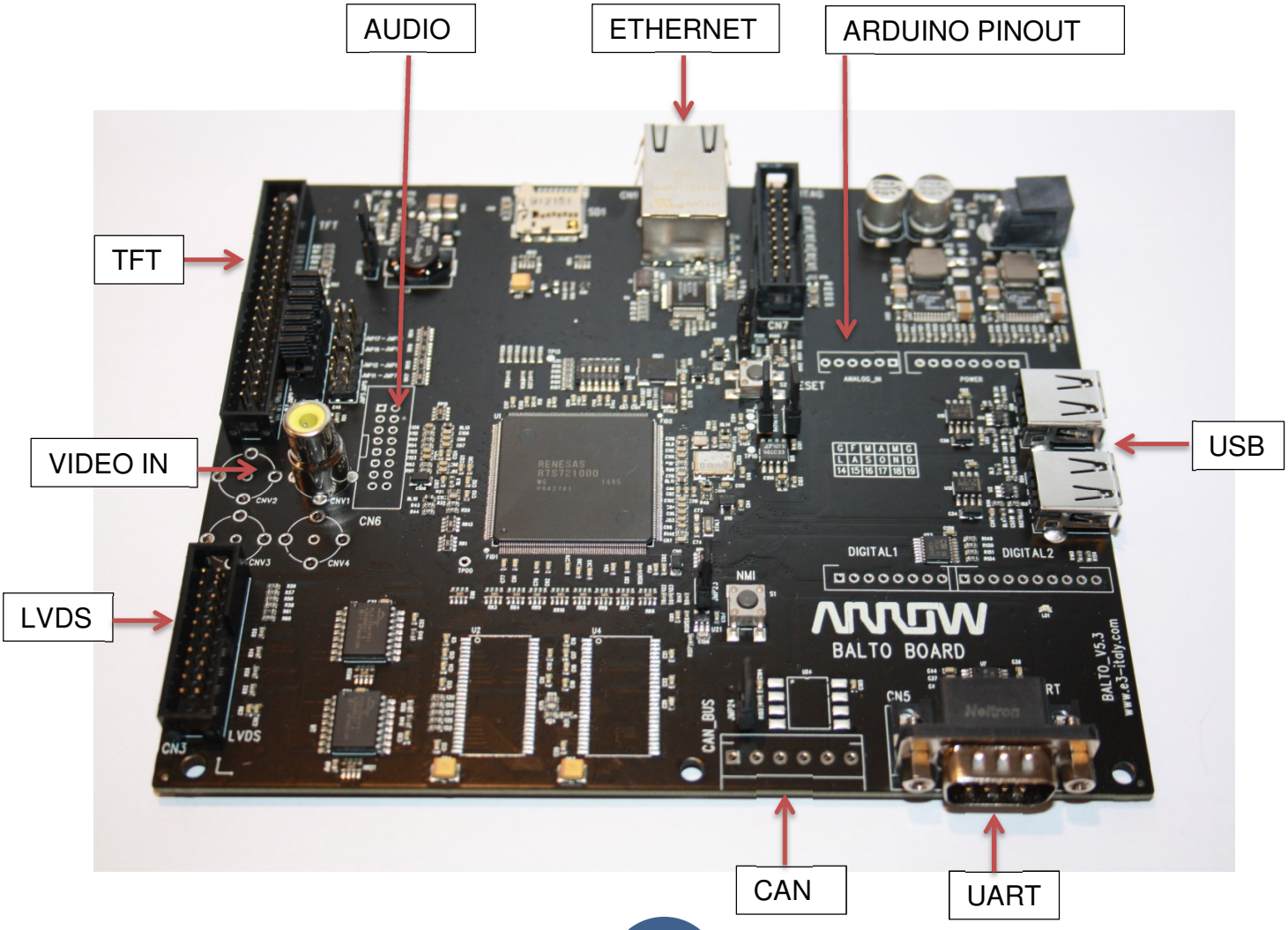
1.1 Purpose

This Balto Board is an evaluation tool for RZ Renesas microcontrollers. This manual describes the technical details of the Balto Board hardware. The Quick Start Guide and Tutorial Manual provide details of the software installation and debugging environment.

1.2 Features

This Balto Board provides an evaluation of the following features:

- RZ/A1H ARM® Cortex™-A9 processor
- TFT TTL and LVDS output
- Audio Output (only with LVDS output)
- Video IN (PAL\NTSC)
- CAN
- UART
- N°2 USB Host
- Ethernet
- Arduino pinout compatible
- N°2 QSPI Flash (64 MB tot)
- Optional SDRAM



2. Power Supply

2.1 Requirements

This Balto Board is supplied without a SEGGER JLink-Lite debugger. **This Balto Board is supplied with a 5Vdc Power Supply using a 5.0mm barrel power jack**

2.2 Power-Up Behaviour

When the Balto Board is supplied, the Balto Board has a Linux BSP pre-programmed with Balto Board WebServer demo:

- connect UART debug to the computer and to Balto Board Uart connector (CN5)
- open a serial terminal with the required settings (115200 bauds, 8-N-1 with no hardware flow control)
- connect the Ethernet cable between computer and the Balto Board Ethernet connector (CN1).
- set up computer with static IP address to 192.168.84.70, the Netmask to 255.255.255.0
- open firefox browser to 192.168.84.170\demo address
- with webpage you can torn on, turn off and heartbeat LED and startup a SSH terminal

3. Board Layout

Balto Board Layout, component placement and board dimension you can find to the **Component Layout & Component Placement.pdf** document.

4. User Circuitry

4.1 Clock Circuit

Clock circuits are fitted to the Balto Board to generate the required clock signals to drive the MCU, and associated peripherals. Refer to the RZ/A1H Group Hardware Manual for details regarding the clock signal requirements, and the Balto Board schematics for information regarding the clock circuitry in use on the Balto Board.
Details of the oscillators fitted to the board are listed in Table 4-1 below.

Crystal/Oscillator	Function	Default Placement	Frequency
OSC1	Audio oscillator	Fitted	22.5792MHz
OSC2	USB Clock	Fitted	48.000MHz
OSC3	Main MCU oscillator	Fitted	12.5MHz
XTAL1	RTC 1 clock	Fitted	32.768kHz
XTAL2	Video oscillator	Fitted	27.000MHz

Table 4-1: Oscillators

4.2 RCA Video Input

The Balto Board provides two channels of RCA video input to the RZ/A1H MCU, on connectors CNV1, CNv2, CNV3 and CNV4 (only CNV1 fitted). These connect to the RZ/A1H MCU on pins VIN1A, VIN2A, VIN1B, VIN2B respectively, via 100nF decoupling capacitors. Refer to the Balto Board schematics for further information.

4.3 Switches

There are two switches located on the Balto board. The function of each switch and its connection is shown in Table 4-2. For further information regarding switch connectivity, refer to the Balto Board schematics.

Switch	Function	MCU Port
S1	Connects to the non-maskable input for user controls.	NMI
S2	When pressed, the microcontroller is reset.	RES

Table 4-2: Switch Connections

4.4 Port Expander

The Balto Board utilise one port expander ICs, U23 in order to provide more I/O signals. This device is the CAT9554 from On Semiconductor. For further information on these devices visit the On Semiconductor website at www.onsemi.com.
The port expander provide 8 parallel I/O lines each, which can be accessed via an I2C/SMBus serial connection. On the Balto Board, it is able to be accessed at addresses on I2C channel 2 on the MCU. The I2C logical address for I U23 is 0x40. Table 4-3 details the signal connections to U23.

Port Number	Signal name	Function
0	IO1	Arduino connector Digital 1
1	IO3	Arduino connector Digital 1
2	IO6	Arduino connector Digital 1
3	IO7	Arduino connector Digital 2

4	IO11	Arduino connector Digital 2
5	IO12	Arduino connector Digital 2
6	LD1	LED output control. Output low = OFF, output high = ON
7	IRQ_IO	External Interrupt P1_6

Table 4-3: Port Expander U23 Connection Details

4.5 CAN

There is one CAN channel which connect to the MCU as listed in Table 4-4.

CAN Signal	Function	MCU Port
CAN_CTX0	CAN Channel 0 Transmit	P9_0
CAN_CRX0	CAN Channel 0 Receive	P9_1

Table 4-4: CAN Connection

4.6 SD

The Balto Board provides an SD card socket, CN2. The connections are detailed in Table 4-5.

SD Signal	Function	MCU Port
SD_POW	Power	P4_9
SD_CMD	Command I/O	P4_13
SD_CLK	Clock	P4_12
SD_DEC	Card Detect	P4_8
SD_DAT0	Data 0	P4_11
SD_DAT1	Data 1	P4_10
SD_DAT2	Data 2	P4_14
CD_SD_DAT3	Data 3	P4_15

Table 4-5: SD Connection

4.7 SDRAM

The SDRAMs, **not fitted**, on the Balto Board are configured in hardware to use the Chip Select line CS2 and CS3. The connections are detailed in Table 4-6.

SDRAM Signal	Function	MCU Port
D0	Data bus	P6_0
D1	Data bus	P6_1
D2	Data bus	P6_2
D3	Data bus	P6_3
D4	Data bus	P6_4
D5	Data bus	P6_5
D6	Data bus	P6_6
D7	Data bus	P6_7
D8	Data bus	P6_8
D9	Data bus	P6_9
D10	Data bus	P6_10
D11	Data bus	P6_11
D12	Data bus	P6_12

D13	Data bus	P6_13
D14	Data bus	P6_14
D15	Data bus	P6_15
A1	Address bus	P7_9
A2	Address bus	P7_10
A3	Address bus	P7_11
A4	Address bus	P7_12
A5	Address bus	P7_13
A6	Address bus	P7_14
A7	Address bus	P7_15
A8	Address bus	P8_0
A9	Address bus	P8_1
A10	Address bus	P8_2
A11	Address bus	P8_3
A12	Address bus	P8_4
A13	Address bus	P8_5
A14	Address bus	P8_6
A15	Address bus	P8_7
CS2	Chip select	P5_8
CS3	Chip select	P7_1
RAS	Row Address Strobe Command	P7_2
CAS	Column Address Strobe Command	P7_3
RDWR	Write Enable	P7_5
DQMLU	x16 Upper Byte Input/Output Mask	P7_6
DQMLL	x16 Lower Byte Input/Output Mask	P7_7
CKE	Clock Enable	P7_4
CKIO_SD1 & CKIO_SD2	System Clock	CKIO

Table 4-6: SDRAM Connection

4.8 Dual QSPI Flash

The Balto Board provides two 64MByte Serial Flash memory ICs, U5 and U6, which connect to the RZ/A1 MCU via the SPI Multi I/O Bus Controller. Signal Connections are detailed in Table 4-7 below.

Signal	Function	MCU Port
SPBCLK_0	Serial Clock (Common)	P9_2
SPBSSL_0	Chip Select (Common)	P4_13
RESET	Device Reset (Common)	RES
SPBIO00_0	Serial Input / IO_0 (U5)	P9_4
SPBIO10_0	Serial Input / IO_1 (U5)	P9_5
SPBIO20_0	Write Protect / IO_2 (U5)	P9_6
SPBIO30_0	Hold / IO_3 (U5)	P9_7
SPBIO01_0	Serial Input / IO_0 (U6)	P2_12

SPBIO11_0	Serial Input / IO_1 (U6)	P2_13
SPBIO21_0	Write Protect / IO_2 (U6)	P2_14
SPBIO31_0	Hold / IO_3 (U6)	P2_15

Table 4-7: SPI Flash Connection

4.8.1 QSPI Modes of Operation

There are several modes of operation of the QSPI memory in conjunction with the serial memory controller in the RZ/A1H MCU. On the Balto Board, there are two QSPI memory devices, attached to ports 0 and 1, of the Multi I/O SPI controller's channel 0.

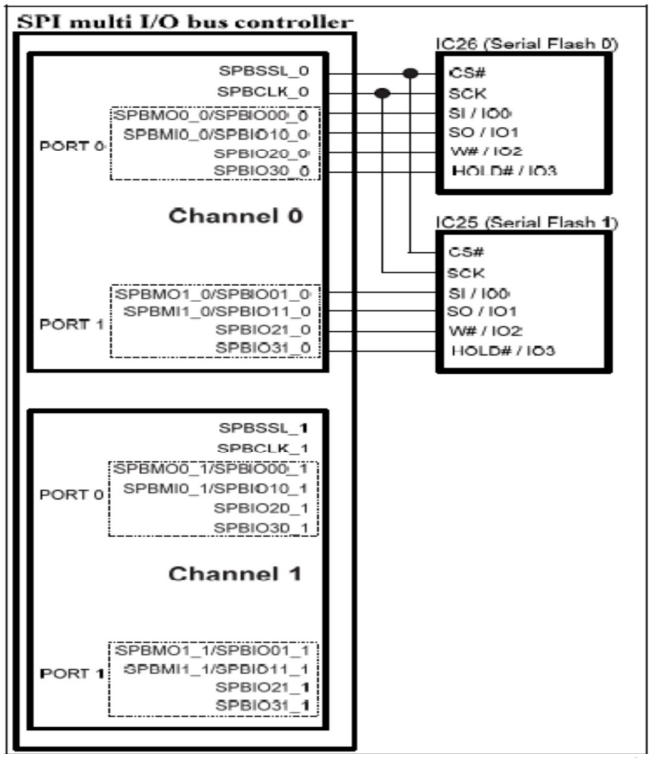


Figure 4-1: RZ/A1H SPI multi I/O controller

Each QSPI memory device can support one, two or four simultaneous serial lines of I/O. Furthermore, the controller allows each channel's ports to work in parallel, providing up to eight simultaneous serial lines of I/O in dual QSPI mode. During the QSPI boot mode Port 0 is used and is accessed using only the clock, SPBMO0 and SPBMI0 signals (Single bit Single channel).

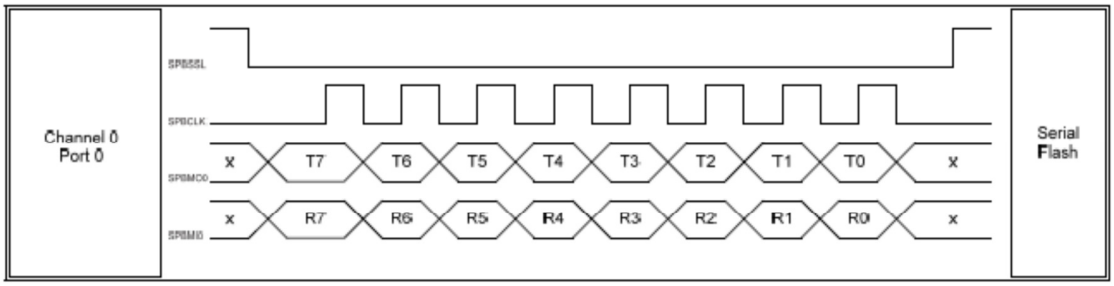


Figure 4-2: Single bit single channel operation mode

It is important to recognize that these eight lines are serial inputs, and are not operating on the same byte, but successive bytes. When operating over the two ports it should be noted that the memory structure is fundamentally different from single channel operation, as lines 1-4 are working with the memory on Port 0 and 5-8 are working with Port 1. Figure 4-3 attempts to show this visually.

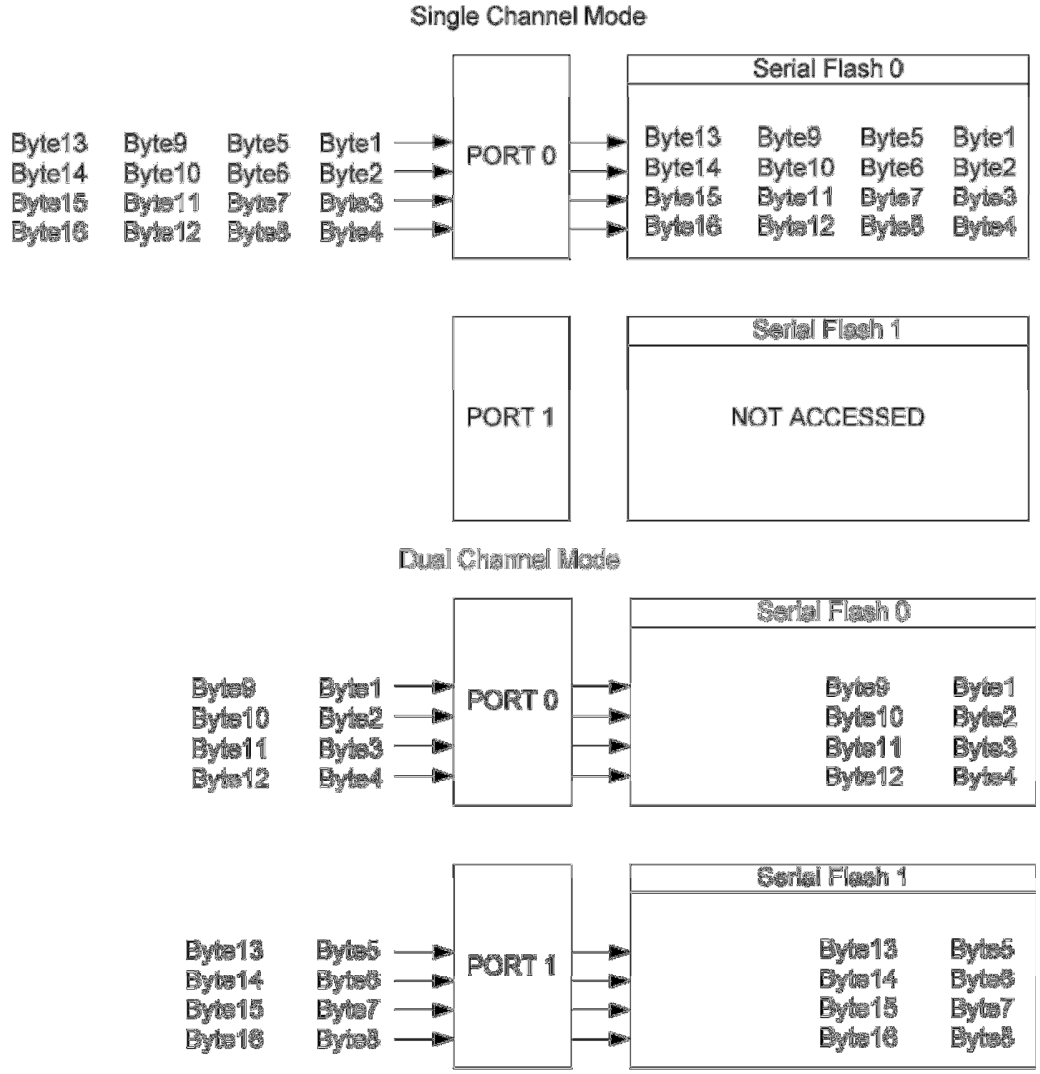


Figure 4-3: Memory access of Single and Dual Mode QSPI Operation

The consequence of this is that data stored in QSPI FLASH needs to be accessed in the same manner as it has been programmed in. If data is accessed in Single QSPI mode when it has been programmed in Dual QSPI mode, then every fourth group of four bytes will be missing. Conversely data accessed in Dual Channel mode when it has been programmed in Single Channel mode will have blocks of four bytes from the other port inserted between every fourth byte of correct data.

4.9 Universal Serial Bus (USB)

This Balto Board is fitted with two channels of USB. Each channel can operate as host. The signal connections to the MCU for Channel 0 and Channel 1 are detailed in Table 4-8 and Table 4-9 respectively.

Signal	Function	MCU Port
VBUS0	Cable monitor pin.	VBUS0
DP0	Positive differential data signal.	DP0
DM0	Negative differential data signal.	DM0

Table 4-8: USB0 Module MCU Connections

Signal	Function	MCU Port
VBUS1	Cable monitor pin.	VBUS1
DP1	Positive differential data signal.	DP1
DM1	Negative differential data signal.	DM1

Table 4-9: USB1 Module MCU Connections

4.10 Ethernet

This Balto Board is fitted with an Ethernet connection. The connections from the Ethernet driver IC, U3, are detailed in Table 4-10. Refer to the Balto Board schematics for further information.

Signal	Function	MCU Port
ET_MDC	Management data clock	P5_9
ET_MDIO	Management data I/O	P3_3
ET_RXCLK	Receive clock	P3_4
ET_RXD3	MII receive data	P2_11
ET_RXD2	MII receive data	P2_10
ET_RXD1	MII receive data	P2_9
ET_RXD0	MII receive data	P2_8
ET_RXDV	Receive data valid	P3_6
ET_RXER	Receive error	P3_5
ET_TXEN	Transmit enable	P2_2
ET_TXD0	MII transmit data	P2_4
ET_TXD1	MII transmit data	P2_5
ET_TXD2	MII transmit data	P2_6
ET_TXD3	MII transmit data	P2_7
ET_TXCLK	Transmit clock	P2_0
ET_CRS	Carrier detection	P2_3
RESET	Connected to reset circuit	
ET_COL	Collision detection	P1_14

Table 4-10: Ethernet Connection

4.11 LEDs

There are two LEDs on the Balto Board. The function of each LED, its color and connection are shown in Table 4-11.

LED	Color	Function
LD1*	YELLOW	User operated LED

LD2	GREEN	Indicates the status of the 3.3V power rail

Table 4-11: LED Connections

*This LED is connected to port expander U23 I/O pin. See section 4.4 for further details.

4.12 Reset Circuit

A reset control circuit is fitted to the Balto Board to generate the required reset signal, and is triggered from the RES switch, power supply monitor and debugger connection. Refer to the RZ/A1 hardware manual for details regarding the reset signal timing requirements and the Balto Board schematics for information regarding the reset circuitry in use on the board.

4.13 Audio

The Balto Board provides an audio interface (CN6) to connect to audio CODEC. The audio data input/output is controlled by the serial sound interface (SSIF) channel 0.
The MCU signals are described in Table 4.12

Signal	Function	MCU Port
SSICK0	Serial bit clock	P4_4
SSIWS0	Word selection	P4_5
SSIRX0	Serial data input	P4_6
SSITDX0	Serial data output	P4_7
MCLK	clock for audio	AUDIO_X1
RSPCK4	Clock I/O pins	P4_0
SSL40	Slave select I/O pins	P4_1
MOSI4	Data I/O pins	P4_2

Table 4-12: Audio Connections

4.14 TFT LCD Panel Connector

A TFT display can connect to the Balto Board, via connector CN4. The signals route to the MCU as described by Table 4.13. Refer to the Balto Board schematic for further information.

TFT TTL Signal	Function	MCU Port
LCD_D00	Video image data 0 for panel	P3_8
LCD_D01	Video image data 1 for panel	P3_9
LCD_D02	Video image data 2 for panel	P3_10
LCD_D03	Video image data 3 for panel	P3_11
LCD_D04	Video image data 4 for panel	P3_12
LCD_D05	Video image data 5 for panel	P3_13
LCD_D06	Video image data 6 for panel	P3_14
LCD_D07	Video image data 7 for panel	P3_15
LCD_D08	Video image data 8 for panel	P4_0
LCD_D09	Video image data 9 for panel	P4_1
LCD_D10	Video image data 10 for panel	P4_2
LCD_D11	Video image data 11 for panel	P4_3
LCD_D12	Video image data 12 for panel	P4_4
LCD_D13	Video image data 13 for panel	P4_5
LCD_D14	Video image data 14 for panel	P4_6

LCD_D15	Video image data 15 for panel	P4_7
LCD0_PCLK	Panel clock 0	P3_0
LCD0_HSYNC	Control signal 0 for panel	P3_2
LCD0_VSYNC	Control signal 0 for panel	P3_1
LCD0_DE	Control signal 0 for panel	P3_7
RES_TOUCH	Touch Reset	P5_10
TOUCH_INT	Touch Init	P1_7
I2C_SDA0	Touch I2C0 Data	P1_1
I2C_SCK0	Touch I2C0 Clock	P1_0

Table 4-13: TFT TTL Connections

4.15 TFT LVDS

A TFT LVDS display can connect to the Balto Board, via connector CN3. The signals route to the MCU as described by Table 4.14. Refer to the Balto Board schematic for further information.

TFT TTL Signal	Function	MCU Port
TXOUT0P	LVDS data output pin 0P	P5_7
TXOUT0M	LVDS data output pin 0M	P5_6
TXOUT1P	LVDS data output pin 1P	P5_5
TXOUT1M	LVDS data output pin 1M	P5_4
TXOUT2P	LVDS data output pin 2P	P5_3
TXOUT2M	LVDS data output pin 2M	P5_2
TXCLKOUTP	LVDS clock output pin CP	P5_1
TXCLKOUTM	LVDS clock output pin CM	P5_0

Table 4-14: TFT LVDS Connections

4.16 Serial Port

A UART can connect to the Balto Board, via connector CN5. The signals route to the MCU as described by Table 4.15. Refer to the Balto Board schematic for further information.

Signal	Function	MCU Port
TXD3	Transmit data output	P8_8
RXD3	Receive data input	P8_9

Table 4-15: Serial Port Connections

4.17 Arduino PinOut

An Arduino PinOut compatible is fitted on the Balto Board, via Header Connection. The signals route to the MCU as described by Table 4.16. Refer to the Balto Board schematic for further information.

Arduino PinOut Signal	Function	MCU Port
ANA_0	Analog In	
ANA_1	Analog In	
ANA_2	Analog In	
ANA_3	Analog In	
ANA_4	Analog In	

ANA_5	Analog In	
TXD3	Digital In/Out	
RXD3	Digital In/Out	
IO1*	Digital In/Out	
IO2_PWM1	Digital In/Out	
IO3*	Digital In/Out	
IO4_PWM2	Digital In/Out	
IO5_PWM3	Digital In/Out	
IO6*	Digital In/Out	
IO7*	Digital In/Out	
IO8_PWM4	Digital In/Out	
IO9_PWM5	Digital In/Out	
IO10_PWM6	Digital In/Out	
IO11*	Digital In/Out	
IO12*	Digital In/Out	

Table 4-13: Arduino PinOut Connections

*This Signal is connected to port expander U23 I/O pin. See section 4.4 for further details.

5. Configuration

5.1 Jumper Link Configuration

Table 5.1 describes the jumper link option configurations available on the Balto Board.

Jumper Link Configuration	Link	Open
JMP5	Serial bit clock for Codec Audio	No Serial bit clock for Codec Audio
JMP6	Word selection for Codec Audio	No Word selection for Codec Audio
JMP7	Serial data input for Codec Audio	No Serial data input for Codec Audio
JMP8	Serial data output for Codec Audio	No Serial data output for Codec Audio
JMP9	Video image data 12 for panel	No Video image data 12 for panel
JMP10	Video image data 13 for panel	No Video image data 13 for panel
JMP11	Video image data 14 for panel	No Video image data 14 for panel
JMP12	Video image data 15 for panel	No Video image data 15 for panel
JMP13	Clock I/O pins for Codec Audio	No Clock I/O pins for Codec Audio
JMP14	Slave select I/O pins for Codec Audio	No Slave select I/O pins for Codec Audio
JMP15	Data I/O pins for Codec Audio	No Data I/O pins for Codec Audio
JMP16	Video image data 8 for panel	No Video image data 8 for panel
JMP17	Video image data 9 for panel	No Video image data 9 for panel
JMP18	Video image data 10 for panel	No Video image data 10 for panel
JMP19	Backlight TFT always ON	Backlight TFT drive to microcontroller
JMP20	Vref from LT1461	No Vref from LT1461
JMP21	External Vref	No External Vref
JMP22	Always reset	No Always reset
JMP23	S1 connect to microcontroller NMI pin	No S1 connect to microcontroller NMI pin

Table 5-1: Jumper Link Configuration

5.2 MCU Boot and Oscillator Configuration

The six-way DIP switch, SW6 provides some configuration options for the Balto Board MCU. Switches 1, 2 and 3 are used to set the boot mode of the RZ/A1H. Table 5.2 provides details of the available modes and the corresponding switch settings. Due to pull-up resistors in the circuit, a “1” is produced when the corresponding switch position is OFF, and a “0” is produced when it is ON.

Switches 4, is used to set Clock Signal Source, Table 5.3 provides details.

Switches 5, is used to set Spread Spectrum Clock Generator, Table 5.4 provides details.

Switches 6, is used to set Boundery Scan, Table 5.5 provides details.

SW6-1	SW6-2	SW6-3	
MD_BOOT0	**MD_BOOT1**	**MD_BOOT2**	**Boot Mode**
ON	ON	–	Boot mode 0 (CS0-space 16-bit booting) Boots the LSI from memory (bus width: 16 bits) connected to the CS0 space. Not supported on Balto Board
ON	OFF	–	Boot mode 1 (CS0-space 32-bit booting) Boots the LSI from memory (bus width: 32 bits) connected to the CS0 space. Not supported on Balto Board

OFF	**ON**	**OFF**	Boot mode 3 (serial flash booting) Boots the LSI from the serial flash memory connected to the SPI multi I/O bus space. The only way of booting this LSI chip is from channel 0 (P9_2 to P9_5) in this mode. Supported on Balto Board
OFF	OFF	ON	Boot mode 4 (eSD booting) Boots the LSI from the NAND flash memory with the SD controller. The only way of booting this LSI chip is from channel 0 (P4_10 to P4_15) in this mode. Supported on Balto Board (not tested)
OFF	OFF	OFF	Boot mode 5 (eMMC booting) Boots the LSI from the NAND flash memory with the MMC controller. The only way of booting this LSI chip is from channel 0 (P3_10 to P3_15) in this mode. Not Supported on Balto Board

Table 5.2: MCU Boot Modes

SW6-4	Clock Signal Source
ON	EXTAL (Uses OSC2, 13.33MHz.)
OFF	USB_X1 (Uses X4, 48MHz.)

Table 5.3: Clock Signal Source

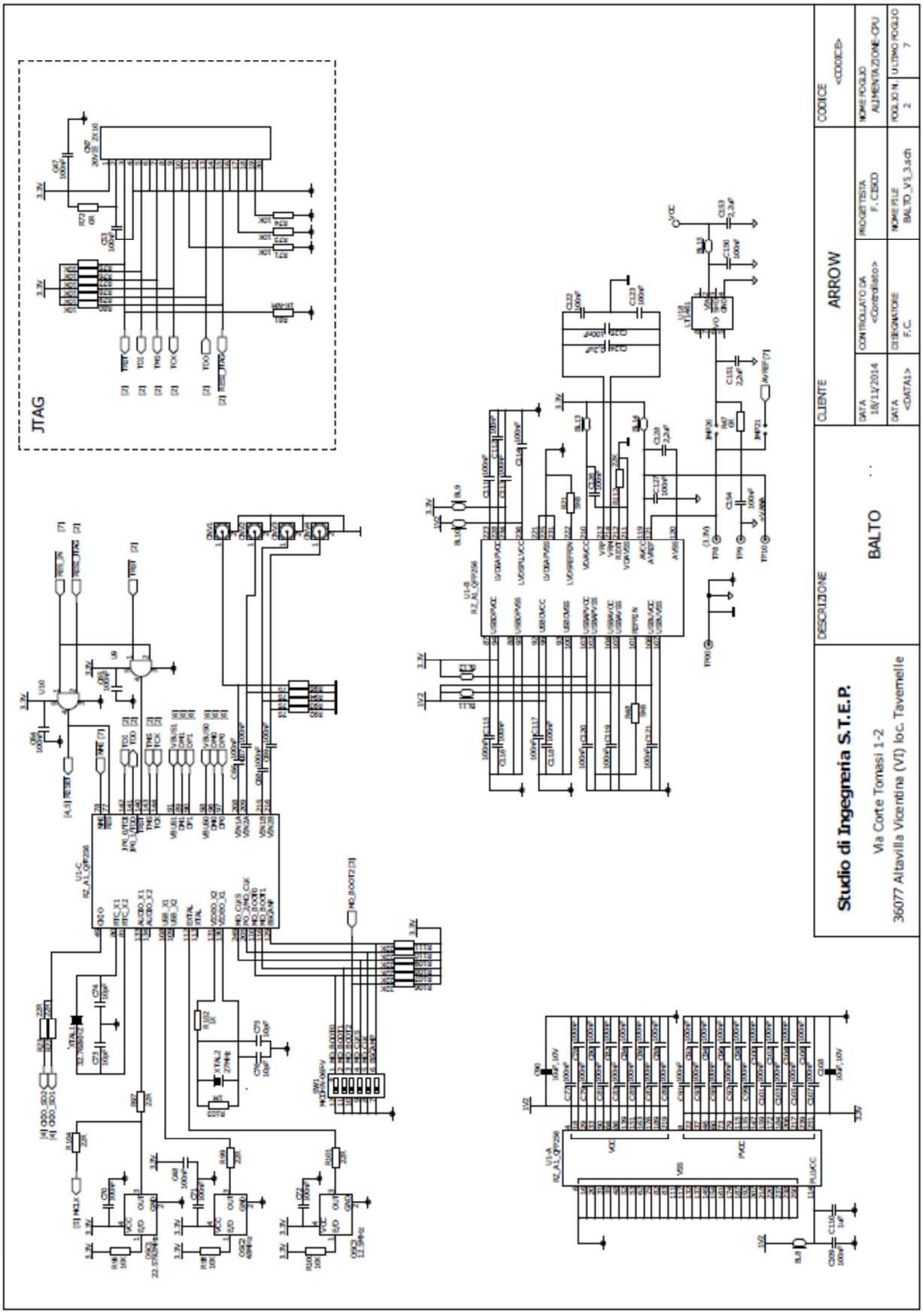
SW6-5	Spread Spectrum Clock Generator (SSCG) Mode
ON	Enables the SSCG function of the MCU's internal PLL circuit. This function attempts to reduce EMI peak levels by slightly modulating the output frequency.
OFF	Disables the SSCG function

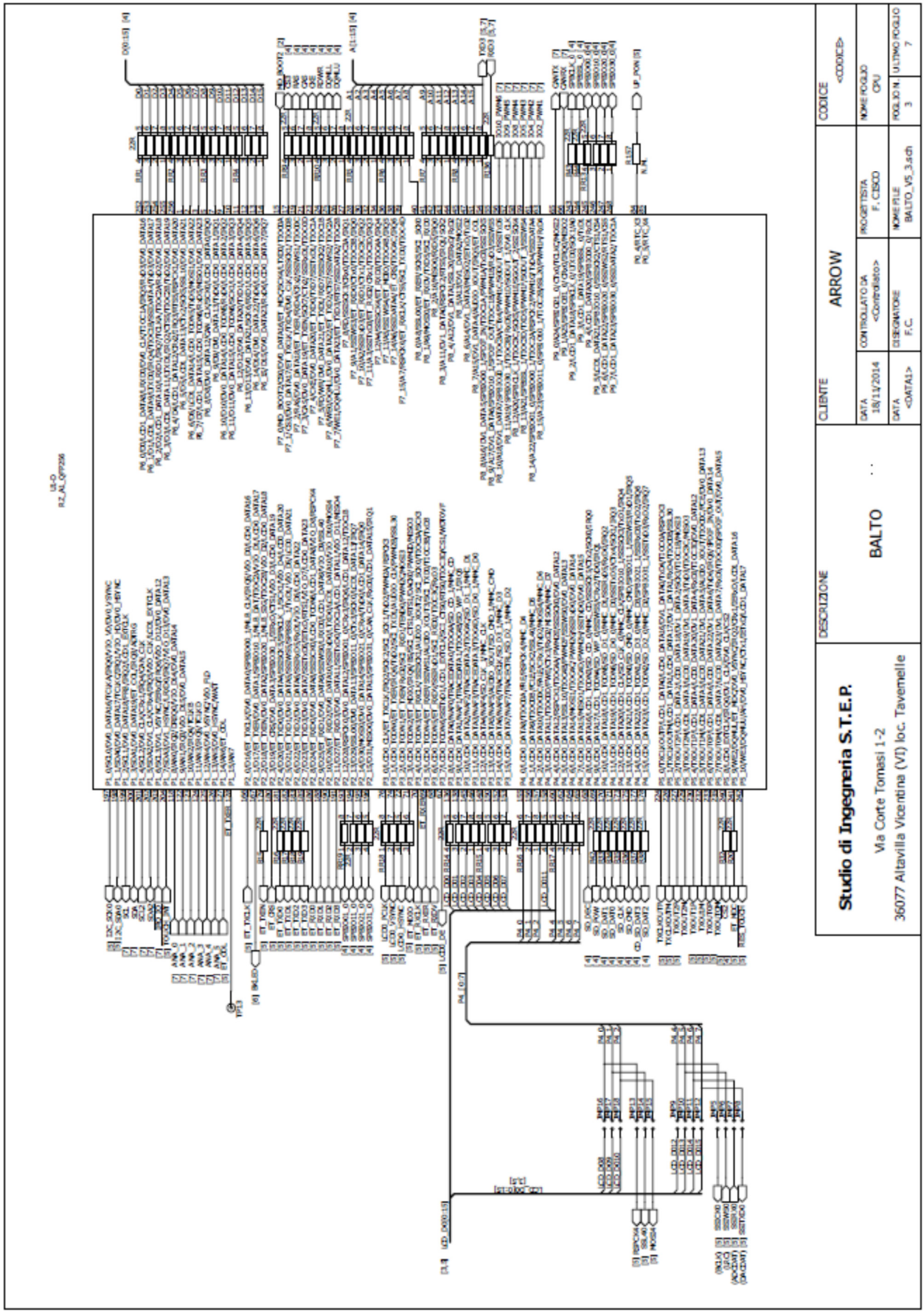
Table 5.4: Spread Spectrum Clock Generator

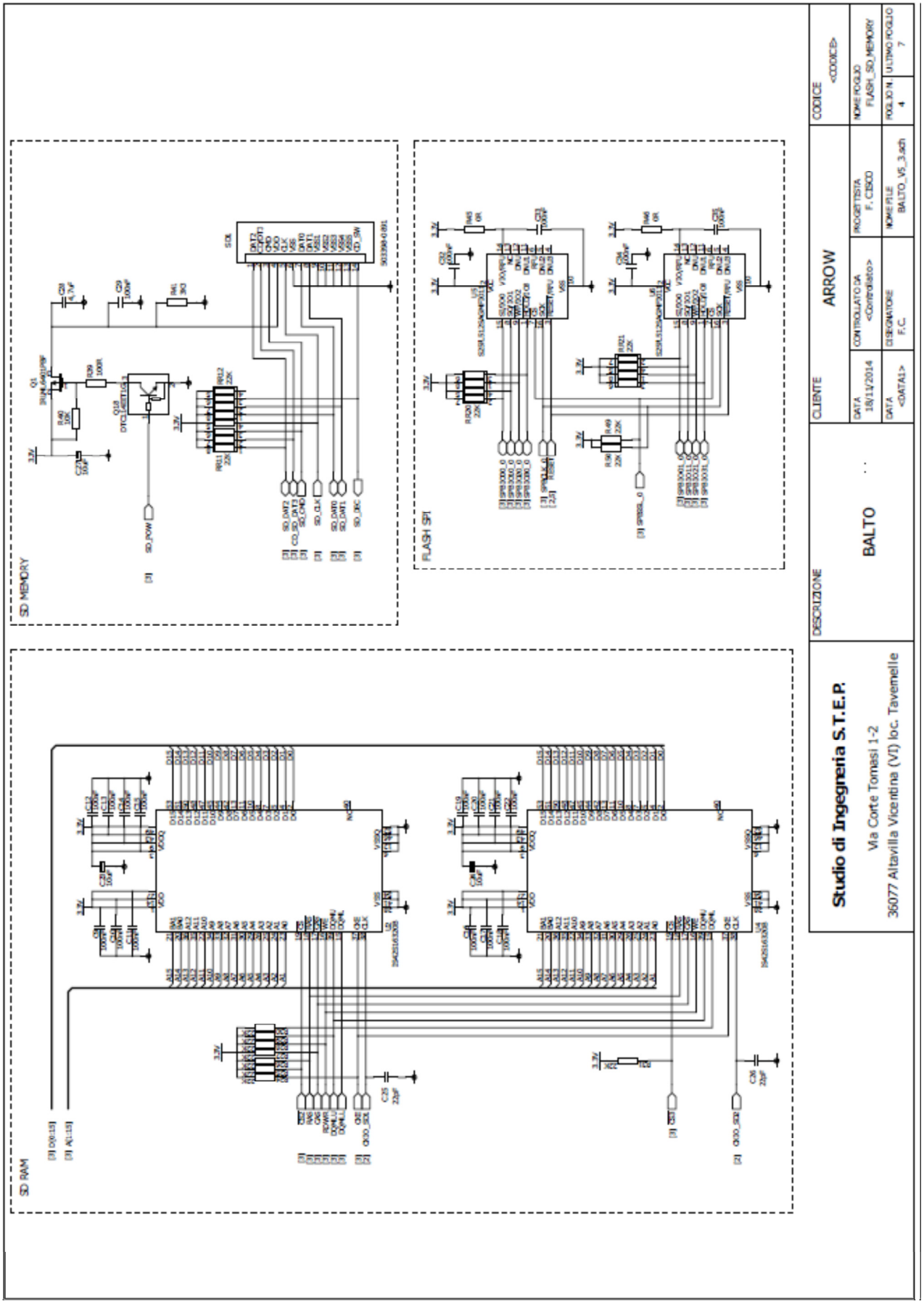
SW6-6	Boundery scan
ON	Normal Operation
OFF	Boundery-Scan

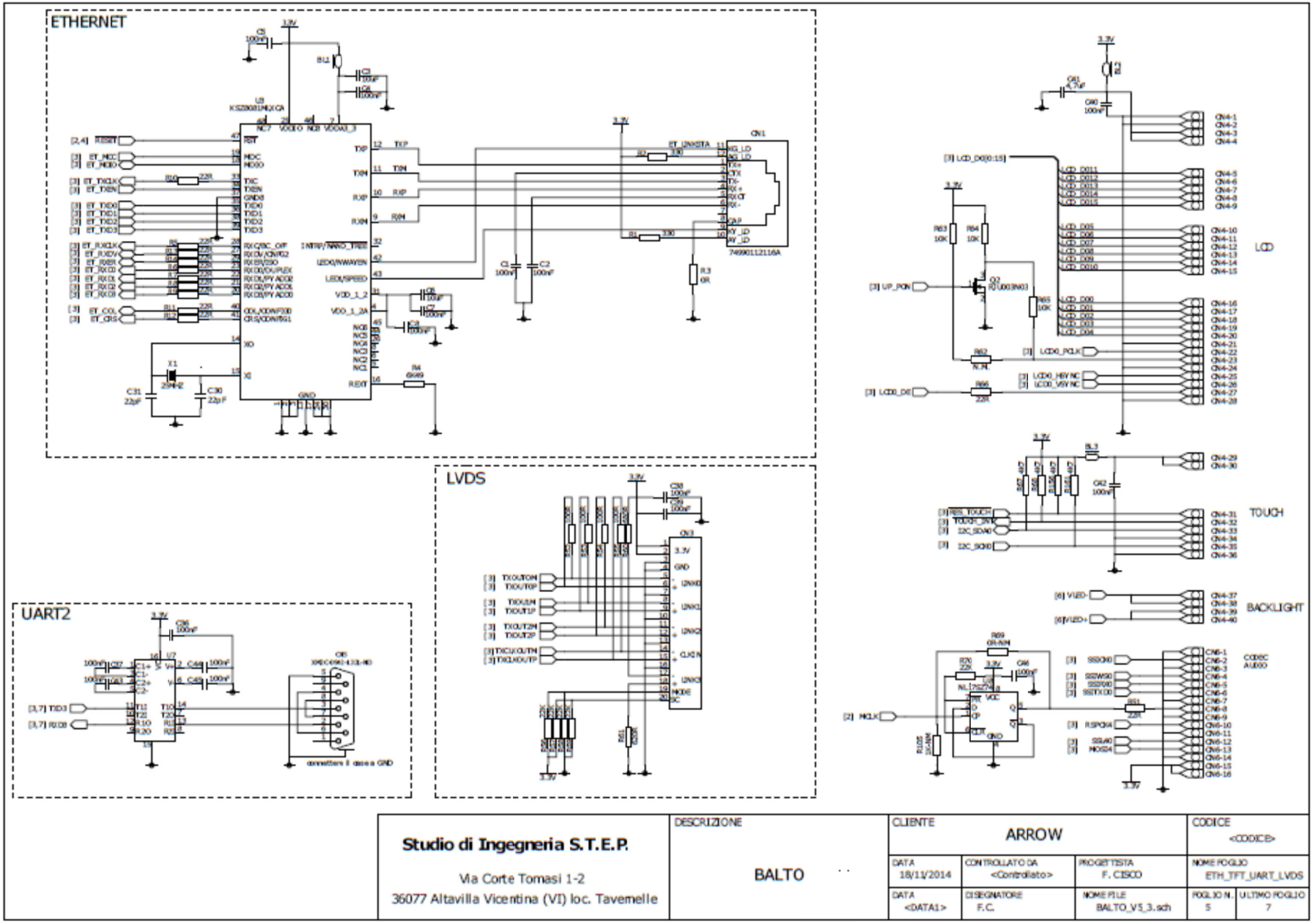
Table 5.5: Boundery Scan

6. Electrical Schematic

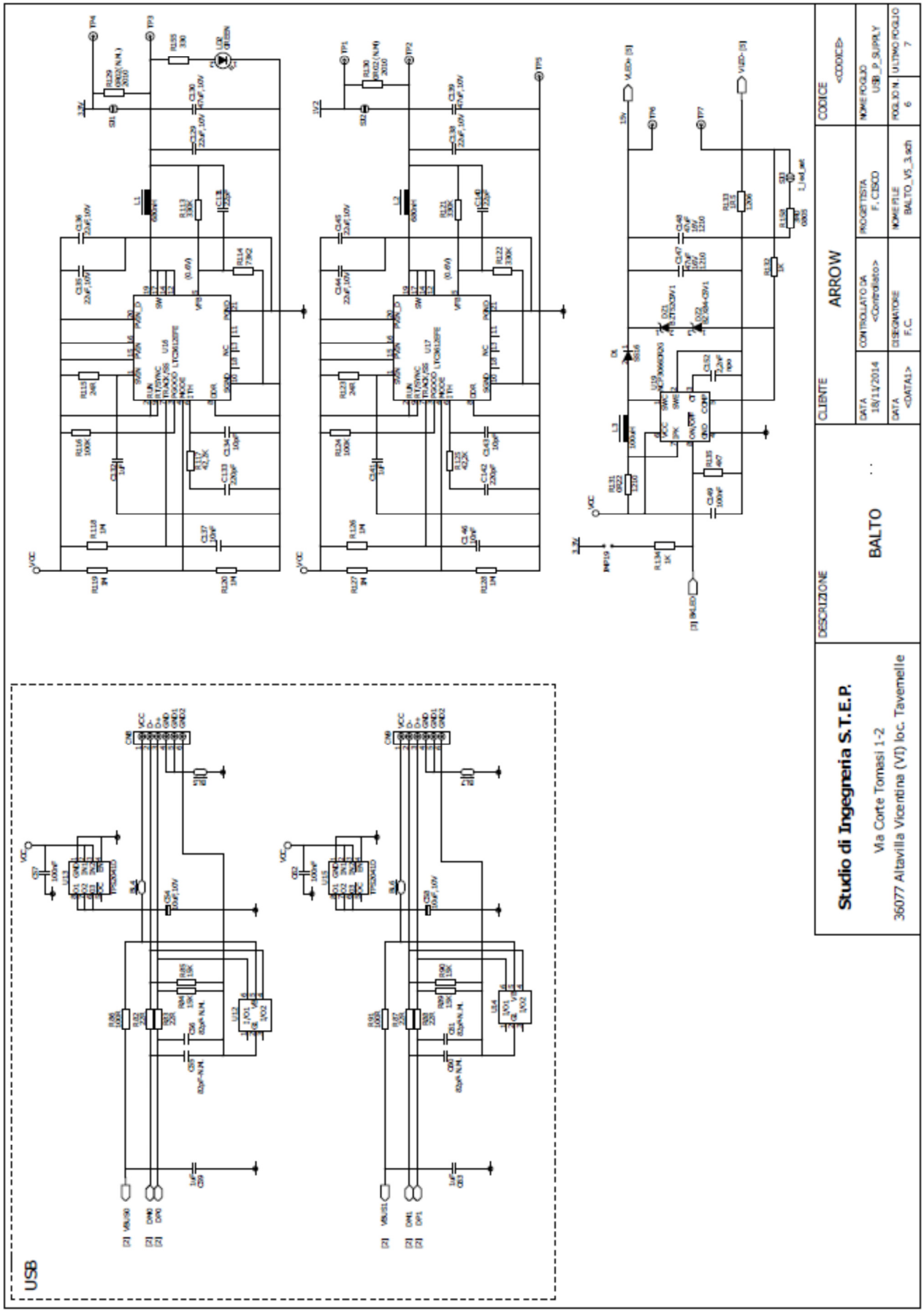


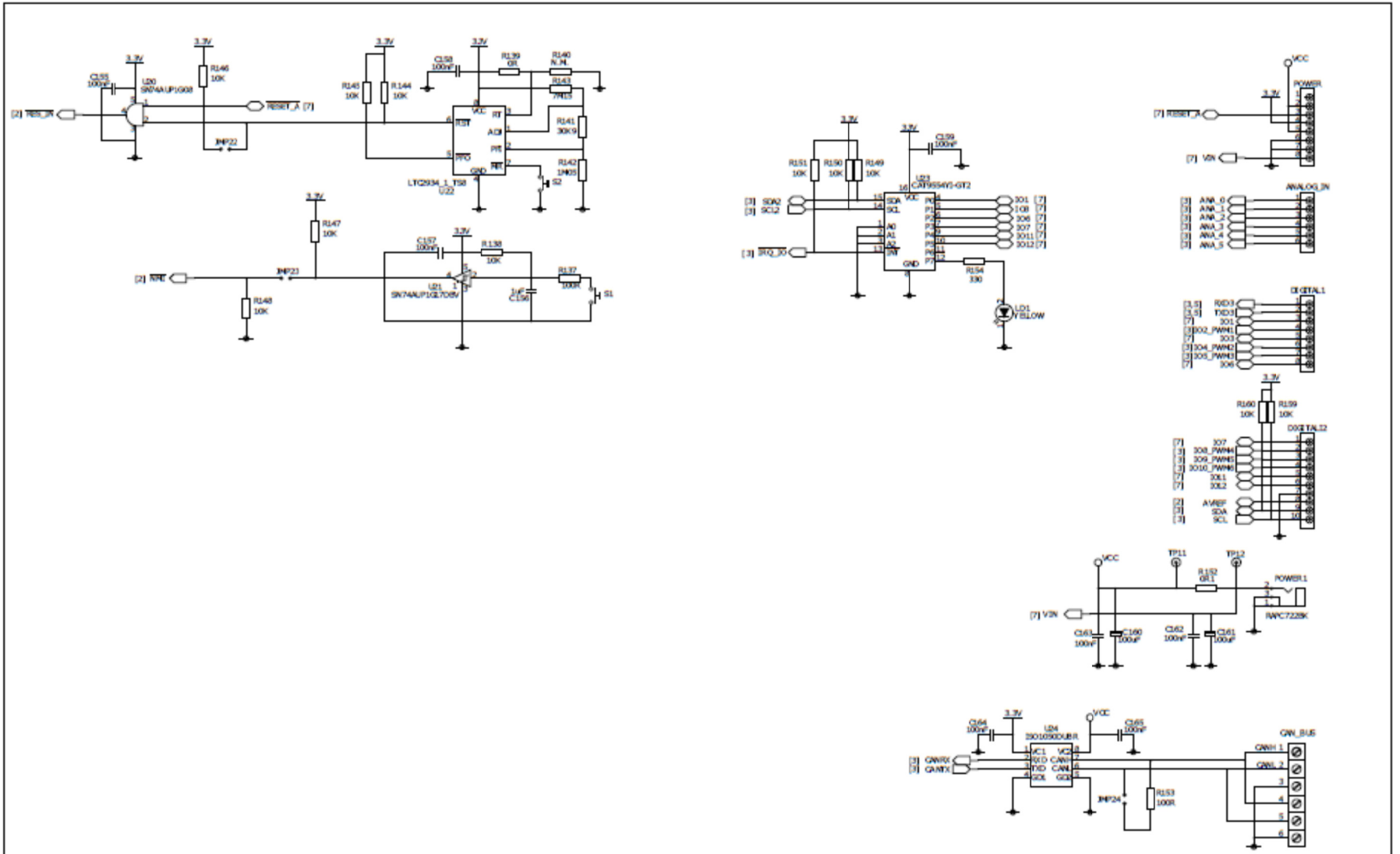

Studio di Ingegneria S.T.E.P.
Via Corte Tomasi 1-2
36077 Altavilla Vicentina (VI) loc. Tavernelle
DESCRIZIONE
BALTO
CLIENTE
ARROW
DATA
18/11/2014
DATA
<DATA1>
CONTROLLATO DA
<Controllato>
DISEGNATORE
F.C.
PROGETTISTA
F. CISCO
NOME FILE
BALTO_V5_3.sch
CODICE
<CODICE>
NOME FOGLIO
CPU
FOGLIO N.
3
ULTIMO FOGLIO
7


SD MEMORY
FLASH SPI
SD RAM
Studio di Ingegneria S.T.E.P.
Via Corte Tomasi 1-2
36077 Altavilla Vicentina (VI) loc. Tavernelle
DESCRIZIONE
BALTO
CLIENTE
ARROW
DATA
18/11/2014
CONTROLLATO DA
<Controllato>
DISEGNATORE
F.C
DATA
<DATA1>
PROGETTISTA
F. CISCO
NOME FILE
BALTO_V5_3.sch
CODICE
<CODICE>
NOME FOGLIO
FLASH_SD_MEMORY
FOGLIO N.
4
ULTIMO FOGLIO
7



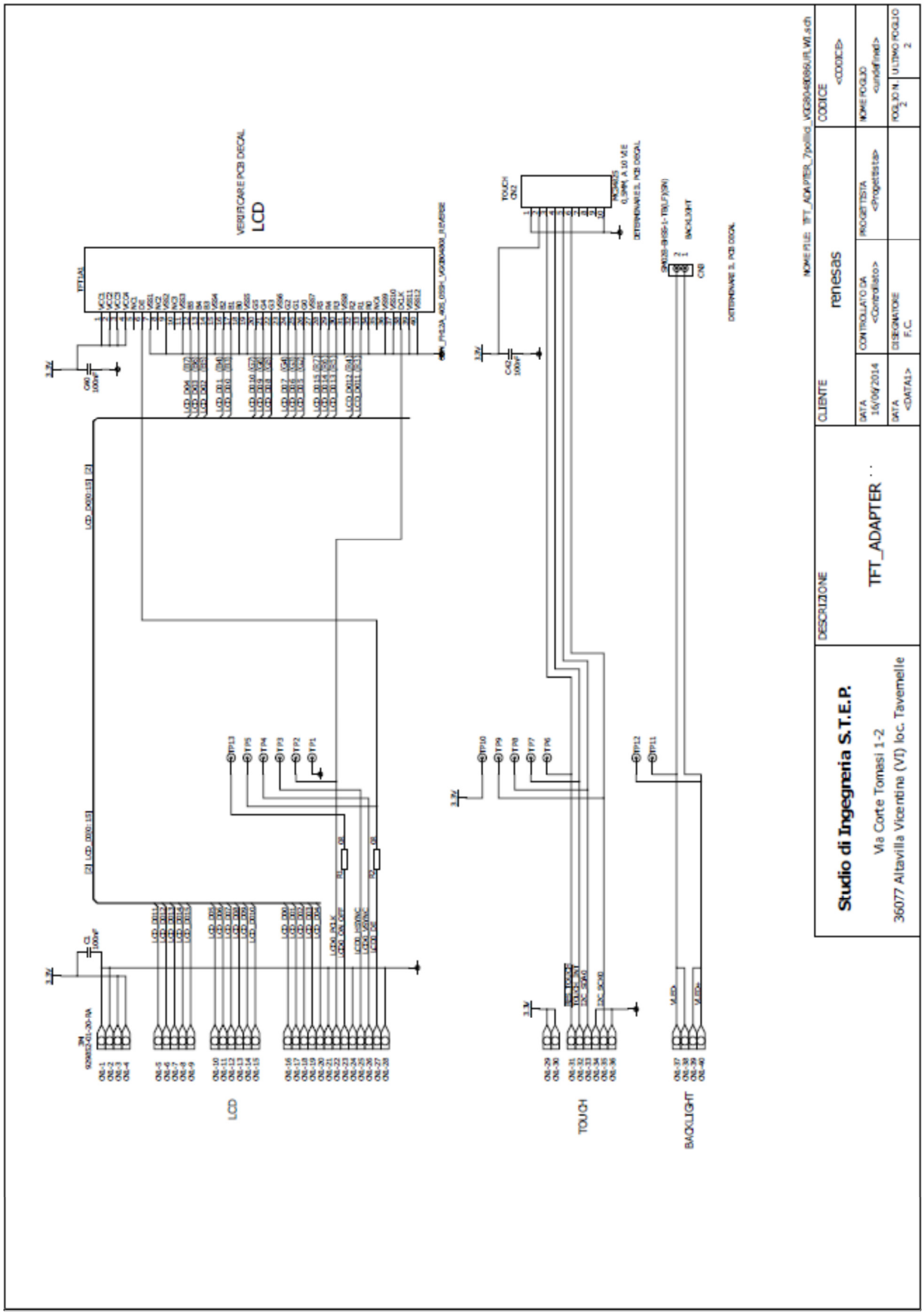
Studio di Ingegneria S.T.E.P. Via Corte Tomasi 1-2 36077 Altavilla Vicentina (VI) loc. Tavernelle	DESCRIZIONE: BALTO	CLIENTE: ARROW	CODICE: <CODICE>
		DATA: 18/11/2014 · CONTROLLATO DA: <Controllato> · PROGETTISTA: F. CISCO	NOME FOGLIO: ETH_TFT_UART_LVDS
		DATA: <DATA1> · DISEGNATORE: F.C. · NOME FILE: BALTO_V5_3.sch	FOGLIO N.: 5 · ULTIMO FOGLIO: 7


Studio di Ingegneria S.T.E.P.
Via Corte Tomasi 1-2
36077 Altavilla Vicentina (VI) loc. Tavernelle
DESCRIZIONE
BALTO
CLIENTE
ARROW
CODICE
<CODICE>
DATA
18/11/2014
CONTROLLATO DA
<Controllato>
PROGETTISTA
F. CISCO
NOME FOGLIO
USB_P_SUPPLY
DATA
<DATA1>
DISEGNATORE
F.C.
NOME FILE
BALTO_V5_3.sch
FOGLIO N.
6
ULTIMO FOGLIO
7
USB



Studio di Ingegneria S.T.E.P. Via Corte Tomasi 1-2 36077 Altavilla Vicentina (VI) loc. Tavernelle	DESCRIZIONE BALTO	CLIENTE ARROW			CODICE <CODICE>
		DATA 18/11/2014	CONTROLLATO DA <Controllato>	PROGETTISTA F. CISCO	NOME FOGLIO IDEXP_RESET_CAN
		DATA <DATA1>	DISEGNATORE F.C.	NOME FILE BALTO_V5_3.sch	FOGLIO N. 7 / ULTIMO FOGLIO 7

7. Ballto Board TFT ADAPTER 7” VGG8048086UFLWI Electrical Schematic



8. Connection

In Figure 8.1 are showed the main Balto Board connection

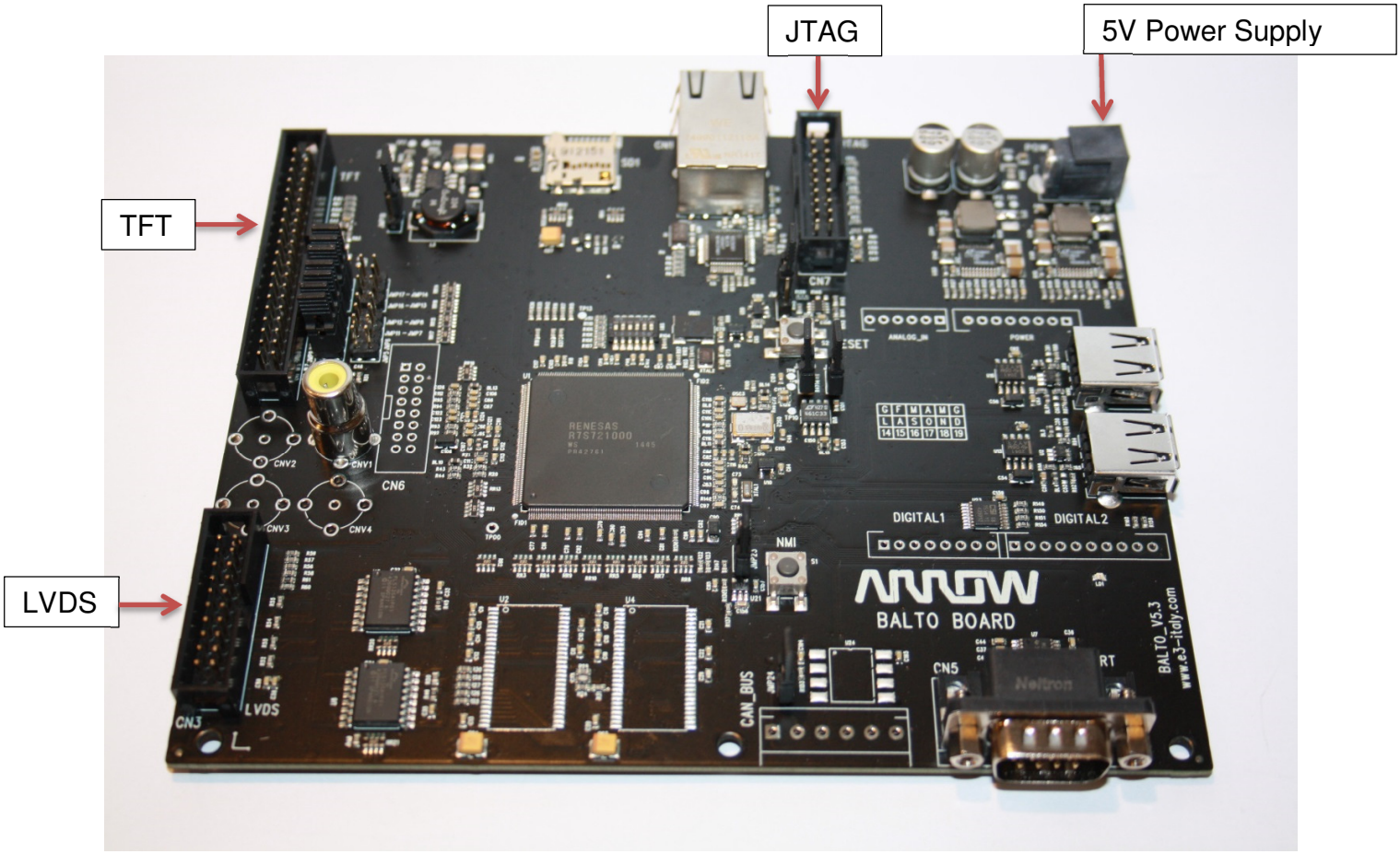


Figure 8.1: Balto Board Connection

Inside the Balto Board Reference Design there are the following items:

N°1 Tft Adapter for VGG8048086UFLWI, see Figure 8.2

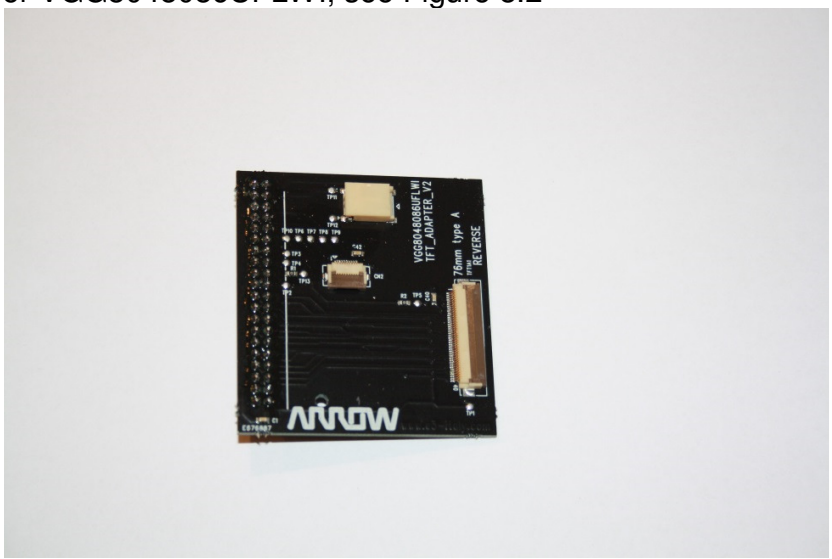


Figure 8.2: Tft Adapter

N°1 parallel cable to connect Balto Board to Tft Adapter for VGG8048086UFLWI, see Figure 8.3

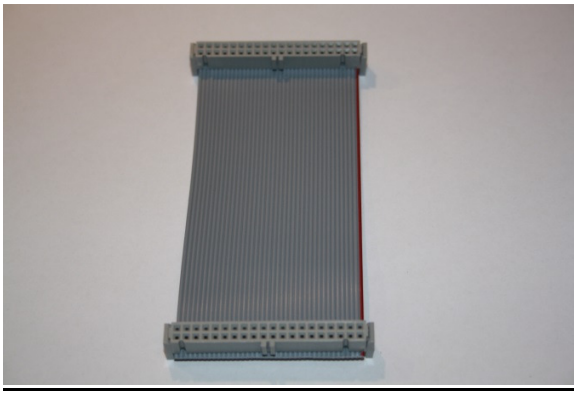


Figure 8.3: Parallel Cable

N°1 parallel cable to connect Tft Adapter to TFT VGG8048086UFLWI , see Figure 8.4

Figure 8.4: Parallel Cable

In figure 8.5 is showed the parallel versus connecting to TFTadapter

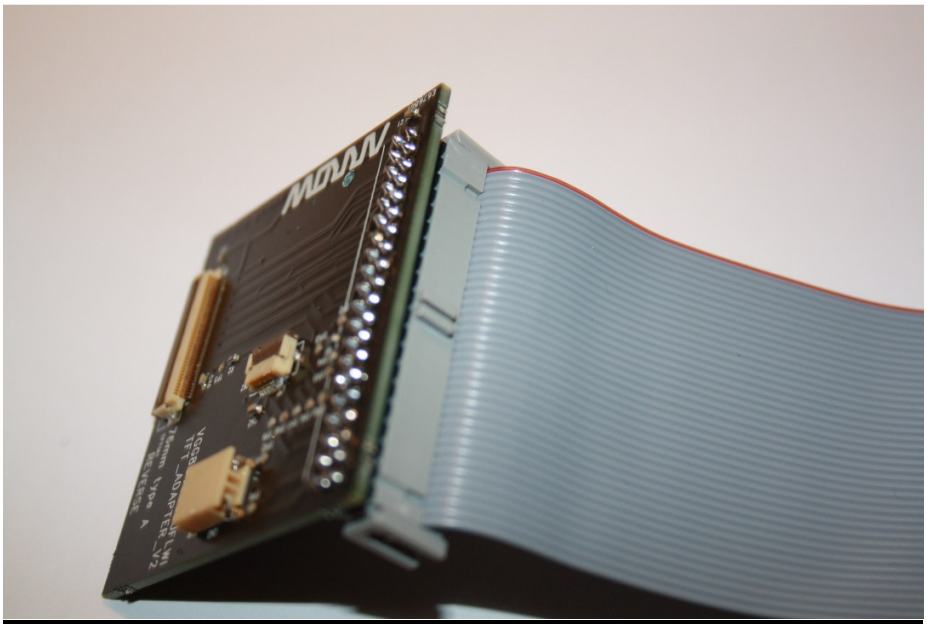


Figure 8.5: Parallel Cable versus