Real Time Synthetic Aperture Radar (SAR) Preprocessor Design Via Three-Dimensional Modular Filtering Architecture

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Abstract – Synthetic Aperture Radar (SAR) systems are increasingly demanding for real real-time performance. As part of an effort to develop a real-time Range-Doppler digital SAR processor to produce image maps of that scanned area immediately as raw data are collected, this paper describes the conceptual architecture design for a high-speed front-end video pre-filtering. The evolved architecture consists of richly interconnected planes of novelly-adapted Modified Transverse FIR parallel tapped delay elements. Both the range and azimuth prefilterings are performed simultaneously in a continuous input-output flow without the need to worry about corner turning caused by azimuth preprocessing on data samples that are collected in the range direction.

Introduction

Synthetic Aperture Radar (SAR) is one of the most important airborne active sensor system that provides all-weather high-resolution imaging for military surveillance, and for remote sensing in geology, agriculture, oceanography etc. A fundamental characteristic of SAR sensor is that a small antenna is used to synthesize an effective antenna aperture that is much longer, based on the motion of the radar to collect data at different points on the flight-path and sophisticated signal processing as the prerequisites.

The video data comes from the RF front end in bursts coinciding with the received microwave pulses from the scene. The preprocessing consists of a range high-pass filter for DC bias cancellation and an azimuth presummer (see Fig.1). The filtering stages are commonly implemented by the use of *finite impulse response* (FIR) structures since they can be designed to have exactly linear phase response and no image artifacts like blurring and geometric distortion will be introduced. As timely surveillance is important for successful military maneuvers, building an on-board real-time video filter which could meet the throughput requirements of SAR processing is important. With the advent of VLSI technology, a recent solution on the use of a class of FIR filter called the Modified Transverse FIR structure, has been proposed as the basic architecture for implementing real-time SAR correlators [1] and it forms the motivation for the proposed SAR preprocessor design.

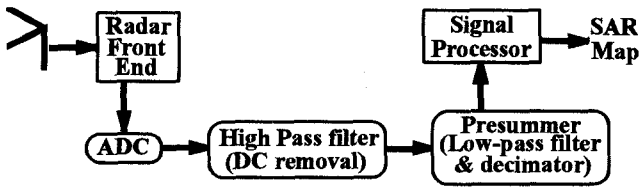


Fig 1 : SAR high-pass filter and presummer configuration

Range Prefiltering

An artifact of the ADC (analog-to-digital conversion) stage is the presence of DC component in the digitized SAR raw data. The presence is due to the component tolerances and temperature drift of the hardware. This DC residual will cause signal saturation in some of the range bins, meaning a voltage spike in the zero frequency bin, since the Fourier transform integrates this DC value over the image. Simple removal of the frequency bins surrounding the DC value is not acceptable since critical scene data may be contained in these bins. High-pass FIR digital filtering is the preferred real-time solution [2] for the elimination of the DC bias in the sampled video data (range lines) before azimuth presumming starts.

For real-time application, the range prefiltering can be performed using high-density programmable gate array consisting of fast multipliers, adders and logic gates. The filtering speed can be significantly improved by exploiting parallelism in the FIR processing flow in a modified transverse structure as shown in Fig.2. The filter coefficients are computed with a designed cut-off frequency that is slightly above zero and the values are pre-stored in discrete memory cells. Data samples collected on every pulse repetition interval (PRI) are fed in sequence into the high-pass filter as they arrived at the outputs of the ADCs. The same set of coefficients is used for filtering in every PRI and each output has a computation latency of only 1 complex multiply and 1 complex add.

Azimuth Presumming

Azimuth presumming [3] is a digital technique for reducing the data rates in the SAR processor. This is possible when the maximum doppler bandwidth is greater than needed for the desired resolution, which is frequently

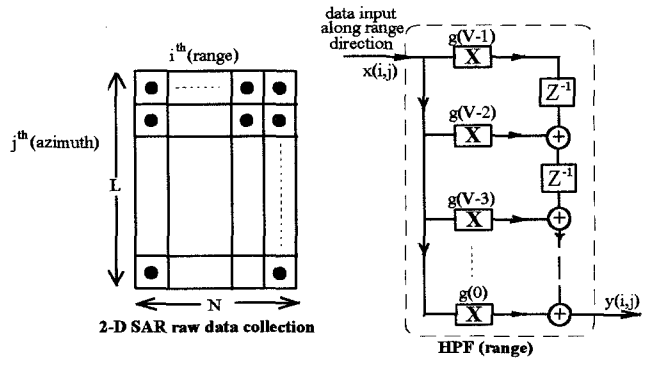
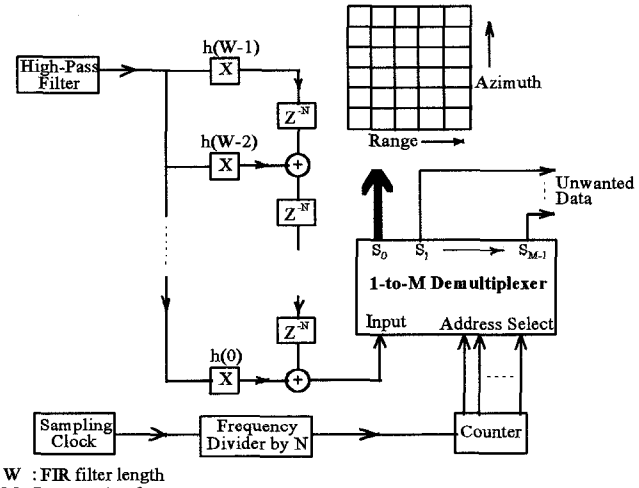


Fig 2 : High-pass filter design for DC bias removal

the case. In SAR processing, azimuth presumming is normally carried out before the range compression stage since it will effectively reduce the number of azimuth data bins. The presummer is commonly implemented using a low-pass FIR filter, followed by a decimator. Due to the low-pass nature of the presumming operation, the signal-to-noise ratio at the output of the presummer is also enhanced.

After the high-pass filtering operation for DC bias cancellation, each range vector is then accumulated in the presummer (vector accumulation in the azimuth direction). For real-time solution, the proposed presumming architecture uses the same modular filtering design as the DC bias cancellation circuitry as shown in Fig.2. However, the SAR presummer needs some novel modifications to take into account that the raw data are collected in the range direction instead of the azimuth direction, by utilising delay elements of length N cells each (size of a range line). This modification will allow continuous data flow and simultaneous pre-filtering operations (see Fig.3). A demultiplexing and timing circuitries are used for implementing the presum decimator.



W : FIR filter length
M : Presumming factor
N : Total number of range bins in one range line

Fig 3 : Real-time implementation of Presummer circuitry

The computation latency for just the azimuth presummer is 1 complex multiply, 1 complex add and the signal propagation delay through the demultiplexer. The filter coefficients are computed with a low-pass cut-off frequency response determined by the minimum Doppler bandwidth.

3-Dimensional SAR Video Filtering Architecture

An integrated video filter design for DC bias cancellation and presumming operation is shown in Fig.4. The structure shows high modularity and regularity. The combined compute latency time for a raw data sample to undergo the two-stage filterings is 2 complex multiplies, 2 complex adds and the propagation delay through the demultiplexer. As multiply operation takes much longer time to compute as compared to adding and the demultiplexer signal delay is also negligible, effort is made to improve the video filter speed via novel architectural modifications. The input SAR raw data is a two-dimensional array, X(i,j). Be it range or azimuth, each filtering stages is 1-dimensional convolution with pre-determined coefficients. The final output of the range/azimuth preprocessing can be written as

$$Z(i,j) = \sum_{k=0}^{L-1} \sum_{l=0}^{N-1} X(l,k) \times \{g(i-l).h(j-k)\} \quad (1)$$

where L : the number of azimuth pulses (very large),
N : number of range gates per range line,
g(i) : range filtering coefficients of length V, and
h(j) : azimuth filtering coefficients of length W.

Equation (1) shows that the two sequence filtering operations can be formulated as the convolution between the incoming raw data and a 2-dimensional filter coefficient set (product of two separable 1-D coefficient sets). Thus for simultaneous range/azimuth filtering operations, the convolution operation is now two-dimensional. Moreover, to account for the fact that the raw data are collected in the range direction instead of the azimuth direction, the final evolved architecture for the SAR preprocessor consists of richly interconnected planes of novelly-adapted Modified Transverse FIR parallel tapped delay elements (see Fig.5). The preprocessor architecture is 3-dimensional and each raw data sample is simultaneously range and azimuth pre-processed in 1 complex multiply and 2 complex adds. The novel design offers rapid continuous input-output data flow without the need to worry about corner turning caused by azimuth preprocessing on data samples that are collected in the range direction.

This modular structure translates easily into an ASIC implementation using high-density programmable gate array consisting of fast multipliers, adders and logic gates. The typical lengths for the 2-D filter coefficients, V and W, are 16 or 32. The coefficients are pre-computed and pre-stored

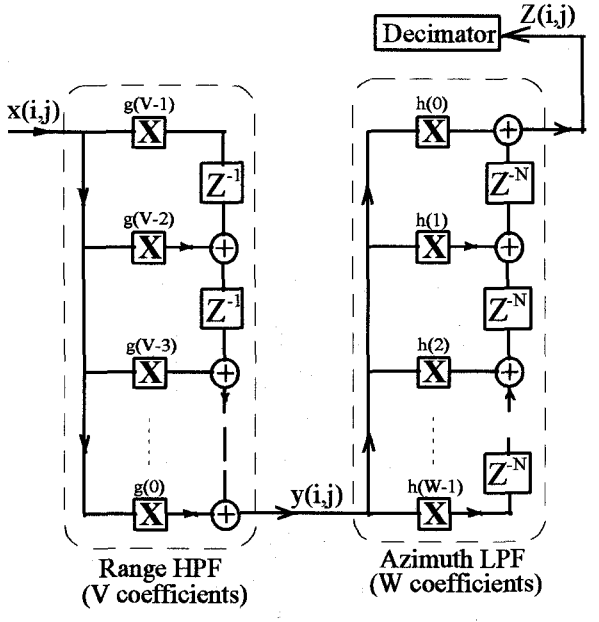


Fig 4 : Cascading of range filter and azimuth presummer

in some memories. Instead of using discrete fast multipliers, the multiplication time between an input sample and the coefficient can be reduced further by using EPROMs as a look-up table. The computation time is only the memory access time which with GaAs technology, is just about 3 ns or less. EPROMs are preferred so that in future when the filter coefficients have to be altered, it can be changed easily. The programmability gives high flexibility to the preprocessor for use in different imaging modes. The real-time SAR prefiltering process is achieved as a result of the high modular data flow in the 3-D processing architecture as well as VLSI advances. However, such a speed enhancement is at the expense of significant increase in hardware complexity.

Conclusions

Real-time SAR image formation is highly important for military surveillance, especially for effective timely actions to counteract any assessed threats. As part of an effort to develop a real-time Range-Doppler digital SAR processor, a conceptual high-speed architecture design for the front-end video pre-filtering is proposed. The DC bias cancellation and azimuth presummer operations are embedded into a single 3-dimensional richly interconnected planes of novelly-adapted Modified Transverse FIR parallel tapped delay elements. The novel design offers rapid continuous input-output data flow without to worry about corner turning caused by azimuth preprocessing on data samples that are collected in the range direction. The compute

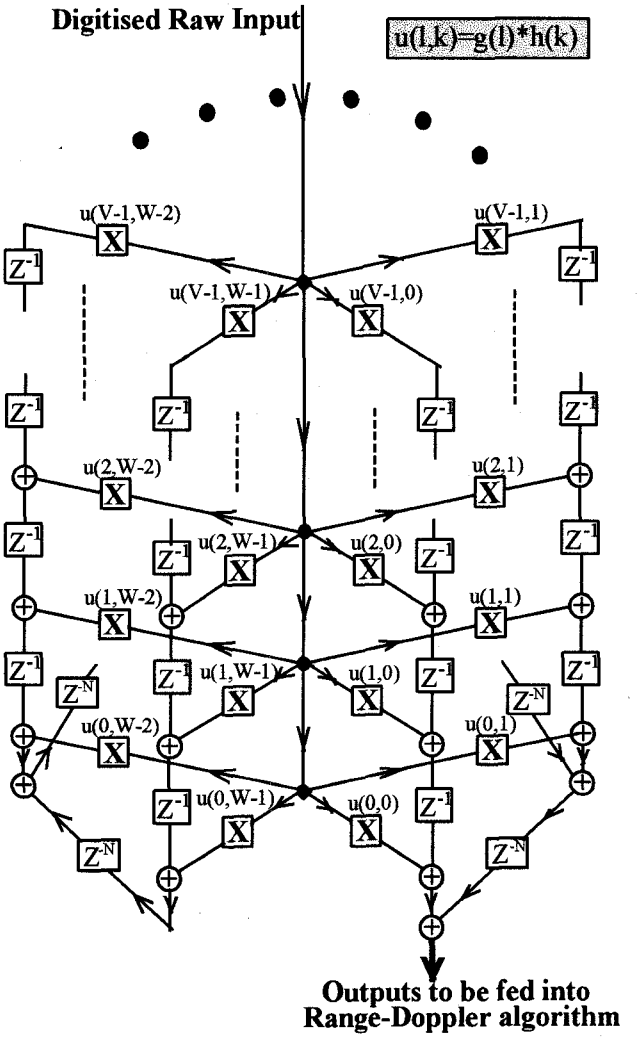


Fig 5 : 3-D geometrical filter for SAR preprocessor

latency has been enhanced to just 1 complex multiply and 2 complex adds. This design is best suited for ASIC implementation.

References

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