

Design of a Switched-Capacitor Amplifier

H05E4a DAMSIC Project 2025

Part I: Parameter derivation, Ideal

Students: Sam Buydens, Efe Ali Akkaya

Group ID: 5

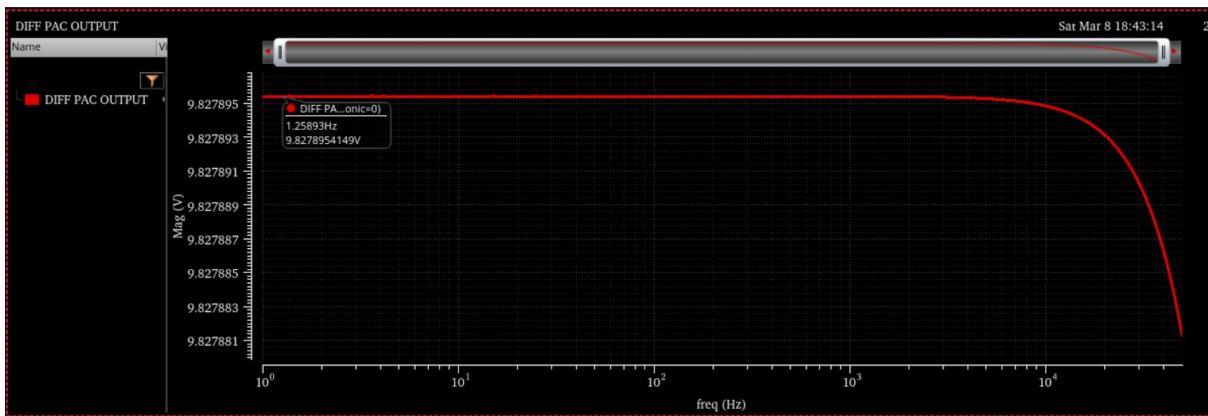
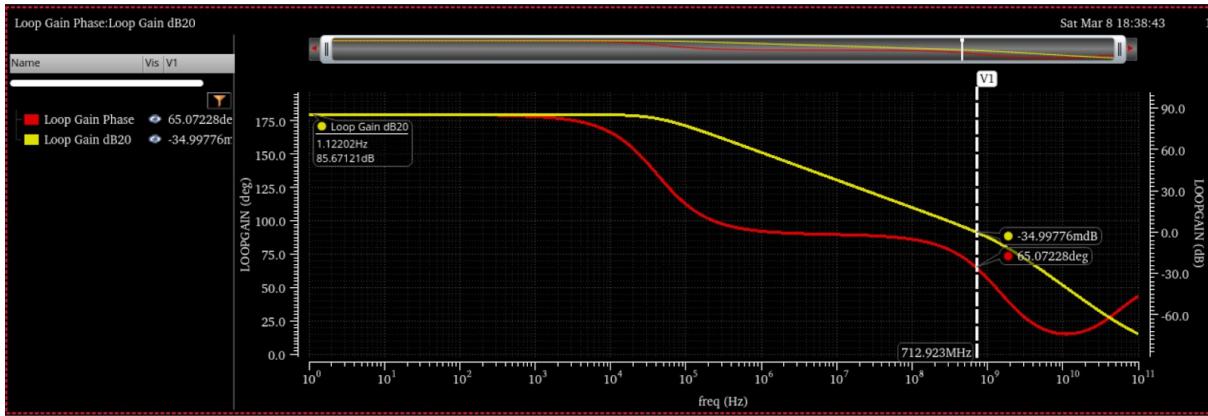
1. GENERAL INFORMATION AND SUMMARY

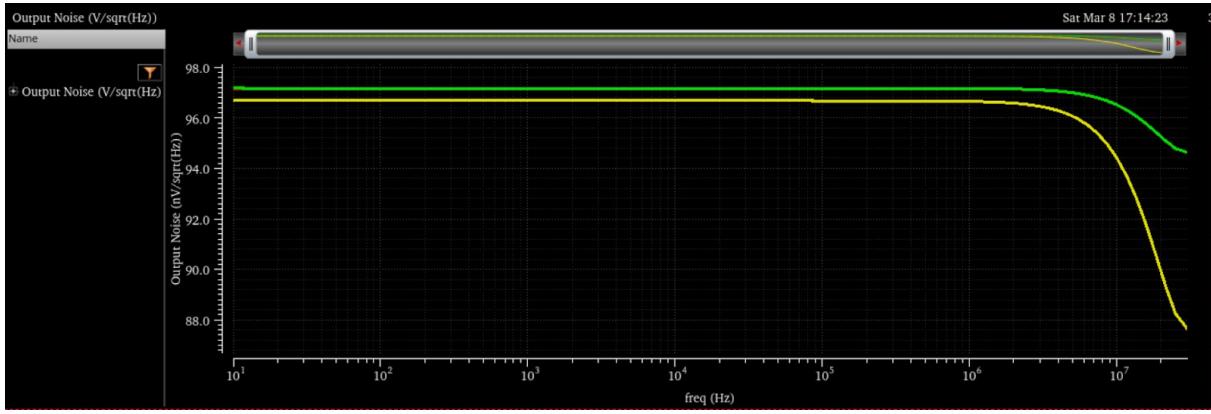
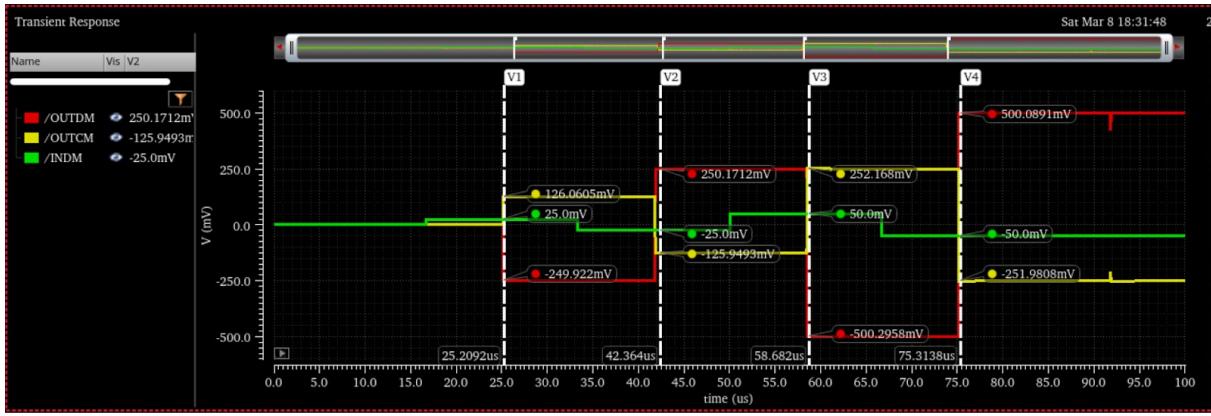
Parameter	Unit	Specification
Sampling Frequency	MHz	60
SNR	dB	45
Static Gain Error	%	0.06
Dynamic Settling Error	%	2.8
Phase Margin (Min.)	deg	60
CL	pF	2
Min. Input Swing	mVpp	50
Max. Input Swing	mVpp	100
Closed-Loop Gain	V/V	10
Input Pair	-	pMOS

1. GIVEN TARGET SPECIFICATIONS

2. DERIVATION OF SYSTEM DESIGN PARAMETERS

1. IDEAL OTA





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Part II: Symmetrical OTA

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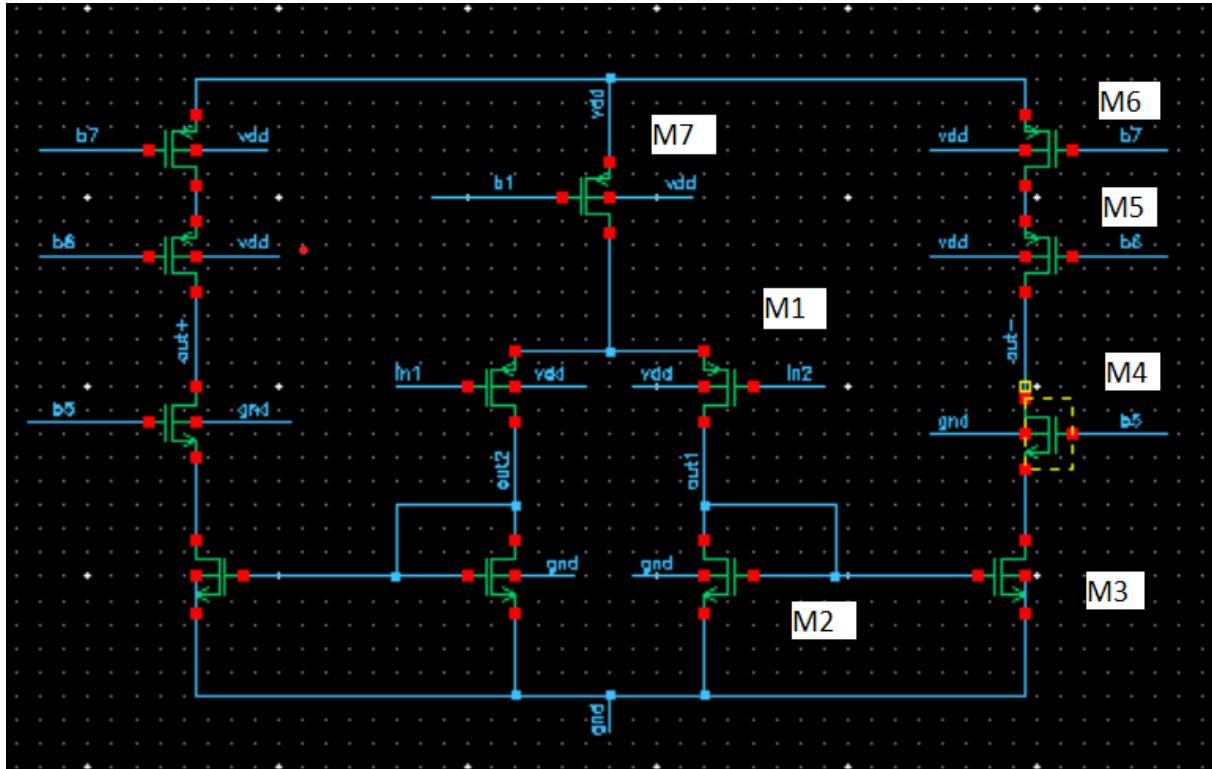
3. SYMMETRICAL OTA

1. TABLE OF ACHIEVED RESULTS (SO FAR)

Enter your achieved results in the below table. You can leave some fields blank if you did not simulate (or design) for the specific parameter yet.

Parameter	Unit	Achieved
Input Swing	mVpp	118.37
Output Swing	mVpp	164.2
Total Integrated Output Noise	mVrms	1.57
SNR	dB	41
CL	pF	2
CFB	pF	0.23
CIN	pF	2.3025
Open-Loop Gain	dB	35
Closed-Loop Gain	V/V	8.35
GBW (Sample Phase)	MHz	2384
Phase Margin (Sample Phase)	deg	65.6
Dynamic Settling Error	%	20.2
Static Gain Error	%	16.5
Power dissipation	mW	10.19

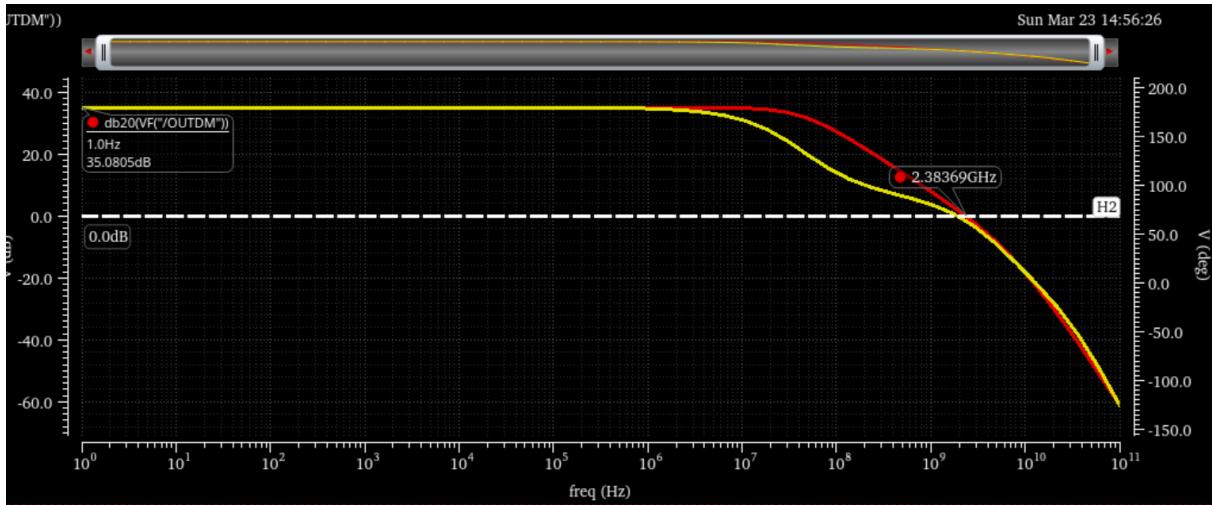
1. SCHEMATIC DESIGN



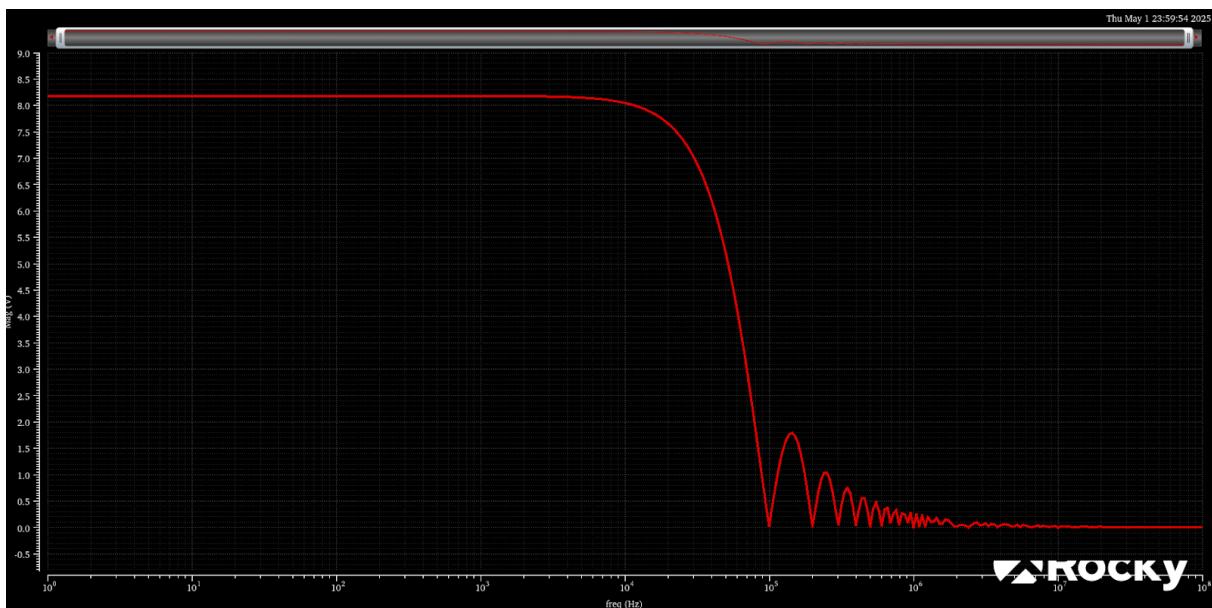
transistor	W (um)	L (nm)	Gm (mS)	VGS	VDS
M1	96	90	13.1	0.48	0.58
M2	27	90	10.8	0.44	0.44
M3	193.5	90	46.5	0.44	0.36
M4	60.5	90	26.9	0.64	0.19
M5	102.5	90	27.8	0.61	0.26
M6	77.5	90	23.5	0.477	0.29
M7	480	90	28	0.4	0.08
Current M1 (mA)	0.85	Current M2 (mA)	3.59		

1. SIMULATION RESULTS

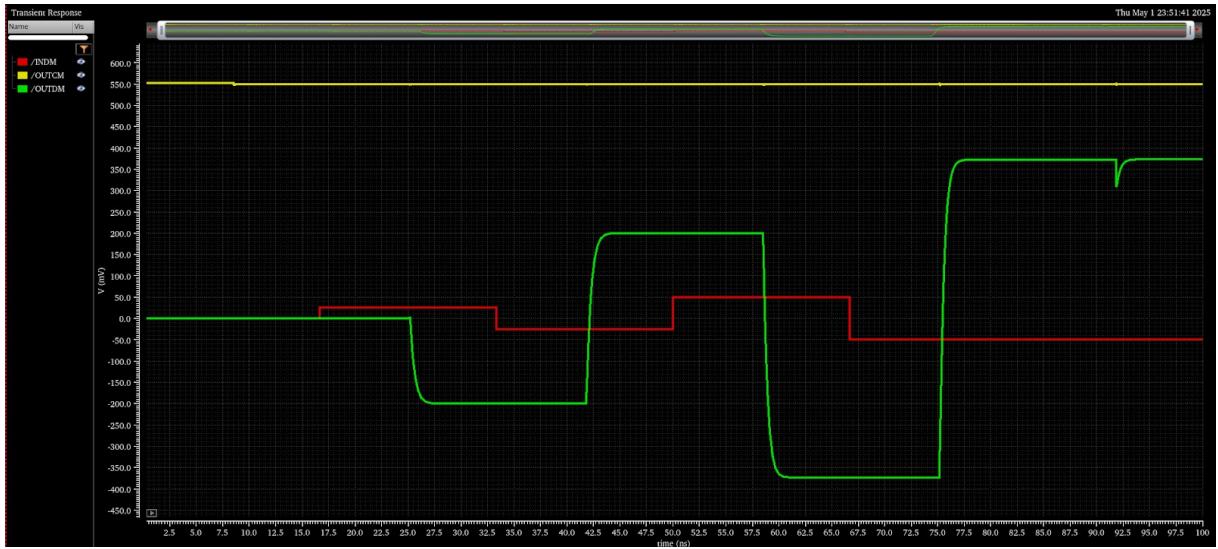
Open loop AC simulation:



Closed loop AC simulation:



Closed loop transient (60 MHz):



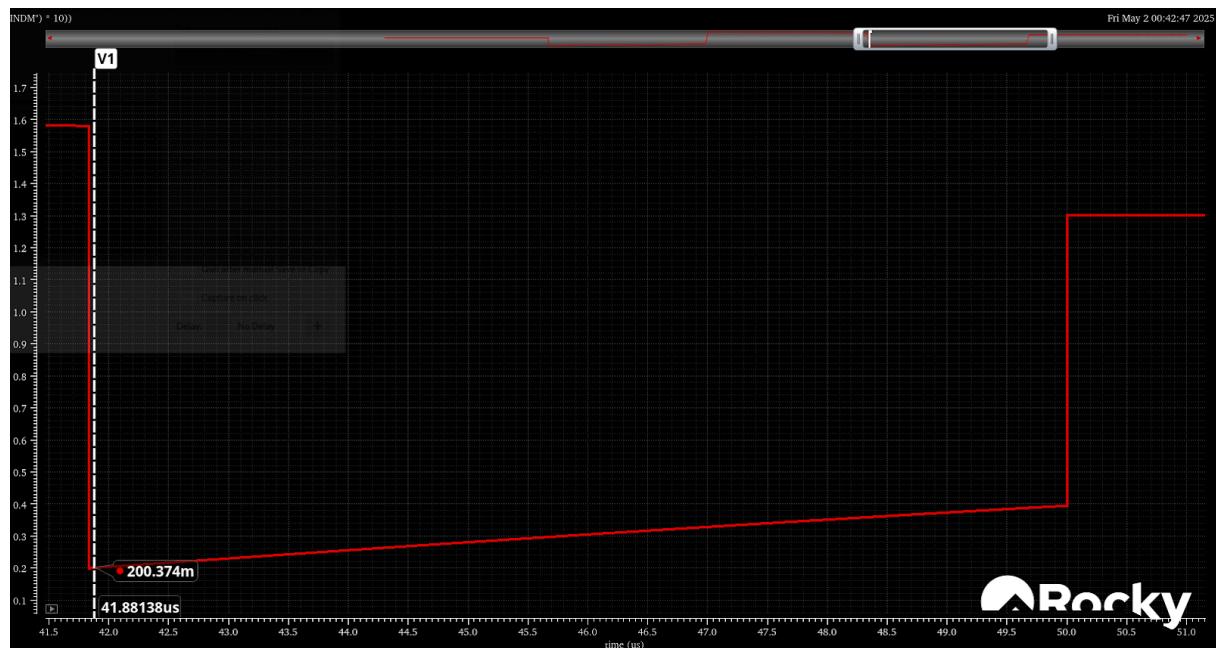
Dynamic error (60kHz):



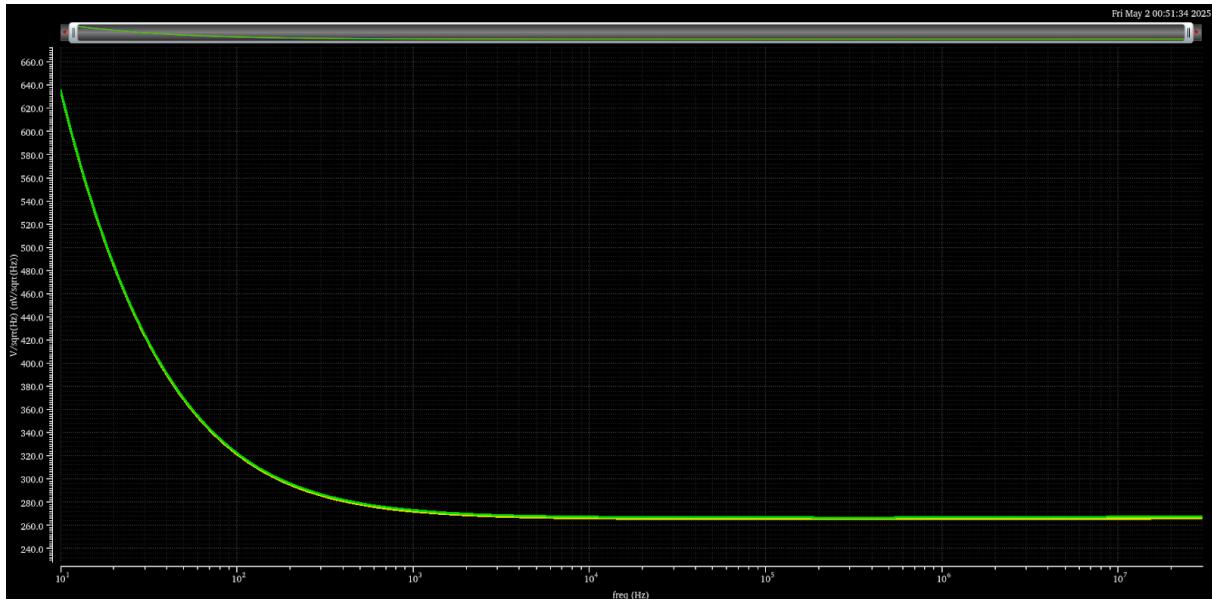
Closed loop transient (60 kHz):



Dynamic error (60kHz):



Noise spectrum:



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Part III: Gain-boosted OTA

Students: Sam Buydens, Efe Ali Akkaya

Group ID: 5

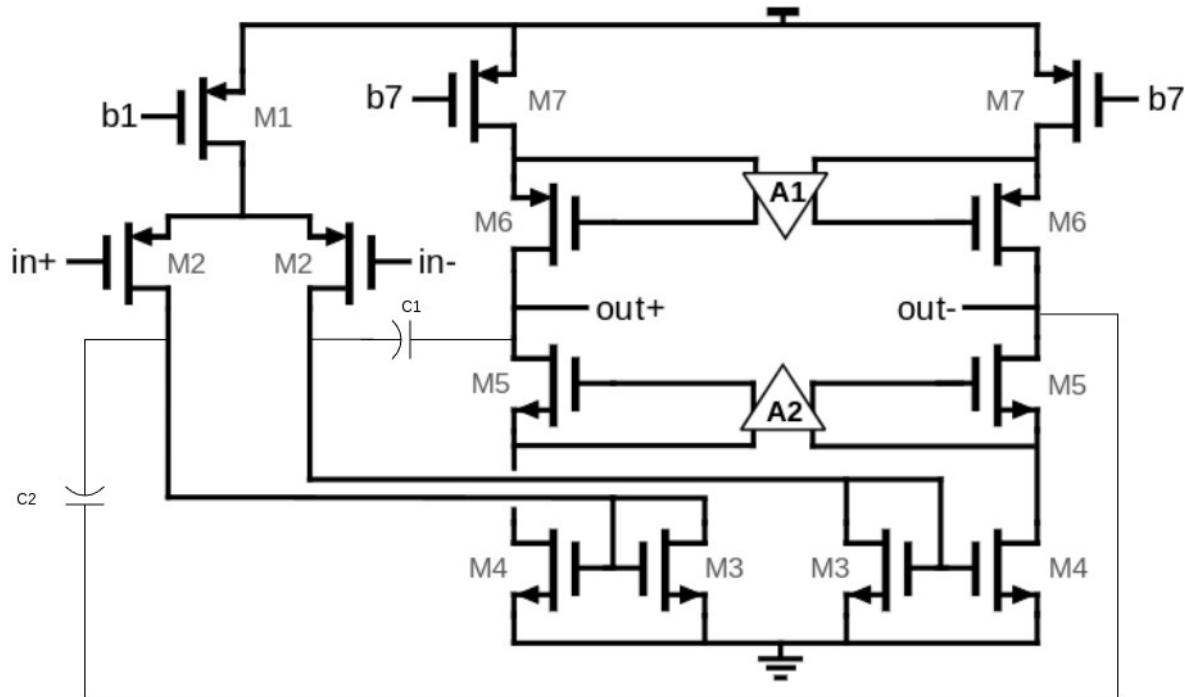
Gain-boosted OTA

1.1 Table of Achieved Results

Enter your achieved results in the below table.

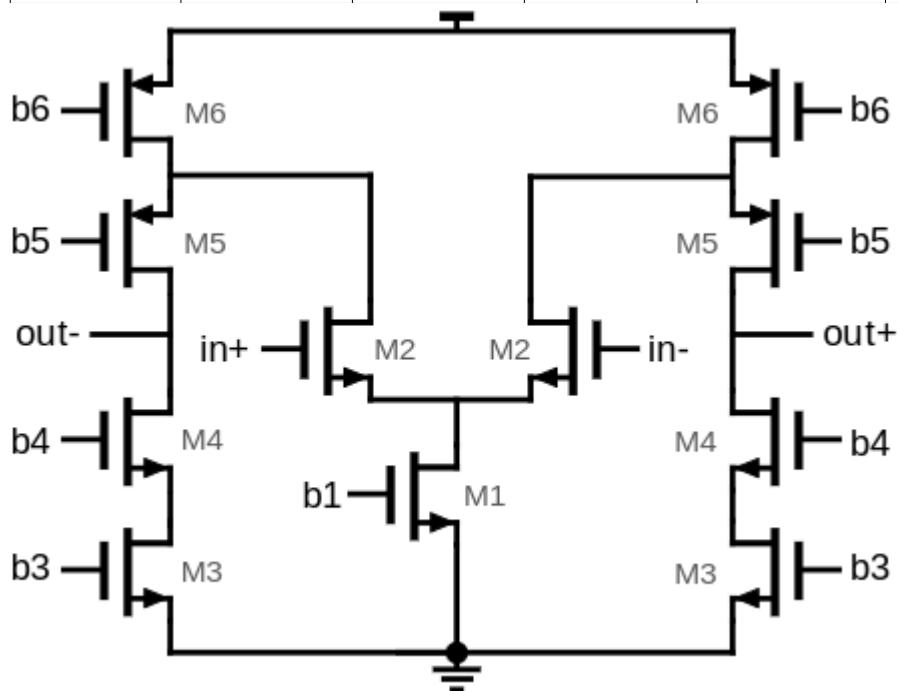
Parameter	Unit	Achieved
Input Swing	mV _{pp}	118.37
Output Swing	mV _{pp}	164.2
Total Integrated Output Noise	mV _{rms}	1.15
SNR	dB	43.73
C _L	pF	2
C _{FB}	pF	0.23
C _{IN}	pF	2.347
Open-Loop Gain	dB	72.2
Closed-Loop Gain	V/V	10.0024
GBW (Sample Phase)	MHz	565
Phase Margin (Sample Phase)	deg	59
Dynamic Settling Error	%	11.2
Static Gain Error	%	0.0426
Power dissipation	mW	30.87

Schematic Design



Transistor	W(um)	L(nm)	V _G (mV)	V _D (mV)	V _{GT} (mV)	V _{DS} (mV)
M1	480	90	700	100.2	-11.2	-99.8
M2	96	90	550	448.5	-45.0	-553.7
M3	40.5	90	448.5	448.5	74.1	448.5
M4	193.5	90	448.5	355.8	60.5	355.8
M5	60.5	90	1000.9	549.0	181.6	193.2
M6	102.5	90	200.5	549.0	-184.6	-271.8
M7	77.5	90	446.1	820.8	-219.1	-279.2
CMFB				Currents(mA)		

A	CMFBEst	R		M1	1.82	
10	0.479	10		M4	3.73	
C1	3pF	C2	3pF			

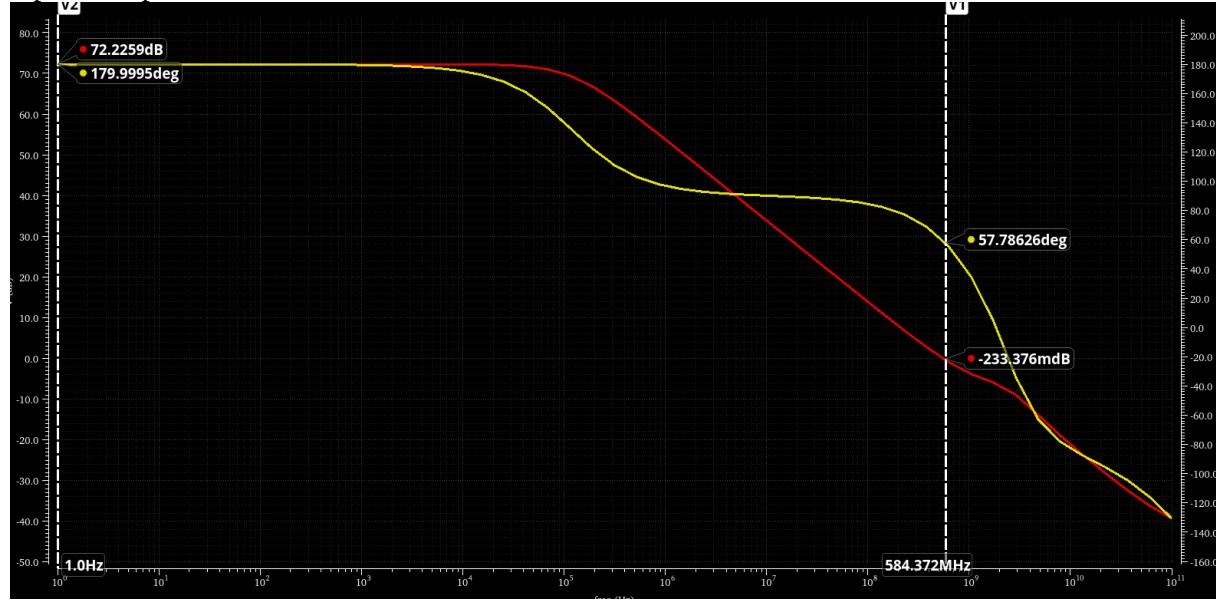


Transistor	W(um)	L(um)	V _G (mV)	V _D (mV)	V _{GT} (mV)	V _{DS} (mV)
M1	15000	1	300.0	150.7	3.18	150.7
M2	250	1.8	820.8	887.8	378.0	737.1
M3	100	1	506	247.4	3.18	247.4
M4	100	1	786....// !"!	500.5	220.4	253.2
M5	182	1	400m	500.52	-215.7	-387.3
M6	529	0.2	645	887.8	-120.4	-212.2

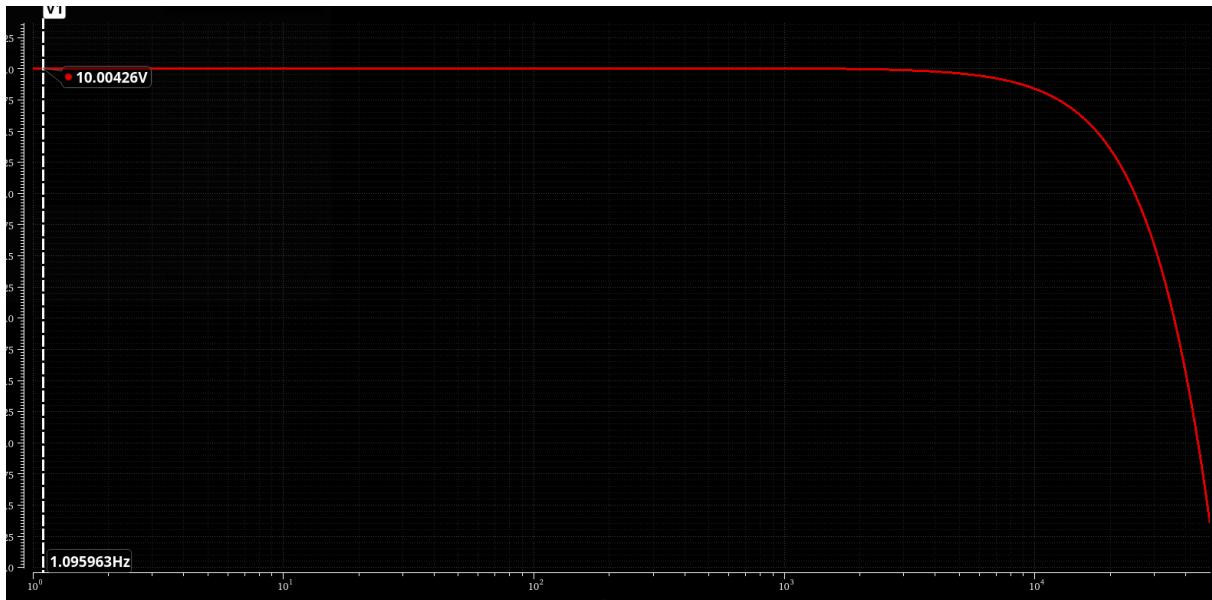
Currents						
M1	7.54	M3	0.929			

Simulation Results

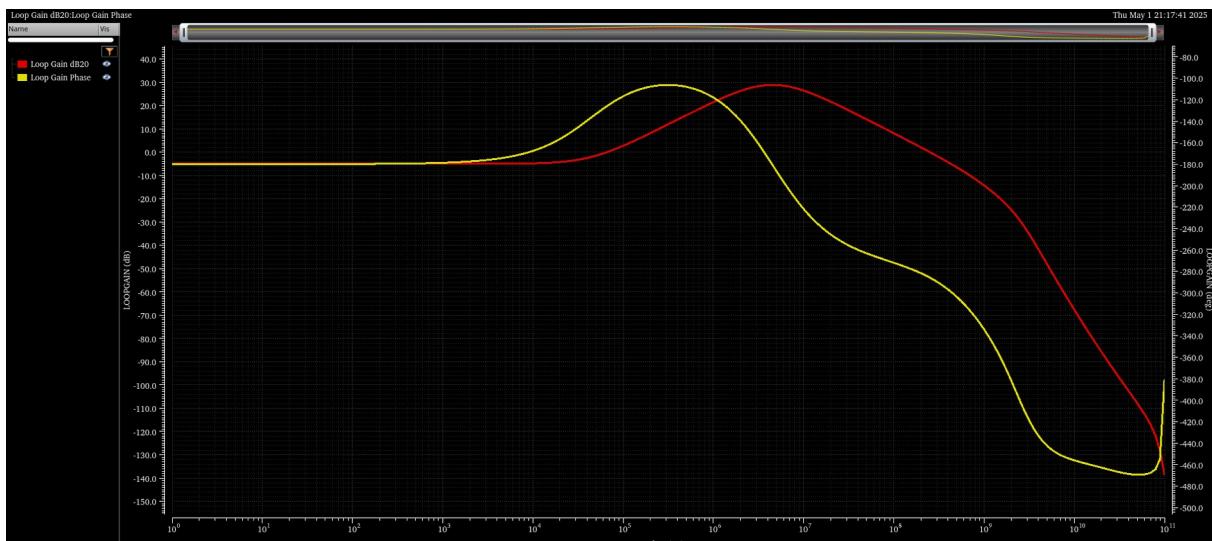
Open-Loop AC simulation:



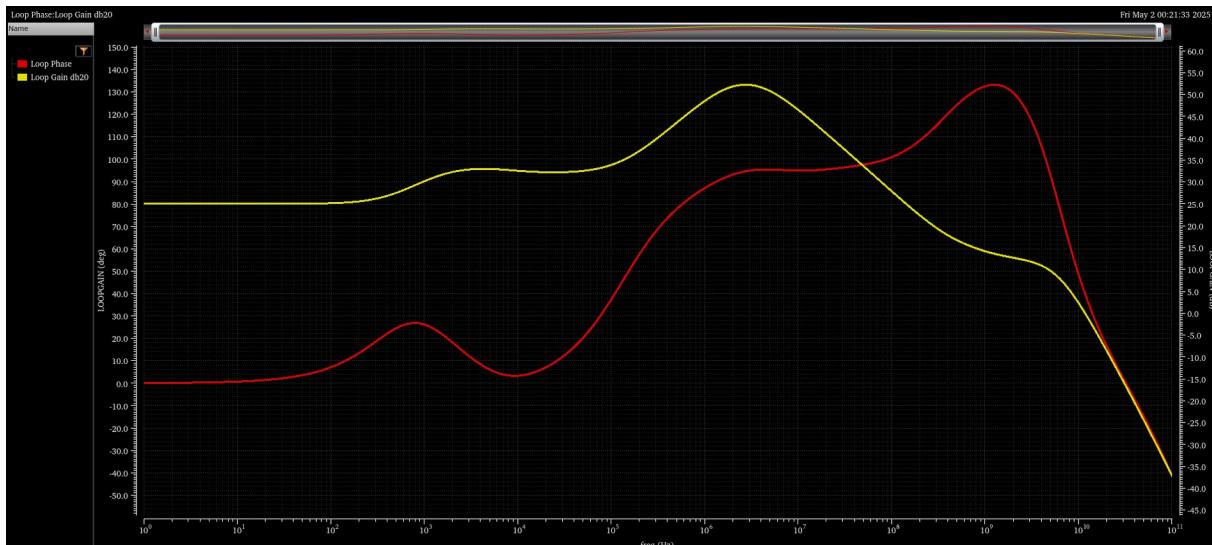
Closed-Loop simulation (main loop):



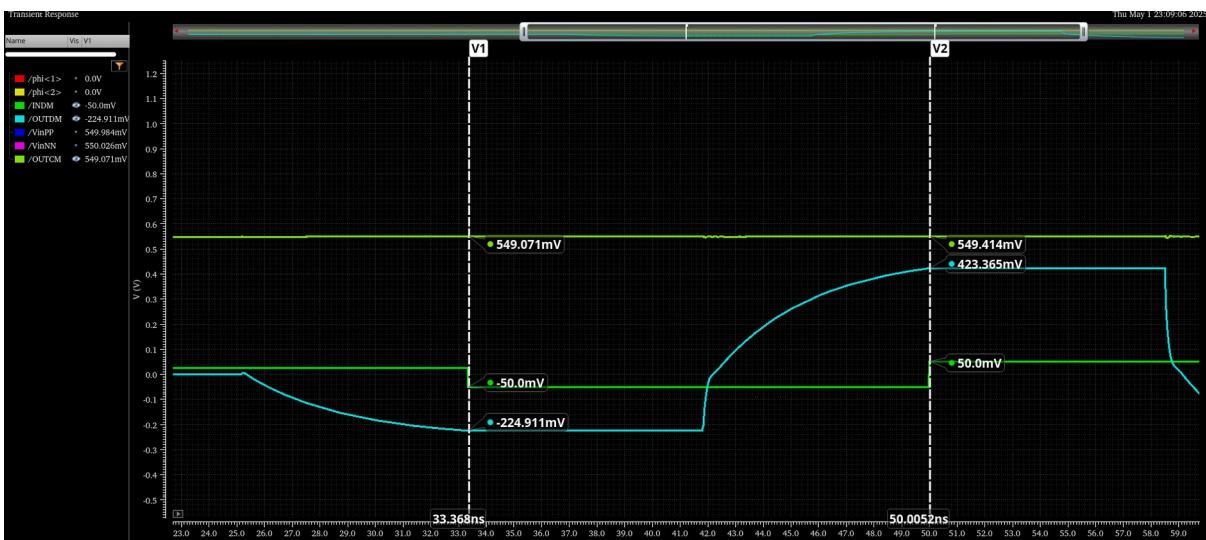
Closed-loop simulation (gain boosting loop):



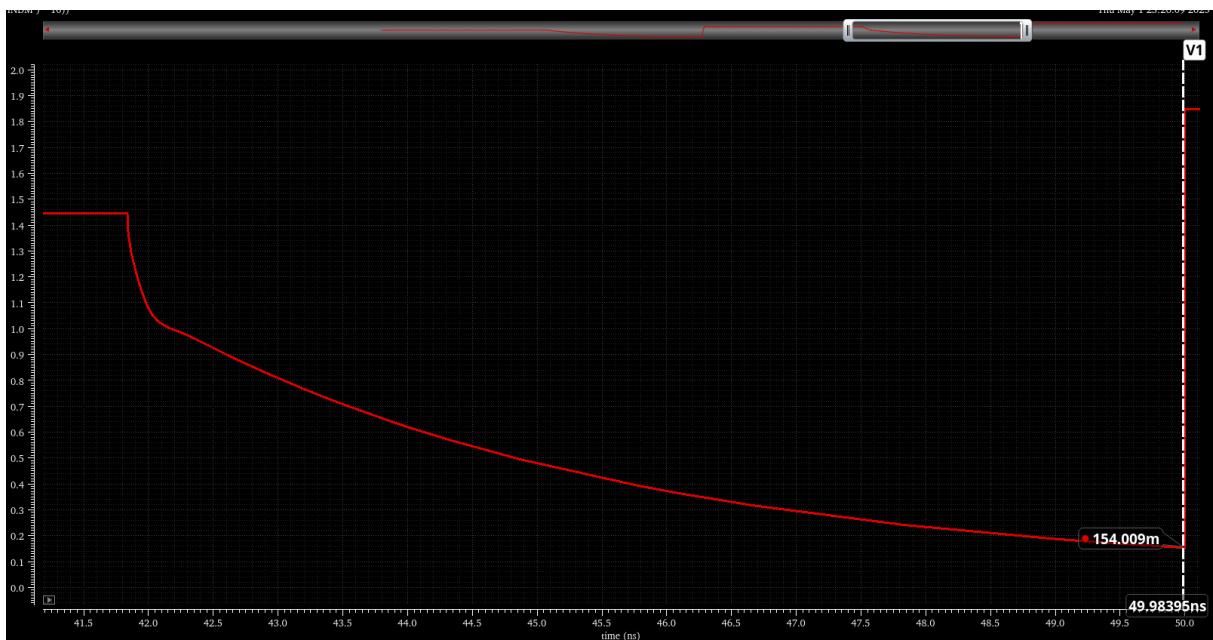
Closed-loop simulation (CMFB loop):



Closed-loop transient simulation:



Dynamic error in second amp phase:



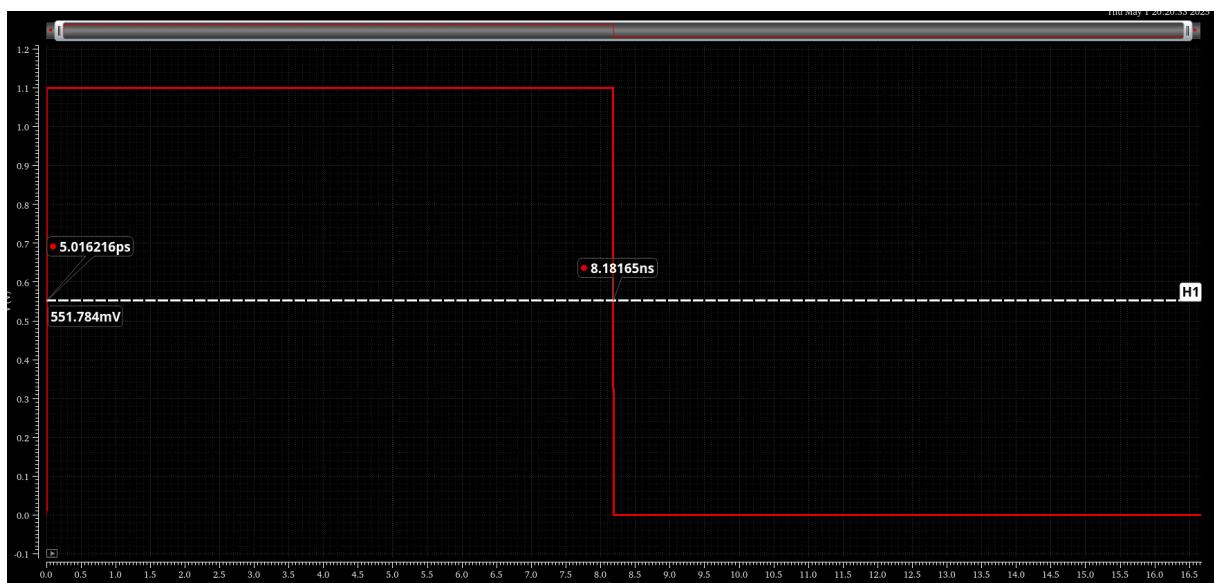
Closed-loop transient simulation (60 kHz):



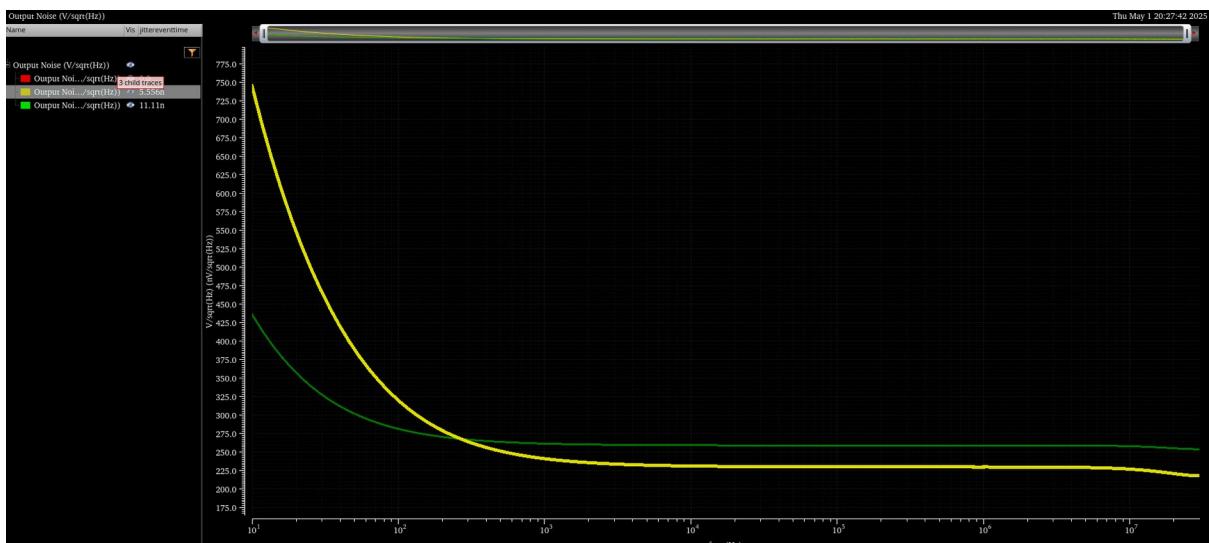
Dynamic error in second amp phase (60 kHz):



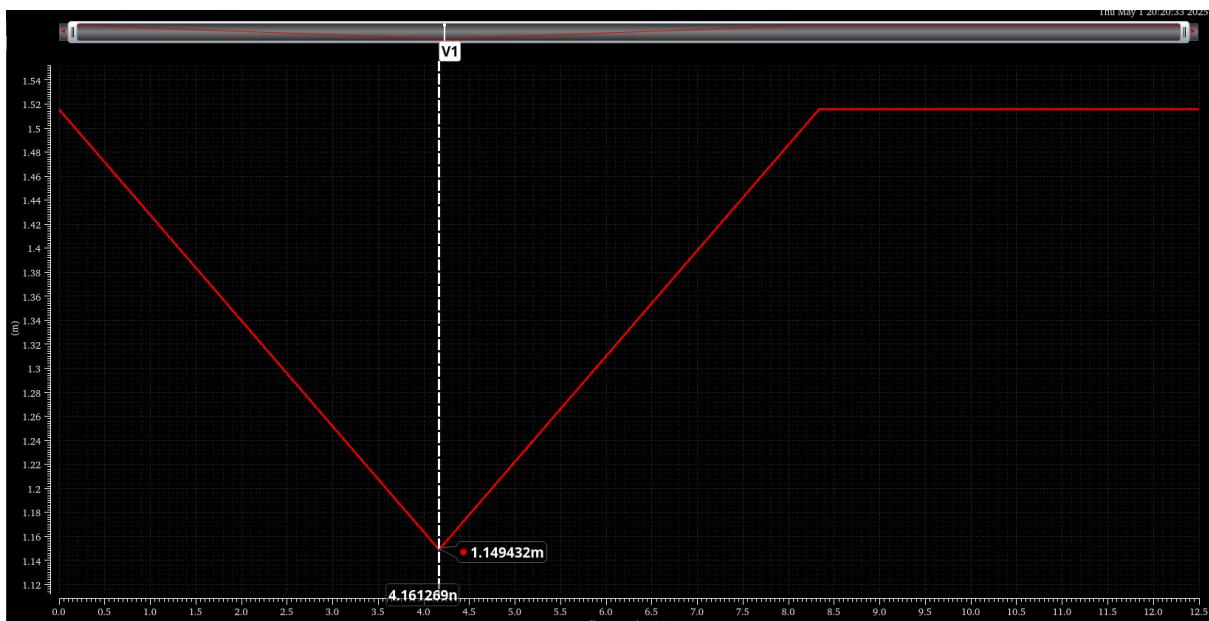
Clock pulse:



Noise spectrum:



Integrated noise:



We were able to get a closed-loop gain of around 10 but were unable to get a lot of the other specifications. Our phase-margin and SNR come close to the specifications but our dynamic error is far from the expected value.

Summary and Additional Remarks

Other Results

The only extra thing we did was adding capacitances between the output and the current mirror in the symmetrical OTA to split the poles which improved our phase margin.