Calibrating Amplifiers Nonlinearity Using Comparator-Based ADCs

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***Abstract*—Amplifiers are widely used within analog-to-digital converters (ADCs) to buffer and increase signal amplitude, alleviating the accuracy, noise, and power constraints of the ADCs. However, any nonlinearity caused by front-end amplifiers is fully or partially inherited by the ADC, compromising its overall linearity. Additionally, as CMOS processes scale, amplifiers become increasingly difficult to design due to reduced intrinsic gain and voltage headroom. Many applications rely on digital calibration to alleviate the amplifier specifications, which may use polynomial fitting or another sort of digital processing. Despite reducing the analog power, these solutions render high complexity and power consumption on the digital part. In this brief, we describe how comparator-based ADCs, such as a flash ADC or a comparator-based asynchronous binary search (CABS) ADC, inherently provide sufficient degrees of freedom to calibrate any monotonic nonlinearity. Then, we exploit this property to propose a low-complexity, low-power, and low-overhead calibration scheme, where we embed the inverse transfer function of the nonlinear amplifier into the decision thresholds of the following ADC. We also propose a statistical-driven algorithm that is used to guide the thresholds adjustment in the background. Finally, we extensively validate the proposed approach through behavioral simulations.**

***Index Terms*—ADC, amplifier, comparator calibration, background calibration, comparator-based, nonlinearity.**

I. Introduction

THE CMOS technology scaling has motivated the replacement of analog signal processing with its digital counterpart. However, since most of the signals in nature are continuous in time and amplitude, analog-to-digital converters (ADCs) are required as interfaces between these two domains. Traditionally regarded as the topology-of-choice for high-speed, medium-resolution ADCs, the pipeline ADC strongly depends on the design of wide-band, high-gain amplifiers that it employs. However, the design of high-performance amplifiers becomes very challenging by the reduced intrinsic gain of transistors and reduced supply voltages in deeply scaled CMOS. If no amplifier calibration is applied, the amplifiers must obey precision requirements (regarding linearity, gain, offset and bandwidth) that match the ADC desired resolution.

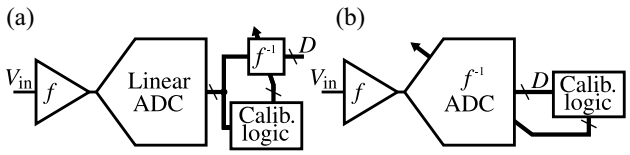

Fig. 1. a) Commonly used and b) proposed calibration of amplifiers nonlinearities in ADCs.

Motivated by the CMOS scaling, it is increasingly common to apply some calibration in the digital domain to relax the amplifier requirements. In such a scenario, a common approach is to model the amplifier as a polynomial while determining its coefficients by minimizing an error function [1]–[4]. Then, the amplifier transfer function could be compensated in the digital domain, leading to a linear ADC response. This procedure is depicted in Fig. 1a. On the other hand, the mentioned approach generally requires complex digital processing, which may include multipliers or a dedicated processor, leading to increased system complexity. Also, the needed digital circuitry grows exponentially with the amplifier model order, evidencing the accuracy-complexity trade-off. Typical implementations use low-order polynomials, thus restricting the amplifier implementation or significantly limiting the calibration performance. Alternatively, some approaches that rely on analog-domain compensation were already proposed, such as [5], that cancels out the input buffer nonlinearities by employing the same amplifier on the feedback loop of a successive approximation register (SAR) ADC.

In this brief, we demonstrate that comparator-based (CB) ADCs, as a flash ADC [6] or a comparator-based asynchronous binary search (CABS) ADC [7], inherently provide the necessary degrees of freedom for compensating any monotonic non-linearity (Section II). As represented in Fig. 1b, we propose a linearization technique that compensates the amplifier nonlinearities by embedding its inverse transfer function to the succeeding CB ADC. The technique can be applied on a standalone CB ADC or a two-step ADC with a CB back-end. Compared to the aforementioned digital calibration schemes, our proposed method enables lower hardware complexity and faster convergence speed by using the comparator thresholds

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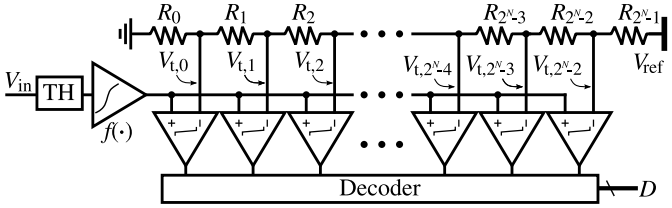

Fig. 2. THA with CB quantizer using a resistor ladder to generate the comparators reference voltage.

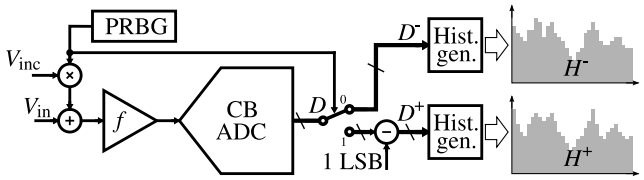

Fig. 3. High-level representation of the 1 LSB increment and histogram generation on a comparator-based ADC with nonlinear front-end.

as knobs inside the CB ADC. To guide the calibration, we propose a low-complexity histogram-based algorithm to identify the amplifier nonlinearities and train the comparator thresholds (Section III). The proposed techniques are validated by extensive behavioral simulations using a 10-bit two-step ADC model, with a 5-bit SAR frontend stage and a 5-bit CB back-end stage. (Section IV). Finally, Section V discusses and concludes this brief.

II. Method

In this brief, a CB ADC is defined as an ADC that relies only on comparators to quantize the sampled input. Therefore, a standard N-bit CB ADC requires $2^N - 1$ thresholds, one for each possible ADC output code. The input is converted by triggering the comparators and evaluating their outputs. Different search engines can be applied on a CB ADC. The flash ADC, to achieve a high throughput rate, triggers all the comparators at once. The CABS ADC, on the other hand, using binary search, requires only N comparisons to convert the input, leading to lower power consumption.

On an N-bit CB ADC, any output code transition can be altered independently by changing its corresponding threshold, which gives $2^N - 1$ degrees of freedom to modify its transfer function. When aiming for a linear transfer function, the thresholds must be uniformly spaced. However, the thresholds may be tweaked to achieve any monotonic transfer function. By exploiting this feature, a CB ADC may implement the inverse transfer function of any nonlinear monotonic amplifier that precedes it in the signal chain. While doing so, the ADC transfer function cancels the nonlinearities coming from the non-ideal amplification.

To illustrate the proposed calibration technique, without loss of generality, a linearization method for an N-bit CB ADC preceded by an open-loop track-and-hold amplifier (THA), shown in Fig. 2, is described. The search engine used for the conversion is irrelevant in this example and is omitted on the representation to improve clarity. The amplifier transfer function $f(\cdot)$ is assumed to be known, and a resistor ladder sets the thresholds. For simplicity of analysis, we neglect the comparator offsets (we will show later in Section III that the proposed calibration algorithm also compensates for offset mismatches). Let us consider that the ADC is targeted to have V_{ref} of reference voltage and zero offset on the transfer function. The j-th threshold voltage in the resistor ladder is denoted by $V_{t,j}$, where j ranges from 0 to $(2^N - 2)$. By definition, $V_{t,j}$ has to force the j-th comparator to have a tripping point when an input of $(j+1)V_{ref}/2^N$ is applied before the amplification stage, therefore, $V_{t,j} = f((j+1)V_{ref}/2^N)$. If all the thresholds are equally spaced by $V_{ref}/2^N$, then the ADC is linear.

If the resistor ladder is built as in Fig. 2, each threshold can be adjusted independently by changing the resistance ratio of its associated resistor to the overall ladder resistance. For example, to create the THA inverse transfer function on the CB ADC reference, the governing function for R_0 is

$$\frac{V_{ref}R_0}{R_{tot}} = V_{t,0} = f\left(\frac{V_{ref}}{2^N}\right), \tag{1}$$

where R_{tot} is the total resistance of the resistor ladder and V_{ref} is the reference voltage. Then, R_0 is set to

$$R_0 = f\left(\frac{V_{ref}}{2^N}\right)\frac{R_{tot}}{V_{ref}}, \tag{2}$$

For the j-th resistor with j from 1 to $2^N - 2$, the governing function is

$$\frac{V_{ref}\left(R_j + \sum_{i=0}^{j-1} R_i\right)}{R_{tot}} = \frac{V_{ref}R_j}{R_{tot}} + f\left(\frac{jV_{ref}}{2^N}\right) = f\left(\frac{(j+1)V_{ref}}{2^N}\right), \tag{3}$$

which leads to

$$R_j = \left[f\left(\frac{(j+1)V_{ref}}{2^N}\right) - f\left(\frac{jV_{ref}}{2^N}\right)\right]\frac{R_{tot}}{V_{ref}}, \tag{4}$$

while the value of R_{2^N-1} is given by

$$R_{2^N-1} = R_{tot} - \sum_{i=0}^{2^N-2} R_i. \tag{5}$$

This analysis reveals that the resistor ladder values can be determined to achieve a combined (amplifier plus ADC) linear transfer characteristic if $f(\cdot)$ is known. In practice, however, $f(\cdot)$ depends heavily on process, voltage and temperature (PVT) variations, suggesting that a mechanism should be devised to track the changes in $f(\cdot)$ on-the-fly.

III. A Background Calibration Algorithm for a CB ADC With Nonlinear Front-End Amplification

Although not targeting for amplifier nonlinearity, the calibration algorithm for a CB ADC on the back-end of a two-step ADC proposed on [6] (for a flash ADC), and also applied on [7] (for a CABS ADC), would compensate the nonlinearities of a front-end residue amplifier. The algorithm assumes that, if ideal, the back-end ADC has an uniform output code distribution. Through inspecting the output histogram, adjacent codes are forced to have the same appearance probability by compensating the comparator thresholds. In this brief, we propose a variation of the mentioned algorithm that is not limited to uniform output histograms, which is a non-realistic scenario for many applications.

The proposed approach is depicted in Fig. 3. The CB ADC converts the input with a positive increment of V_{inc} (which can be added through the charge-redistribution principle) in half

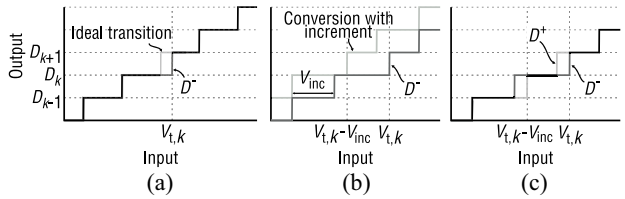

Fig. 4. Amplifier plus ADC transfer function of D^- with one misplaced threshold compared to a) ideal transfer function, b) with increment added to the input and c) with D^+.

of the conversion cycles, according to the output of a pseudo-random bit generator (PRBG) with ~ 50 % duty cycle. The increment is considered for now to be exactly 1 V_{LSB}. The injection could be made alternatively, the PRBG is considered to reduce the input signal dependency, providing more robustness. To properly convert the input signal when the increment is added, the CB ADC requires one extra threshold, as its input range can exceed the reference voltage. Furthermore, an amplifier with an arbitrary nonlinear transfer function $f(\cdot)$, preceding the ADC, is considered. The ADC raw output is hereafter referred as D, the output of a conversion without increment is called D^-, while the result from a conversion with analog increment, succeeded by a 1-LSB decrement in digital-domain, is named D^+. Then, the histograms H^- and H^+ are generated for D^- and D^+, respectively, by counting the number of occurrences of each output code.

Consider an input signal with quasi-static code density at the amplifier, which is a shared assumption by most, if not all, the histogram-based calibration algorithms. If the amplifier and the ADC are linear, the histograms H^- and H^+ should be the same (they would be shifted by one bin in the x-axis if we have not performed the 1-LSB output decrement digitally). On the other hand, if the combined system is nonlinear, due to nonlinearities on the amplifier, ADC or both, these two histograms diverge.

Now, to understand how a non-ideal threshold manifests on the histograms, allowing a calibration through their inspection, consider a case where the ADC has only one misplaced threshold seen from the amplifier input, $V_{\mathrm{t},k}$, that discriminates the codes D_k and D_{k+1} and is slightly above its ideal value. Fig. 4a shows a representation of the amplifier plus ADC transfer function, without the increment, near the non-ideal region. By the definition of the CB operation principle, $V_{\mathrm{t},k}$ only causes a shift in the transition between the codes D_k and D_{k+1}.

As shown in Fig. 4b, when the input is converted with the increment, the transfer function suffers only a $-V_{\mathrm{LSB}}$ shift on the input axis, having the non-ideal transition occurring at $V_{\mathrm{t},k} - V_{\mathrm{LSB}}$ input. When the increment is digitally removed (-1 LSB shifted on the output axis), as seen in Fig. 4c, the transfer functions diverge. Due to errors in both conversions, the largest mismatch is expected on H_k bins, as D_k^- results from a larger input range, when compared to D_k^+, and should be more frequent. To accommodate the disturbances in H_k, H_{k-1} and H_{k+1} are also affected. A possible histogram for this case is shown in Fig. 5. The same analysis, conducted with $V_{\mathrm{t},k}$ slightly under its typical value, would end up on a symmetric conclusion (with histograms flipped). After inspecting the histograms, $V_{\mathrm{t},k}$ can be slightly decreased when H_k^- overcomes H_k^+, or increased if the other way around. The convergence of this method is evidenced through the results shown in Section IV.

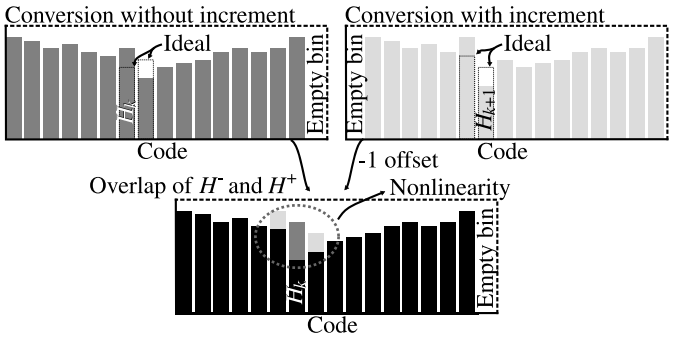

Fig. 5. Histograms H^- and H^+ and superposition when only one of the threshold is not at its ideal place.

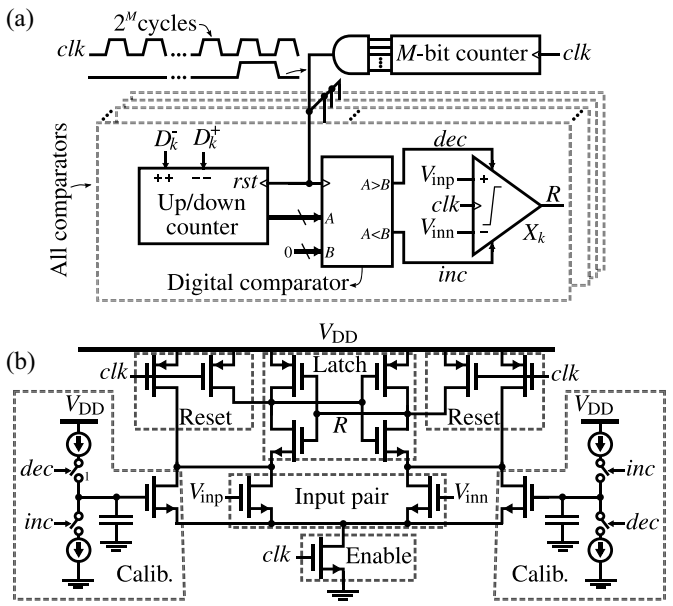

Fig. 6. Possible circuitry implementation for a) the proposed calibration algorithm b) the comparators.

Fig. 6a shows a possible implementation for the control engine of the proposed calibration. The full histograms generation is not required, as the only interest is to know which code between D_k^- and D_k^+ is the most frequent. Thus, for each threshold $V_{\mathrm{t},k}$, an up/down counter can be used to track this information. The $V_{\mathrm{t},k}$ up/down counter is reset to its middle output (considered to be 0 in the given example) at the start of each calibration cycle, having its output incremented by 1 every time that D_k^- is the output and decremented by 1 if D_k^+ is the conversion result. When a calibration cycle is requested, all the up/down counters are verified and computed to the comparator thresholds using a digital comparator. The threshold $V_{\mathrm{t},k}$ is decremented by a small step if the output of the up/down associated to it is higher than 0, or incremented by a small step if smaller. An M-bit counter can be used to generate the calibration trigger, having its size defining the number of conversion cycles required between each calibration. This procedure can run continuously along with the ADC conversion, tracking PVT variations. Fig. 6b shows how the analog comparators can be implemented. By using current sources (or charge-pumps), the threshold of a strong-ARM comparator can be increased or decreased by modifying the voltage of capacitors connected to the gates of an extra input pair.

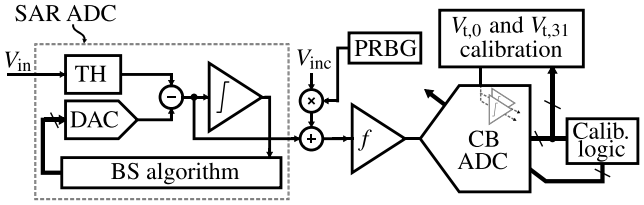

Fig. 7. Architecture used for proof-of-concept of the proposed algorithm.

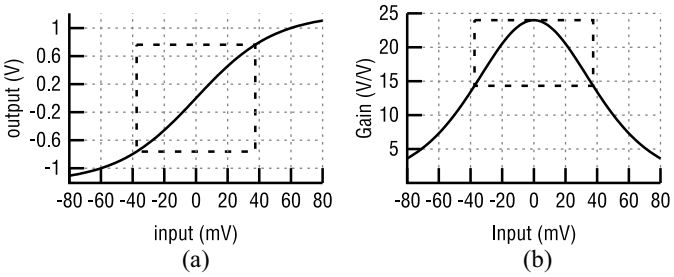

Fig. 8. a) Employed amplifier typical transfer function and b) its derivative (gain), with the typical operation range usage inside the dashed rectangle.

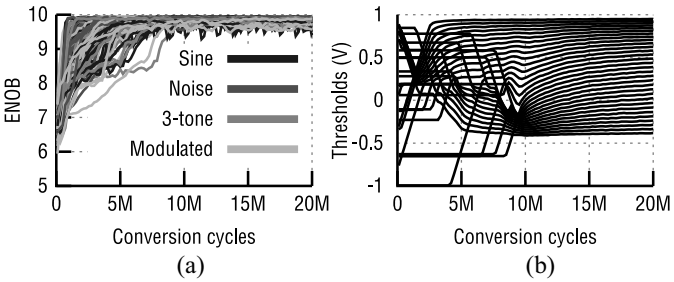

Fig. 9. a) ENOB convergence for 200 Monte Carlo simulation and b) thresholds evolution of a particular case for a 10-bit two-step ADC.

Other analog calibrated comparator approaches are presented in greater details on works [7] and [8].

However, the proposed algorithm does not calibrate the CB ADC offset, which forces that at least one of the thresholds has to be independently determined by another method. Furthermore, the gain is susceptible to mismatches on V_{inc}. Assuming a full-range input on the CB ADC, the lower threshold, $V_{t,0}$, has to be placed precisely on the input range bottom limit when the signal is converted with increment. Therefore, the input with increment can be used to probe $V_{t,0}$. A comparison, using this threshold, over an incremented input that results in "0" implies that $V_{t,0}$ is above its ideal voltage and should be decreased. If this comparison always results in "1", $V_{t,0}$ may be under the incremented input range and should be increased. The same can be done with the upper threshold, $V_{t,2^N-1}$, which should lay on top of the input converted without the increment range. By calibrating both of the border thresholds, all the other thresholds become bound to the CB ADC full-range input, which forces the ADC the desired gain and gives some tolerances to PVT variations on V_{inc}.

IV. Simulation Results

Extensive high-level simulations were performed to validate the effectiveness of the proposed technique. As shown in Fig. 7, a 10-bit two-step ADC (5-bit SAR ADC + 5-bit CB ADC) with a nonlinear amplifier in between is simulated, and the algorithm calibrates the thresholds of the CB ADC. All the simulations presented in this section were obtained using the CABS ADC topology. However, no significant performance difference was observed when a flash ADC was employed. The increment can be added through capacitors on the SAR residue using the same principle of the SAR DAC. Without loss of generality, the SAR and the CB ADCs can also be pipelined to increase the conversion rate.

In the simulations, the amplifier transfer curve is modeled by a sigmoid function and is given by (6).

$$f(v) = r\left(\frac{2}{1+e^{-l(v+V_{os})}} - 1\right) \tag{6}$$

The input-referred offset, V_{os}, has zero nominal voltage, but variations are considered in the Monte Carlo simulation. A common issue of this topology is that an offset on the SAR residue, resulted from an offset on the SAR comparator, or an amplifier offset, can imply on a saturated amplification. Therefore, the amplification gain was selected to allow some tolerance for offset variations. The output range, r, and curve shape, l, were chosen to be typically 1.2 and 40, respectively. The typical transfer curve of the amplifier and its derivative, or gain, are represented in Figs. 8a and 8b, respectively. The typical amplifier operation range is also indicated.

TABLE I
Monte Carlos Simulation Statistics for Each Input Signal Profile

	Sine	Noise	3-tone	Modulated
ENOB (μ±σ)	9.84±0.08	9.86±0.05	9.84±0.05	9.81±0.08
ENOB (min, max)	9.29, 9.95	9.58, 9.96	9.59, 9.94	9.47, 9.95
Cycles to conv. (μ±σ)	3.25M±1.85M	2.84M±1.71M	3.1M±2M	3.14M±1.84M
Cyc. to conv. (min, max)	0.8M, 7.41M	0.7M, 7.66M	0.5M, 9.1M	0.7M, 8.28M

A 200-run Monte Carlo simulation was performed to check the robustness of the proposed algorithm. The ADC reference voltage is set to 2.4 V (differential). The M-bit counter of Fig. 6 is set to 10-bit, implying on one calibration step at every 1024 samples, while the size of up/down counters is 4 bits and a 10-bit PRBG (1024-bit sequence). All the CB ADC comparators have a calibration step of 1 mV and an input-referred noise of 2 mV. An ideal SAR comparator and an amplifier output noise of 2 mV were adopted. The parameters under variation (mean±standard deviation) are, as follows, $V_{t,x}$: nominal±200mV; V_{inc}: $1V_{LSB}$±5%; r: 1.2±10%; l: 40±10%; V_{os}: 0±5 mV; minimum SAR DAC capacitor size: 20 fF±0.2%.

The ADC is simulated using four different input profiles: sinusoidal, white noise, 3-tone and a modulated sine-wave. The parameters of these signals (amplitude, frequency and modulation index) were also randomly sampled. For this simulation, the sample rate is not important as no frequency-dependent effects, such as track-and-hold frequency response and DAC and amplifier settling times, were modeled. In Fig. 9a, the calibration curves for all simulated cases are presented. The statistics for the MC simulation are given on Table I. The low minimum ENOB obtained using the sine profile is due to correlations between the input signal and PRBG periods. Those simulations consider a very ideal input signal, in a practical application, where noise, phase noise and other spectral components are always present on the input,

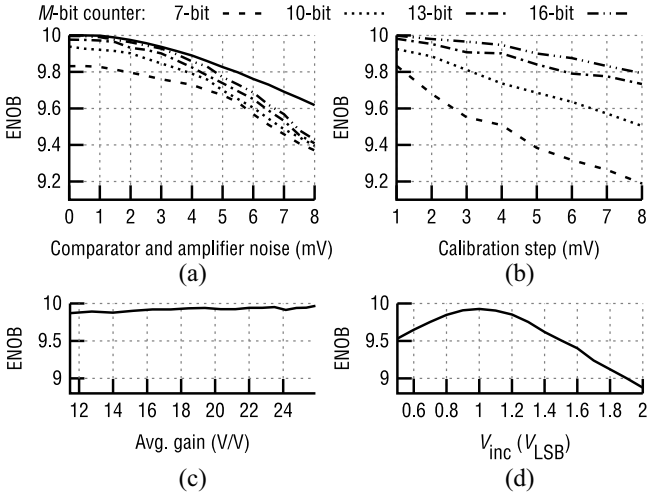

Fig. 10. ADC performance for different calibration histograms sizes under variations of a) comparator and amplifier noise levels b) calibration step voltage and performance under variations of: a) amplifier gain; and b).

this correlation may be attenuated and the ADC performance improved. The convergence speed can be increased by the design of comparators with less mismatch, or by the use of a more dynamic calibration: keeping the calibration step large and the refresh rate high at the ADC startup and then switching to a more conservative configuration for the fine-tunning. Fig. 9b shows the thresholds calibration evolution for a particular case, where all thresholds start with random positions. In this plot, we notice a non-constant threshold spacing, which is a consequence of the front-end amplifier nonlinearity calibration.

Variations over other ADC parameters were also considered and evaluated. In Fig. 10a the ADC performance is shown for different calibration histograms sizes (controlled by the M-bit counter) under comparator and amplifier noise variation, swept together, compared to the one obtained with an ideal thresholds ADC. The main reason for the ENOB drop, compared to the ideal thresholds case, when large noise is considered is the less accurate border thresholds calibration in such conditions. Fig. 10b shows the ADC ENOB considering different M-bit counter sizes and comparators calibration step. To demonstrate the performance of the algorithm under amplifier gain variations, Fig. 10c shows the achieved ENOB after calibration while sweeping l in (6). Furthermore, mismatches on the increment are tolerated and Fig. 10d shows the ADC ENOB as a function of V_{inc}. The main cause for the ENOB drop is the inaccurate increment digital subtraction, which implies on an offset between the conversion with and without the increment.

Although the proposed method is limited to CB ADCs, mostly known by the power-hungry flash ADC, a calibrated CABS ADC can be very power efficient [7], [8]. The amplifier specifications are also relaxed, as open-loop amplification can be used with minimum penalties. Furthermore, the calibration engine has the benefit of a simple digital circuitry and Table II summarizes a comparison with the state-of-the-art. The required calibration digital circuitry for the proposed algorithm requires approximately 500 logic gates and 160 flip-flops, leading to an area overhead of 0.015 mm^2 (already including 50% for routing) in the 130nm-1.2V employed process. Although a fair comparison is difficult, given the fact

TABLE II
POWER CONSUMPTION COMPARISON BETWEEN DIGITAL CALIBRATIONS CIRCUITRY

	[1]	[2]	[3]	[4]	This work
CMOS tech.	90 nm	40 nm	65 nm	350 nm	130 nm
Technique	Adaptive**	Adaptive	Adaptive	Ref. ADC**	Analog
Multipliers	Yes	Yes	Yes	Yes	No
Limitations	3rd ord. poly.	3rd ord. poly.	3rd ord. poly.	Monotonic	Monotonic
Resolution	14 bits	12 bits	10 bits	12 bits	10 bits
ENOB	11.14 bits	10.47 bits	8.39 bits	11.75 bits	9.84 bits
Quant.	Pipeline	Pipeline	Pipeline	Pipeline	CB
Power/MHz	170 μW*	7.7 μW	13.9 μW*	665 μW	~0.5 μW

*Includes all ADC digital power consumption. **Calibrates also DAC capacitors.

that totally different approaches are used to solve the same problem, the advantages of the proposed method concerning digital power consumption are clear. While our algorithm relies only on simple blocks, works [1]–[3] require multipliers to adapt the amplifier transfer function and work [4] uses a linear ADC as the reference and a complex decoder to compensate the nonlinearities.

V. CONCLUSION AND DISCUSSION

In this brief, a novel nonlinearity calibration for an amplifier preceding a CB ADC was presented. To avoid the use of power-hungry amplifiers and complex digital algorithms that can calibrate the nonlinearity of open loop amplification, the calibration of nonlinearities by inverting the amplifier transfer function on the comparators of a comparator-based ADC was proposed. A histogram-based algorithm that calibrates the thresholds of a CB ADC compensating the front-end nonlinearity was also presented and evaluated through behavioral simulations. The concept can be applied on a two-step ADC, having the only limitation of requiring a CB ADC at the back-end. Thresholds mismatches are also accounted by the proposed algorithm and the CB ADC can be designed power-efficient by employing the CABS topology. When compared to algorithms that calibrate the amplifier on the digital domain, the proposed algorithm has the advantage of requiring only simple and low-power logic circuitry, theoretically being able to calibrate any monotonic amplifier transfer function.

REFERENCES

[1] A. Panigada and I. Galton, "A 130 mW 100 MS/s pipelined ADC with 69 dB SNDR enabled by digital harmonic distortion correction," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.

[2] R. Sehgal, F. van der Goes, and K. Bult, "A 12 b 53 mW 195 MS/s pipeline ADC with 82 dB SFDR using split-ADC calibration," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1592–1603, Jul. 2015.

[3] S.-H. W. Chiang, H. Sun, and B. Razavi, "A 10-bit 800-MHz 19-mW CMOS ADC," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 935–949, Apr. 2014.

[4] J. Yuan, S. W. Fung, K. Y. Chan, and R. Xu, "A 12-bit 20 MS/s 56.3 mW pipelined ADC with interpolation-based nonlinear calibration," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 3, pp. 555–565, Mar. 2012.

[5] M. J. Kramer, E. Janssen, K. Doris, and B. Murmann, "A 14 b 35 MS/s SAR ADC achieving 75 dB SNDR and 99 dB SFDR with loop-embedded input buffer in 40 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2891–2900, Dec. 2015.

[6] Z. Gu and W. M. Snelgrove, "A novel self-calibrating scheme for video-rate 2-step flash analog-to-digital converter," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, May 1992, pp. 601–604.

[7] G. Van der Plas and B. Verbruggen, "A 150MS/s 133 μW 7b ADC in 90nm digital CMOS using a comparator-based asynchronous binary-search sub-ADC," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2008, pp. 242–610.

[8] F. Rabuske, T. Rabuske, and J. Fernandes, "A 5-bit 300–900-MS/s 0.8–1.2-V supply voltage ADC with background self-calibration," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 1, pp. 1–5, Jan. 2017.