An 8-bit 1.25GS/s CMOS IF-Sampling ADC with Background Calibration for Dynamic Distortion

Si Chen and Boris Murmann

Dept. of Electrical Engineering, Stanford University, Stanford, CA 94305, USA
E-mail: chenbill@stanford.edu

Abstract—An 8-bit, 1.25-GS/s subsampling ADC with digital background calibration for frequency-dependent distortion is presented in this paper. The derivative-based dynamic distortion model is extended to linearize the ADC frontend including the input buffer and the T/H. A low sampling rate auxiliary ADC is included on chip to acquire real-time, high-linearity reference samples to enable continuous background calibration. The digital post-distortion (applied off chip) enables SFDR improvements of 10 dB for 2.5 GHz inputs. Temperature sweeps from 10°C to 80°C confirm the scheme's robustness.

Keywords—A/D conversion; subsampling; auxiliary ADC; frequency-dependent nonlinearity; background calibration

I. INTRODUCTION

Modern phased array applications, such as radar systems, require many parallel medium-resolution, high-speed ADCs in the receiver chain [1]. There is a trend toward designing these ADCs to subsample and down-convert signals from the intermediate frequency (IF) directly to the baseband, eliminating the need for additional mixers to reduce the overall component count and system cost [2, 3] (see Fig. 1). As a result, achieving high linearity performance at IF poses a challenging design task, especially when the ADC must be realized at a cost-efficient, trailing CMOS node. The ADC's input buffer and track-and-hold (T/H) bandwidth limitation, coupled with other frontend static nonlinearity sources (nonlinear buffer g_m) generates frequency dependent distortion that limits the overall linearity (see Fig. 2).

To mitigate frequency-dependent nonlinearities at the ADC frontend, prior art has mainly focused on analog approaches [4-6]. In such implementations, the ADCs' input buffers operate at
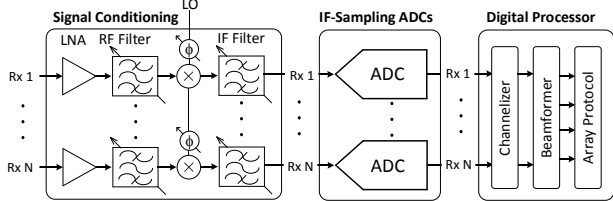

Fig. 1. Digital beamforming radar system block diagram.

very large bias currents and provide large amount of excess bandwidth only to minimize dynamic distortion products. Beyond the power concerns, the resulting large ADC input capacitance renders this approach inappropriate in many applications. On the other hand, digital techniques have been proposed to correct the dynamic distortion at the ADC output. This approach is particularly attractive for radar applications,

since it off-loads power expenditure and complexity from the densely arrayed analog domain to the digital backend processor (see Fig. 1). In the digital backend, power consumption is less critical and the required computing resources are readily available, typically within a leading-node FPGA.

The digital linearization techniques used in [2] and [7] are based on derivative-based distortion models, but the implementation of [7] limits the input frequency to the first Nyquist zone. The work of [2] considers higher Nyquist zones, but the solution requires up-sampling and interpolation of the ADC output data. Moreover, both of these works are limited to foreground calibration, which is insufficient for applications like airborne radar systems, where continuous model updates are needed to adapt to environmental variations (voltage, temperature).

In this paper, we present an improved digitally-assisted ADC implementation that achieves distortion correction up to the 4th Nyquist zone without up-sampling the ADC output data. In addition, our ADC is the first to demonstrate background model calibration capability for dynamic distortion at the ADC frontend. The ADC is implemented in TSMC's 65nm CMOS process.

This paper is organized as follows. In Section II, the ADC frontend implementation and its dynamic distortion modeling are discussed. Section III presents the overall ADC architecture. The detailed digital filter implementation is elaborated in Section IV. In Section V, the test-chip measurement result is shown. Section VI concludes this paper.

II. IF-SAMPLING ADC FRONTEND DESIGN AND DISTORTION MODELING

Fig. 3(a) shows the simplified half-circuit design of the ADC frontend buffer and T/H. Transistors M0 and M1 form a source-follower buffer that drives the bootstrapped T/H switch M2 and its sampling capacitance, Cs. Unlike the conventional approach in [6] where the source-follower biasing current, I_B, is designed to be much larger than the maximum load-driving current, i_o at high input frequency, the I_B in this source-follower is reduced by 3x. The new I_B value only needs to satisfy the settling requirement of the T/H at the desired sampling speed. In addition to this power reduction, the ADC input capacitance also decreases as a result of the smaller device sizes, significantly relaxing the driving requirement for the previous stage. The downside of the current reduction is a large relative variation in i_d at higher frequency and this increases buffer distortion.
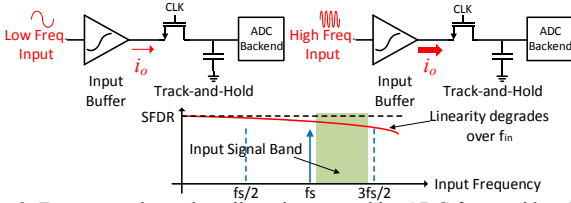
Fig. 2. Frequency dependent distortion caused by ADC frontend bandwidth limitation and nonlinear buffer g_m.
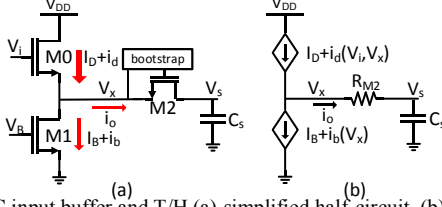

Fig. 3. ADC input buffer and T/H (a) simplified half-circuit. (b) track-mode model.

However, this frequency-dependent nonlinearity can be modeled and subsequently canceled in the digital domain as shown below.

Since track-mode nonlinearity is the dominant distortion source at high frequencies [2], we model the frontend in the track-mode as shown in Fig. 3(b). The currents i_d and i_b are modeled as nonlinear functions of (V_i, V_x) and (V_x), respectively. The following polynomials are sufficient to model the nonlinear functions with the required accuracy:

$$i_d = d_1 V_i + d_2 V_i^2 + d_3 V_i V_x + d_4 V_x + d_5 V_x^2 \qquad (1)$$

$$i_b = b_1 V_x + b_2 V_x^2 + b_3 V_x^3 \qquad (2)$$

Here, d_1 to d_5 and b_1 to b_3 are circuit-specific constants. Summing all currents at V_x node and substituting into (1) and (2), we obtain:

$$I_D + i_d = I_B + i_b + C_s V_s' \qquad (3)$$

$$I_B + d_1 V_i + d_2 V_i^2 + d_3 V_i V_x + d_4 V_x + d_5 V_x^2 \\ = I_D + b_1 V_x + b_2 V_x^2 + b_3 V_x^3 + C_s V_s' \qquad (4)$$

where V_s' is the time derivative of V_s. Equation (4) shows the single-ended version of the input and output relationship. If we substitute $V_i = V_{ic} \pm \frac{1}{2} V_{id}$, $V_x = V_{xc} \pm \frac{1}{2} V_{xd}$, $V_s = V_{sc} \pm \frac{1}{2} V_{sd}$ into (4) and subtract the two resulting equations for the positive

and negative half-circuits, we have the following relationship for differential signals:

$$V_{id} = A_1 V_{xd} + A_2 V_{xd}^3 + A_3 V_{sd}' \qquad (5)$$

where A_1, A_2 and A_3 are the model coefficients which depend on the constant d's and b's and the common-mode voltages, V_{ic} and V_{xc}. Variations in V_{ic} and V_{xc} could potentially generate even order distortions in the output. However, our differential input network is well phase-balanced to ensure stable common-mode voltages. As a result, (5) is sufficient for modeling the nonlinearity and it is not necessary to include even order terms in the model.

We subsequently substitute $V_{xd} = V_{sd} - R_{M2} C_s V_{sd}'$ in (5) to obtain an explicit relationship between the input and the output:

$$V_{id} = B_1 V_{sd} + B_2 V_{sd}' + B_3 V_{sd}^3 + B_4 V_{sd}^2 V_{sd}' + B_5 V_{sd} V_{sd}'^2 \\ + B_6 V_{sd}'^3 \qquad (6)$$

Equation (6) takes into account of both static and dynamic distortion generated in the ADC frontend. Similar to [2], the model is already conveniently in inverse form. The desired input, V_{id} is directly expressed as a linearizing function of the nonlinear ADC output, V_{sd}. In addition, the model is linear in its coefficients and can be trained using linear regression methods or direct least squares solution. The frequency-dependent part of the model is captured in the derivative terms, for which we devise an estimation method in the following sections.

III. ADC ARCHITECTURE

To test the effectiveness of our dynamic distortion correction model for the entire IF-Sampling frontend, we designed and evaluated an 8-bit, 1.25 GS/s time-interleaved SAR ADC in silicon. This ADC was custom-designed to meet the requirements of a digital beamforming Radar system [1].

The ADC architecture is shown in Fig. 4. As described in the previous section, the ADC frontend consists of an NMOS source-follower input buffer followed by a bootstrapped T/H, which samples at the full clock rate of 1.25 GHz. We employed bottom-plate sampling in this T/H to eliminate charge injection related distortion and to allow the freedom of choosing the common-mode voltage for the next stage. The following sample
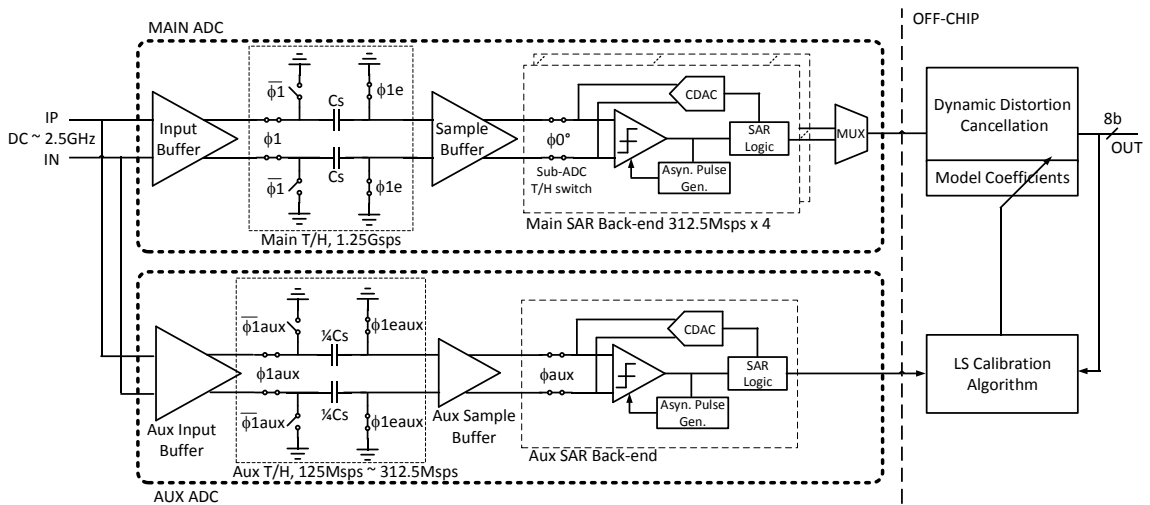

Fig. 4. ADC architecture.

buffer is implemented as a PMOS source-follower. It isolates the ADC frontend and drives the subsequent conversion stage. To achieve the aggregate conversion speed of 1.25 GS/s, we time-interleaved four 8-bit asynchronous SAR ADCs, each running at 312.5 MS/s. The implementation of the SAR ADC is based on a previous design [8].

In order to achieve continuous digital post-distortion model updates in the background, we need to provide a real-time linearity reference for the current ADC output signal. As a solution, we implemented a parallel auxiliary ADC on the same chip. The auxiliary ADC shares the same frontend structure as the main ADC. To ensure good linearity performance throughout the input band, aux ADC frontend bandwidth is extended by reducing its sampling capacitance by 4x. As a result, the thermal noise in the auxiliary ADC increases. However, since random noise is averaged out in the calibration process, the post-distortion filter performance is not affected. Furthermore, since it is not necessary to update the model coefficients on every ADC sample, we reduced the sampling speed of the auxiliary ADC and made it programmable from a tenth to a quarter of the sampling speed of the main ADC to save power. As a result of the speed reduction, the settling requirement for the auxiliary sample buffer is relaxed. Its power is reduced to 3.6mW, only half that of the main ADC buffer. Moreover, due to the reduced sampling rate, the auxiliary ADC backend can also be realized with only a single-channel SAR ADC.

The post-distortion filter and its model calibration is implemented in software off-chip. The detailed description of the implementation is described in the next section.

IV. DIGITAL FILTER IMPLEMENTATION

The main ADC streams output samples at 1.25 GHz, using LVDS I/O into a 512 kB (512 kSamples) memory inside a logic analyzer for post-processing, while the aux ADC outputs the reference samples up to the quarter rate (312.5 MS/s) into a 128 kB memory. The post-distortion filter is implemented in synthesizable Verilog code to operate on these samples. ModelSim and MATLAB are used to verify the design. Fig. 5 shows the block diagram of the digital post-distortion filter implementation.

The post-distorter first computes the derivative of the main ADC output using a discrete-time differentiator corresponding to the desired Nyquist zone. The differentiator introduces a fractional delay to the signal. Therefore, a fractional delay filter is also needed to help re-align the signal sample to its computed derivative. The next block is a multiplier-adder bank which computes the required distortion correction terms according to our model. Finally, the linearized ADC output is computed through a weighted sum of these model terms. The weights k_1 to k_6 are updated through the background calibration block. We stream the reference auxiliary ADC output and the down-sampled main ADC model terms (matched to aux ADC sample-rate) into memory. We then update the model parameters using least-square solution on every one-thousand-sample blocks. Direct least-square solution is achievable here because our model only requires a small 6-by-6 matrix inversion.
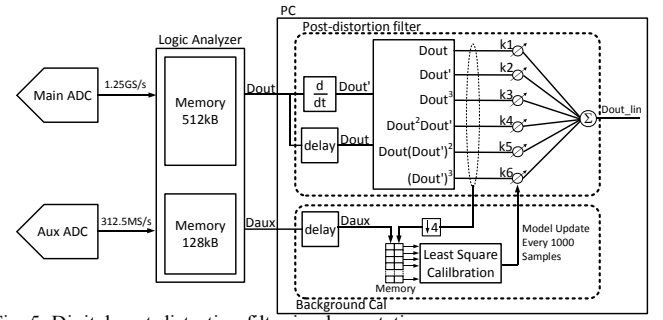
Fig. 5. Digital post-distortion filter implementation.

Since the dynamic distortion is directly modeled through the derivative terms, it is crucial to ensure good accuracy in the discrete-time differentiator design. In addition, low complexity design is also important for achieving power efficiency because derivative estimation is carried out on every ADC output sample. As shown in Fig. 6(a), the frequency response of a differentiator when aliased back into baseband, does not follow $|j2\pi f|$ for signals beyond the first Nyquist zone. To implement a discrete-time differentiator for higher Nyquist zone signals, we need to replicate the aliased version of the frequency response. Fig. 6(b) shows the frequency response of the ideal 4th Nyquist zone differentiator and the FIR filter that we implemented using the Kaiser windowing method. The FIR filter replicates the ideal response for 90% of the Nyquist zone. Unlike [2], this differentiator implementation avoids the need for up-sampling and interpolation of higher Nyquist zone signals before feeding into the differentiator which in turn relaxes the digital clock speed requirement and reduces implementation complexity.

V. MEASUREMENT RESULTS

The test chip was fabricated in TSMC's 65nm CMOS process. Fig. 7 shows a die photo of the chip. The ADC occupies an active area of 390 μm x 300 μm.

Fig. 8 shows that the auxiliary ADC maintains a linearity performance around 60 dB SFDR across the entire input frequency range. On the other hand, the main ADC is affected by frequency-dependent nonlinearity without post-distortion correction and its SFDR reduces to 50 dB at 2.5 GHz. To demonstrate the effect of the correction filter and background calibration, we feed in several single-tone sine wave signals with different frequencies one after another and turn on the calibration algorithm to allow model coefficient update on these input data. To evaluate the correction result, we fix the trained model coefficients, and look at the ADC output spectrum of a sine wave signal with and without the correction filter. Fig. 9 shows that for a full-scale input signal at 2305 MHz, the 3rd order harmonic is reduced by 9 dB. The SFDR of the main ADC is recovered close to that of the auxiliary ADC. The frequency of the evaluation sine wave signal is specifically chosen to differ
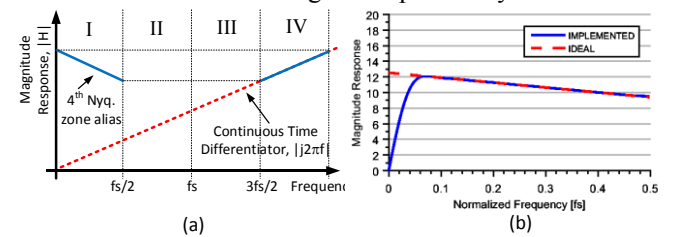
Fig. 6. Frequency response of differentiator (a) effect of aliasing in digital domain (b) 4th Nyquist zone implementation.
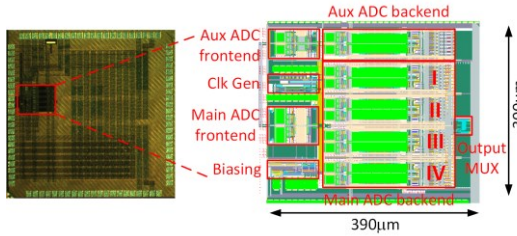
Fig. 7. Die photo

from those of the training signals. This is important in showing that our correction model can generalize to unseen data. Furthermore, to verify that the nonlinearity correction model works across the whole band, we sweep the input frequency across the Nyquist zone and measure the corresponding SFDR improvement. Fig. 10(a) plots the SFDR improvement for signals in the 4th Nyquist zone. It is noticed that at frequencies beyond 2.4 GHz, the SFDR improvement is reduced. This is due to the discrete-time differentiator's inaccuracy close to the band edge as shown in the previous section.

Fig. 10(b) demonstrates the robustness of background calibration over foreground calibration. We compare the SFDR improvement of the two calibration methods when the ADC's operating temperature varies. For one set of tests, we conduct a single model-calibration at a fixed temperature, in this case 60°C. While fixing the model coefficients, we vary the chip temperature from 10°C to 80°C and observe the SFDR improvement. For the next set of tests, we turn on background calibration while varying the temperature. The results show that the model coefficients are sensitive to temperature changes and that a robust post-distortion filter requires continuous model updates in the background.

The main ADC core consumes 49.2 mW of power excluding I/O. The frontend draws 10.8 mW of power from a 1.8 V supply; the clock distribution, the backend SAR ADC and biasing circuit draws 38.4 mW from a 1.2 V supply. The auxiliary ADC, when operating at the quarter speed of the main ADC, draws 19.2 mW. If model-update is not needed, the auxiliary ADC can be turned off to save power. Based on the number of multipliers and adders required in the digital post-distortion filter, we roughly estimate its power consumption to be 140 mW if it were implemented in a 65 nm process. However, in the actual system, the digital resources will be amortized within the digital beamforming processor, which will use a leading edge CMOS process.

VI. CONCLUSION

In this paper, we presented the first IF-sampling ADC with an on-chip background calibration path for dynamic distortion. A derivative-based distortion model is employed to linearize the ADC frontend input buffer and T/H. The off-chip post-distortion filter improves linearity up to the 4th Nyquist zone with a maximum SFDR improvement of 10 dB. The robustness of the ADC and background calibration is tested by varying the operating temperature by 70°C.
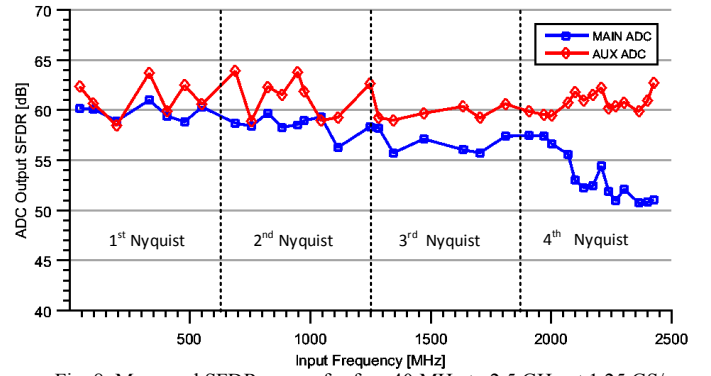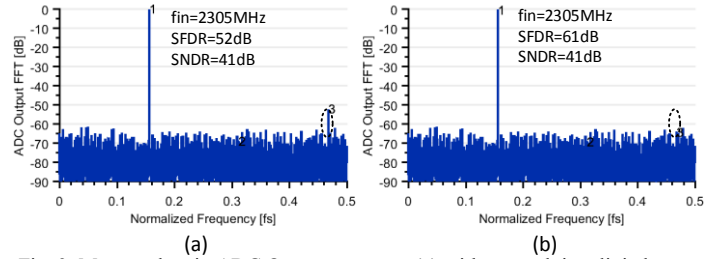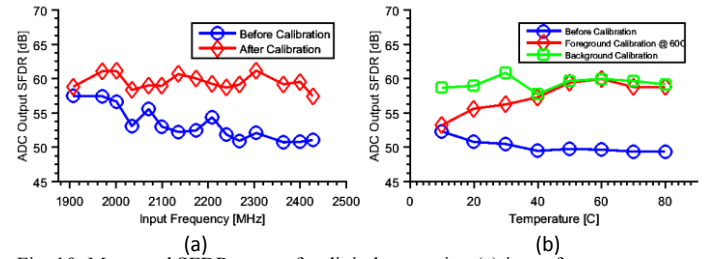
ACKNOWLEDGMENT

Fig. 8. Measured SFDR sweep for f_{in} = 40 MHz to 2.5 GHz at 1.25 GS/s.

Fig. 9. Measured main ADC Output spectrum (a) without applying digital correction, (b) with digital correction.

Fig. 10. Measured SFDR sweep for digital correction (a) input frequency sweep for 4th Nyquist zone (b) temperature sweep for fin = 2400 MHz.

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