A 12-bit 75-MS/s Pipelined ADC Using Open-Loop Residue Amplification

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***Abstract*—Precision amplifiers dominate the power dissipation in most high-speed pipelined analog-to-digital converters (ADCs). We propose a digital background calibration technique as an enabling element to replace precision amplifiers by simple power-efficient open-loop stages. In the multibit first stage of a 12-bit 75-MSamples/s proof-of-concept prototype, we achieve more than 60% residue amplifier power savings over a conventional implementation. The ADC has been fabricated in a 0.35-μm double-poly quadruple-metal CMOS technology and achieves typical differential and integral nonlinearity within 0.5 LSB and 0.9 LSB, respectively. At Nyquist input frequencies, the measured signal-to-noise ratio is 67 dB and the total harmonic distortion is −74 dB. The IC consumes 290 mW at 3 V and occupies 7.9 mm^2.**

***Index Terms*—Analog-to-digital conversion, adaptive systems, calibration, CMOS analog integrated circuits, linearization techniques, parameter estimation.**

I. Introduction

THE pipelined analog-to-digital converter (ADC) in switched-capacitor CMOS technology is a popular architecture for high-speed data conversion in communication systems, imaging, ultrasound front-ends, and many other applications. Fuelled by aggressive device scaling in modern integrated circuit technology, practically attainable operating speeds of this converter have increased by almost two orders of magnitude in the last 15 years [1], [2]. In addition to the ever-growing demands in conversion bandwidth, low power dissipation, and compatibility with deep-submicron technology have emerged as important metrics in state-of-the-art designs. For the most part, this trend is explained by the increasing demand for portability, as well as recent efforts in system-on-chip (SoC) integration. In SoC implementations, data converters are embedded on the same chip with powerful fine-line digital signal processing, resulting in a limited budget for their total heat and power dissipation.

Among the key building blocks in pipelined ADCs are the residue amplifiers that interface successive converter stages. Especially in the converter front-end, these gain elements have to meet very stringent speed, noise, and linearity requirements and tend to dominate overall power dissipation. To address this issue, a variety of techniques have been developed to minimize amplifier power in pipelined ADCs. Among them, stage scaling [3], [4], optimization of the per-stage resolution [5]–[7], and amplifier sharing techniques [8], [9] are commonly used. In addition to their dominance in power consumption, it has also been recognized that residue amplifiers are most susceptible to complications that arise from continuing integrated circuit technology scaling [10], [11]. For implementations in future deep-submicron processes, it is often predicted that limited supply headroom and low intrinsic device gain may lead to a relative power increase in such noise-limited precision analog circuit blocks [12], [13].

This work explores an alternative to the residue amplification approach used in conventional pipelined ADCs. We propose a digital background calibration technique as an enabling element to replace precision amplifiers by simple power-efficient open-loop stages. In the proposed implementation, a digital postprocessor continuously estimates and removes errors from the imprecise and nonlinear open-loop gain. In fine-line technologies, this translation of the analog precision problem into the digital domain results in significant overall power savings and may help overcome future scaling limitations. As an additional benefit, the use of simplified amplifiers may also help to increase the maximum conversion speed for a given technology.

In this paper, we describe the implementation and measurement results of a 12-bit 75-MSamples/s pipelined ADC that uses open-loop residue amplification in its multibit first stage [14]. In order to facilitate and expedite the evaluation of the proposed open-loop approach, we based our design on an existing commercially available pipelined ADC in 0.35-μm CMOS technology [15]. In Section II, we briefly review the architecture of this proof-of-concept prototype. Section III highlights the key differences between conventional pipeline stages and the open-loop approach proposed herein. In Section IV, we establish a first-order model for errors in the open-loop pipeline stage, followed by a methodology for their digital compensation in Section V. Section VI describes the digital background calibration technique that is used to continuously estimate and track the required compensation parameters. Finally, Sections VII and VIII elaborate on implementation details and measured results.

II. ADC Architecture

Fig. 1 shows a block diagram of the experimental converter, which closely resembles the architecture of the original design before reuse [15]. The pipeline core of this converter is partitioned into a multibit first stage with an effective resolution of three bits, followed by eight stages, each resolving one bit effectively, and finally, a 3-bit flash sub-ADC. Out of the 14 bits of raw data, the two least significant digits are used for calibration

Manuscript received April 13, 2003; revised July 6, 2003. This work was supported by Analog Devices and UC MICRO under Grant 01-006.

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Digital Object Identifier 10.1109/JSSC.2003.819167

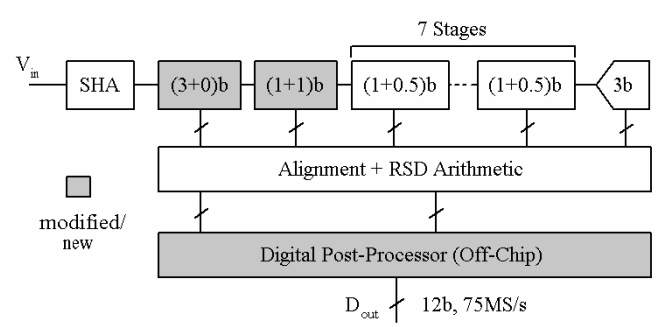

Fig. 1. ADC block diagram.

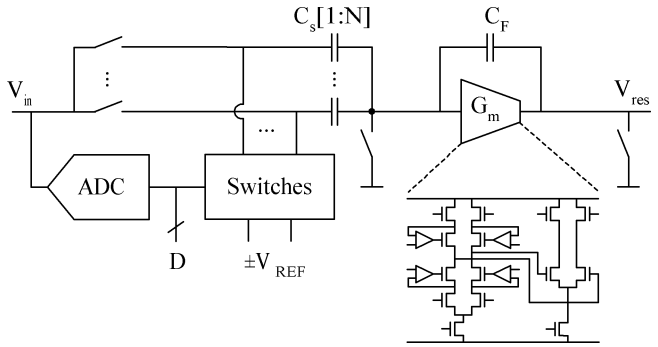

Fig. 2. Conventional pipeline stage.

purposes only and are truncated in the final conversion result. Stages 3–9 are implemented with 0.5 bit redundancy as standard 1.5-bit stages. As explained in Section V, the second stage of this design was modified to use one full bit of redundancy.

Compared to [15], the key modifications in the context of this work are the replacement of the stage-1 precision amplifier with an open-loop topology, and the addition of an off-chip digital postprocessor to correct for resulting conversion errors. Conceptually, the proposed scheme can be extended to multiple open-loop stages in the converter front-end. For simplicity and improved transparency, only the first and most critical converter stage is converted to open-loop amplification in this demonstration vehicle.

III. Pipeline Stage Residue Amplification

A. Conventional Approach

Fig. 2 shows a conceptual single-ended block diagram of the first pipeline stage in the original state-of-the-art reference design [15]. This circuit consists of a flash-type sub-ADC, a capacitive charge redistribution network, and a high-performance operational transconductance amplifier (OTA). The circuit operates in two main clock phases. During the sampling phase, the stage input signal $V_{\rm in}$ is acquired. In a second phase, a residual charge packet, controlled by the local conversion result D, is redistributed onto the feedback capacitor C_F to produce the amplified stage residuum $V_{\rm res}$. In this conventional scheme, the use of electronic feedback around the OTA results in a precise and drift insensitive stage transfer function. As in many other electronic systems, feedback in this circuit serves two main purposes: 1) to mitigate the impact of device nonlinearities in the OTA; and 2) to desensitize the overall transfer

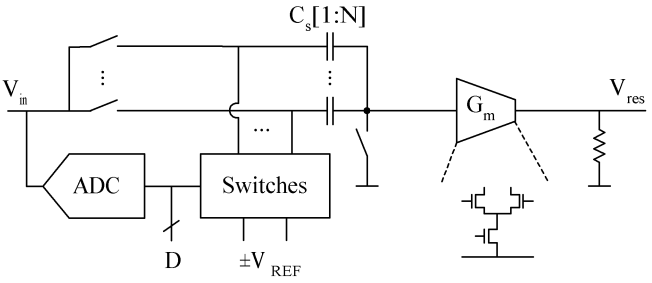

Fig. 3. Proposed open-loop pipeline stage.

function to changes in ambient operating conditions, such as temperature. The cost of these desirable features is an excessive OTA voltage gain requirement. Since the effectiveness of feedback is proportional to the system's loop gain, high precision necessitates the use of complex high-gain OTA topologies. As is typical in high-resolution pipelined ADC front-ends, [15] uses a two-stage gain-boosted amplifier with an open-loop gain $>$100 dB to meet the stringent design requirements. In fine-line technology with low intrinsic device gain and limited supply headroom, such amplifiers are hard to implement and tend to be power inefficient.

B. Proposed Open-Loop Circuit

Recently, the benefits of using open-loop structures in high-speed pipelined ADCs have been recognized and demonstrated. The 8-bit ADCs reported in [16] and [17] use open-loop current-mode residue amplification to achieve excellent power efficiency at high conversion speeds. In this work, we use a voltage-mode topology in conjunction with appropriate calibration techniques to push the applicability of open-loop structures into the 12-bit domain. Fig. 3 shows a conceptual schematic diagram of the proposed stage implementation. Except for the charge redistribution phase, the operation of this circuit is similar to the conventional topology described above. Unlike in the closed-loop implementation, the residual charge packet on the capacitive array is not redistributed onto a feedback capacitor, but remains in place to produce a small voltage at node V_x. This residuum is fed into a resistively loaded differential pair to produce the desired full-swing residue voltage $V_{\rm res}$. In this modified circuit, the high gain requirement in the transconductor is dropped, resulting in a simple power-efficient amplifier topology with improved deep-submicron compatibility. These advantages, however, come at the price of several new nonidealities in the stage transfer function that have not been addressed in previous work. With particular focus on the implementation in stage 1 of our design, the remainder of this paper will focus on the analysis of these errors, their digital domain compensation, and experimental verification of the approach.

IV. Error Model for Open-Loop First Stage

With sufficient loop gain in the conventional implementation of Fig. 2, deviations of the stage transfer function from ideality are mostly due to capacitor mismatch and offset errors in the coarse sub-ADC. With the introduction of the simplified

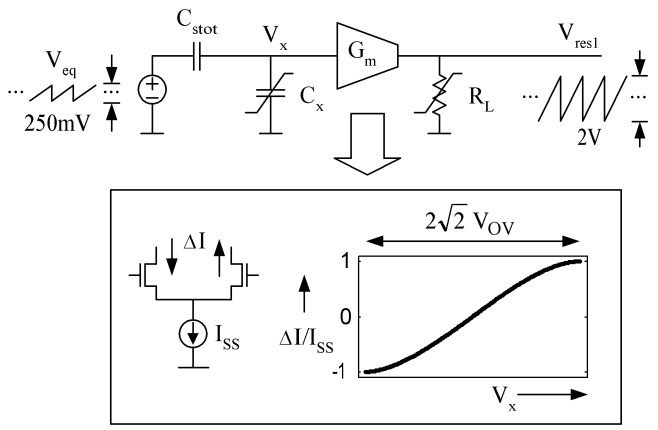

Fig. 4. Model for nonlinearity analysis.

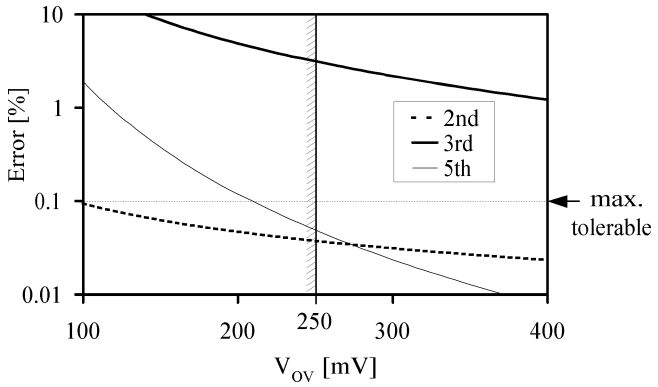

Fig. 5. Differential pair nonlinearity error.

open-loop amplifier of Fig. 3, several additional error sources must be considered. Fig. 4 depicts an appropriate model for further analysis. Here, the capacitor array is replaced with its Thévenin equivalent, consisting of the total array capacitance $C_{\rm stot}$ and an equivalent voltage source $V_{\rm eq}$ that represents the local stage residuum before amplification. Ideally, the transfer function from $V_{\rm eq}$ to the output $V_{\rm res}$ should be linear with a precise gain of 2^R, where R is the effective stage resolution, taking on a value of three in our particular implementation. In the circuit of Fig. 4, the transfer function is neither linear nor precisely defined. The linear gain term from source to output is set by the amount of parasitic capacitive attenuation at node V_x and the $G_m \cdot R_L$ product, which typically cannot be accurately controlled. Furthermore, the amplification is nonlinear, primarily due to three effects: 1) voltage dependence of the capacitor C_x, which represents the differential pair input load and parasitic junction capacitors; 2) nonlinearity in the resistive load; and 3) gain compression and mismatch in the differential pair. With respect to the tolerable errors in the first pipeline stage of this design, none of the above nonlinearities are negligible. However, for a practical and optimized implementation, it is reasonable to assume that the differential pair dominates the overall cascade nonlinearity that links $V_{\rm eq}$ and $V_{\rm res1}$. In this analysis, we therefore focus on this particular error component, noting that some of the distortion is actually caused by other nonidealities. Assuming an ideal square law transistor model and memoryless nonlinearities, one can express the differential pair I–V relationship, graphically illustrated at the bottom of Fig. 4, through a power series of the form [18]

$$\frac{\Delta I}{I_{\rm SS}} = \left(\frac{V_x}{V_{\rm OV}}\right) + \frac{1}{4}\frac{\Delta\beta}{\beta}\left(\frac{V_x}{V_{\rm OV}}\right)^2 - \frac{1}{8}\left(\frac{V_x}{V_{\rm OV}}\right)^3 - \frac{1}{128}\left(\frac{V_x}{V_{\rm OV}}\right)^5 - \dots \quad (1)$$

where ΔI and $I_{\rm SS}$ are the differential pair output and tail current, respectively, $V_{\rm OV}$ is the quiescent point gate overdrive $(V_{GS} - V_T)$, and $\Delta\beta/\beta$ is the current factor mismatch between the two transistors. It should be noted that the expression given in (1) overestimates distortion for short channel transistors with velocity saturation. In principle, velocity saturated transistors can be modeled as resistively degenerated square law devices [19], which leads to a reduction in the expected nonlinearity. However, for the qualitative arguments made in this section, (1) can be regarded as a sufficiently accurate conservative expression.

Based on the derived nonlinearity model, we now investigate on a reasonable choice for the gate overdrive $V_{\rm OV}$, which in turn dictates the minimum required tail current $I_{\rm SS}$ for the differential pair. Fig. 5 shows the relative peak magnitude of the nonlinear terms in (1) as a function of $V_{\rm OV}$. In this graph, it is assumed that the peak-to-peak input voltage of the transconductor at node V_x is 250 mV. This approximate value is dictated by the implementation, with a desired full-scale swing at $V_{\rm res1}$ of 2 V, an approximate stage gain of 8, and only a small amount of capacitive attenuation from C_x. For the second-order term in the diagram we assume a transistor matching of $\Delta\beta/\beta = 0.3\%$. Shown as a horizontal line is the tolerable stage-1 residue error. Since $V_{\rm res1}$ feeds into a back-end with 9-bit effective resolution, an upper bound for the error is given by 1/2 LSB at the 9-bit level or approximately 0.1%.

As is apparent from the graph, choosing a large $V_{\rm OV}$ results in small nonlinearity errors. However, in order to maintain constant transconductance $G_m \cong I_{\rm SS}/V_{\rm OV}$ in the differential pair, any increase in gate overdrive must be proportionally compensated by additional tail current. As a compromise, the goal in this work was to choose $V_{\rm OV}$ only reasonably large to yield a compact low-order model for stage nonlinearities. As illustrated in Fig. 5, this is accomplished by choosing the gate overdrive voltage larger than 250 mV. Beyond this value, both the second- and fifth-order error contributions become negligible compared to the available error budget. For all practical values of $V_{\rm OV}$, however, cubic distortion is unavoidable and must be compensated in the digital domain. With these considerations, Fig. 6 summarizes the overall model for the open-loop converter stage of this design. In addition to the discussed third-order nonlinearity and the uncertainty in the linear gain term Δ, offset errors in the amplifier and sub-ADC are added for completeness. Also present are capacitor matching errors, which result in nonideal sub-DAC levels. However, as in the implementation of [15], these errors did not exceed their tolerable budget and were not addressed in this work.

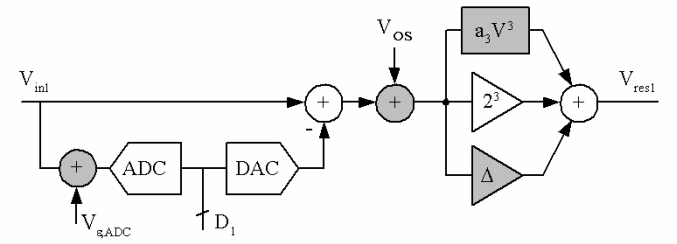

Fig. 6. Open-loop pipeline stage model with error sources.

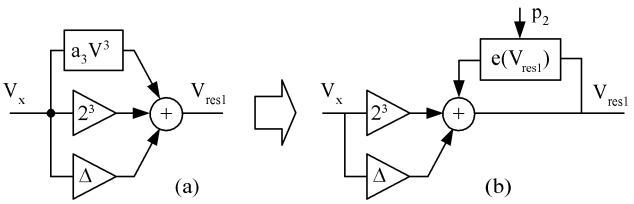

Fig. 7. Amplifier model with: (a) input referred nonlinearity, (b) output referred nonlinearity.

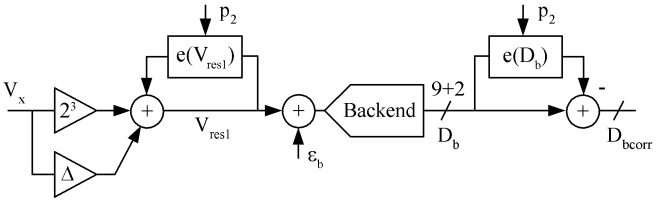

Fig. 8. Digital nonlinearity compensation.

V. Digital Domain Error Compensation

Based on the model established in the previous section, we now describe the digital domain correction mechanism for the stage-1 nonidealities under consideration, which are shown as shaded blocks in Fig. 6. Compensation techniques for the sub-ADC decision errors, amplifier offset, and linear gain error have been described in numerous publications. In order to tolerate the additive errors $V_{\varepsilon,\mathrm{ADC}}$ and V_{OS} in stage 1, we use a full bit of comparator redundancy in the succeeding second stage. Similar to the approach in [20], we thereby achieve overranging tolerance, allowing the stage-1 residue to exceed its full-scale boundaries. The linear stage gain error Δ is addressed by digitally modifying the weight of sub-ADC decisions, as described in [21]. For this correction, a single parameter that captures the deviation of the actual gain from its ideal value must be known. In the remainder of this paper, we will refer to this quantity as calibration parameter p_1.

In addition to the existing correction techniques quoted above, we have developed a digital compensation scheme for the third-order nonlinear residue error caused by gain compression in the open-loop amplifier. In Fig. 7(a), this nonideality is modeled as a function of the amplifier input V_x. Alternatively, as illustrated in Fig. 7(b), the error can be modeled as a function of the residuum V_{res1}. Through inversion of the overall cubic amplifier polynomial with $a_3 < 0$ (gain compression), the following expression for the equivalent output referred error function in Fig. 7(b) can be found:

$$e(V_{\mathrm{res1}}) = V_{\mathrm{res1}} - 2\sqrt{-\frac{1}{3p_2}} \times \cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{V_{\mathrm{res1}}}{2\cdot\sqrt{-\frac{1}{27p_2}}}\right)\right] \quad (2)$$

with a single parameter

$$p_2 = \frac{a_3}{(2^3-\Delta)^3}. \quad (3)$$

Since the back-end stages of the converter produce a quantized digital representation of V_{res1}, the error can be compensated by operating on the digital back-end code, as shown in Fig. 8. This correction mechanism is accurate provided that the back-end conversion error (ε_b in Fig. 8) is small. This term can be decomposed into three components: 1) quantization error; 2) a static input-referred offset; and 3) linear and nonlinear or code-dependent errors. In a practical functioning converter, the third component must inherently be kept small, either by design or some form of calibration. The static offset error component is tolerable in a conventional converter, usually due to the presence of comparator redundancy and digital correction arithmetic. For the converter described here, it can be shown that several tens of millivolts in back-end offset can be tolerated before the proposed code domain linearization becomes inaccurate. This requirement is easily met in the actual implementation of the prototype. As a last nonideality to be considered, the inherent quantization error of the back-end would limit the correction steps to 1-LSB increments. To overcome this problem, our converter uses two redundant back-end bits to provide for additional decision levels, resulting in sub-LSB nonlinearity correction.

In a practical implementation of the nonlinearity correction scheme depicted in Fig. 8, the required two-dimensional correction function $e(D_b, p_2)$ can be precomputed and stored in a ROM lookup table. Since the expression of (2) describes smooth continuously varying data, incremental lookup or compression techniques [22] can be used to minimize the required memory size.

Since the proposed converter uses open-loop amplification, any drift of errors is not attenuated by feedback. Consequently, both of the required calibration parameters p_1 and p_2 must not only be precisely determined, but also track variations caused by changing ambient conditions during converter operation. The digital background calibration algorithm described in the next section was designed to meet these requirements.

VI. Digital Background Calibration Technique

Background calibration of monolithic ADCs has been a popular research topic since the mid-1990s [23]. In previous work, it was often argued that the key advantage of a continuous calibration mechanism is its transparency to the user, who no longer needs to schedule calibration cycles that would interrupt normal ADC operation. In the proposed converter, the calibration coefficients relate to temperature-sensitive open-loop amplifier coefficients that may drift substantially in short time intervals and strictly dictate the implementation of a continuously tracking compensation approach.

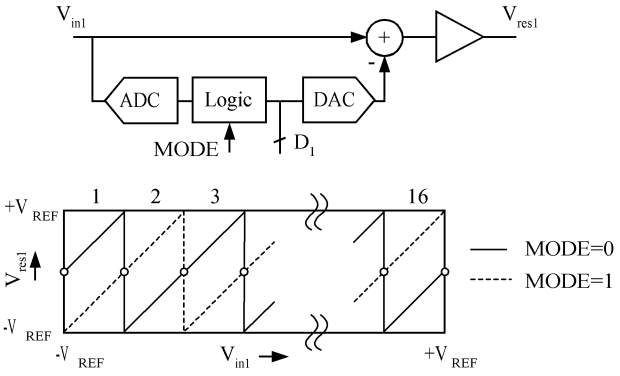

Fig. 9. Pipeline stage with two-residue transfer characteristics.

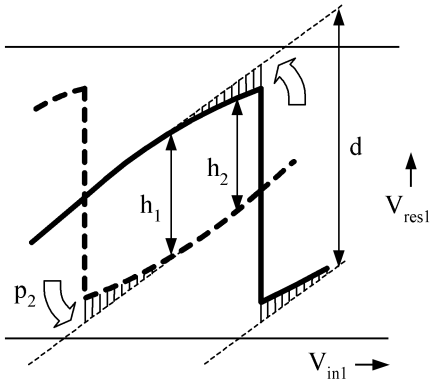

Fig. 10. Segment detail.

A particularly interesting property of the technique described herein is that it does not require the generation of an analog domain test signal, unlike other background calibration approaches. Instead, the calibration is based on evaluation of signal statistics, similar to the technique described in [24]. Conceptually, the estimation uses the fundamental property that perfectly linear systems at most scale, but never distort a signal's amplitude distribution. Deviations from this ideal case can be used to obtain information about the presence and magnitude of any nonlinearity. In some sense, the (arbitrary) input amplitude distribution of the converter assumes the role of the calibration test signal.

In this section, we describe the basic elements of the proposed calibration technique, followed by an overview of the complete digital postprocessing scheme and a brief discussion of its fundamental properties and limitations.

A. Two-Residue Characteristics

One key ingredient in the proposed background calibration technique is the addition of a second, redundant residue mode as shown in Fig. 9. Through the addition of a simple digital logic block and one bit of extra resolution in the stage's sub-ADC and sub-DAC, the open-loop converter stage can switch between two distinct overlapping residue transfer functions. In principle, the two residues of Fig. 9 can be used interchangeably and would yield identical conversion results in the case of ideal stage operation. The power penalty for the additional transfer function is low, since the redundant comparators needed in the sub-flash-ADC typically consume only a small fraction of the total stage power [4]. The redundant states needed in the sub-DAC can be generated at even lower cost by simply splitting up its unit elements. In designs with small unit capacitors, this may adversely affect the sub-DAC element matching. In the design presented here, the minimum capacitor size used still met the precision requirements.

B. Parameter Estimation From Residue Distances

Fig. 10 shows a single enlarged segment of the overlapping gain compressive stage transfer characteristic. Also shown are the residue differences h_1 and h_2 for two input voltages near the center and edge of the segment, respectively. The digital linearity correction in the converter back-end operates on both residues, controlled by parameter p_2. Perfect adjustment of p_2 maps both residues onto straight lines. In this case, the difference between the two residues is constant and independent of measurement location, consequently yielding $h_1 = h_2$. On the contrary, a measurement of, e.g., $h_1 > h_2$ indicates incomplete nonlinearity error cancellation. Based on this argument, it is conceptually possible to construct a recursive algorithm that converges to the optimum solution for p_2 by repeatedly measuring the two residue differences h_1 and h_2.

After the optimum value for p_2 is found, and assuming ideal sub-DAC operation, it can be seen from Fig. 10 that both h_1 and h_2 take on precisely 1/2 of the transition height δ of the linearized residue. Therefore, the distance estimates directly relate to the required correction parameter p_1 for linear gain error correction, as described in [21].

C. Statistics-Based Distance Estimation

If it were possible to process constant input voltages using both characteristics, the distances could be directly determined from the individual back-end conversion results. In this work, we have developed a statistics based estimation technique that avoids the need for constant inputs and, therefore, allows calibration in the background during normal converter operation. Fig. 11 illustrates the general concepts of the approach for the simplified case of a single residue segment and estimation of h_1 only. As a further simplification in this discussion, we assume that the input signal to the segment is a stationary and "white" discrete time random process, whose samples are described by a well behaved but otherwise arbitrary probability density function (PDF).

The distance estimation process is based on evaluating cumulative histograms of the digital back-end conversion results (D_{bcorr} in Fig. 8). Fig. 11(a) introduces the basic concept of a cumulative histogram. In this simple example, we consider only one of the two residue curves and one histogram bin at a particular code location q. The cumulative histogram count $n = \mathrm{CH}(q)$ is found by counting the number of samples seen in the back-end that are less than or equal to the reference code q. Hence, the expected value of n will be proportional to the total number of samples processed times the hatched area underneath the PDF, which represents the probability of an input sample being below the code threshold V_q.

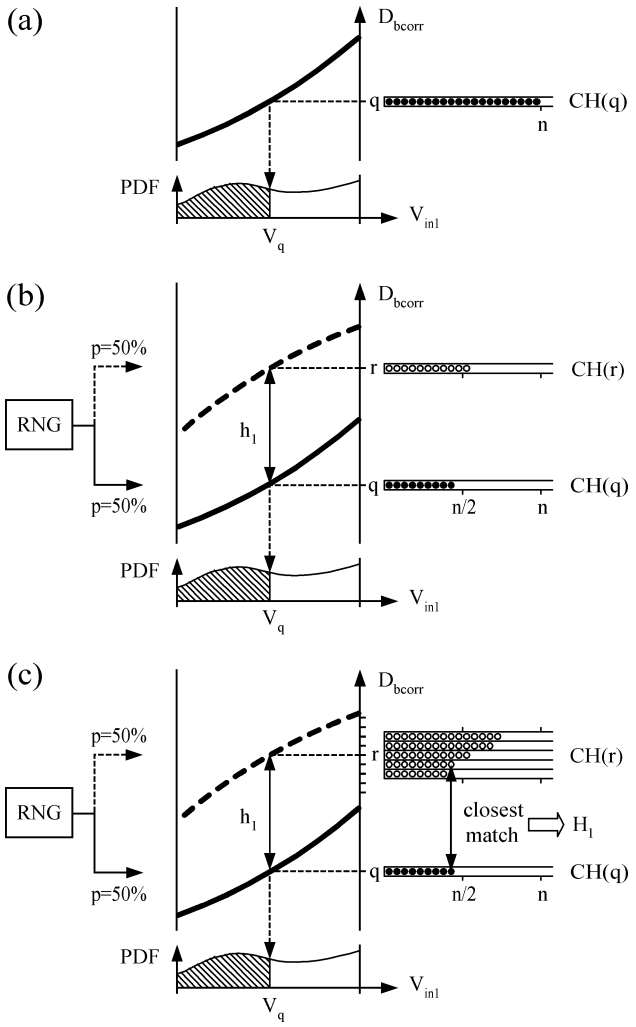

Fig. 11. Statistics-based distance estimation. (a) Cumulative count from one segment. (b) Random split. (c) Distance estimate from closest cumulative count.

Fig. 11(b) illustrates the next fundamental concept of the technique. For each input sample to the segment, a binary random number generator (RNG) chooses with equal probability and independent of the sample value between one of the two residue modes. Consider now a second cumulative code bin $\mathrm{CH}(r)$ that is associated with the top residue as shown in Fig. 11(b). For simplicity, assume that the decision level of code r precisely coincides with V_q (the decision level of code q). Due to the RNG modulation, the count $\mathrm{CH}(q)$ of Fig. 11(a) is now split into two histogram bins. Analysis shows that the expected value in each bin is $n/2$, but due to randomness in the modulation, particular outcomes will vary and most often not result in a perfect $n/2$ split. This fact is illustrated as slightly imbalanced counts in Fig. 11(b).

Consider now the setup of Fig. 11(c), in which several additional cumulative code bins have been added around code r. With the random modulation in progress, and after processing a large number of samples, the top bins are evaluated and compared to the reference count $\mathrm{CH}(q)$. From the closest match, the distance estimate H_1 is obtained [in the example of Fig. 11(c), $H_1 = r - 1 - q$]. It can be shown that H_1 is an asymptotically unbiased estimate of the true residue distance h_1, i.e., for increasingly large sample sizes, the estimate approaches the true value. The variance of H_1 is approximately inversely proportional to the total number of samples processed until counter evaluation.

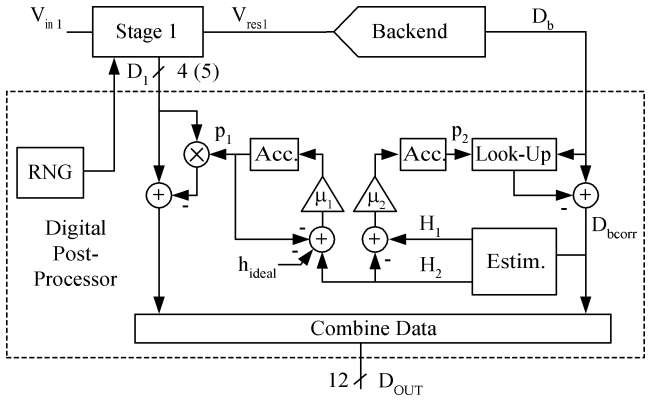

Fig. 12. Postprocessor block diagram.

D. Complete Algorithm

Combining the concepts discussed in the previous sections, Fig. 12 shows a block diagram of the complete digital postprocessing system. The procedure described above is duplicated to produce a second estimate H_2, located close to the residue transitions as depicted in Fig. 10. For the estimation process, the back-end data from all residue segments is combined. No distinction is made between the 16 segments; only bottom and top segment contributions are processed separately as required by the algorithm. The difference $H_1 - H_2$ is fed into an adaptive least mean square (LMS) loop [25], which assumes the task of finding and tracking the parameter p_2. The mean value of $H_1 - H_2$ is forced to zero through the presence of the accumulator in this feedback loop, resulting in optimum digital linearization. Similarly, parameter p_1 is obtained through recursive mean filtering on the estimator H_2.

E. Properties and Limitations

An important property of the calibration technique is that the required analog circuit modifications result in only minor overhead and introduce no additional accuracy requirements or precision elements in the pipeline stage. One key requirement for proper operation of the algorithm, however, is that the nonlinearity coefficients in each segment must be identical. Mathematically, the stage transfer function must be described by a family of power series of the form

$$V_{\mathrm{res1}} = b_1[V_{\mathrm{in}} - V_{\mathrm{DAC}}(D_1)] + b_3[V_{\mathrm{in}} - V_{\mathrm{DAC}}(D_1)]^3 + \ldots \quad (4)$$

In this expression, D_1 is the local conversion result, and $V_{\mathrm{DAC}}(D_1)$ represents the DAC-code-dependent position of each transfer segment along the V_{in1} axis of Fig. 9. Equation (4) simply restates an assumption made in the block diagram of Fig. 9: The sub-DAC must operate on the stage input in a purely additive manner (ideal summing block). Nonlinearity is only present in the stage gain element. Analysis shows that this requirement is met in the implementation of this design

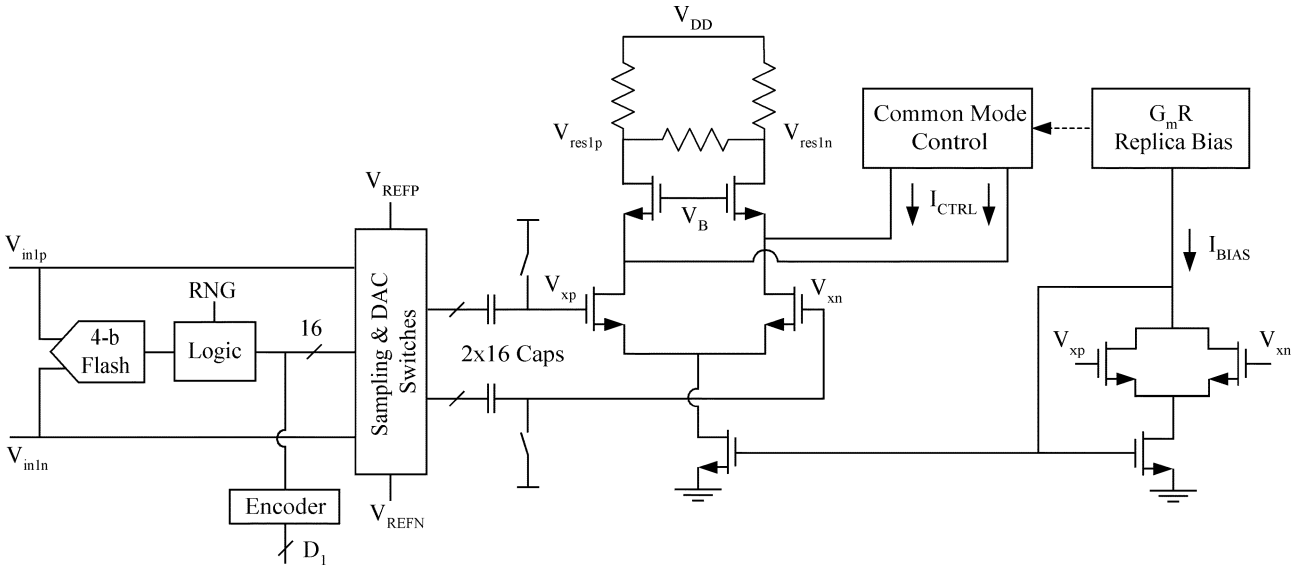

Fig. 13. Stage-1 implementation.

mainly for two reasons: 1) linear capacitors in the switched capacitor DAC result in an "ideal" linear summing node; and 2) one single amplifier is used to produce all residue segments, which therefore have identical power series descriptions that differ only in their $V_{\rm DAC}(D_1)$ terms [see (4)].

As explained above, the proposed algorithm operates continuously in the background, without interrupting normal converter operation. However, certain restrictions apply to the amplitude distribution of the converter input signal for successful calibration. Through qualitative arguments from the illustration in Fig. 11, it can be seen that the algorithm fails if the input signal is not sufficiently "busy" around the input voltages at which the distance estimates are taken. Inactivity results in a flat cumulative histogram with indistinguishable bins in the top counter array. It can be argued that this property only mildly affects the practicality of the approach. First, insufficient amplitude activity can be easily detected, making it possible to avoid miscalibration due to low-swing quasi-dc input signals. Furthermore, the estimation process in this work combines back-end data from 16 segments, so that activity spanning only about 1/16th of the converter's full-scale range is sufficient for calibration.

A more fundamental constraint exists in the tradeoff between the accuracy and tracking time constants in the LMS loops. Bounds on the tolerable variance in the correction parameters necessitate small loop coefficients μ_1 and μ_2, which in turn limits the achievable tracking speed. Assuming busy inputs, our system shows time constants of approximately 100–200 ms, which is sufficient to track, e.g., ambient temperature variations, slow changes in supply voltage, and device aging effects. Measures to reduce the sensitivity of the open-loop pipeline stage to potentially faster variations are briefly summarized in the next section.

VII. Circuit Details

A. Open-Loop Pipeline Stage

Fig. 13 shows a schematic of the circuit used in the first stage of this converter. As in [15], a 4-bit flash converter is used to generate the coarse local conversion result. This sub-ADC is shared between the two implemented residue modes. A logic block, controlled by the random number generator bit RNG, assigns even/odd flash transitions to cause the appropriate breakpoints in either transfer function mode (Fig. 9). The sampling and DAC capacitor network of this circuit is identical to the implementation in [15], with the exception that here the 16 poly–poly capacitors drive a resistively loaded open-loop amplifier. Based on the considerations outlined in Section IV, the quiescent point gate overdrive of the differential pair was chosen slightly larger than 250 mV.

As a conservative measure, cascode devices were included in the amplifier to yield improved power supply rejection. A pi-load configuration was chosen to decouple the choice of common mode output level from differential gain requirements. Replica tail biasing [26] was used to improve the stage's input common-mode rejection ratio.

Of particular importance in the presented open-loop stage are appropriate design techniques for thermal desensitization. Our design uses $G_m \cdot R$ replica biasing to reduce the overall sensitivity to ambient temperature changes. On the layout level, device interleaving and the use of n+ diffusion load resistors with low thermal resistance aim to mitigate the effect of signal-dependent self-heating.

B. Postprocessor Implementation

The digital postprocessor, depicted in Fig. 12, was designed and implemented on an external FPGA using Verilog HDL. The calibration is performed in real time and operates on the converter's raw data at the full clock speed of 75 MHz. In order to investigate the required on-chip hardware complexity, we carried out synthesis and place and route design iterations using standard CMOS gate and memory libraries. Our results show that the digital logic can be implemented using 8400 gates, 64 bytes of RAM and 64 kb of ROM. In 0.35-μm CMOS technology, this translates into approximately 1.4 mm^2 of chip area. Using 0.18-μm technology for comparison, the area decreases to 0.37 mm^2. The simulated power consumption of the postpro-

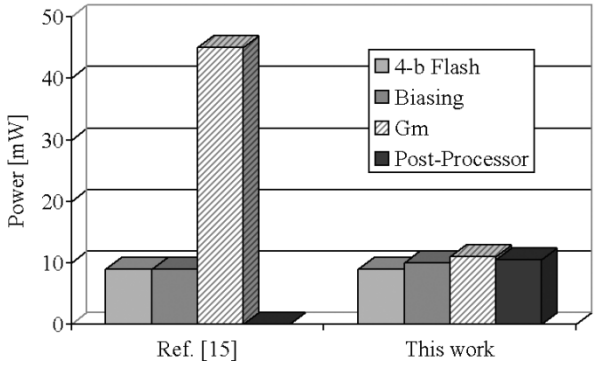

Fig. 14. Stage-1 power breakdown.

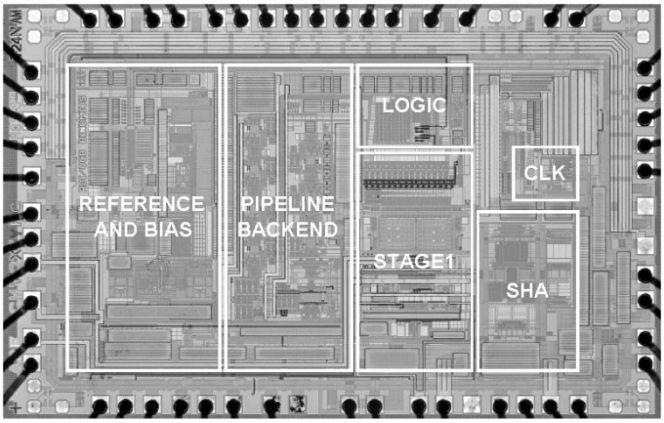

Fig. 15. Die micrograph.

cessing unit is 11.5 mW in 0.35-μm and 6.6 mW in a 0.18-μm process.

C. Power Reduction

For direct comparison, the open-loop amplifier in stage 1 of our converter was designed to meet the same settling and noise specifications as the precision closed-loop amplifier in [15]. Fig. 14 compares the stage power breakdown in the original design and this work. Pure transconductor power, accounting only for tail current spent to produce G_m, was reduced by 75% (34 mW). Including biasing networks, the overall amplifier power improved by 62% (33 mW). Also shown in the diagram is the simulated power for digital postprocessing. In the 0.35-μm technology of this design, digital calibration power is only about 1/3 of the power saved in the analog domain. For technologies using finer line widths, this benefit is expected to increase.

VIII. Experimental Results

The prototype ADC was fabricated in a 0.35-μm double-poly quadruple-metal (DPQM) CMOS process. A micrograph of the 7.9 mm^2 chip is shown in Fig. 15. Except for the redesign of stage 1 and the minor modifications in stage 2, the layout is largely unchanged from the original design [15].

Figs. 16 and 17 compare the DNL and INL of the experimental converter with and without digital postprocessing. Except for the removal of missing codes, differential nonlinearity does not improve significantly. The remaining peak DNL is set by capacitor mismatch errors in all stages, which are not corrected in this converter. The uncalibrated INL, shown for both residue modes separately, exhibits large peaks due to the visible cubic gain compression of the open-loop amplifier. Upon activation of the postprocessor, the measured INL improves from a peak value of 19 LSB to within 0.9 LSB. Shown in Fig. 18 is the measured output spectrum at an input frequency of 40 MHz. With calibration, spurious components are below -76 dB. Fig. 19 shows the measured spectral performance as a function of sampling frequency.

In order to evaluate the robustness of the converter, we applied external temperature transients to its package. Fig. 20 illustrates the raw sensitivity of the system without any temperature compensating mechanisms. In this measurement, the open-loop amplifier was biased with a constant tail current and the adaptive

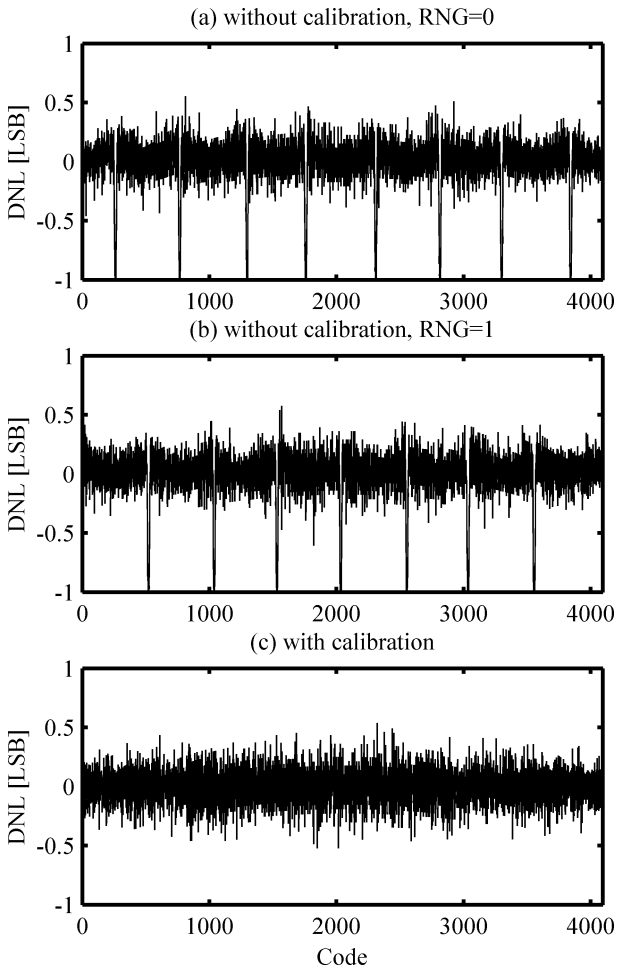

Fig. 16. Measured differential nonlinearity ($f_s = 75$ MHz, $f_{\rm in} = 1$ MHz).

LMS estimation loops were disabled ($\mu_1 = \mu_2 = 0$ in Fig. 12) prior to the transient. The temperature variation is measured using an on-chip temperature sensor and the effective number of converter bits (ENOB) is continuously computed from the converter's response to a 1-MHz sine wave. In contrast, Fig. 21 shows the system response to a similar temperature pulse, but now with active LMS loops. The converter's ENOB and calibration parameter p_1 are plotted for two cases: (a) with constant tail current, and (b) with $G_m \cdot R$ replica biasing. In both cases,

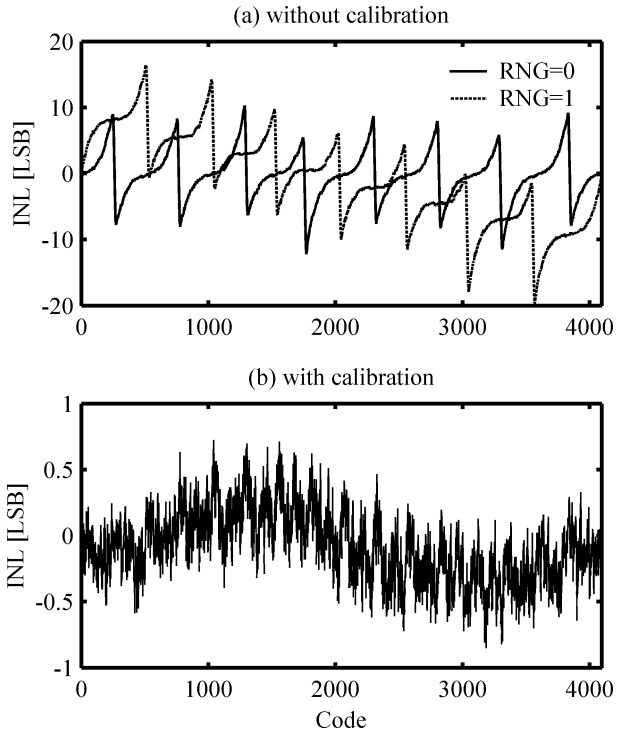

Fig. 17. Measured integral nonlinearity ($f_s = 75$ MHz, $f_{\rm in} = 1$ MHz).

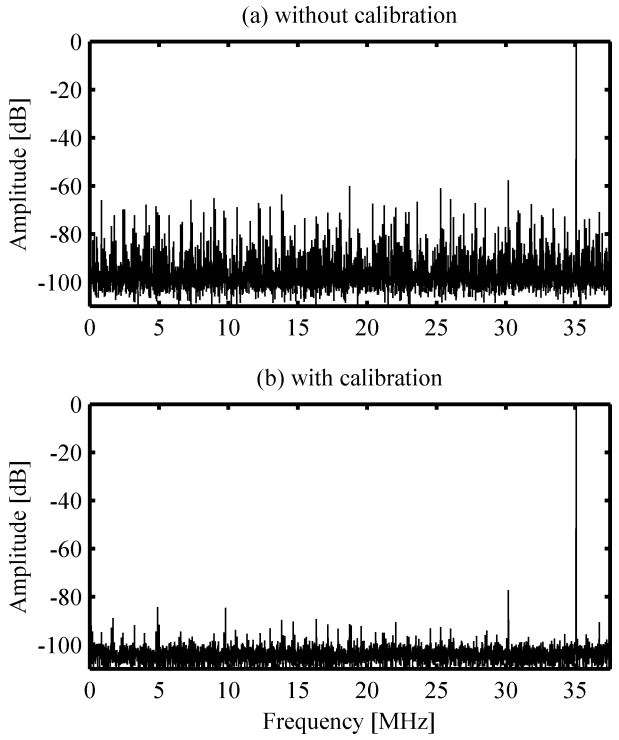

Fig. 18. Measured output spectrum ($f_s = 75$ MHz, $f_{\rm in} = 40$ MHz, 8 k FFT).

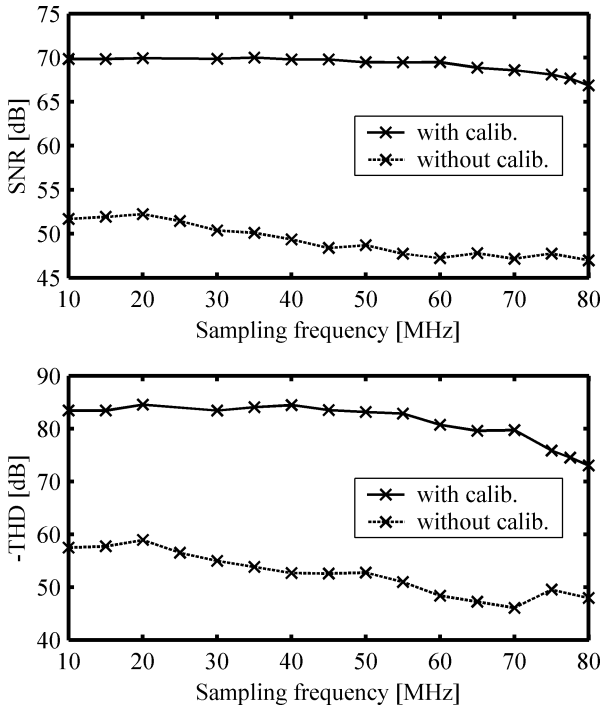

Fig. 19. Measured SNR and total harmonic distortion ($f_{\rm in} = 1$ MHz).

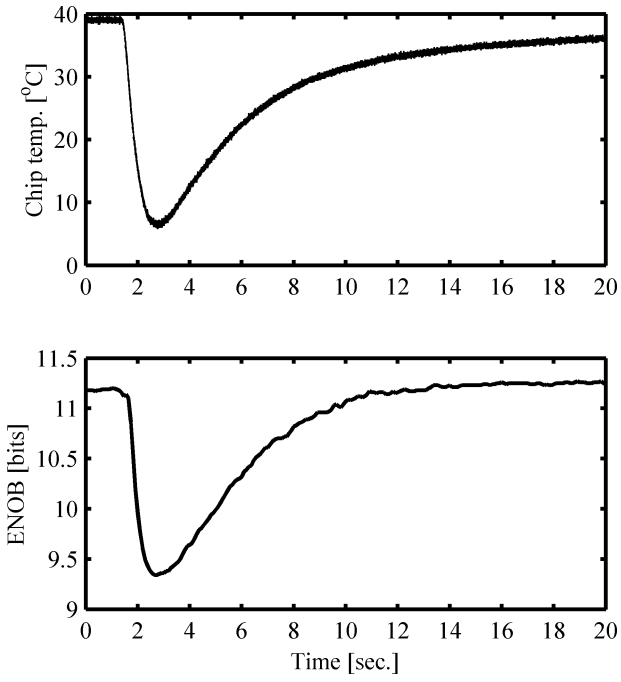

Fig. 20. Measured temperature transient. Constant tail bias and LMS loops disabled ($\mu_1 = \mu_2 = 0$).

the ENOB remains relatively constant and exhibits mostly statistical ripple. With replica biasing, however, the tracking requirements on p_1 are reduced, resulting in a more robust overall system that can tolerate larger time constants in the LMS loops. As mentioned in Section VI, the choice of larger time constants reduces statistical variations in the estimation loops and thereby helps improve the converter's overall accuracy ripple. In our prototype, with adequate loop time constants (100–200 ms), the statistical nature of the calibration accounts for an average signal-to-noise ratio (SNR) penalty of about 1–2 dB.

Table I summarizes the overall converter performance. Several effects account for the residual errors seen with calibration. More detailed measurement results reveal that the residual integral nonlinearity (INL) (Fig. 17) is due to capacitor mismatch in the first two stages, uncompensated second- and fifth-order

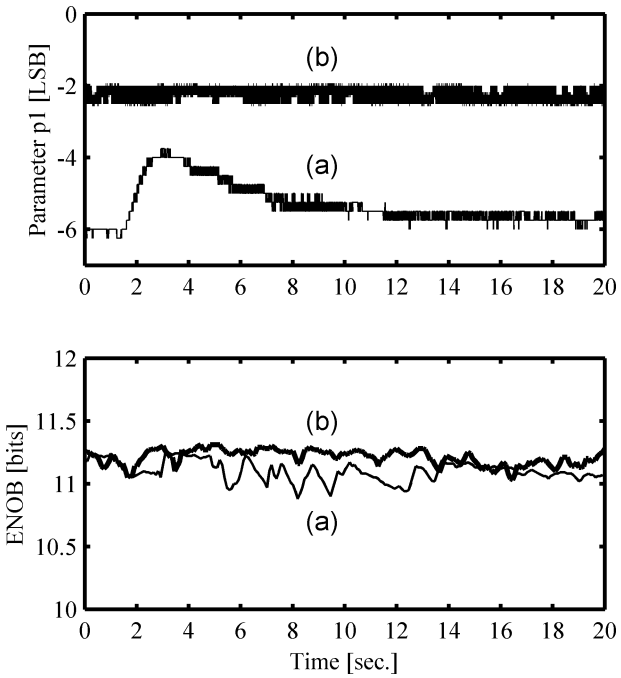

Fig. 21. Measured temperature transient with active LMS loops: (a) constant tail bias current, (b) with replica bias.

TABLE I
PERFORMANCE SUMMARY (25 °C)

Process, Area	0.35µm CMOS, 7.9mm ^{2}		
VDD	3V		
Full Scale Range	2V $_{pp}$ (differential)		
Resolution	12b		
Conv. Rate	75 MS/s		
	Without Post-Proc.	With Post-Proc.	
SNR	48dB	68.2dB 67dB	(f_{in}=1MHz) (f_{in}=40MHz)
THD	-50dB	-76dB -74dB	(f_{in}=1MHz) (f_{in}=40MHz)
SFDR	58dB	80dB 76dB	(f_{in}=1MHz) (f_{in}=40MHz)
DNL	-1, 0.6 LSB	-0.5, +0.5 LSB	
INL	-19, +16 LSB	-0.9, +0.6 LSB	
PSRR (LF)	46dB		
Power: ADC Core Output Drivers	 290mW 24mW		

open-loop amplifier distortion, and the onset of incomplete settling in the converter stages at $f_s = 75$ MHz.

IX. CONCLUSION

We have developed a digital background calibration technique that helps alleviate precision requirements in the critical interstage gain elements of pipelined A/D converters. Digital domain estimation and cancellation of nonlinearities, combined with simple power-efficient open-loop stages results in significant power reduction. Particularly in fine-line processes with low intrinsic device gain and limited supply headroom, the proposed scheme can be used to efficiently trade off analog precision for low-power digital signal processing.

ACKNOWLEDGMENT

The authors would like to thank Analog Devices for providing their design for reuse. The help of K. Nakamura, S. Korrapati, D. Kelly, L. Singer, W. Yang, and other members of the High-Speed Converter group is greatly appreciated.

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