# Digital Domain Measurement and Cancellation of Residue Amplifier Nonlinearity in Pipelined ADCs

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***Abstract*—Digital correction and calibration techniques have been extensively used to cancel linear circuit imperfections in pipelined analog-to-digital converters (ADCs). The self-calibration technique proposed in this paper provides a means of measuring and canceling nonlinear errors of interstage amplifiers in the digital domain. The calibration of nonlinearity coefficients is based on pseudorandom signal modulation and evaluation of digital code histograms. The scheme does not introduce additional precision hardware or test signals and operates in the background without interrupting normal converter operation. The simulation results of a 12-bit ADC show that the calibration is capable of improving the effective number of bits from 7 to 11.8 while achieving parameter adaptation time constants on the order of 100 ms at a sampling rate of 100 MS/s.**

***Index Terms*—Adaptive systems, analog–digital conversion, calibration, linearization techniques, parameter estimation.**

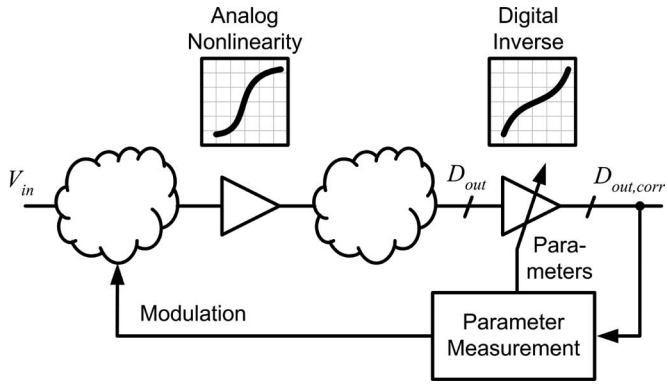


Fig. 1. Conceptual overview.

## I. Introduction

THE AVAILABILITY of low-power digital signal processing in modern complementary metal–oxide–semiconductor technology has fueled a trend toward the digital compensation of analog circuit imperfections in analog-to-digital converters (ADCs) (e.g., [1]–[8]). Particularly in pipelined converters, digital correction and calibration have been routinely used to compensate for offsets [9], unit element mismatch, and linear gain errors [10]. In this paper, we describe a calibration technique that can be used to estimate and digitally cancel errors from nonlinear amplification in interstage amplifiers. As demonstrated in [1], this approach enables significant power savings, since conventional precision feedback amplifiers can be replaced by simple weakly nonlinear open-loop gain stages.

Fig. 1 illustrates the basic concept of the proposed scheme. Applying an appropriate inverse function in the digital domain linearizes a weakly nonlinear amplifier in the analog signal path of the ADC. One of the main problems in this arrangement is to precisely measure the parameters that describe the optimum digital inverse function. In this paper, the parameters are obtained by applying a pseudorandom modulation to the signal path and continuously analyzing digital code histograms at the converter output. Conceptually, the described technique uses the fact that linear systems at most scale but do not distort statistical distributions. Deviations from this property are used to measure nonlinearity and optimize the digital correction. With this approach, the parameters of the digital inverse function can be measured without interrupting the normal operation of the device. The calibration tracks variations in the background and instantaneously responds to parameter drift in the nonlinear analog gain stage.

The design and implementation of an experimental ADC that uses the presented technique have been discussed in [1]. The primary purpose of this paper is to provide a more elaborate analysis and to introduce an extension that allows the cancellation of quadratic error terms, which were previously ignored.

Among the many papers on digital calibration in pipeline ADCs, this paper falls in the class of techniques that target the correction of amplifier nonlinearities [6]–[8]. Within this class, [8] is most closely related as it offers the same functionality, i.e., background calibration of second- and third-order amplifier distortion. The primary difference lies in the choice of implementation tradeoffs, such as, for instance, the required complexity of the sub-ADC/digital-to-analog converter (DAC) and digital processing versus sensitivity to signal statistics and the algorithm's convergence time. Other related works such as [2]–[4] primarily address first-order nonidealities, such as linear gain errors and mismatch only.

This paper is organized as follows: Section II details the error model and the proposed digital correction mechanism within the architecture of a pipelined ADC. Section III describes the

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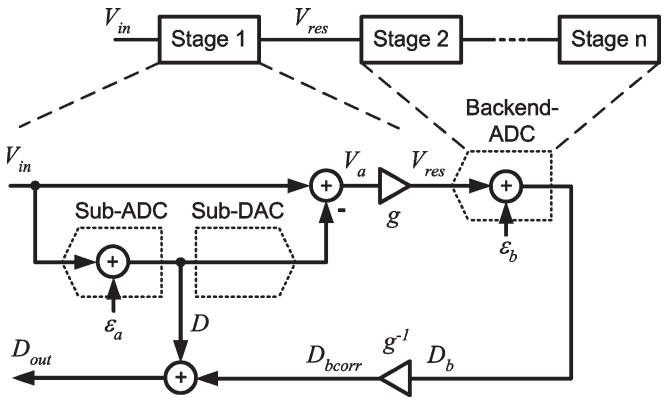


Fig. 2. Pipelined ADC block diagram.

background calibration technique that is used to measure the digital correction parameters. In Section IV, we further examine the approach through a numerical example and simulation. A brief conclusion is drawn in Section V.

## II. Amplifier Error Model and Correction Mechanism

### A. Error Analysis

Fig. 2 shows a pipelined ADC block diagram for further discussion. While in general a pipelined converter consists of $n$ stages and $n-1$ interstage amplifiers, we focus here on the calibration of the first stage only. For simplicity, all the remaining stages are lumped into a backend ADC block that is assumed to be ideal. Conceivably, the technique could be canonically extended to include the calibration of backend stages, which is similar to the "accuracy bootstrapping" approach used in [11] and [12].

Furthermore, the remaining components of the first stage (i.e., differencing node, sub-ADC, and sub-DAC) are modeled as ideal components. In practical high-resolution implementations, DAC errors are critical and must be minimized by appropriate layout techniques or by a separate calibration mechanism (e.g., [12]) used in addition to the technique described herein. For notational convenience, we consider both analog and digital signals as unitless quantities whose full-scale ranges are normalized to 1.

Similar to the arrangement in Fig. 1, the block diagram in Fig. 2 contains a digital inverse block $g^{-1}$ that is used to mitigate the impact of weakly nonlinear amplification in the interstage amplifier $g$. Here, it is important to note that the precision of the inverse compensation is fundamentally impaired by the additive quantization error $\varepsilon_b$, which is introduced between the two blocks. In the following discussion, we derive an expression that quantifies the impact of this error.

From the block diagram in Fig. 2, we obtain

$$D_{\text{out}} = V_{\text{in}} + \varepsilon_a + g^{-1}\left[g(-\varepsilon_a) + \varepsilon_b\right] \tag{1}$$

where $\varepsilon_a = -V_a$ and $\varepsilon_b$ represent the quantization errors in the coarse sub-ADC and the pipeline backend, respectively. Assuming that $g^{-1}$ is only weakly nonlinear over the range of the small additive term $\varepsilon_b$, we can use a first-order Taylor expansion to approximate (1) with

$$\begin{aligned} D_{\text{out}} &\cong V_{\text{in}} + \varepsilon_a + g^{-1}\left[g(-\varepsilon_a)\right] + \varepsilon_b \left.\frac{dg^{-1}(y)}{dy}\right|_{y=g(-\varepsilon_a)} \\ &= V_{\text{in}} + \varepsilon_b \left(\left.\frac{dg(x)}{dx}\right|_{x=-\varepsilon_a}\right)^{-1}. \end{aligned} \tag{2}$$

This result can be interpreted as follows: If the interstage amplifier is perfectly linear, then the derivatives in (2) are constants, and the overall quantization error of the ADC is given by the quantization error of the backend ADC ($\varepsilon_b$), which is reduced by the gain of the first stage. This case corresponds to the well-known ideal operation of a pipelined ADC.

For further investigation of the nonlinear case, and for the remainder of this paper, we assume that $g$ is sufficiently well described by a third-order polynomial of the form

$$g(V_a) = V_{\text{res}} = a_1 V_a + a_2 V_a^2 + a_3 V_a^3. \tag{3}$$

Note that in practical circuits, higher-order terms are also present. However, as argued in [1], these terms can be minimized by appropriate circuit design. To assess the impact of nonlinear terms in (3), we assume the worst-case deviation from linearity, which occurs at the maximum possible value for $V_a(V_{a,\max})$. Since $V_{\text{res}}$ in our normalized framework is bounded by $\pm 1$, it follows that $V_{a,\max} \cong 1/a_1$. With this assumption, and substituting (3) into (2), we obtain

$$\begin{aligned} D_{\text{out}}|_{V_a = V_{a,\max}} &= V_{\text{in}} + \frac{\varepsilon_b}{a_1}\left(\frac{1}{1 - 2\frac{a_2}{a_1^2} + 3\frac{a_3}{a_1^3}}\right) \\ &\cong V_{\text{in}} + \frac{\varepsilon_b}{a_1}\left(1 + 2\frac{a_2}{a_1^2} - 3\frac{a_3}{a_1^3}\right). \end{aligned} \tag{4}$$

The bracketed term in this expression accounts for the deviation from the ideal 1/2 LSB quantization error bound without the nonlinearities present. To estimate how much nonlinearity can be tolerated until this residual error becomes significant, we express the coefficient ratios of (4) in terms of the amplifier's harmonic distortion metrics [13] as

$$HD_2 = \frac{1}{2}\frac{a_2}{a_1} V_{a,\max}, \quad HD_3 = \frac{1}{2}\frac{a_3}{a_1} V_{a,\max}^2. \tag{5}$$

Using (5), and assuming that the signs of the distortion terms are such that the errors add, (4) can now be rewritten as

$$D_{\text{out}}|_{V_a = V_{a,\max}} \cong V_{\text{in}} + \frac{\varepsilon_b}{a_1}\left(1 + 4|HD_2| + 12|HD_3|\right). \tag{6}$$

In the implementation of [1], harmonic distortions on the order of 1% were achieved using a simple open-loop amplifier. Assuming $HD_2 = HD_3 = 1\%$ as an example, it is seen from (6) that the maximum deviation from ideality is approximately 16%. This means that the quantization error (ideally bounded

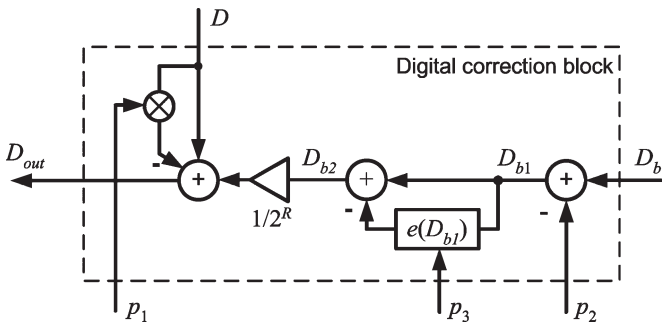


Fig. 3. Implementation of the digital inverse function $(g^{-1})$ combined with summing element.

by $\pm 1/2$ LSB) increases by no more that 0.08 LSB near the full-scale ends of the residue.

The impact of this residual error, along with the quantization error in the digital realization of the inverse function $g^{-1}$, can be reduced by increasing the number of bits in the converter's backend ADC beyond the target spec requirements. The addition of extra pipeline stages for calibration and correction purposes is common to most digital enhancement techniques and is known to add only minor overhead in terms of complexity and power dissipation. In [1], and in the simulation example in Section IV, two redundant backend bits are added to improve the precision in the digital inverse operation and the required correction parameter measurement.

### B. Inverse Decomposition

Although an explicit form for the inverse of (3) exists, a more hardware-efficient decomposition is desirable. Fig. 3 shows a suitable realization in which the digital inverse function $(g^{-1})$ was lumped together with the summing element for the sub-ADC output $D$. This block is controlled by three parameters $p_1, \ldots, p_3$ that are used to cancel errors due to linear, quadratic, and cubic errors in $g(V_a)$, respectively. The correction based on this approach is approximate in the sense that it introduces a global gain and offset error to the ADC's transfer function [see (17) below]. These errors are tolerable in many ADC applications.

In the following analysis, we will derive the optimum values for $p_1, \ldots, p_3$ and the required form of the correction function $e(D_{b1}, p_3)$. Neglecting the quantization error of the backend ADC $(\varepsilon_b)$, we can write

$$D_b = g(V_a) = a_1 V_a + a_2 V_a^2 + a_3 V_a^3. \tag{7}$$

With the additive correction parameter $p_2$ applied as shown in Fig. 3, we have

$$D_{b_1} = a_1 V_a + a_2 V_a^2 + a_3 V_a^3 - p_2. \tag{8}$$

With proper adjustment of $p_2$, i.e., $p_2 = p_{2\text{opt}}$, (8) can be rewritten as

$$D_{b1} \stackrel{!}{=} b_1(V_a - V_{\text{off}}) + b_3(V_a - V_{\text{off}})^3. \tag{9}$$

Comparing the coefficients of (8) and (9) yields

$$\begin{aligned} p_{2\text{opt}} &= \frac{2a_2^3}{27a_3^2} - \frac{a_1 a_2}{3a_3} \\ b_1 &= a_1 - \frac{a_2^2}{3a_3} \\ b_3 &= a_3 \\ V_{\text{off}} &= -\frac{a_2}{3a_3}. \end{aligned} \tag{10}$$

This result holds for $a_3 \neq 0$. This condition is not restrictive since cubic nonlinearity is typically the dominant distortion mechanism in a practical fully differential circuit.

Next, the error lookup table $e(D_{b1}, p_3)$ is used with the goal of removing the cubic term in (9), i.e.,

$$D_{b2} = D_{b1} - e(D_{b1}, p_3) \stackrel{!}{=} b_1(V_a - V_{\text{off}}) \tag{11}$$

where the last equality follows for optimum adjustment of the cubic correction parameter, i.e., $p_3 = p_{3\text{opt}}$. To solve (11) for the required form of $e(D_{b1})$, we first solve (9) for $(V_a - V_{\text{off}})$ using trigonometric substitutions [14]. For the common case of gain compression $(b_1/b_3 < 0)$, we find

$$(V_a - V_{\text{off}}) = 2\sqrt{\frac{b_1^3}{-3b_3}} \cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_{b1}}{2 \cdot \sqrt{\frac{b_1^3}{-27b_3}}}\right)\right]. \tag{12}$$

Substituting this result into (11) yields

$$e(D_{b1}, p_3) = D_{b1} - 2\sqrt{\frac{1}{-3p_3}} \cdot \cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{D_{b1}}{2 \cdot \sqrt{\frac{1}{-27p_3}}}\right)\right]. \tag{13}$$

For optimum adjustment, i.e., perfect cancellation of the cubic term, we require

$$p_3 = p_{3\text{opt}} = \frac{b_3}{b_1^3}. \tag{14}$$

Despite its mathematically complex form, (13) can be efficiently implemented in hardware. The correction function $e(D_{b1}, p_3)$ only depends on the digital backend data and $p_3$ as a single parameter. As demonstrated in [1], a precomputed 2-D lookup table implementation requires only a fairly small amount of memory (~64 kb).

The remaining operation needed is scaling by the inverse linear gain term $1/b_1$. This is most efficiently accomplished by scaling the low-bit-width signal $D$ rather than the higher-resolution digital backend code. In the approach illustrated in Fig. 3, $D_{b2}$ is scaled by a simple bit shift operation. Right shifting the digital word by $R$ bits corresponds to a multiplication with $1/2^R$, where $2^R$ should be chosen close to the nominal value of $b_1$ (the nominal amplifier gain in pipeline ADCs is usually chosen to be a power of 2).

Mathematically, assuming $p_2 = p_{2\mathrm{opt}}$ and $p_3 = p_{3\mathrm{opt}}$, we have

$$\begin{aligned} D_{\mathrm{out}} &= \frac{1}{2^R} D_{b2} + (1 - p_1) D \\ &= \frac{b_1}{2^R}(V_a - V_{\mathrm{off}}) + (1 - p_1) D \\ &= \frac{b_1}{2^R}(-\varepsilon_a - V_{\mathrm{off}}) + (1 - p_1)(V_{\mathrm{in}} + \varepsilon_a). \end{aligned} \tag{15}$$

By choosing

$$p_1 = p_{1\mathrm{opt}} = 1 - \frac{b_1}{2^R} \tag{16}$$

we arrive at the final result

$$D_{\mathrm{out}} = \frac{b_1}{2^R}(V_{\mathrm{in}} - V_{\mathrm{off}}). \tag{17}$$

In practice, the amplifier coefficients $a_1, \ldots, a_3$ and hence $b_1, \ldots, b_3$ are not precisely known and may also substantially drift over time and varying operating conditions. The digital background calibration algorithm described in the next section was designed to precisely measure and continuously update $p_1, \ldots, p_3$ without interrupting normal ADC operation.

## III. Background Calibration Technique

From (2), we see that the local quantization error $(\varepsilon_a)$ in a perfect pipeline ADC does not affect the overall conversion result. In the proposed scheme, this observation also holds to within arbitrary precision when the digital inverse is perfectly adjusted, and the resolution of the backend ADC is chosen sufficiently high to mitigate residual error components, as discussed in Section II-A.

The above property invites approaches in which the response to a sub-ADC error modulation is used to determine and minimize errors due to parameter maladjustment. After the introduction of this principle in [1], a similar approach used for the background calibration of linear gain errors was described in [15]. In the remainder of this section, we describe the technique in [1] and its extension for quadratic error compensation, which allows continuous background calibration of all the three parameters $p_1, \ldots, p_3$ introduced in Section II-B.

### A. Modulation and Required Sub-ADC and Sub-DAC Redundancy

Fig. 4 shows a modified ADC model with an additive digital modulation signal applied to the output of the sub-ADC. Since $V_a = -(\varepsilon_a + MOD)$, it is clear that such a modulation calls for an additional dynamic range in the system. Adding this dynamic range in the backend ADC may result in a significant power penalty for a large modulation amplitude.

An efficient way to overcome this problem is to reduce the maximum quantization error $|\varepsilon_{a|\max}$ such that the overall peak magnitude of $V_a$ does not increase compared to an unmodulated system. For instance, this can be accomplished by increasing the sub-ADC resolution by 1 bit, which amounts to a negligibly small power and area overhead in a typical pipeline design [16]. This approach is illustrated in Fig. 5 for the example of a 2-bit sub-ADC. Adding an extra bit reduces the quantization error by a factor of 2. The extra headroom that is now available for modulation corresponds to $\pm 1/2$ LSB $(\pm\Delta/2)$ of the 3-bit quantizer. Using this entire range for modulation translates into a simple hardware implementation and is also imperative for maximizing the signal-to-noise ratio of the estimation process.

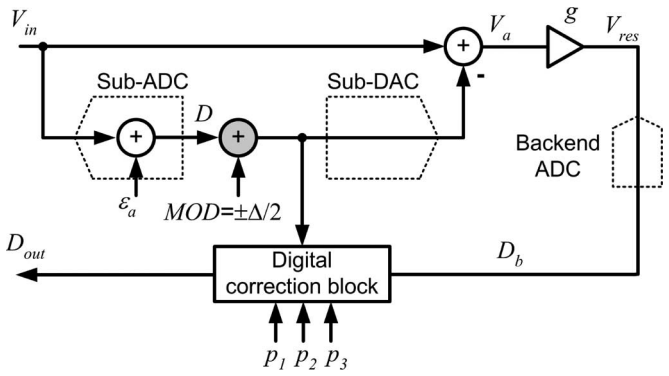


Fig. 4. ADC model with digital code modulation $(MOD)$.

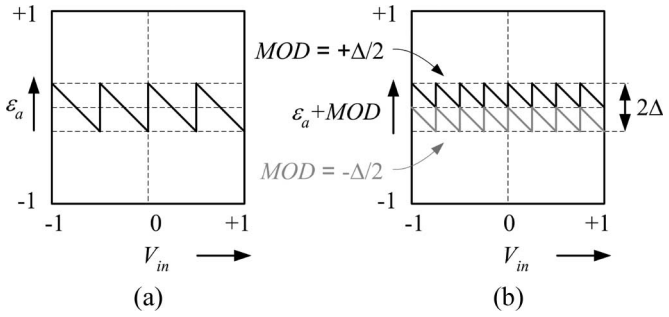


Fig. 5. Introducing sub-ADC redundancy. (a) Quantization error of a 2-bit sub-ADC. (b) Error of a $(2+1)$-bit sub-ADC with superimposed modulation.

The introduction of additional sub-ADC resolution also necessitates an appropriate increase in the resolution of the sub-DAC. Assuming that the sub-ADC has a resolution of $B$ bits, and hence $2^B$ distinct output codes, the sub-DAC needs to provide $2^B + 1$ output levels due to the random addition of one LSB. As explained in [1], this modification represents only minor overhead and does not sacrifice performance. The required DAC unit element precision remains essentially the same since tolerable errors are dictated by the backend ADC resolution rather than the local DAC resolution.

It should be noted that the introduced redundancy for modulation purposes does not help accommodate threshold errors in the sub-ADC. As in any practical design, some additional redundancy must be provided to accommodate these errors through either one of the three approaches described in [9], [10], and [17].

### B. Parameter Estimation Based on Residue Differences

In this section, we establish a procedure that allows parameter measurement based on evaluating transfer function

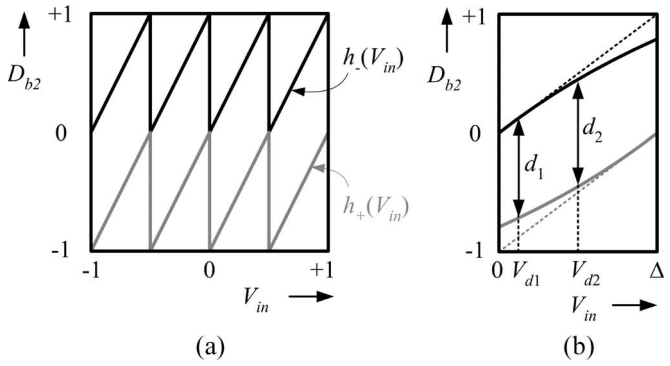


Fig. 6. (a) Residue plot for both modulation states. (b) Single transfer function segment without correction and $b_3 < 0$, $b_0 = 0$.

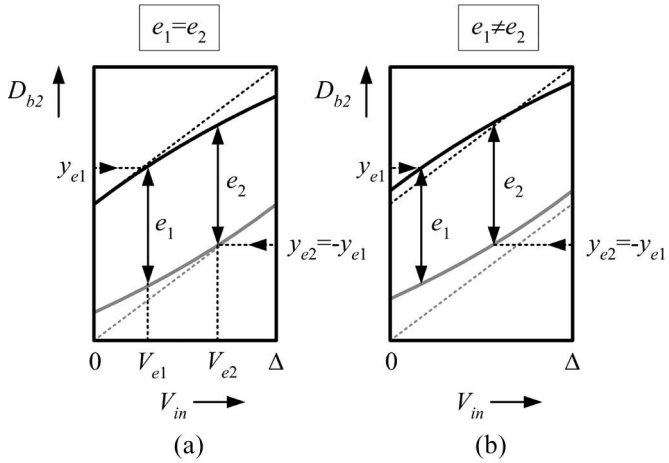


Fig. 7. Difference measurement with symmetrical ordinates ($b_3 < 0$, $b_0 = 0$). (a) Symmetry with ($b_0 = 0$). (b) Asymmetry caused by $b_0 \neq 0$.

differences in the two modulation states. For this discussion, we examine the converter with respect to the commonly used stage residue plots, i.e., the transfer function from $V_{\rm in}$ to the output $V_{\rm res}$ and its corrected digital representations ($D_{b1}$ and $D_{b2}$ in Fig. 3). Based on the reasoning in Section II, we ignore the backend quantization error $\varepsilon_b$ to simplify the analysis.[1]

Fig. 6(a) illustrates the digitized residue plot $D_{b2}$ as a function of $V_{\rm in}$ for the two possible states of $MOD$. In this example, we assume a 2-bit sub-ADC and perfectly adjusted parameters $p_1, \ldots, p_3$. The two resulting graphs are annotated as $h_+$ and $h_-$ to indicate the respective polarity of $MOD$. Without loss of generality, the following algebraic analysis focuses on one single segment of this periodically repeating characteristic. Fig. 6(b) shows the chosen transfer function segment in the presence of nonlinearities. First, consider the case with only cubic amplifier distortion and no correction applied ($b_3 < 0, b_0 = 0, p_1 = p_2 = p_3 = 0$). In this case, the analysis yields

$$\begin{aligned} h_-(V_{\rm in}) &= b_1 V_{\rm in} + b_3 V_{\rm in}^3 \\ h_+(V_{\rm in}) &= b_1 (V_{\rm in} - \Delta) + b_3 (V_{\rm in} - \Delta)^3 \end{aligned} \tag{18}$$

where $\Delta$ corresponds to the peak-to-peak modulation amplitude or equivalently the sub-DAC LSB size. Shown graphically in Fig. 6(b) are the residue differences $d_1$ and $d_2$ for two fixed input voltages ($V_{d1}$ and $V_{d2}$) near the center and edge of the segment, respectively. Mathematically, the difference between these two quantities follows from (18) as

$$\Delta d_{12} = d_1 - d_2 = 3 b_3 \Delta \left[ (V_{d1} - V_{d2}) \left( \Delta - (V_{d1} + V_{d2}) \right) \right]. \tag{19}$$

As we can see from this expression and also graphically from Fig. 6(b), the difference in the two measurements vanishes for $b_3 = 0$, i.e., a perfectly linear amplifier. Alternatively, this could also be achieved for $b_3 \neq 0$ but with active perfectly adjusted digital correction that maps both residues onto straight lines. When the correction function $e(D_{b1})$ is applied, i.e., with nonzero $p_3$, we find

$$\begin{aligned} \Delta d &= d_1 - d_2 \\ &\cong 3 b_1^3 \Delta \cdot (p_3 - p_{3\rm opt}) \cdot \left[ (V_{d1} - V_{d2}) \left( \Delta - (V_{d1} + V_{d2}) \right) \right]. \end{aligned} \tag{20}$$

This result indicates that the deviation of the parameter $p_3$ from its ideal value is directly proportional to $\Delta d$. In principle, this gradient information could be used in a search algorithm that minimizes (20) and thus optimizes $p_3$ over a sequence of measurements with the constant test voltages $V_{d1}$ and $V_{d2}$ applied in both modulation states. Section III-C introduces a statistics-based difference measurement approach that avoids the need for constant inputs and therefore allows calibration in the background during normal converter operation.

To further the idea of parameter calibration based on residue differences, consider now choosing the measurement locations of a second set of differences ($e_1$ and $e_2$ in Fig. 7). Here, the ordinates are chosen symmetrically such that $y_{e2} = -y_{e1}$ so that $V_{e1} = h_-^{-1}(ye1)$ and $V_{e2} = h_+^{-1}(-ye1)$. Using appropriate algebra, we now find

$$\Delta e = e_1 - e_2 = h_- \left( h_-^{-1}(-y_{e1}) + \Delta \right) + h_+ \left( h_+^{-1}(y_{e1}) - \Delta \right). \tag{21}$$

This expression equals zero if and only if $h_-$ and consequently its inverse $h_-^{-1}$ are also odd functions. Since $h_-$ is odd if and only if the quadratic error term is perfectly cancelled, a vanishing $\Delta e$ indicates perfect calibration ($p_2 = p_{2\rm opt}$). This is also seen graphically in Fig. 7. With only the cubic distortion present [Fig. 7(a)], the point symmetry around $(\Delta/2, 0)$ results in $e_1 = e_2$ independent of the amount of cubic distortion.[2] With a quadratic component ($a_2 \neq 0 \Rightarrow b_0 \neq 0$), the point symmetry is lost, which results in a difference between the two

[1] As pointed out in [8], this approximation must be considered with care if one attempts to estimate very small levels of distortion, e.g., in a converter with a target linearity of $\geq 14$ bits.

[2] Mathematically, this is confirmed by the trivial root in (19), i.e., $\Delta d = 0$ for $(V_{d1} + V_{d2})/2 = \Delta/2$, independent of $b_3$.

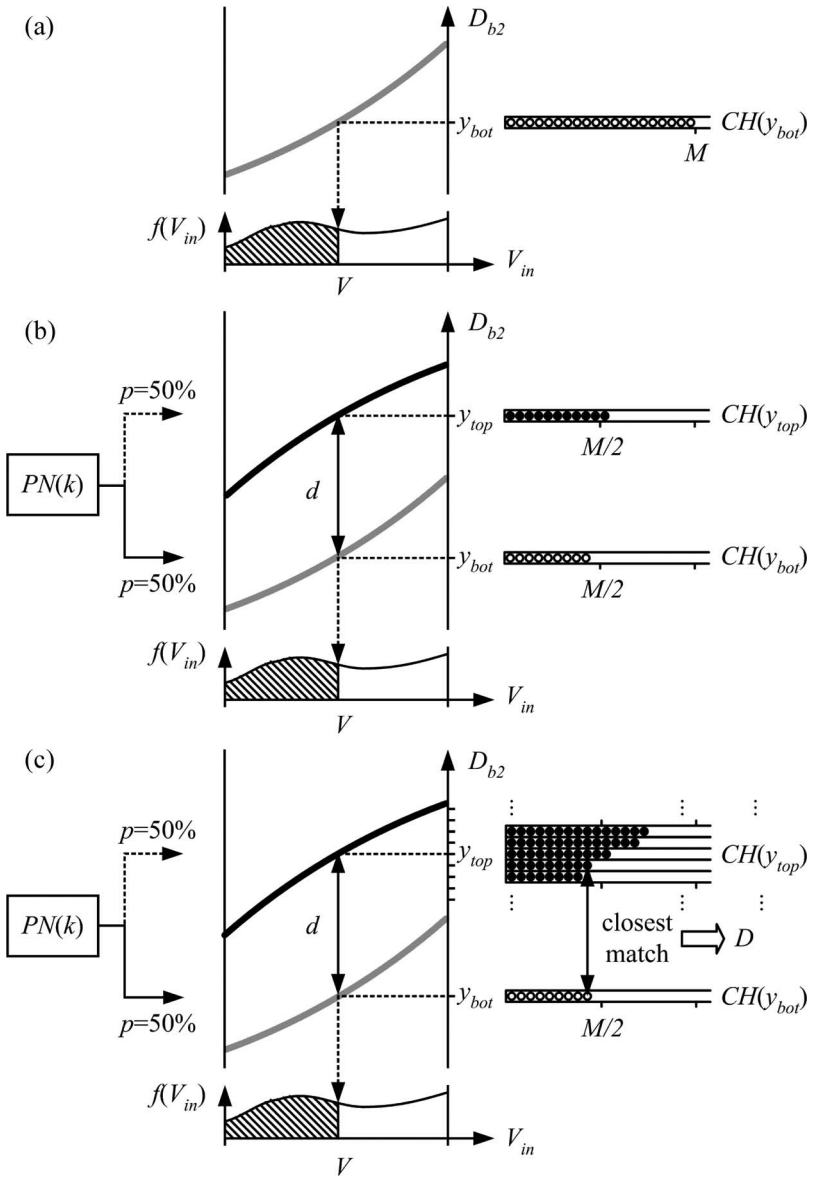


Fig. 8. Statistics-based distance estimation. (a) Cumulative count with $MOD$ fixed. (b) Random split with active random modulation. (c) Difference estimate from closest cumulative count.

measurements. Using suitable approximations, and assuming weak nonlinearity, we find

$$\Delta e = e_1 - e_2 \cong -3\frac{b_3}{b_1}\Delta\left(\Delta - \frac{y_{e1}}{4}\right)(p_2 - p_{2\mathrm{opt}}). \quad (22)$$

Hence, the two distance measurements based on symmetric ordinates provide a suitable gradient for calibrating the parameter $p_2$. Once $p_2$ and $p_3$ are perfectly adjusted, all the residue curves are mapped onto perfectly straight lines with slope $b_1$, and we have

$$d_1 = d_2 = e_1 = e_2 = b_1\Delta \quad (23)$$

independent of the measurement location. Combining (16) and (23), we obtain

$$p_{1\mathrm{opt}} = 1 - \frac{b_1}{2^R} = 1 - d_1 \cdot \frac{1}{\Delta \cdot 2^R}. \quad (24)$$

Therefore, the optimum value for the calibration parameter $p_1$ can be directly found from one or several difference measurements at any location. In the implementation example in Section IV, the estimates for cubic calibration are reused to obtain $p_1$. Alternatively, one could measure this parameter with separate hardware based on the correlation principle in [15].

### C. Statistics-Based Difference Measurement

Fig. 8 illustrates the proposed statistics-based residue difference measurement, which does not require constant or known inputs. In the following discussion, we focus on the estimation of a single residue difference in one transfer function segment. As a further simplification, we assume that $V_{\mathrm{in}}(k)$ is a stationary "white" discrete-time random process whose samples are described by a well behaved but otherwise arbitrary probability

density function (pdf). The modulation signal $MOD$ is chosen such that

$$MOD(k) = PN(k) \cdot \frac{\Delta}{2} \tag{25}$$

where $PN(k) \in \{-1, 1\}$ is a sequence of fair Bernoulli trials that are assumed to be uncorrelated with $V_{\rm in}(k)$. The parameter measurement is based on evaluating cumulative histograms of the digital backend data ($D_{b1}$ or $D_{b2}$).

Fig. 8(a) reviews the concept of a cumulative histogram. In this simple example, we consider only the bottom residue curves (fixed $PN(k) = 1$) and one histogram bin at a particular code location $y_{\rm bot}$. The cumulative histogram count $M = CH(y_{\rm bot})$ is found by counting the number of samples seen by the backend converter that are less than or equal to $y_{\rm bot}$. Hence, the expected value of $CH(y_{\rm bot})$ will be proportional to the total number of samples processed times the hatched area underneath the pdf, which represents the probability of an input sample being below the code threshold $V$.

With $PN(k)$ randomly switching, one of the two residue curves is chosen for each sample with equal probability and independent of $V_{\rm in}(k)$. Consider now a second cumulative code bin $CH(y_{\rm top})$ that is associated with the top residue, as shown in Fig. 8(b). For the time being, assume that the decision level of code $y_{\rm top}$ precisely coincides with $V$. Due to the modulation, the count $CH(y_{\rm bot})$ in Fig. 8(a) is now split into two histogram bins. From basic probability, it follows that the expected value in each bin is $M/2$, but due to randomness in the modulation, particular outcomes vary and will typically not result in a perfect $M/2$ split. This fact is illustrated as slightly imbalanced counts in Fig. 8(b).

Consider now the setup in Fig. 8(c), where several additional cumulative code bins have been added around code $y_{\rm top}$. With the random modulation in progress, and after processing a large number of samples $N$, the top bins are evaluated and compared to the reference count $CH(y_{\rm bot})$. From the closest match, it is straightforward to obtain the distance estimate $D$. It can be shown that the random variable $D$ is an asymptotically unbiased estimate of the true residue distance $d$, i.e., for increasingly large $N$, the expected value of the estimate approaches the true value. The analysis given in the Appendix shows that

$$\mathrm{var}(D) \cong \frac{4}{N} \cdot \frac{F(V)}{f(V)^2} \tag{26}$$

where $F(V)$ and $f(V)$ denote the pdf and cumulative distribution function of the input samples $V_{\rm in}(k)$ evaluated at $V$. For the special case of a uniform input distribution, and letting $b_1 = 1/\Delta$ [full-swing residues as in Fig. 6(a)], (26) becomes

$$\mathrm{var}(D) \cong \frac{4}{N} \cdot \frac{V}{\Delta}. \tag{27}$$

Qualitatively, it is clear that the above approximation does not hold for $V = 0$, i.e., placement of an estimator at the segment edge. Moreover, this choice is impractical, since there is uncertainty in the segment boundaries due to sub-ADC noise and offset. From a practical perspective, there exists a reasonable minimum $V = V_{\rm min}$ that is commensurate with the expected sub-ADC precision.

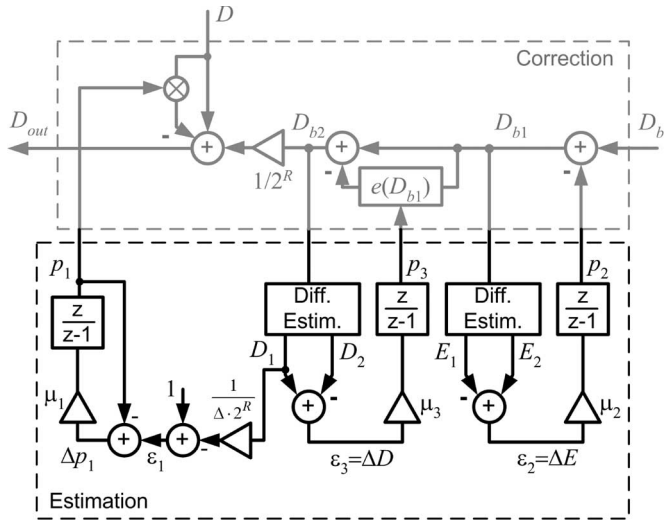


Fig. 9. Parameter estimation using LMS loops.

Furthermore, it must be noted that the above-described algorithm fails if the input signal is not sufficiently "busy" around the input voltages at which the distance estimates are taken. In this context, a criterion for sufficient business could be defined from the minimum signal spread required to distinguish between cumulative bins around the estimator location. Inactivity results in a flat cumulative histogram, which leaves the bins indistinguishable. We argue that this property only mildly affects the practicality of the proposed technique approach. First, insufficient activity can be easily detected, which makes it possible to avoid parameter maladjustment due to low-swing quasi-dc input signals. Furthermore, since the estimation process combines backend data from several segments, an activity spanning only a fraction of the converter's full-scale range is sufficient for calibration.

Combining samples from different segments in one single set of histograms also alters the shape of the effective net distribution seen by the algorithm. Even if the input distribution is Gaussian, as in many communications applications, combining samples from several segments tends to produce net distributions that are fairly uniform. Hence, especially for multibit stages with a large number of segments, (27) is a good signal independent approximation for the estimator variance.

### D. Complete Estimation Block

Combining the concepts outlined above, we now construct a block diagram realization for the parameter calibration hardware. Fig. 9 shows a possible implementation using adaptive least mean square (LMS) loops [18]. Here, the scheme described in the previous section is replicated to generate statistics-based estimates for the deterministic quantities $d_1$, $d_2$, $e_1$, and $e_2$. In Fig. 9, these variables are denoted by their respective uppercase symbol. In all three estimation loops, the presence of a discrete-time integrator forces the mean value of the loop inputs to zero, which corresponds to optimum

calibration. For the case of the linear calibration loop, the mean of the difference

$$\Delta p_1 = \left(1 - D_1 \frac{1}{\Delta \cdot 2^R}\right) - p_1 \tag{28}$$

is forced to zero. We therefore have

$$E(p_1) = E\left(1 - D_1 \frac{1}{\Delta \cdot 2^R}\right) = 1 - d_1 \frac{1}{\Delta \cdot 2^R} = p_{1\mathrm{opt}}. \tag{29}$$

Similarly, in both quadratic and cubic calibration loops, the mean of the difference in a pair of estimators is forced to zero, which produces optimum estimates for $p_2$ and $p_3$ [see (20) and (22)]. Due to the statistical variations in the measurements, there exists a certain variance in the loop outputs $p_1, \ldots, p_3$. Further analysis shows that [19]

$$\mathrm{var}(p_i) \cong \frac{1}{2}\frac{\mu_i}{\delta_i}\mathrm{var}(\varepsilon_i) \tag{30}$$

where $\mu_i$ and $\varepsilon_i$ are as indicated in Fig. 9, and

$$\delta_i \cong \frac{d\varepsilon_i}{dp_i}. \tag{31}$$

By inspection of Fig. 9, we see that $\delta_1 = 1$. For the quadratic and cubic loops, the $\delta$ terms can be found by differentiating (20) and (22).

From (30), it follows that the loop gain parameters $\mu_i$ should be chosen as small as possible to minimize inaccuracy in the correction parameters. For the given precision requirements in each of the three LMS loops, this translates into an upper bound for the loop gain parameters of the form

$$\mu_i \leq \frac{\delta_i}{\alpha_i} L_i^2 \left(\frac{2}{2^{B_b}}\right)^2 N \tag{32}$$

where $N$ is the number of samples processed until histogram evaluation, $B_b$ is the effective resolution of the backend converter, and $L_i$ quantifies the worst-case error budget allocated to each loop in LSBrms. The loop-specific parameters $\alpha_i$ can be found by evaluating (27) for the respective estimator locations (i.e., $V = V_{\min}$ for $D_1$, $D_2$, and $E_1$; and $V = \Delta/2$ for $E_2$) and the subsequent calculation of the resulting $\varepsilon_i$ variance terms into (30). This yields

$$\alpha_1 = 2\frac{V_{\min}}{\Delta}, \quad \alpha_2 = 4\frac{V_{\min}}{\Delta}, \quad \alpha_3 = 1 + \frac{2 \cdot V_{\min}}{\Delta}. \tag{33}$$

Unfortunately, reducing the parameters $\mu_i$ increases the LMS loop time constants and therefore impairs the tracking capability of the system. For equality in (32), this translates into minimum attainable time constants given by

$$\tau_{i\min} \cong \frac{N}{f_s}\frac{1}{\mu_{i\max}\delta_i} = \frac{1}{f_s}\frac{\alpha_i}{\delta_i^2}\frac{1}{L_i^2}\left(\frac{2^{B_b}}{2}\right)^2 \tag{34}$$

where $f_s$ is the sampling frequency of the converter, and all the other parameters are as discussed above. Note that this result is independent of $N$, i.e., the number of samples in one estimation cycle. Heuristically, we can argue that $N$ should be chosen such that the standard deviation of the distance estimates corresponds to several LSBs (bin widths) of the backend ADC. Under this condition, the estimator error is dominated by its inherent statistical variance rather than the quantization noise of the backend. In some sense, the estimator variance then acts as a "dither" signal that reduces the relative impact of the finite granularity of the histogram bins.

## IV. Simulation Example

In this section, we illustrate the capabilities of the proposed calibration technique through numerical example and simulation. For this demonstration, we use a simulation model that closely resembles the pipelined ADC implementation in [1]. This converter consists of a 3-bit first stage and a backend with an effective resolution of 9 bits plus two redundant bits to minimize residual errors. An appropriate model for the first-stage amplifier that conforms with (3) is given by [1]

$$g(V_a) = g_m R \cdot \left[\left(\frac{V_a}{V_{\mathrm{ref}}}\right) + \frac{1}{4}\frac{\Delta\beta}{\beta}\left(\frac{V_{\mathrm{ref}}}{V_{\mathrm{OV}}}\right)\left(\frac{V_a}{V_{\mathrm{ref}}}\right)^2 - \frac{1}{8}\left(\frac{V_{\mathrm{ref}}}{V_{\mathrm{OV}}}\right)^2\left(\frac{V_a}{V_{\mathrm{ref}}}\right)^3\right]. \tag{35}$$

With $V_{\mathrm{ref}} = 1$ V, $V_{\mathrm{OV}} = 0.25$ V, $\Delta\beta/\beta = 5\%$, and $g_m R = 7.6$, (35) becomes

$$g(V_a) = 7.6V_a + 0.38V_a^2 - 15.2V_a^3. \tag{36}$$

Next, we consider the design parameters for the LMS loops. Using $V_{\min} = \Delta/8$, we obtain $\delta_2 = 0.136$ and $\delta_3 = 0.422$. From (34), we see that the expected loop time constant is inversely proportional to $\delta^2$. To compensate for the low $\delta_2$, we allocate most of the total worst-case error budget to the second-order loop. With a total error budget of

$$L_{\mathrm{tot}} = \sqrt{L_1^2 + L_2^2 + L_3^2} = 0.5\,\mathrm{LSBrms} \tag{37}$$

and allocating approximately 80% of this budget for $L_2^2$, 15% for $L_3^2$, and the remaining 5% for $L_1^2$, we obtain $\mu_1 = 1/170$, $\mu_2 = 1/40$, and $\mu_3 = 1/170$.

Fig. 10 shows the parameter convergence upon startup of the converter with a full-scale sine wave applied. The expected convergence envelopes have been found by computing the time constant for each loop using (34) and the numerical values given above. The parameter $p_2$ converges as predicted by its calculated time constant. The deviation of the other two parameters from their expected envelope is caused by the fact that the three estimation loops are not independent. For instance, $p_3$ must first follow the transients in $p_2$ before it can approach its steady-state mean. The parameter $p_1$ must track the settling of both $p_2$ and $p_3$. Fig. 11 shows the effective number of bits[3] (ENOB) during

[3]Measured by computing the signal-to-noise-and-distortion ratio (SNDR) at the output of the converter during the simulated transient with sinusoidal input, ENOB = [SNDR (in decibels) − 1.76]/6.02.

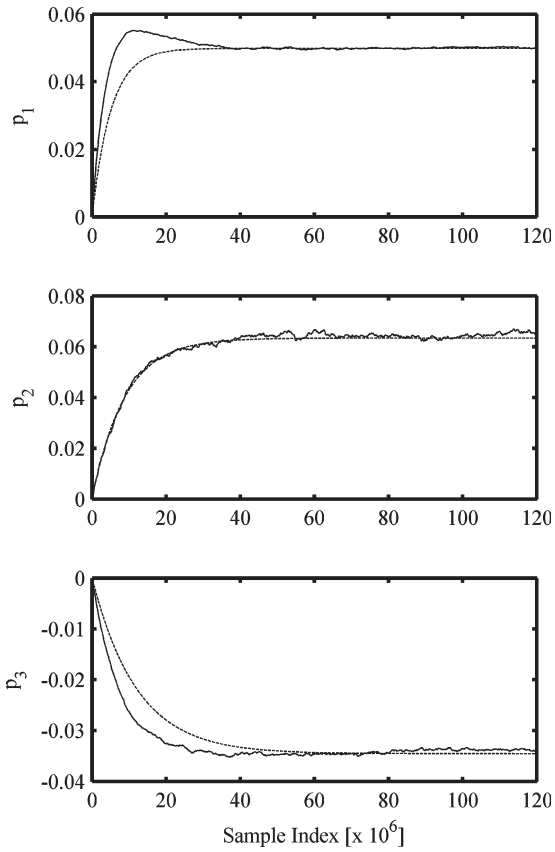


Fig. 10. Parameter convergence (dashed lines show expected envelope).

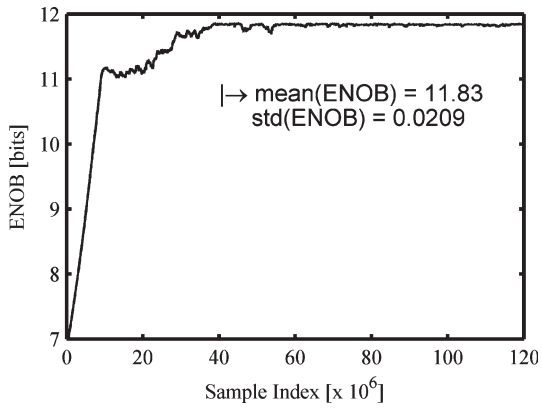


Fig. 11. Convergence of ENOB.

parameter settling with the final output truncated to 12 bits. The ENOB of the converter reaches its steady state after roughly 40 million samples. This number corresponds to approximately three time constants of the quadratic and cubic estimation loops.

As we can see from this example, the statistical nature of the parameter measurement dictates fairly large tracking time constants. For the discussed 12-bit implementation, time constants on the order of 10 million samples are necessary. Assuming a conversion rate of 100 MS/s in a typical state-of-the-art ADC, this translates into 100 ms on an absolute time scale. For ADC resolutions of 8–12 bits, the attainable tracking speed is sufficient to compensate, e.g., ambient temperature variations, slow changes in supply voltage, and device aging effects. For higher-resolution ADCs, e.g., 14 or 16 bits, the required time constants tend to approach unmanageably large values. From (34), it follows that each additional bit in ADC precision results in quadrupling the time constant. Hence, for a 16-bit converter, we would expect time constants of 100 ms $\cdot\, 4^4$ or roughly 25 s. For cases where such slow adaptation cannot be tolerated, a modified estimation process that uses a "split-ADC" approach could be considered [5], [15].

## V. Conclusion

We have developed a digital background calibration technique that helps alleviate precision requirements in the critical interstage gain elements of pipelined ADCs. Particularly in fine line technology, the proposed scheme can be used to efficiently tradeoff analog complexity and precision for low-power digital-signal processing. Potentially, a variant of the digital nonlinearity compensation and parameter estimation approach could be used in other applications, including transducers and transmission media.

## Appendix
## Estimator Variance Derivation

The analysis below derives (26). Ignoring finite histogram resolution, it follows from the setup in Fig. 8 that

$$\mathrm{var}(D) = \mathrm{var}(Y^*_{\mathrm{top}}). \tag{38}$$

To proceed, it is useful to partition the possible outcomes for each input sample $V_{\mathrm{in}}(k)$ into the following three distinct events: 1) $PN(k)=1$, $V_{\mathrm{in}}(k)\leq V$; 2) $PN(k)=1$, $V_{\mathrm{in}}(k)>V$; and 3) $PN(k)=0$. Provided that $V_{\mathrm{in}}(k)$ is independent of $PN(l)$ for all $k$ and $l$, we can identify the following probabilities for each one of the above events:

$$\begin{aligned} p_1 &= 0.5 \cdot F(V) \\ p_2 &= 0.5 \cdot (1 - F(V)) \\ p_3 &= 0.5 \end{aligned} \tag{39}$$

where $F(V)$ denotes the cumulative distribution function of $V_{\mathrm{in}}(k)$ that is evaluated at $V_{\mathrm{in}} = V$.

Now let the random variables $N_1$, $N_2$, and $N_3$ denote the number of occurrences for each possible event within a cycle of $N$ samples. It then follows that these random variables have a multinomial distribution with parameters $N$ and $p_1$, $p_2$, and $p_3$, respectively [20]. With respect to the setup in Fig. 8, we see that $N_1 = CH(y_{\mathrm{bot}})$, and that $N_3$ is the total number of samples that were processed using the upper transfer function segment $(PN(k) = 0)$.

After each processing cycle, the cumulative histogram bins are evaluated, and we find $Y^*_{\mathrm{top}}$ such that its bin count is closest to the count in the reference bin $y_{\mathrm{bot}}$, i.e.,

$$\begin{aligned} Y^*_{\mathrm{top}} &= \arg\min_y \left(|CH(y_{\mathrm{bot}}) - CH(y)|\right) \\ &= \arg\min_y \left(|N_1 - CH(y)|\right). \end{aligned} \tag{40}$$

In the limit case of infinitely dense bins and a large number of samples, (40) is minimized such that $CH(Y^*_{\rm top})$ is exactly equal to $N_1$. If we order all the samples that make up $CH(Y^*_{\rm top})$, it follows that the largest one of these $N_1$ samples corresponds to the upper bin edge and consequently $Y^*_{\rm top}$ itself. Therefore, $Y^*_{\rm top}$ is given by the $N_1$th-order statistic in the sample of size $N_3$. Equivalently, $Y^*_{\rm top}$ represents the $(N_1/N_3)$th $= P$th quantile of the samples processed by the upper transfer function segment.

Expressions for the variance of order statistics exist in the literature, but they usually assume a fixed rank and sample size. Important to note in this analysis is that both the rank $N_1$ and the sample size $N_3$ are random variables. A derivation from first principles that takes this randomness into account is desirable but tends to yield complex results (see, e.g., [21]). In the following steps, we use suitable simplifications to obtain an approximate but sufficiently accurate result. First, to relate the variance of $Y^*_{\rm top}$ to the statistics of $V_{\rm in}$, we can approximate for weakly nonlinear segment transfer functions

$$\mathrm{var}\left(Y^*_{\rm top}\right) = \mathrm{var}(h_-(V^*)) \cong \mathrm{var}(b_1 V^*) = b_1^2 \mathrm{var}(V^*) \quad (41)$$

where $V^*$ is the $P$th quantile of an input sample of size $N_3$, and $P = N_1/N_3$. By conditioning on $P$, we can rewrite

$$\mathrm{var}(V^*) = \mathrm{var}(E(V^*|P)) + E\left(\mathrm{var}(V^*|P)\right). \quad (42)$$

For a uniform input distribution [$f(V_{\rm in}(k)) = 1/\Delta$, $F(V_{\rm in}(k)) = V_{\rm in}(k)/\Delta$], the conditional expectation of $V^*$ in the first term of (42) is simply $F^{-1}(P) = P \cdot \Delta$. To capture a more general case, we use a linear gradient approximation for $F(V_{\rm in})$ in the small region of interest around the estimation site $V$ as

$$F\left(V_{\rm in}(k)\right) \cong F(V) + f(V) \cdot \left(V_{\rm in}(k) - V\right). \quad (43)$$

Inverting this expression gives the approximate location of the quantile as

$$F^{-1}(P) = \frac{P - F(V)}{f(V)} + V. \quad (44)$$

The first term in (42) then becomes

$$\begin{aligned}\mathrm{var}(E(V^*|P)) &= \mathrm{var}\left(\frac{P - F(V)}{f(V)} + V\right) \\ &= \frac{1}{f(V)^2}\mathrm{var}(P) \\ &= \frac{1}{f(V)^2}\mathrm{var}\left(\frac{N_1}{N_3}\right). \end{aligned} \quad (45)$$

It is not straightforward to derive an exact expression for the variance of the quotient $N_1/N_3$. However, it is possible to obtain a good approximation through a second-order Taylor expansion of the quotient [22]. This approximation is given by

$$\mathrm{var}\left(\frac{N_1}{N_3}\right) \cong \left(\frac{E(N_1)}{E(N_3)}\right)^2 \cdot \left[\frac{\mathrm{var}(N_1)}{E(N_1)^2} + \frac{\mathrm{var}(N_3)}{E(N_3)^2} - \frac{2 \cdot \mathrm{cov}(N_1, N_3)}{E(N_1) \cdot E(N_3)}\right]. \quad (46)$$

Using formulas for the moments of the multinomial distribution of $N_1$ and $N_3$, and using (39), (45), and (46), we find

$$\mathrm{var}(E(V^*|P)) = \frac{2 \cdot F(V) \cdot (1 + F(V))}{N \cdot f(V)^2}. \quad (47)$$

Next, consider the second term in (42). If $F(V_{\rm in})$ is strictly increasing and continuous, a general approximation formula exists for the variance of a $p$th quantile $Q$ in a sample of size $M$ with local density $f(Q)$ [22], i.e.,

$$\mathrm{var}(Q) \cong \frac{p(1-p)}{M \cdot f(Q)^2}. \quad (48)$$

Using this result, and noting that the sample size under consideration corresponds to $N_3$, we obtain for the second variance component of (42)

$$\begin{aligned} E\left(\mathrm{var}(V^*|P)\right) &\cong \frac{1}{f(V)^2} E\left(\frac{P(1-P)}{N_3}\right) \\ &= \frac{1}{f(V)^2} E\left(\frac{\frac{N_1}{N_3}\left(1 - \frac{N_1}{N_3}\right)}{N_3}\right). \end{aligned} \quad (49)$$

In general, the expected value of a function of random variables can be approximated through an appropriate Taylor series. Analysis shows that a first-order approximation suffices here. Consequently, we approximate the bracketed term in (49) as

$$E\left(\frac{\frac{N_1}{N_3}\left(1 - \frac{N_1}{N_3}\right)}{N_3}\right) \cong \frac{\frac{E(N_1)}{E(N_3)}\left(1 - \frac{E(N_1)}{E(N_3)}\right)}{E(N_3)} \quad (50)$$

to obtain

$$E\left(\mathrm{var}(V^*|P)\right) \cong \frac{2 \cdot F(V) \cdot (1 - F(V))}{N \cdot f(V)^2}. \quad (51)$$

Finally, adding (47) and (51) yields

$$\mathrm{var}(D) \cong \frac{4}{N} \cdot \frac{F(V)}{f(V)^2}. \quad (52)$$

This final result matches appropriate Monte Carlo simulations with good precision.

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