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Exploiting Smallest Error to Calibrate Non-Linearity in SAR Adcs

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ABSTRACT This paper presents a statistics-optimized organization technique to achieve better element matching in successive approximation register (SAR) analog-to-digital converter (ADC) in smart sensor systems. We demonstrate the proposed technique ability to achieve a significant improvement of around 23 dB on a spurious free dynamic range (SFDR) of the ADC than the conventional, testing with a capacitor mismatch $\sigma_u = 0.2\%$ in a 14-bit SAR ADC system. For the static performance, the max root mean square (rms) value of differential nonlinearity reduces from 1.63 to 0.20 LSB and the max rms value of integral nonlinearity (INL) reduces from 2.10 to 0.21 LSB. In addition, it is demonstrated that by applying grouping optimization and strategy optimization, the performance boosting on the SFDR can be effectively achieved. Such a great improvement on the resolution of the ADC only requires an off-line pre-processing digital part.

INDEX TERMS Analog-to-digital converter, capacitor mismatch calibration, smart sensor, successive approximation register (SAR) ADC.

I. INTRODUCTION

Smart sensors are devices which integrate transducers, signal conditioning and processing electronics, and have played an important role in changing our society and lifestyle. The merit goes to the explosive growth of embedded applications for smart sensors [1].

Fig. 1 shows the block diagram of a smart sensor node: the sensor detects a physical, chemical or biological quantity, then the small signal at the output of the sensor is amplified and filtered, after that, an analog-to-digital converter (ADC) converts the analog sensing signal into digital codes. Since the ADC is an important block in smart sensor node, the designer must optimise performance of the ADC specifically, high resolution in order to satisfy the demands of low power and small silicon area at the same time as required by multi-functional smart sensor nodes.

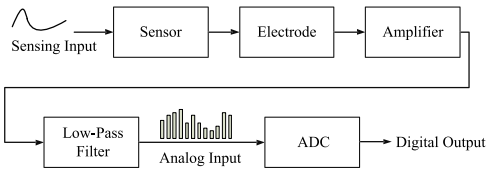

FIGURE 1. Basic architectural components of smart sensor node.

The simple architecture and the high resolution characteristic make the successive approximation register (SAR) converter (obtains the analog-to-digital conversion using a binary search algorithm) the optimal choice for medium

speed sensor applications. However, the weight error due to the capacitive array mismatch and the cumulative error results from using the same configuration of capacitors severely limit the resolution of the converter hence the quality of the output digital sinal. For high-resolution SAR ADC, the limits require using large unity capacitors and calibration circuits normally with off-line operation. This paper presents a method that allows using the minimum capacitance imposed by the kT/C limit and requires a limited digital control to reach high Spurious Free Dynamic Range (SFDR) and Signal-to-Noise-and-Distortion Ratio (SNDR). The proposed calibration method is inspired by the merits of two previous techniques [2] and [3]. With the proposed grouping and strategy optimisation in this work, an optimal linearity for a given set of elements can be achieved.

The remainder of this paper is organised as follows. Section II describes previous work on performance enhancement methods, including averaging technique, reconfiguring technique and swapping technology, section III discusses the theory background, grouping method optimisation and strategy optimisation. Section IV gives detailed description of the implementation of the proposed technique, then section V compares performance between conventional, early presented method and the proposed statistics-optimised organisation technique. The conclusions are finally drawn in section VI.

II. PERFORMANCE ENHANCEMENT METHODS STATE-OF-THE-ART

A swapping technology used for minimising the INL is presented by [2]. The implementation steps in swapping technology are as follow: first, split the capacitive array into two groups (do the same to the positive and negative DAC in a differential SAR ADC); then, use two groups alternatively to represent the MSB or the LSBs during the conversion.

For a large number of input samples, the swapping technology swaps the capacitors to get each result for each input sample and thus to reduce the INL without sacrificing the speed.

Recently, a capacitor reconfiguring technique was proposed in [3], extra 64 capacitors were added to the capacitive array. With the understanding [3], it is analysed that the capacitors after sorting can also be reorganised by using ''one head and one tail'' approach and subsequently assemble them into capacitor pairs so that the mismatch can be counteracted to a large extent. Although sampling rate remains the same as that of the conventional SAR ADC, extra 64 capacitors lead to inevitable extra chip area consumption.

III. STATISTICS OPTIMISATION OF THE PROPOSED TECHNIQUE

A. SIMULATION SETTING

The simulations in this work are completed by using Matlab, which is a time saving tool [4] to run extensive Monte Carlo simulations. In our behavioral simulation model, we adopt a 14-bit SAR schematic shown in Fig. 2, a capacitor-resistor

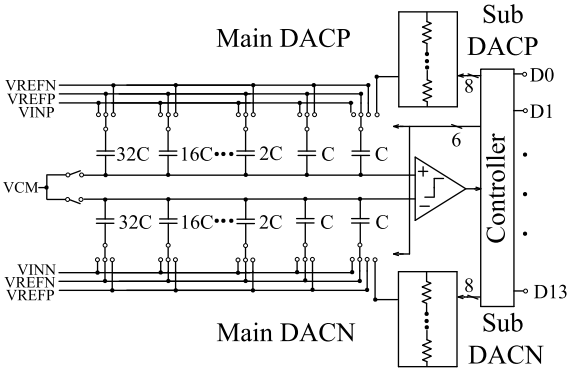

FIGURE 2. A capacitor-resistor combined 14-bit SAR ADC architecture.

architecture with a 6-bit capacitive DAC and an 8-bit resistive sub-DAC as the LSBs. The element mismatch for the capacitive DAC is assumed to follow a Gaussian distribution [5]. And for the sake of simplicity, we assume no mismatch in the 8-bit sub-resistive DAC for its minor effect compared to the MSBs and other circuit components to be ideal.

The basic idea of the proposed organisation technique is to incorporate the merits of the reconfiguring technique and swapping technology, to improve the linearity and counteract the element mismatch. In this work, two statistical robust optimisation methods to achieve the best element matching and linearity performance of the SAR ADC systems are proposed.

B. CAPACITOR MISMATCH IN ADC

Before delving into the theory analysis of the proposed technique, let's recall the element mismatch problem in SAR ADC design. As well known, in common SAR ADC architecture, the capacitive DAC always suffers an error, which is due to the limitation of the technology and is often treated as an error following the Gaussian distribution. While in a N-bit binary SAR ADC system, high linearity always addresses a strict binary weight requirement on the DAC. For example, the binary voltage should be like

$$V_{DAC} = -\sum_{i=0}^{N} (-1)^{D_i} \frac{V_{REF}}{2^{i+1}} \tag{1}$$

In a most commonly used SAR ADC architecture with a capacitive DAC, the binary reference voltage is represented by the form of capacitors

$$V_{DAC} = -\sum_{i=0}^{N} (-1)^{D_i} \frac{C_i V_{REF}}{C_{tot}} \tag{2}$$

Ideally, the C_i has a form of

$$C_i = 2^{N-i} C_u \tag{3}$$

While, consider the mismatch

$$C_i = 2^{N-i} C_u + \Delta C_i \tag{4}$$

in which, $\Delta C_i = \sqrt{2^{N-i}}\Delta C_u$ and ΔC_u is the unit capacitor mismatch.

In our capacitor-resistor combined SAR ADC architecture, a resistor sub-DAC is introduced to reduce the total amount of the capacitor. In previous introduction, we assume no mismatch in the sub-DAC for its minority (see equation (4)). It remains a problem that the capacitive DAC suffers element mismatch. Due to equation (4), the MSB and MSB-1 weight capacitor suffer the most serious mismatch and will directly affect the nonlinearity (DNL/INL), thus are the first targets to deal with.

C. THEORY OF SWAPPING TECHNOLOGY

The merit of averaging technique or swapping technology is the reduction of INL. By dividing the capacitor array into two or four groups and then alternate (swap) them in each conversion, the accumulation of MSB weight error or both MSB and MSB-1 weight error can be eliminated.

To have a better understanding of one key of this work, we briefly review the theory of the previous swapping technology. Assuming first that C_{tot} equals an ideal value $64C_u$ for simplicity. Then we divide half of the elements into MSB group, and the other half into LSBs group. Due to the deviation between the ideal value cause by element mismatch, we have

$$MSB = 32C_u(1 + \Delta P/2) \tag{5}$$

$$LSBs = 32C_u(1 - \Delta P/2) \tag{6}$$

The error term ΔP is defined as twice the deviation of the MSB from the ideal value, which is half of the C_{tot}, $32C_u$.

From equation (5) and (6), it can be revealed that the elimination of INL at the MSB decision is because of error term cancelling. The weight error elimination is clearly shown in the INL test on two and four-group case as presented in Fig. 3. A noticeable feature of the INL curve in the Fig. 3 is that the INL curve is folded at the MSB and MSB-1 decision point after level-1 and level-2 swapping, respectively. It's shown by applying the level-2 swapping, the max INL error is double halved than before. The theoretical insight for the folding has been discussed in detail in [2]. According to [2], level-2 swapping technology (corresponding the four-group case) needs the whole binary capacitive array dividing into four groups and the next level requires eight groups, and so on.

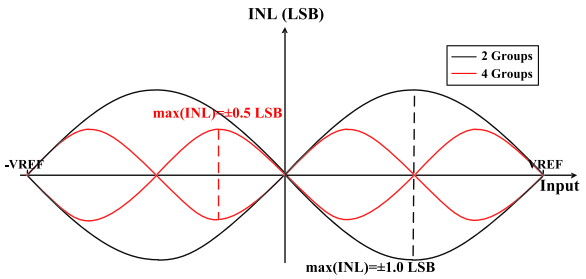

FIGURE 3. INL of level-1 and level-2 Swapping in [2].

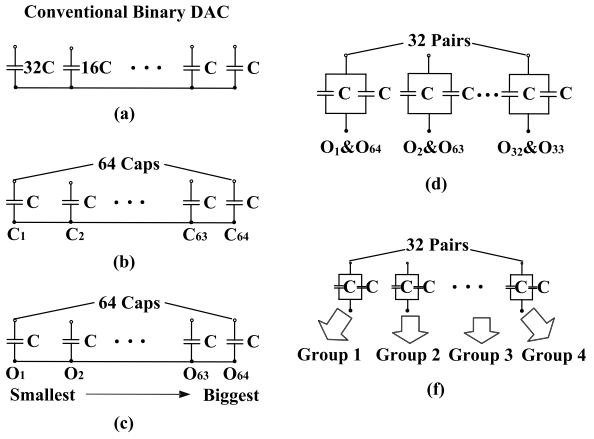

FIGURE 4. Capacitor Reconfiguring with 64 unit capacitors: (a) Conventional binary capacitive array in Fig. 2; (b) Split binary capacitive array into unary architecture; (c) Sort the 64 unit capacitors; (d) Reconfigure the 64 sorted unit capacitors into 32 pairs. (d) Divide the 32 pairs into 4 groups.

In the ideal condition, twice the number of groups will divide the max INL. However, the exponentially increasing logic cost and power consumption will compromise the overall performance.

D. THEORY OF RECONFIGURING TECHNIQUE

The reconfiguring technique shapes the elements towards a lower effective element mismatch, which exploits the order statistic principles [6], [7]. As Fig. 4 shows, the elements after sorting and reconfiguring (pairing) demonstrate a significant reduction on the mismatch error. However, our test results on the reconfigured elements reveal that the statistical distribution of each capacitor pair is not well-balanced but follows an "hourglass" shape as shown in Fig. 5. This means that after sorting and reconfiguring, the error of capacitor pairs is no longer uniform but differ as the order of pair changes.

For a differential SAR ADC in this work, the complementary capacitors on positive and negative DACs could be regarded as one element, because of the complementary behaviour during the differential SAR process [8]. For example, C_{1p} and C_{1n} are processed together. Then, the sorting and

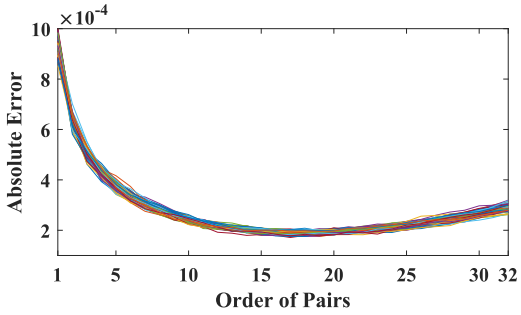

FIGURE 5. Element mismatch error (absolute value) distribution using reconfiguring technique, testing on 64 unary elements, which is sorting and reconfiguring to 32 pairs.

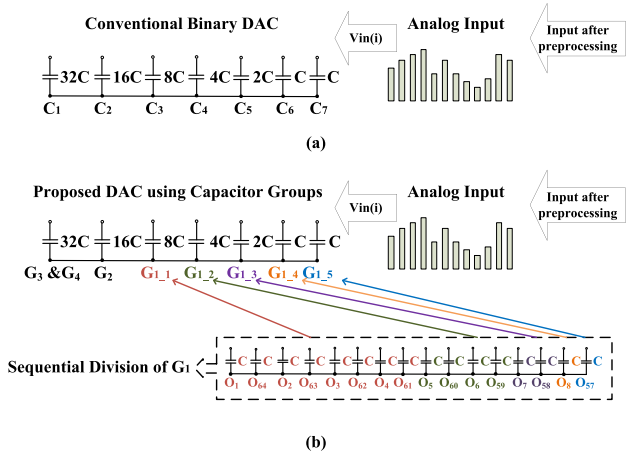

FIGURE 6. The conventional Binary DAC (a) and proposed DAC using capacitor groups (b).

reconfiguring(pairing) technique as well as grouping are used for all 64 elements. However, the sorting number is reduced to a half of the number in previous work [3] and thus an extra 64C capacitive array is avoided. In addition, a four-group swapping method is adopted to eliminate the MSB and MSB-1 weight error and double halve the INL as discussed.

E. GROUPING OPTIMISATION

For a four-group case as discussed earlier, the grouping setting is different from a two-group case (refer to [2]). One example is shown in Fig. 6, the MSB is represented by two capacitor groups G3&G4, the MSB-1 weight by group G2, and the rest LSBs are represented by a binary DAC made by sequentially divide the last group G1. The four groups' setting in Fig. 6 is not fixed but alternating following a certain strategy (for simplicity, here the swapping strategy used here is the same with the strategy 1 in the later Table 1).

As mentioned, the element mismatch error after sorting demonstrates an unbalanced statistic distribution as the upper half of an "hourglass" shape. The unbalanced error distribution addresses the importance for a careful selection of the grouping method. For a bad grouping method will disturb the binary weight hence affect the resolution. Here, three

TABLE 1. Three possible strategies to alternate four groups.

		32C	16C	8C 4C 2C C C
Strategy 1	Vin(i)	Group1 & Group2	Group3	Group4
	Vin(i+1)	Group3 & Group4	Group1	Group2
	Vin(i+2)	Group1 & Group2	Group4	Group3
	Vin(i+3)	Group3 & Group4	Group2	Group1
Strategy 2	Vin(i)	Group1 & Group3	Group2	Group4
	Vin(i+1)	Group2 & Group4	Group1	Group3
	Vin(i+2)	Group1 & Group3	Group4	Group2
	Vin(i+3)	Group2 & Group4	Group3	Group1
Strategy 3	Vin(i)	Group1 & Group4	Group2	Group3
	Vin(i+1)	Group2 & Group3	Group1	Group4
	Vin(i+2)	Group1 & Group4	Group3	Group2
	Vin(i+3)	Group2 & Group3	Group4	Group1

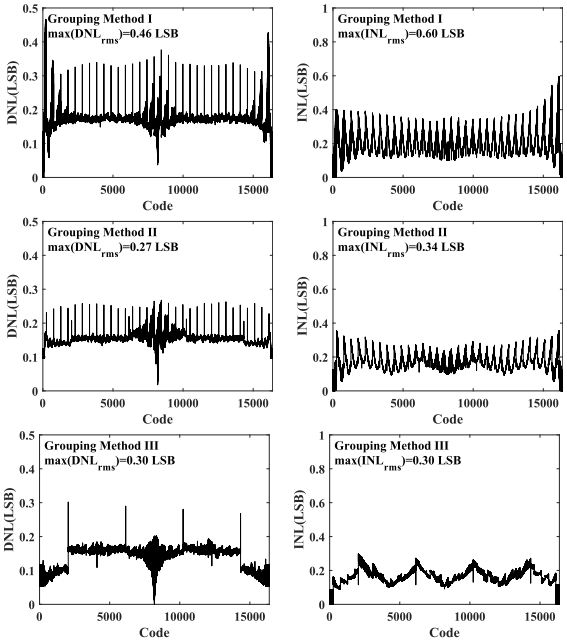

FIGURE 7. 500 Monte Carlo root-mean-square(rms) of DNL/INL simulation results using different grouping methods in a 14-bit SAR ADC system.

different grouping methods are implemented in a 64 elements DAC array to show the difference.

Grouping Method I: selecting pairs sequentially. Group 1 consists of Pair 1, Pair 2, …, Pair 8. Group 2 consists of Pair 9 to Pair 16. Group 3 consists of Pair 17 to Pair 24 and Group 4 consists of the rest pairs.

Grouping Method II: selecting pair number with a mode of 2. Group 1 consists of Pair 1, Pair 3, Pair 5, …, Pair 15. Group 2 consists of Pair 2, Pair 4 to Pair 16. Group 3 consists of Pair 17, Pair 19 to Pair 31 and Group 4 consists of Pair 18, Pair 20 to Pair 32.

Grouping Method III: selecting pair number with a mode of 4. Group 1 consists of Pair 1, Pair 5, Pair 9, …, Pair 29. Group 2 consists of Pair 2, Pair 6, Pair 10, …, Pair 30. Group 3 consists of Pair 3, Pair 7, Pair 11, …, Pair 31 and Group 4 consists of Pair 4, Pair 8, Pair 12, …, Pair 32.

Moreover, we test the DNL_{rms} and INL_{rms} (a popular method to investigate the non-linearity [9]) on the three grouping methods. The element mismatch of capacitors is set at 0.2% and the results are shown in Fig. 7.

Compared to grouping method I and II, grouping method III shows a lower rms value for DNL and INL.To have a clear view of this, three grouping methods are mapped on the "hourglass" error distribution figure, as shown in Fig. 8, in which group 1 to 4 are represented by red, green, purple and yellow colour, respectively.

In the aspect of symmetry. As we can see in grouping method I (Fig. 8 (a)), a large mismatch exists between G1, G2, G3 and G4. Thus it leads to the worst performance. In grouping method II (Fig. 8 (b)), the mismatch is lessen by using a interval of 2 to group the pairs. However, the asymmetry of

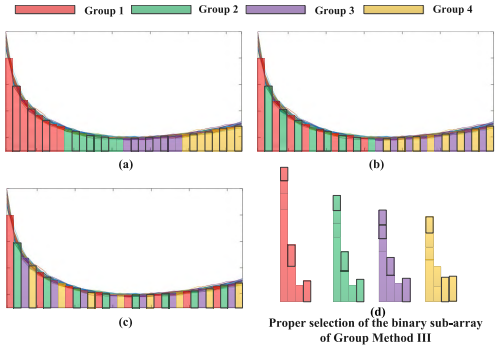

FIGURE 8. (a) Grouping Method I; (b) Grouping Method II; (c) Grouping Method III; (d) Proper binary selection for the last group.

the first half and the other half of the ''hourglass'' leads to a large mismatch existing among the four groups. The grouping method III (Fig. 8 (c)) uses a interval of 4 to fully separate the selection of four groups. The mismatch between four groups is thus be lessen.

In the aspect of linearity. The DNL peaks in 1C decision points (the last capacitor) in grouping method I and II are due to the large difference between the last two 1C capacitors depicted in Fig. 6. For instance, in the grouping method I's setting, the last two 1Cs, G1_4 and G1_5 are made by the 8-th pair which consists of the 8-th smallest and the 57-th smallest capacitors. When it comes to the last capacitor decision, the large mismatch between the G1_4 and G1_5 contributes to the DNL peaks.

Clearly, grouping method III treats the 1C peaks well for using the middle capacitors to represent the last 1C-1C. But the DNL peaks in the 8C decision points of grouping method III remain a problem. It's mainly because of the asymmetry from the sequential division of the last group, such as G1 in Fig. 6. In previous grouping method III, the 8C capacitor is represented by the first 4 sequential pairs in the first half of the ''hourglass'' (refer to Fig. 8 (c)), which still has a large mismatch with the rest 4 pairs.

The peaks can be further reduced by manually tuning the binary selection of the last group. Here, the simulation result of the manually tuned binary selection method is shown in Fig. 9. The tuning rule is to balance the error of the MSB with LSBs' towards a binary DAC. A proper binary tuning for the last group is shown in Fig. 8 (d).

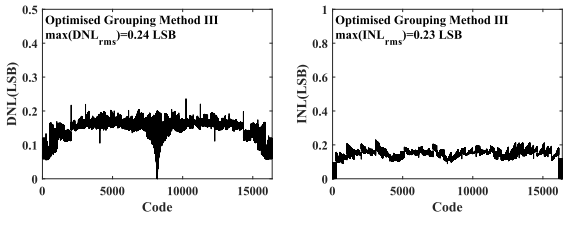

FIGURE 9. 500 Monte Carlo root-mean-square(rms) of DNL/INL simulation results after implementing optimised grouping methods III.

In conclusion, by optimising grouping method, we are able to reduce the INL_{rms} by 50% than a simple sequential grouping (grouping method I). The optimised grouping method could benefit sorting a lot with almost no cost.

F. STRATEGY OPTIMISATION

For MSB which corresponds to the biggest weight canceling, as discussed before, the quality of the cancelling depends merely on the error term. Thus the statistical property such as standard deviation and absolute value of the error term will affect the MSB error a lot.

Therefore, a feasible way to achieve the best MSB error cancelling is to reduce the standard deviation and the absolute value of the error terms used in equation (5) and equation (6). An accessible way to achieve this is to design an alternating strategy which uses the minimum error term during every conversion.

Strategy optimisation is done by determining the minimum absolute error term, then choosing the corresponding alternating strategy based on it. Instead of using a random error term by implementing a fixed strategy in previous techniques [2], the alternating strategy is optimised by only using the minimum error term.

Theoretically, the same procedure as the derivation of error term in equation (5) and equation (6) has been followed in this work, assuming the total capacitance is 64 C_u. For a four-group case, there exist three possible ways of two-two grouping. Thus three independent error terms ΔP_I, ΔP_{II} and ΔP_{III} are derived for three two-two grouping choices.

$$G1 + G2 = 32C_u(1 + \Delta P_I/2) \quad (7)$$
$$G3 + G4 = 32C_u(1 - \Delta P_I/2) \quad (8)$$
$$G1 + G3 = 32C_u(1 + \Delta P_{II}/2) \quad (9)$$
$$G2 + G4 = 32C_u(1 - \Delta P_{II}/2) \quad (10)$$
$$G1 + G4 = 32C_u(1 + \Delta P_{III}/2) \quad (11)$$
$$G2 + G3 = 32C_u(1 - \Delta P_{III}/2) \quad (12)$$

After simplification, we get

$$G1 = 16C_u(1 + \Delta P_I/2 + \Delta P_{II}/2 + \Delta P_{III}/2) \quad (13)$$
$$G2 = 16C_u(1 + \Delta P_I/2 - \Delta P_{II}/2 - \Delta P_{III}/2) \quad (14)$$
$$G3 = 16C_u(1 - \Delta P_I/2 + \Delta P_{II}/2 - \Delta P_{III}/2) \quad (15)$$
$$G4 = 16C_u(1 - \Delta P_I/2 - \Delta P_{II}/2 + \Delta P_{III}/2) \quad (16)$$

Noticed that three error terms that are independent to each other (see Appendix A). Thus the same as the capacitor mismatch, their values follow a Gaussian distribution. In Fig. 10, the 10^6 Monte Carlo simulation results compare the absolute value of the smallest error term and the error term which is randomly picked. It is shown that the smallest error term is confined to a probability distribution with a sharper shape, which represents a lower standard deviation of 2.3×10^{-3} compared to 4.8×10^{-3} of the random error term. It also shows a mean absolute value of 6.4×10^{-3} and 2.7×10^{-3} for the random term and the smallest error term, respectively. Thus, we strongly desire to utilise the smallest error term

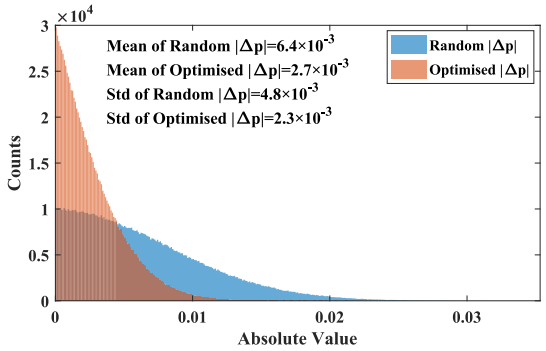

FIGURE 10. 10^6 Monte Carlo simulation results of the error terms.

in our technique. The first step for this is to determine the smallest error term.

To determine the minimum error term (absolute value), comparisons are done on each two out of four capacitor groups. For instance, G1 compare with G2, which is equivalent to $\Delta P_{II} + \Delta P_{III}$ compare with 0 by using equation (13) and (14). Then G3 compare with G4, equivalent to $\Delta P_{II} - \Delta P_{III}$ compare with 0 by using equation (15) and (16). If the two comparison results turn out to have the same sign, the relationship between error terms could be settled: $|\Delta P_{II}| > |\Delta P_{III}|$. If the results are in opposite signs, $|\Delta P_{II}| < |\Delta P_{III}|$.

Thus, the smallest error term could be derived by doing comparisons for six times in total. Next, three possible alternating strategies are designed to match three possible cases.

According to the theory in section III, the design of alternating strategy must meet two conditions: (1) error terms accumulation in one period for MSB and MSB-1 must be zero; (2) to utilise the optimised error term, alternating strategies must match every possible error term after error term optimisation. The design of three possible strategies are summarised in Table 1. For Strategy 1, in one hand, the error term accumulation of MSB and MSB-1 in one period is zero. On the other hand, the MSB weight is represented by G1 & G2 or G3 & G4 during alternative conversion. In addition, in each period of conversion, the sum of error terms in MSB will maintain an accumulative error which is characterised by $-\Delta P_I + \Delta P_I$ equals to zero. Thus, strategy 1 is typical for error term ΔP_I and strategy 2 and strategy 3 represent the other two error terms ΔP_{II} and ΔP_{III}, respectively.

The strategy optimisation is done after determining the smallest error term and the corresponding alternating strategy.

IV. MIXED-SIGNAL IMPLEMENTATION OF THE PROPOSED ORGANIZATION TECHNIQUE

The proposed organisation technique is described using the main capacitive DAC of capacitor-resistor combined SAR ADC in Fig. 2 as a test vehicle and follows the sorting and grouping steps shown in Fig. 4. The grouping method used here utilises the proposed grouping method, which is proved to have the best performance. It followed by strategy optimisation to derive the optimised error term and hence the corresponding alternating strategy. During every analog to digital conversion, the optimised alternating strategy was used for the four capacitor groups to do the binary search in successive approximation.

A. COMPARISON IMPLEMENTATION

For the sake of precise comparisons among unit capacitors, an accurate sorting poses a high-resolution request on the comparator. Trade-off issue within the sorting performance and the resolution of the comparator needs to be considered. To investigate this, we test the the relationship between the comparison accuracy and the comparator resolution on a 14-bit SAR ADC system, as shown in Fig. 11, with an element mismatch from 0.1% to 0.4%. It is shown that as the resolution goes up, the accuracy follows a linear decay function. A super high accuracy (above 99%) also has a super high resolution (around 28 μV) request on the comparator design.

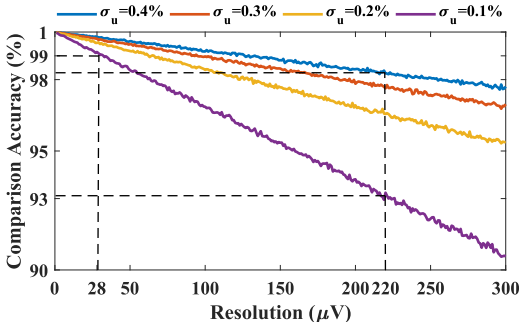

FIGURE 11. The comparison accuracy versus resolution of the comparator.

On the other hand, the resolution requirement to achieve an above 90% of comparing accuracy is totally feasible. For a typical differential 14-bit SAR ADC with a 1.8V VREF, the basic request for the comparator design is about $2 \times 1.8/2^{14} \approx 220\mu V$, and our test shows a 98.2% down to 93.0% of comparison accuracy for a 220 μV-resolution comparator design.

We advance this issue to investigate the error tolerance of the proposed technique by considering the limited accuracy. our sorting algorithm is redesigned by adding an accuracy term in every comparison (every comparison has a probability which is equal to the accuracy to give the correct result, otherwise give random result).

Again we run 50 times Monte Carlo simulation on a 14-bit SAR ADC system and set the mismatch from 0.1% to 0.4%, as shown in table 2. The results show that with a 90% of accuracy, the SFDR performance decreases about 9 dB. For a 95% accuracy sorting which is quite easy to obtain, the SFDR is only 4 dB worse than a 100% accuracy with σ_u=0.1%.

TABLE 2. 50 Monte Carlo SFDR simulation results with limited accuracy.

mean(SFDR)/dB	σ_u=0.1%	σ_u=0.2%	σ_u=0.3%	σ_u=0.4%
Accu=100%	105.2	100.3	97.3	95.5
Accu=99%	104.6	99.0	95.2	93.3
Accu=98%	103.0	97.7	94.3	91.2
Accu=95%	101.3	95.2	90.6	88.2
Accu=90%	97.9	91.8	88.8	86.4

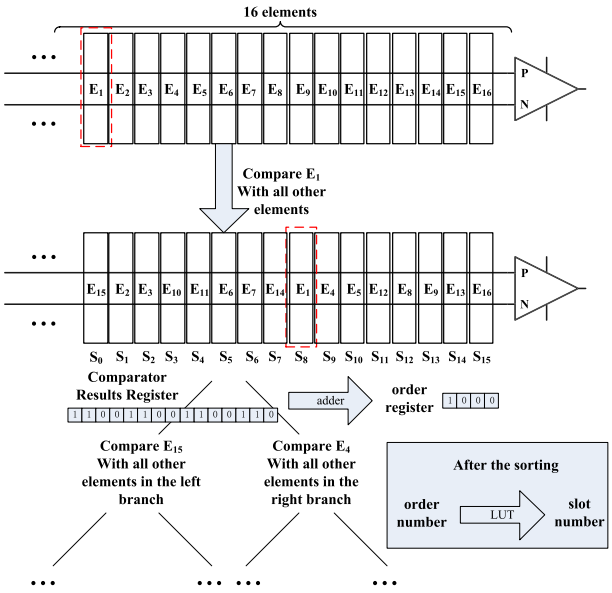

FIGURE 12. Diagram of a sorting instance.

TABLE 3. Cost of the proposed technique.

Technique	Area (mm^2)	Power (mW)	Logic Gates	Clock Cycles
Without SO	0.887	0.612	40788	992
With SO	0.930	0.620	43192	998

B. IMPLEMENTATION OF SORTING AND GROUPING

For the sorting part, we design a binary-tree sorting algorithm with a complexity of O($n \log n$). The digital implementation of the sorting algorithm on a simplified 16 elements example is shown in Fig. 12.

The sorting starts with the first element E1 (root element) comparing with all other elements. Recording all the results in a N=16 register, which capacitor is larger as well as which capacitor is smaller than E1 could also be known. We do a sum function on the result register to determine the order for E1. After that the smaller elements are put into the left branch and the larger are put into the right. We again take E15 and E4 in the left branch and right branch respectively as root element to do comparisons, and so forth to determine all the capacitor order.

Noticed that the order register is a large register recording the order information for all elements, we need access this register to read the order information thus one decoder is needed for this sorting design. Next, we map the order register to the slot register following a look-up-table (LUT)

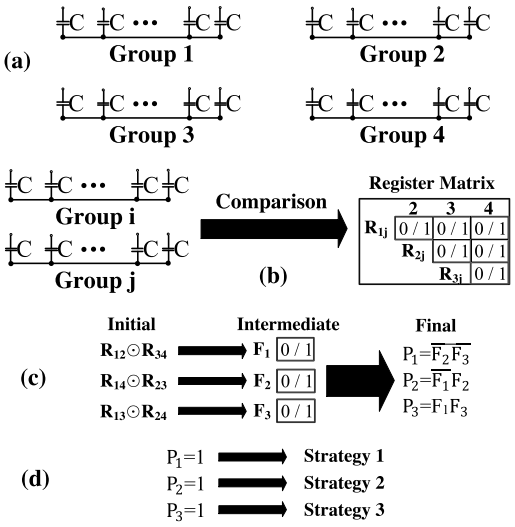

FIGURE 13. The process to determine the error term and select the corresponding strategy.

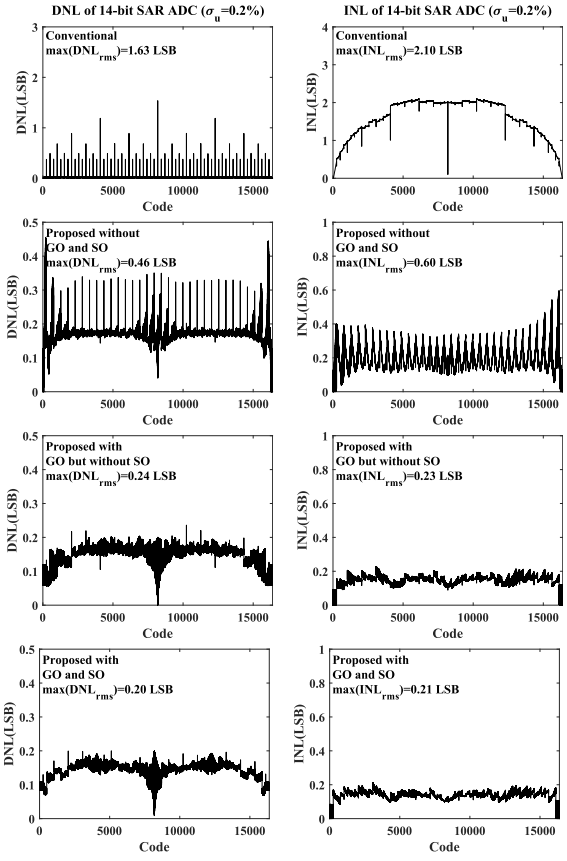

FIGURE 14. 500 Monte Carlo root-mean-square(rms) of DNL/INL simulation results for 14-bit SAR ADC with conventional and the proposed techniques.

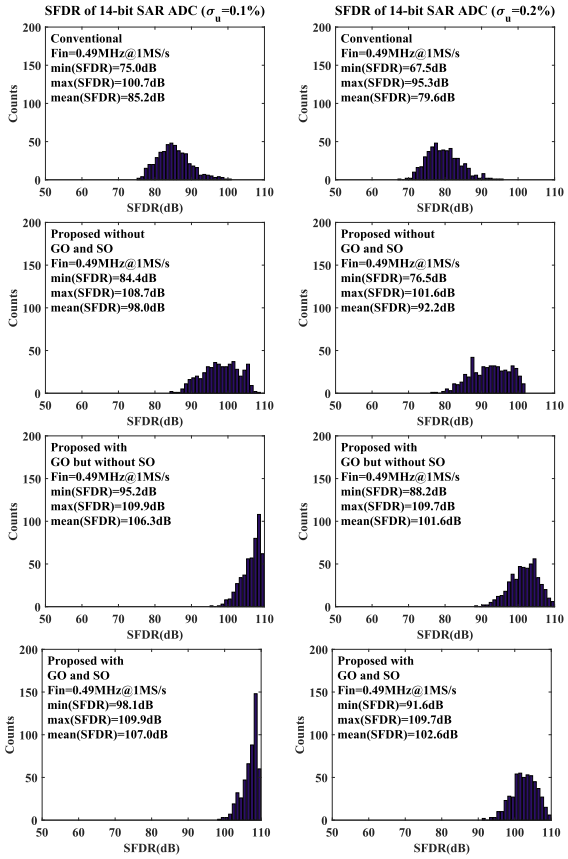

FIGURE 15. 500 Monte Carlo SFDR simulation results for 14-bit SAR ADC with respectively conventional and the proposed techniques with σ_u=0.1% (left) and σ_u=0.2% (right).

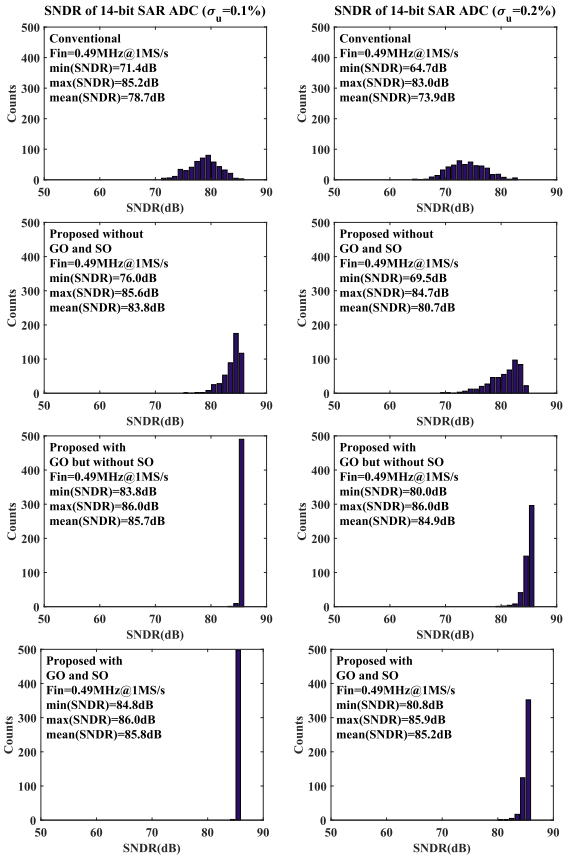

FIGURE 16. 500 Monte Carlo SNDR simulation results for 14-bit SAR ADC with respectively conventional and the proposed techniques with σ_u=0.1% (left) and σ_u=0.2% (right).

to finally rearrange the elements to corresponding slot. The LUT maps the order to the slot following optimised grouping method III.

The comparing times for this sorting design vary from $\sim N\log_2 N$ (best case) to $\sim N^2/2$ (worst case), which could be improved by a asynchronous design to trigger the next LUT process immediately rather than wait for the longest clock period for the worst case.

The sorting and grouping process start at the beginning of power-on, and are disabled once it has been done.

C. IMPLEMENTATION OF STRATEGY OPTIMISATION

After grouping, the process of the strategy optimisation is shown in Fig. 13. Four capacitor groups are presented at the beginning, as shown in (a) and to compare with each other in (b). After comparing six times in total, we save the results in six registers. Then in (c), we do "XNOR" operations on these registers and derive the intermediate value written in F1, F2 and F3, which indicates the larger one in each two error terms. We further obtain P1, P2, P3 as three flag registers to show which is the minimum error term, as shown in (d). Then we select strategy 1, 2 or 3 which matches the number of the flag registers whose value is "1".

After the strategy optimisation, the whole process of the proposed technique is completed.

D. COST EVALUATION

In order to estimate the area and power consumption of the proposed organisation technique, Design Compiler (L-2016.03-SP1) is applied to synthesise the digital logic. The circuits are set to work at 1MS/s in a 0.18 μm CMOS technology with a 1.8V power supply. Area and power of the sorting circuits are shown in Table 3. For the strategy optimisation will cost extra digital cost, we compare the proposed organisation with and without the strategy optimisation.

V. SIMULATION RESULTS

To show the improvement on static and dynamic performance, in this section, we took conventional, proposed without grouping optimisation (GO) and strategy optimisation (SO) and proposed with GO but without SO as comparisons of the proposed technique with GO and SO.

Fig. 14 shows root-mean-square(rms) of DNL/INL results of 500 Monte Carlo runs in a SAR ADC architecture the same as Fig. 2 with $\sigma_u = 0.2\%$. The addition of the grouping optimisation solely can reduce the max rms of DNL from

TABLE 4. 500 Monte Carlo SFDR, SNDR and SNR simulation summary.

	Conventional (dB)	Proposed (dB)	Improvement (dB)
mean(SFDR)(σ_u=0.1%)	85.2	107.0	21.8
mean(SFDR)(σ_u=0.2%)	79.6	102.6	23.0
mean(SFDR)(σ_u=0.3%)	75.6	99.4	23.8
mean(SFDR)(σ_u=0.4%)	73.1	97.0	23.9
mean(SNDR)(σ_u=0.1%)	78.7	85.8	7.1
mean(SNDR)(σ_u=0.2%)	73.8	85.2	11.4
mean(SNDR)(σ_u=0.3%)	70.2	84.4	14.2
mean(SNDR)(σ_u=0.4%)	67.8	83.4	15.6
mean(SNR)(σ_u=0.1%)	83.2	86.0	2.8
mean(SNR)(σ_u=0.2%)	79.5	85.6	6.1
mean(SNR)(σ_u=0.3%)	76.7	85.1	8.4
mean(SNR)(σ_u=0.4%)	74.6	84.4	9.8

0.46 LSB to 0.24 LSB and max rms of INL from 0.60 LSB to 0.23 LSB. Moreover, the strategy optimisation can further reduce the max rms of DNL from 0.24 LSB to 0.20 LSB and max rms of INL from 0.23 LSB to 0.21 LSB.

Fig. 15 and Fig. 16 show the SFDR and SNDR results of 500 Monte Carlo runs. The proposed with GO solely can improve the averaged SFDR from 79.6 dB to 101.6 dB with $\sigma_u = 0.2\%$, a significant 22.0 dB improvement of SFDR is achieved. And with SO, another 1 dB improvement is achieved in SFDR. And the extra costs for another 1 dB improvement is minor as the DC results shown in Table 3.

Briefly, the proposed technique in this work can achieve excellent performance enhancement with only a small cost on the digital logic without sacrificing the sampling rate of conventional SAR ADC.

Table 4 concludes 500 Monte Carlo SFDR and SNDR simulation results for conventional and the proposed technique. The proposed technique has an improvement of 23.9 dB on SFDR, of 15.6 dB on SNDR and of 9.8 dB on SNR.

VI. CONCLUSION

In this work, a statistic optimised organisation technique was proposed. Monte Carlo simulation results show that improvement on SFDR, SNDR are better than capacitor reconfiguring technique, without using the extra capacitor array. We also proved that with the proposed grouping optimisation and strategy optimisation, the performance of the SAR ADC is greatly improved. The proposed technique is a promising calibration technique using on SAR ADC to achieve high linearity hence high resolution digital radiography systems.

APPENDIX
INDEPENDENCY VERIFICATION

We rewrite equation (13) to separate the capacitor terms and the error terms, and transform the right side to matrix

$$G1 - 16C_u = \begin{pmatrix} 1 & 1 & 1 \end{pmatrix} \begin{pmatrix} 16C_u\Delta P_I \\ 16C_u\Delta P_{II} \\ 16C_u\Delta P_{III} \end{pmatrix} \tag{A.1}$$

in which, $16C_u = \frac{G1+G2+G3+G4}{4}$.

And we transform the left side into matrix

$$\frac{1}{4}\begin{pmatrix} 3 & -1 & -1 & -1 \end{pmatrix}\begin{pmatrix} G1 \\ G2 \\ G3 \\ G4 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} 16C_u\Delta P_I \\ 16C_u\Delta P_{II} \\ 16C_u\Delta P_{III} \end{pmatrix} \tag{A.2}$$

Then we apply the same process on the equation (14) to equation (16)

$$\frac{1}{4}\begin{pmatrix} 3 & -1 & -1 & -1 \\ -1 & 3 & -1 & -1 \\ -1 & -1 & 3 & -1 \\ -1 & -1 & -1 & 3 \end{pmatrix}\begin{pmatrix} G1 \\ G2 \\ G3 \\ G4 \end{pmatrix} = \begin{pmatrix} 1 & 1 & 1 \\ 1 & -1 & -1 \\ -1 & 1 & -1 \\ -1 & -1 & 1 \end{pmatrix}\begin{pmatrix} 16C_u\Delta P_I \\ 16C_u\Delta P_{II} \\ 16C_u\Delta P_{III} \end{pmatrix} \tag{A.3}$$

Multiply by the inverse of the coefficient matrix on the right side and we get

$$\frac{1}{4}\begin{pmatrix} 1 & 1 & -1 & -1 \\ 1 & -1 & 1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix}\begin{pmatrix} G1 \\ G2 \\ G3 \\ G4 \end{pmatrix} = I\begin{pmatrix} 16C_u\Delta P_I \\ 16C_u\Delta P_{II} \\ 16C_u\Delta P_{III} \end{pmatrix} \tag{A.4}$$

The G1, G2, G3 and G4 are four independent identically distributed variables. Given the $cov(Gx, Gy) = 0$ when $x \neq y$ and $cov(Gx, Gy) = D$ when $x = y$, and D is the variance of G1, G2, G3 or G4 (they have the same variance), the covariance can be easily computed by doing cross-product on the coefficient vectors of the three error terms in equation (A.4). It turns out that the cross-product of any two coefficient vectors are zero. Thus the independence has been verified.

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