A Digital Self-Calibration Algorithm for ADCs Based on Histogram Test Using Low-Linearity Input Signals

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Abstract—**This paper describes a test-based digital self-calibration algorithm for high-resolution ADCs. The algorithm uses low-linearity signals, small number of memory cells, and simple computations in code-density test to characterize an ADC's nonlinearity, determines corresponding correction codes, and digitally calibrates the ADC's output. Simulation results show that INL_k's of a 16-bit ADC can be tested to 1-LSB accuracy by using 7-bit linear ramp signals and 256 histogram counts. Linearity of the ADC can be improved from 12-bit to 14-bit by using 256 correction codes. The proposed algorithm provides a promising solution to on-chip calibration of high-speed high-precision ADCs.**

I. Introduction

The analog-to-digital converter (ADC) is identified as one of the system drivers for mixed-signal chip design by the *International Technology Roadmap for Semiconductors* [1], since the ADC is an interface between the digital processing systems and the analog world. Digital calibration of ADCs has been studied for over a decade to improve the precision of ADCs, because of its simple circuit architecture, low computational complexity, and small hardware consumption. Karanicolas, Lee, and Bacrania proposed a self-calibration algorithm for pipelined ADCs in 1993 [2]. Erdogan, Hurst, and Lewis reported a digitally-calibrated algorithmic ADC in 1999 [3]. Because of the page limit, only a very small number of representative works are listed here. There are actually much more good exercises. These works corrected distinct errors and improved the linearity of ADCs with different architectures. However, there is not much industry adoption of self-calibration algorithms in high-performance commercial ADCs. Most of the existing algorithms specify the ADC architecture and calibrate individual circuit errors. They may not guarantee after-calibration performance, since errors other than the types considered in the algorithms can also have negative effects on ADC linearity, especially significant for high-precision ADCs. These drawbacks limit the usage of the algorithms on ADCs.

Authors of this work are proposing test-based calibration algorithms that are independent of specific ADC structures and blindly correct different kinds of circuit errors. A code-density test approach developed in authors' previous work achieved very high accuracy in precision ADC test by using low-linearity signals that can be easily generated on chip [4]. The accurately tested ADC nonlinearity can be converted and used to calibrate an ADC's output. However, this algorithm is intended for full-code production test and requires about 2^{n+1} memory cells and a comparable amount of computations for testing an n-bit ADC. The hardware requirement and computational complexity are too much for self-calibration of stand-alone ADC products.

This work introduces a practical test-based calibration strategy for high-resolution ADCs. This strategy preserves the beneficiary characteristic of the above mentioned algorithm that utilizes easy-to-generate signals in ADC test, but only requires a much smaller number of memory cells and computations in ADC characterization. Using the precision test results, the proposed algorithm can correct different types of linear and nonlinear errors in an ADC and achieve high ADC linearity after calibration. Simulation results show that by using 256 histogram counts and some low complexity computations, INL_k test errors of a 16-bit ADC can be limited to 1 LSB when a 7-bit linear signal is used, and the ADC's linearity can be improved from 12-bit to 14-bit after applying digital-calibration that uses 256 correction codes.

The rest of the paper is organized as follows. Section II will review the testing strategy using low-precision signals. The calibration algorithm that uses small circuits and simple computations will be described in Section III. Some simulation results will be presented in Section IV. Section V will evaluate the algorithm and conclude the paper.

II. Review of an ADC Test Strategy that Uses Low-Linearity Stimulus Signals

The stimulus error identification and removal (SEIR) algorithm developed in [4] uses nonlinear ramp signals to test the integral and differential nonlinearity (*INL and DNL)* of high-resolution ADCs. Conceptually, it takes following steps to test an n-bit ADC by applying the SEIR algorithm.

1) Generate a ramp and use it to excite the ADC;
2) Collect 2^n histogram counts, $H_{k,1}$, for the ramp signal;

This work is supported by the Semiconductor Research Corporation.

0-7803-8834-8/05/$20.00 ©2005 IEEE

3) Generate the same ramp, shift it by a constant offset, and use the shifted ramp to excite the ADC;

4) Collect a second set of 2^n histogram counts, $H_{k,2}$, for the second ramp signal;

5) Generate two estimates for each of the 2^n ADC transition points, T_k, using M parameters, a_j, that characterizes input nonlinearity;

6) Use the least squares (LS) method to identify the M parameters by minimizing the difference between the estimates associated with the same transition point;

7) Estimate T_k by using the identified input nonlinearity;

8) Identify ADC's linearity performance based on the transition point estimation.

These steps are summarized in Figure 1, where a 14-bit ADC is under test by using 16 parameters for input nonlinearity identification.

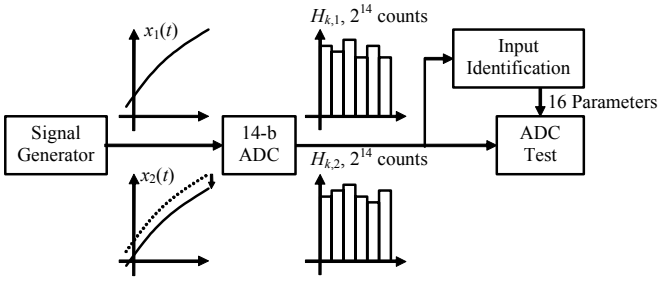


Figure 1. Test of a 14-b ADC using SEIR algorithm.

The SEIR algorithm can provide very accurate test results of ADC nonlinearity, comparable to results of conventional code-density test approaches that use highly linear signals to generate the histogram data. Distinct from conventional approaches, the SEIR algorithm dramatically relaxed the linearity requirement on the input signals used in ADC test, which makes on-chip generation of the signals become possible. The approach is promising for either built-in self-test or production test of precision ADCs. The SEIR algorithm requires 2^{n+1} memory cells for storing the histogram data to estimate 2^{n+1} INL_k and DNL_k parameters. This storage requirement is necessary and acceptable for a full code test. The total computational complexity of steps from 5) to 8) is at the level of $O(M*2^{n+1})$. Experimental results show that computation time is much smaller than data acquisition time when the algorithm is implemented on a PC, which is fast enough for production test. However, the memory requirement and computational complexity are not acceptable for on-chip implementations. A test approach that requires much less hardware and computation overhead is necessary to enable integrated designs of self-test and calibration for high-resolution ADCs.

III. A Test-Based Self-Calibration Algorithm for High-Performance ADCs

This work is proposing a test-based calibration algorithm for high-resolution ADCs that utilizes low-linearity ramp signals in test and requires a very small amount of memories and computations for ADC identification and calibration. The calibration scheme consists of input identification, ADC characterization, correction code generation and output code calibration. Since low-linearity ramps signals are used in test, the algorithm will first identify the ramp nonlinearity and use it to estimate errors of an ADC under test. Appropriate correction codes will be generated based on the estimated ADC errors and used to calibrate output codes of the ADC, eliminate the error effects, and improve an ADC's linearity.

A. Input Nonlinearity Identification

It's assumed in the SEIR algorithm, and easy to guarantee, that ramp signals used in test have only low frequency nonlinearity so that they can be accurately characterized by a small number of variables. For the example of 14-bit ADC test as shown in Figure 1, 16 variables are used to parameterize the input nonlinearity. Theoretically, 16 independent equations are sufficient to determine these variables, but more equations are usually required to average out the noise effect. Two estimates, from two test signals, for one transition point of the ADC under test can provide an equation of the 16 variables characterizing the input nonlinearity. There are totally 2^n such equations for an n-bit ADC and all of them were used in the SEIR algorithm to give an LS estimation of the 16 parameters. The estimation error in the SEIR algorithm is extremely small because of the huge number of equations. Tens of well selected equations, however, can also provide estimation results of input nonlinearity that are sufficiently precise for testing high-resolution ADCs. Intuitively a set of equations evenly spaced over the ADC input range can give good estimation accuracy. The proposed calibration approach uses equations at the major transition points associated with the first 7 MSB digits of the ADC's output codes to test input nonlinearity, so 128 equations will be used to estimate 16 parameters, as shown in Figure 2, in which we use D_0 to notate the MSB and D_{13} to notate the LSB of the ADC output code.

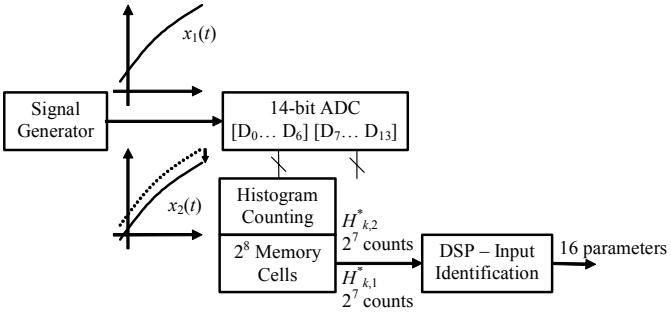


Figure 2. Input nonlinearity identification using the 7-MSB histogram.

In the proposed algorithm, the ADC under test is first used as a 7-bit device to generate two sets of histogram data of the shifted ramp signals. There are 128 code counts, $H^*_{k,1}$ and $H^*_{k,2}$, in each histogram, so totally 256 memory cells are required. Based on the two histogram data, equations can be generated to identify input nonlinearity, which is

parameterized by a_j's. (Construction of the equations and the LS estimation are identical to those in the SEIR algorithm. Please refer to [4] for the detailed algorithm with mathematical derivation and description.) Since the size of the equation set used in estimation is dramatically reduced, the computational complexity of the current algorithm becomes much lower, from dominated by the number of ADC transition levels to be determined by the total number of equations and variables used in input nonlinearity parameterization. The required amount of memory cells and computations are reduced by over 99% for a 14 bit ADC and even more for higher resolutions as compared to the SEIR algorithm.

B. *ADC Characterization and Correction Code Generation*

The ADC will then be tested again by using a third ramp signal generated by the same signal source as in Figure 3.

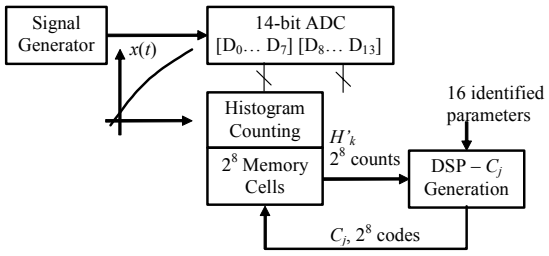


Figure 3. Correction code generation based on 8 MSBs.

We consider an example that the ADC with 6 bit linearity is under test and calibrate the first 8 MSB digits, but this method can be applied likewise to ADCs with less or more intrinsic linearity. Then the ADC is used as an 8-bit device and a histogram of 256 code counts, H'_k, will be saved in the same memory cells used during input identification. The integral nonlinearity of the ADC at 255 major transition points associated with the first 8 MSB digits, INL'_j, can be accurately estimated based on H'_k, when effects of ramp nonlinearity are removed by using the 16 parameter a_j's which are identified earlier. Correction code C_j's can be determined based on the estimated INL'_j as

$$C_j = \begin{cases} round(\hat{INL}'_j / 2) & j = 0; \\ round((\hat{INL}'_{j-1} + \hat{INL}'_j)/2), & j = 1, 2, 3 \ldots 254; \\ round(\hat{INL}'_{j-1} / 2), & j = 255. \end{cases} \quad (1)$$

A correction code C_j will be used to calibrate the ADC's output when the value of an output code's 8 MSB digits is equal to j. Theoretical analyses show that the correction codes picked up in (1) can minimize the errors in transition points of the ADC after calibration.

C. *Output Code Calibration*

When the ADC is quantizing, the output code k will be calibrated by a correction code C_j associated with it. The calibrated output code is

$$D_k = k + C_j, \quad k = 0,1 \ldots 2^n - 1, \quad (2)$$

where j=floor(k/2^{n-8}). To physically implement the digital calibration, the memory cells that save the correction codes need to be addressed by the 8 MSB digits of the ADC's output, so that when an output code k is determined by the un-calibrated structure, an associated correction code C_j will be read out from a specific memory location and added to k, as shown in Figure 4. Because the correction codes are calculated from the estimated INL'_j values, they can effectively eliminate the errors in the ADC's transfer curve and the ADC's linearity performance after calibration can be significantly improved.

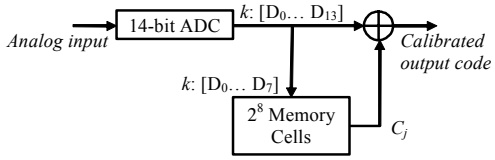


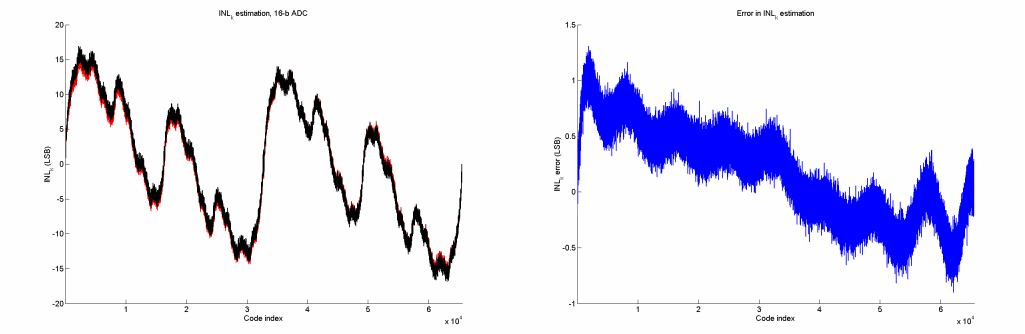
Figure 4. A 14-bit ADC with self calibration based on 8 MSBs.

The proposed test-based calibration algorithm uses nonlinear ramp signals and requires a small amount of hardware, such as 256 memory cells, an adder and some simple logic circuits, to calibrate high-resolution ADCs. The input identification, ADC test, and correction code generation can be done with a cost-effective on-chip DSP circuit because of the low computational complexity. Therefore this algorithm is practical for serving as a self-calibration solution for high-resolution ADCs.

IV. Simulation Results

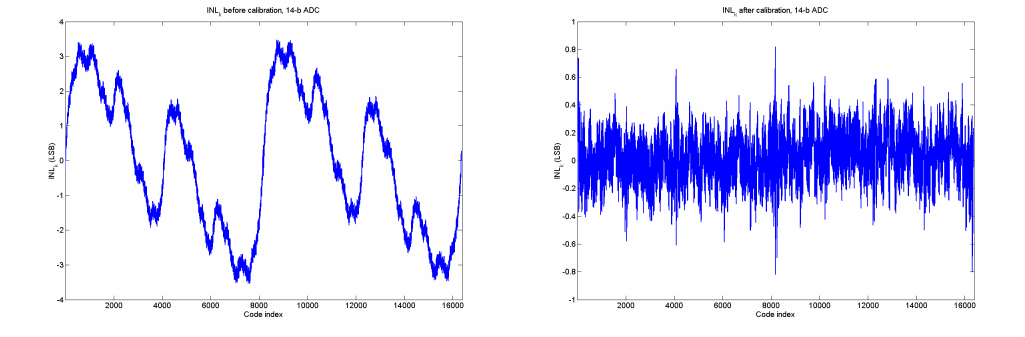
Simulation has been done for both the full-code linearity test and digital calibration based on the proposed algorithm. A 16-bit pipelined ADC is modeled for the purpose of simulation. Different types of errors such as comparator offset, capacitor mismatch, reference voltage errors, and amplifier nonlinearity are included in the ADC modeling. The simulated ADC has about 12 bit linearity and its INL_k is plotted in red in Figure 5 (a). The input ramp signal used in the code-density test has about 7-bit linearity with 2nd and 3rd order nonlinear errors. A noise with a half LSB standard deviation is added at the input to the ADC. Approximately 8 samples are taken for one code bin of the ADC.

In simulation, the input nonlinearity is parameterized by 16 coefficients of sine basis functions. The proposed algorithm estimates the 16 parameters by using 128 equations generated when the ADC is tested as a 7-bit device. By using the identified parameters to do a full-code test of the 16-bit ADC, the estimated INL_k is plotted in black in Figure 5 (a). It can be seen from the figure that the estimated INL_k curve matches very well with the true curve. The error in INL_k estimation is about 1 LSB at 16-bit level as plotted in Figure 5(b). That means the input nonlinearity identified by using 128 equations is sufficiently accurate for testing 16-bit ADCs.



(a) (b)

Figure 5. INL_k estimation for the 16 bit structure.



(a) (b)

Figure 6. INL_k of a 14-bit ADC, before and after calibration using 256 correction codes.

To simulate digital calibration, the INL'_j and 256 correction codes are calculated based on the identified input nonlinearity and added to the ADC output codes as discussed in Section III *B* and *C*. Figure 6 shows the improvement in the linearity performance of the ADC when it is used as a 14-bit device, before and after digital calibration by using the 256 correction codes. The *INL* of the ADC after calibration is less than 1 LSB at the 14-bit level as shown in Figure 6(b), while it's more than 3 LSB without calibration as in Figure 6 (a). The linearity performance of the ADC is improved from 12-bit to 14-bit by using 256 correction codes. A remark is that this 14-bit linearity after calibration is mostly limited by the number of calibration codes, not the original linearity of the ADC. An ADC with 10-bit linearity can also be calibrated to have 14-bit accuracy as well.

V. Conclusions

A practical test-based calibration strategy for precision ADCs is discussed in this work. This strategy preserves the beneficiary characteristic of the previously developed SEIR algorithm that utilizes easy-to-generate signals in ADC test and only requires a very small number of memory cells and computations for input identification, ADC characterization, correction code generation and digital calibration. Details of the proposed strategy are discussed in the paper and the performance of the calibration algorithm is validated in simulation. Simulation results show that by using 128 equations in input identification and 256 correction codes for digital calibration, INL_k's of an ADC can be tested to 1 LSB accuracy at the 16 bit level and its linearity can be improved from 12-bit to 14-bit, when 7-bit linear ramp signals are used in code density test. This calibration algorithm uses low-linearity signals to accurately test high-resolution ADCs. The calibration is based on precision test results so that it is applicable to ADCs of different architectures and can calibrate various kinds of errors. Since the hardware and computational complexity of this algorithm is low, it can be easily integrated on chip. Therefore this algorithm is capable of doing self-calibration for high-performance ADCs.

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