A 130 mW 100 MS/s Pipelined ADC With 69 dB SNDR Enabled by Digital Harmonic Distortion Correction

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***Abstract*—This paper presents a pipelined ADC with two fully integrated digital background calibration techniques: harmonic distortion correction (HDC) to compensate for residue amplifier gain error and nonlinearity and DAC noise cancellation (DNC) to compensate for DAC capacitor mismatches. It is the first IC implementation of HDC, and the results demonstrate that HDC and DNC together facilitate low-voltage operation and enable reductions in power dissipation relative to comparable conventional state-of-the-art pipelined ADCs. The pipelined ADC achieves a peak SNR of 70 dB and a −1 dBFS SFDR of 85 dB at a sample-rate of 100 MHz. It is implemented in a 90 nm CMOS process and consumes 130 mW from 1.2 V and 1.0 V analog and digital power supplies, respectively.**

***Index Terms*—ADC, calibration, digital, mixed signal.**

I. Introduction

PIPELINED ADCs are advantageous and widely used in applications with signal bandwidths that are too high for oversampling delta-sigma ADCs and resolution requirements that are too high for flash ADCs. Nevertheless they are sensitive to distortion introduced by the residue amplifiers in their first few stages, and residue amplifier distortion tends to be inversely related to both power supply voltage and power consumption. Therefore, the residue amplifiers are usually the dominant consumers of power in high-resolution pipelined ADCs, particularly in low supply voltage designs [1]–[6].

Recently, digital calibration techniques that measure and cancel pipelined ADC error arising from distortion introduced by the residue amplifiers have been proposed [7]–[10]. By relaxing the residue amplifier distortion requirement for a given level of ADC accuracy, they offer the potential to significantly reduce power consumption and supply voltage in high-resolution pipelined ADCs. One such technique, harmonic distortion correction (HDC), is applied to the pipelined ADC described in this paper. It enables the ADC to achieve a peak signal to noise and distortion ratio (SNDR) of 70 dB over its 50 MHz Nyquist band despite the use of residue amplifiers with a DC loop gain of only 23 dB and a unity gain bandwidth of 200 MHz.

The pipelined ADC also incorporates a recently proposed digital calibration technique called DAC noise cancellation (DNC) to compensate for error introduced by DAC capacitor mismatches [11]. Together, HDC and DNC enable the pipelined ADC to achieve state of the art power consumption relative to comparable published ADCs despite a low analog power supply voltage of 1.2 V.

The work presented in this paper is the first IC implementation of HDC, so the focus of the paper is to describe the practical implementation issues associated with HDC. The paper consists of four main sections. Section II provides a brief description of the conventional portion of the implemented pipelined ADC, a model for the residue amplifier distortion, and a brief description of the theory underlying HDC. Section III describes the system-level implementation details and issues associated with HDC, Section IV describes the analog circuit implementation details of the pipelined ADC, and Section V presents measurement results.

II. Background Information

A. The Underlying Pipelined ADC Architecture

A conventional six-stage 14-b pipelined ADC architecture is shown in Fig. 1. Each stage except the last consists of a 9-level flash ADC, a 9-level DAC, and a *residue amplifier* with an ideal gain of 4. The last stage is just a 17-level flash ADC. This structure is well known in literature and it is described below using the same notation as in [8].

Each 9-level flash ADC ideally behaves as a uniform quantizer with quantization step of size Δ and input range extending from -4.5Δ to 4.5Δ. In this design, the nominal value of Δ is 170 mV. The output of the kth flash ADC at the nth sample time is given by

$$x_k[n] = v_{\text{in},k}(nT_S) + e_{\text{ADC},k}[n] \tag{1}$$

where $v_{\text{in},k}(nT_S)$ is the flash ADC input signal, T_S is the sample interval, and $e_{\text{ADC},k}[n]$ is the error introduced by the flash ADC, i.e., the output minus the input of the flash ADC with the least significant bit (LSB) of the flash ADC output taken to have a weight of Δ. It is customary to refer to $e_{\text{ADC},k}[n]$ as quantization error although in practice it contains both error arising from quantization as well as error arising from non-ideal circuit behavior such as comparator offset voltages. In the absence of non-ideal circuit behavior it is bounded in magnitude by $\Delta/2$.

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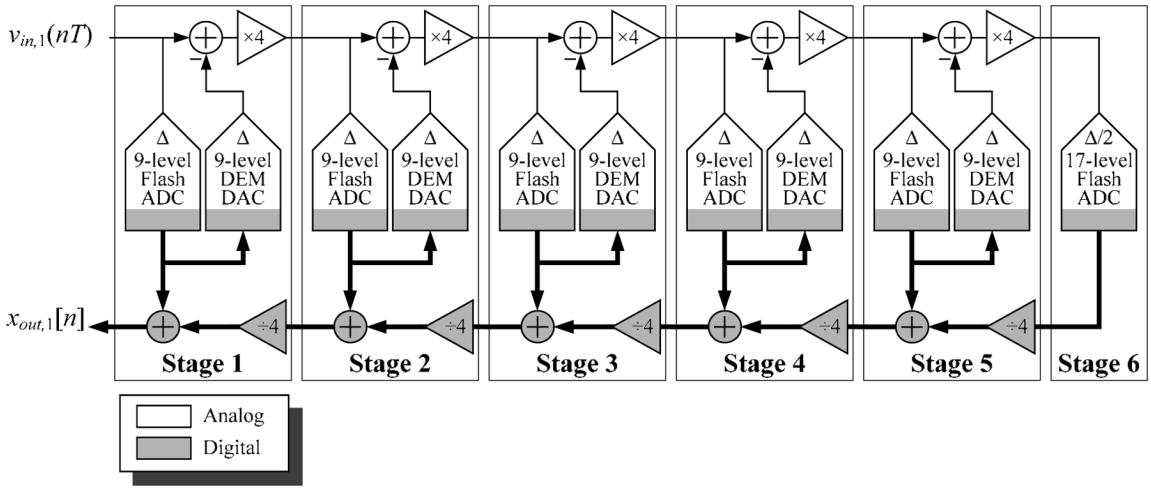

Fig. 1. Block diagram of a 14-b pipelined ADC.

The 9-level DAC converts the output of the flash ADC into analog format. The difference between the pipelined ADC input sample and the output of the DAC, called the *residue*, is amplified by the residue amplifier and the result is fed to the next pipeline stage.

It follows from (1) that in the absence of non-ideal circuit behavior, the input to and output of the kth residue amplifier at the nth sample time are

$$v_k(nT_S) = -e_{\mathrm{ADC},k}[n], \quad \text{and} \quad v_{\mathrm{in},k+1}(nT_S) = 4v_k(nT_S) \tag{2}$$

respectively. In this case the output of the kth residue amplifier is bounded between -2Δ and 2Δ, whereas the input range of the subsequent stage to which it is applied extends from -4.5Δ to 4.5Δ. The extra input range is called *over range margin*. Its purpose is to accommodate error from non-ideal circuit behavior such as flash ADC threshold deviations.

As indicated in Fig. 2, the output of the divide-by-four block in the kth pipeline stage, referred to as the stage's *digitized residue*, can be written as $r_k[n] = (r_{k+1}[n] + x_{k+1}[n])/4$. Therefore, it follows from (1) and (2) that the output of the kth stage can be written as

$$\begin{aligned} x_{\mathrm{out,k}}[n] &= x_k[n] + r_k[n] \\ &= v_{\mathrm{in},k}(nT_S) + \frac{e_{\mathrm{ADC,k+1}}[n]}{4} + r_{k+1}[n] \end{aligned} \tag{3}$$

where $k = 1, 2, \ldots, 5$, and $r_6[n] = 0$. Recursive application of (1) and (2) in (3) gives

$$x_{\mathrm{out},k}[n] = v_{\mathrm{in},k}(nT_S) + \frac{1}{4^{6-k}} e_{\mathrm{ADC},6}[n]. \tag{4}$$

This implies that for each k, stages k through 6 together behave as a (16–2 k)-b ADC. For example, stages 2 through 6 together behave as a 12-b ADC.

B. The Residue Amplifier Distortion Problem

The residue amplifier is usually implemented as an op-amp in a switched capacitor feedback loop [1]–[6], [10], [12], [17], [20], [24], [25]. When op-amp hard nonlinearities caused by effects like slew rate limiting or clipping are negligible, the residue amplifier tends to be well modeled as a memoryless, weakly nonlinear function of the amplifier's input voltage, as shown in Fig. 3, with

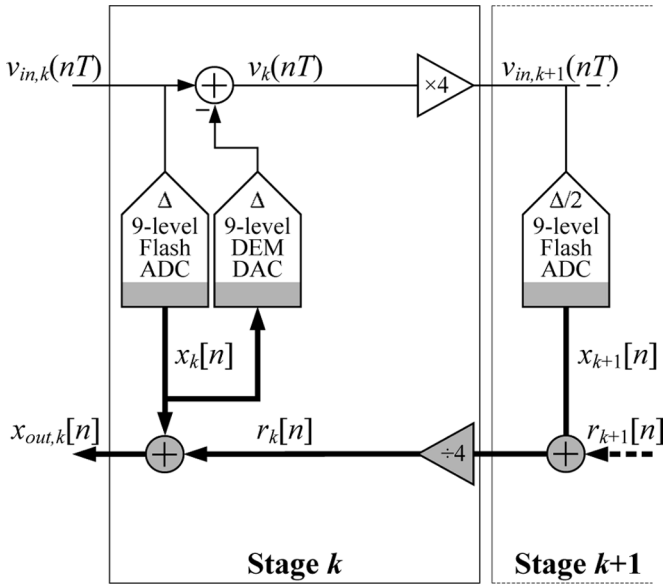

Fig. 2. Pipeline stages k and $k+1$.

$$f(v) = \sum_{i=1}^{N} \alpha_i v^i \tag{5}$$

where α_1 is a linear gain error coefficient and α_i for $i > 1$ are nonlinear distortion coefficients.

Fig. 4 shows a simplified representation of the pipelined ADC that includes the effect of op-amp nonlinearity in the first stage. Applying the same reasoning used above to obtain (4), it follows that

$$\begin{aligned} x_{\mathrm{out},1}[n] &= x_{\mathrm{out},1}[n]|_{\mathrm{ideal}} + f\left(v_1(nT_S)\right) \\ &= v_{\mathrm{in},1}(nT_S) + \frac{1}{4^5} e_{\mathrm{ADC},6}[n] + f\left(v_1(nT_S)\right) \end{aligned} \tag{6}$$

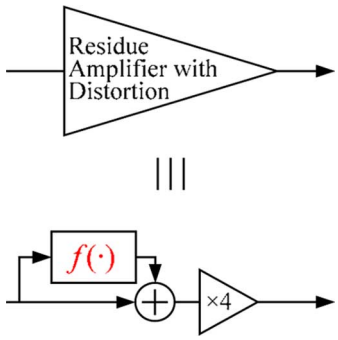

Fig. 3. Model of the residue amplifier with distortion.

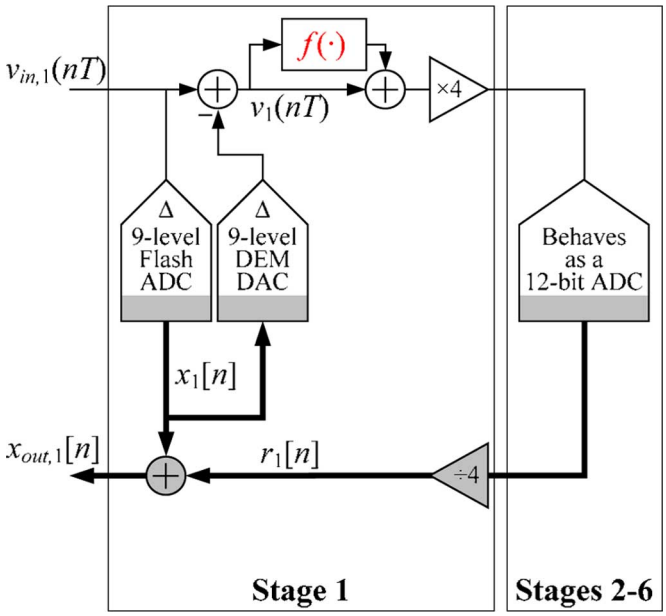

Fig. 4. Simplified representation of the 14-b pipelined ADC including distortion from the residue amplifier.

where in the last expression $x_{\text{out},1}[n]|_{\text{ideal}}$ has been replaced by (4) with $k = 1$. Therefore, the $f(v_1(nT_S))$ term appears in the output of the pipelined ADC. Furthermore, it follows from (2) that the $f(v_1(nT_S))$ term is a function of the quantization noise from the flash ADC in Stage 1 which is a nonlinear function of the input signal.

The conventional way to address this problem is to rely on feedback to suppress the residue amplifier distortion: the higher the gain and bandwidth of the op-amp, the better the suppression. Therefore, in a conventional pipelined ADC design, the magnitudes of the α_i coefficients in f are reduced to the point that f has negligible effect on the digital output signal. Unfortunately, this is usually done at the expense of increased power consumption and circuit area.

C. HDC Overview

The alternative approach taken in this design is to use op-amps with larger magnitudes of the α_i coefficients in f, in return for lower op-amp power and area consumption, and then digitally estimate and cancel the resulting nonlinear distortion in the pipelined ADC output via HDC.

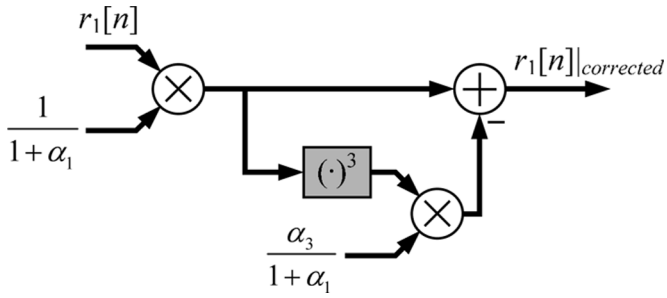

Fig. 5. Correction of the distortion in the digitized residue.

As described in Section IV, the op-amp used in this design has an open loop DC gain of 43 dB which translates into a residue amplifier DC loop gain of 23 dB. Transistor level simulations under typical conditions indicate that the residue amplifier is well-modeled as shown in Fig. 3 with $\alpha_1 = -0.06$, $\alpha_2 = 0$, $\alpha_3 = -0.3\,\text{V}^{-2}$, $\alpha_5 = -2\,\text{V}^{-4}$ and $\alpha_i = 0$ for $i > 5$. Without HDC, the resulting -1 dBFS signal-to-noise and distortion ratio (SNDR) for the pipelined ADC would be 43 dB, which is 26 dB below the target specification.

Extensive circuit simulations run during the design phase of the pipelined ADC IC further indicate that only the distortion introduced by α_1 and α_3 must be corrected to achieve the 70 dB SNDR target specification. The magnitudes of α_i for even values of i are negligible because of the differential circuitry used throughout the ADC, and magnitudes of α_i for odd values of $i \geq 5$ are negligible because hard nonlinearities such as slew rate limiting in the op-amps are small. Therefore, HDC is configured in this work to compensate only for residue amplifier distortion associated with α_1 and α_3.

A full description of the theory behind HDC is presented in [8]. The purpose of this section is to provide a brief overview of HDC with enough information to support the subsequent description of its application to the pipelined ADC prototype.

HDC can be applied to each stage of a pipelined ADC to compensate for the distortion introduced by that stage's residue amplifier. In each stage it consists of an *estimation* portion and a *correction* portion. The former estimates the α_i coefficients in (5) for that stage's residue amplifier, and the latter uses the estimates to compensate for the distortion. In the following, the correction portion is described prior to the estimation portion, both in the context of HDC applied to the first pipeline stage.

1) Correction Portion of HDC: Neglecting the quantization error $e_{\text{ADC},6}[n]$ and assuming ideal behavior of the stages 2–6, $r_1[n]$ can be expressed as

$$r_1[n] \simeq v_1(nT_S) + \underbrace{\alpha_1 \cdot v_1(nT_S) + \alpha_3 \cdot v_1^3(nT_S)}_{f(v_1(nT_S))}. \quad (7)$$

Fig. 5 shows the proposed correction method, which implements:

$$\begin{aligned} r_1[n]|_{\text{corrected}} &= \frac{r_1[n]}{1+\alpha_1} - \frac{\alpha_3}{(1+\alpha_1)^4}(r_1[n])^3 \\ &\simeq v_1(nT_S) \\ &\quad + \text{terms with fifth and higher order.} \end{aligned} \quad (8)$$

As detailed in [8], the correction process introduces fifth and higher order distortion terms in $r_1[n]|_{\text{corrected}}$, but they can be neglected because the power of the error they introduce in the pipelined ADC output is much lower than the target noise floor.

2) Estimation Portion of HDC: A digital calibration sequence, $c[n]$, is added to the output of the flash ADC as shown in Fig. 6 to enable estimation of the α_1 and α_3 coefficients associated with the residue amplifier in the first pipeline stage. As indicated in the figure, $c[n]$ is converted to analog form by the DAC, so it is subtracted from the input of the residue amplifier. This causes several extra terms related to $c[n]$ to appear as components in the digitized residue. Two of the extra terms are proportional to $\alpha_1 c[n]$ and $\alpha_3(c[n])^3$, and the HDC estimation algorithm uses these terms to estimate the α_1 and α_3 coefficients.

HDC is a background calibration technique so it must estimate the α_1 and α_3 coefficients during normal operation of the ADC. Therefore, $c[n]$ must be such that the terms proportional to $\alpha_1 c[n]$ and $\alpha_3(c[n])^3$ can be measured in the digital residue even in the presence of other, potentially much larger and unknown terms related to the pipelined ADC input signal. Furthermore, it must have a relatively small magnitude so it only occupies a portion of the over range margin of the subsequent pipeline stage.

The simplest known calibration sequence with these properties is a four-level sequence of the form $c[n] = t_1[n] + t_2[n] + t_3[n]$, where the three $t_i[n]$ sequences are 2-level, independent, zero-mean pseudo-random sequences that take on values of $\pm A$ (in this design $A = \Delta/16$). For example, with this calibration sequence the $\alpha_3(c[n])^3$ term in the digitized residue contains the term $6\alpha_3 t_1[n]t_2[n]t_3[n]$. Since $t_1[n]t_2[n]t_3[n]$ is a known, 2-level, zero-mean pseudorandom sequence that takes on values of $\pm A^3$ and is uncorrelated with all the other signal components in the digitized residue, it follows that the average of the product of the digitized residue and $t_1[n]t_2[n]t_3[n]$ converges to $6A^6\alpha_3$ regardless of the input signal to the pipelined ADC.

The HDC algorithm calculates the following correlations:

$$\begin{aligned}\gamma_1 &= -\frac{1}{A^2 P}\sum_{n=0}^{P-1} s_1[n]t_1[n]\\ \gamma_3 &= -\frac{1}{6A^6 P}\sum_{n=0}^{P-1} s_1[n]t_1[n]t_2[n]t_3[n]\\ \eta_2 &= \frac{1}{P}\sum_{n=0}^{P-1} s_1^2[n]\end{aligned} \tag{9}$$

where $s_1[n] = r_1[n] + c[n]$ and P is the number of samples averaged (e.g., $P = 2^{32}$ was used for most of the measurement results presented in Section V). It can be verified that, provided the residue amplifier is the only significant source of nonlinearity in the system, these correlations converge to

$$\begin{aligned}\gamma_1 &= \alpha_1 + \left(7A^2 + 3\left\langle e_{\text{ADC},1}^2[n]\right\rangle\right)\alpha_3,\\ \gamma_3 &= \alpha_3, \text{ and } \eta_2 \sim \left\langle e_{\text{ADC},1}^2[n]\right\rangle\end{aligned} \tag{10}$$

in the limit as $P \longrightarrow \infty$ regardless of the input to the pipelined ADC, where $\langle\cdot\rangle$ indicates the infinite time average operation.

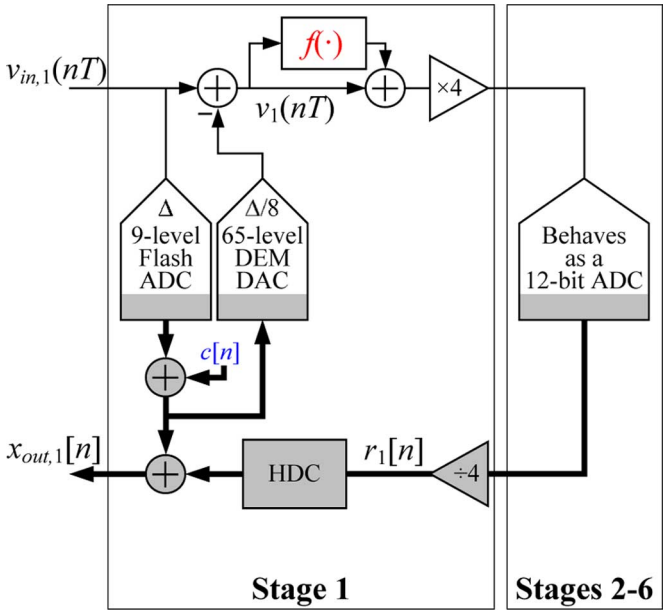

Fig. 6. Simplified representation of a 14-b pipelined ADC with HDC applied to the first pipeline stage.

The HDC algorithm uses these correlation values to calculate the coefficients required by (8) as follows:

$$\begin{aligned}\frac{1}{1+\alpha_1} &= \frac{1}{1+\gamma_1-(7A^2+3\eta_2)\gamma_3}\\ \frac{\alpha_3}{1+\alpha_1} &= \frac{\gamma_3}{1+\gamma_1-(7A^2+3\eta_2)\gamma_3}.\end{aligned} \tag{11}$$

It follows from (10) that γ_3 is an unbiased estimate of α_3, whereas γ_1 is an estimate of α_1 that is biased by α_3. Therefore, accurate estimation of α_1 requires knowledge of α_3. Unlike HDC, the gain error correction (GEC) technique presented in [12] calculates the equivalent of γ_1 and uses it as an estimate of α_1 directly, so it implicitly assumes that α_3 is negligible. Consequently, highly linear residue amplification is a prerequisite for GEC to function properly.

Simulation results under the typical conditions described in Section II-B indicate that if the HDC correction is performed as indicated in Fig. 5 except with α_3 set to zero, then the SNDR and SFDR decrease by 1.7 dB and 3 dB, respectively. However, if HDC correction is performed as indicated in Fig. 5 except with γ_3 set to zero in (11), which is equivalent to the correction performed by GEC, then the SNDR and SFDR drop by about 7 dB and 13 dB, respectively.

III. Digital Calibration System-Level Details

A. Required Analog Enhancements for HDC

Most of the enhancements required to implement HDC in a pipelined ADC stage are digital. The only exception is that the DAC must be modified as described in this section. To simplify the notation, the description is in the context of HDC applied to first stage.

The calibration signal, $c[n]$, described above takes on values of $-3\Delta/16$, $-\Delta/16$, $\Delta/16$, and $3\Delta/16$ and the output of the flash ADC, $x_1[n]$, takes on values of -4Δ, -3Δ,

$-2\Delta, \ldots, 3\Delta$, and 4Δ, so a 69-level DAC with step size of $\Delta/8$ is required to represent the signal $x_1[n] + c[n]$. Although a 69-level DAC could be implemented, as explained later it is more convenient to implement a 65-level DAC. Therefore, a 65-level DAC has been implemented in this design. To ensure that $x_1[n] + c[n]$ stays within the 65 level range of the DAC, the addition of $c[n]$ is disabled when $x_1[n] = \pm 4\Delta$, i.e., when the input to the flash ADC has a magnitude between 3.5Δ and 4.5Δ.[1]

A 65-level DAC can be implemented by adding the outputs of 64 unity-weighted 1-b DACs. In absence of mismatches among the 1-b DACs, the output of the DAC would be $y[n] = x_1[n] + c[n]$. Unfortunately, mismatches among the 1-b DACs inevitably introduced during fabrication cause the output of the DAC to be

$$y[n] = \alpha_{DAC}\,(x_1[n] + c[n]) + \beta_{DAC} + e_{DAC}[n] \qquad (12)$$

where α_{DAC} is a constant gain, β_{DAC} is a constant offset, and $e_{DAC}[n]$ is non-constant error referred to as *DAC noise* [11]. If each possible value of $x_1[n] + c[n]$ is mapped to a unique set of input bits to the 64 1-b DACs, then $e_{DAC}[n]$ is a deterministic nonlinear function of the flash ADC output signal, in which case the DAC is a source of nonlinear distortion.

Dynamic element matching (DEM) is used in this design to eliminate the DAC as a significant source of nonlinear distortion. The idea behind DEM is that for most values of $x_1[n] + c[n]$, there are multiple ways to set the input bits of the 1-b DACs that would yield $y[n] = x_1[n] + c[n]$ in the absence of mismatches among the 1-b DACs. A *DEM encoder* prior to the 1-b DACs pseudo-randomly selects one of these valid sets of input bits each sample period, in such a way that $e_{DAC}[n]$ has zero mean and is uncorrelated with $x_1[n] + c[n]$.

In a pipeline stage, the propagation delay between the output of the Flash ADC and the output of the DEM encoder must be minimized, because it reduces the time available for the sampling phase or the amplification phase of the stage. Reducing the time for the sampling phase reduces the pipelined ADC's input signal bandwidth, whereas reducing the time for the amplification phase reduces the settling time available for the op-amp. In this implementation, the time allocated for the propagation delay is about 300 ps.

One way to achieve this target propagation delay is to use two layers of parallel transmission gates (T-gates). The first layer of $4 \times 64 = 256$ T-gates would compute the sum $x_1[n]$ and $c[n]$, and the second layer of $64^2 = 4096$ T-gates would implement the DEM encoder. Unfortunately this solution requires 4352 T-gates with an estimated area of 60,000 μm^2 not including the overhead due to routing. Therefore, this strategy was considered impractical.

Instead the segmented DEM DAC shown in Fig. 7 has been implemented. The structure has 14 1-b DACs, 8 with weight Δ, 2 with weight $\Delta/2$, 2 with weight $\Delta/4$ and 2 with weight $\Delta/8$. As quantified below, the benefit of this structure is that the DEM encoder can be implemented with much lower circuit area than the DEM encoder mentioned above. However, as explained in [13], a fundamental limitation of segmented DEM DACs is that to achieve the desired $e_{DAC}[n]$ properties they must limit the range of their input sequences to less than the total possible output range of their 1-b DACs. In this case, the input bits of the 1-b DACs shown in Fig. 7 could be set to achieve any of 79 output levels, but the DEM encoder is only able to achieve the desired $e_{DAC}[n]$ properties if it limits the range of the DAC to 65 levels. Therefore, the segmented DEM DAC requires 22% more capacitance in its set of 1-b DACs than would be required in a comparable DEM DAC with 64 unity-weighted 1-b DACs. Furthermore, the extra capacitance introduces a 0.5 dB increase in KT/C noise. Nevertheless, these drawbacks are considered worthwhile tradeoffs for the reduction in DEM encoder complexity.

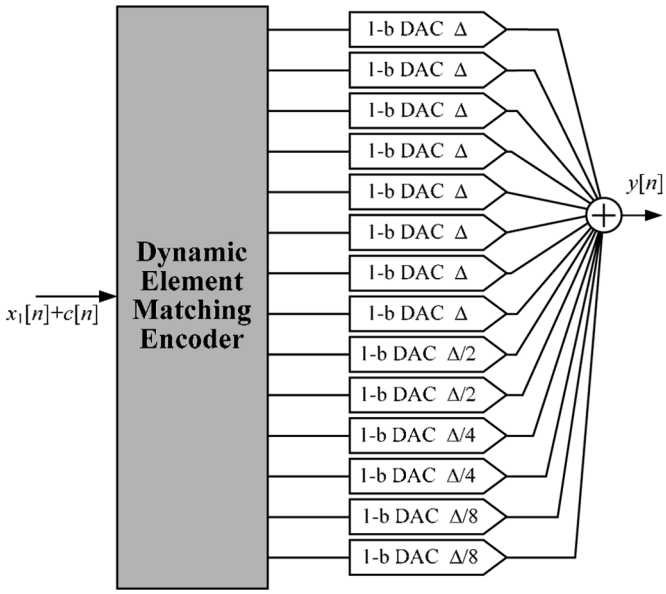

Fig. 7. Simplified block diagram of the implemented segmented DEM DAC.

The signal processing performed by the DEM encoder is that of the segmented tree-structured DEM encoder shown in Fig. 8 with an input sequence given by[2]

$$c_{6,1}[n] = 8 \cdot \frac{x_1[n] + \left(c[n] - \frac{\Delta}{16}\right)}{\Delta} + 39. \qquad (13)$$

The DEM encoder is similar to that presented in [13], [14][3]. It consists of 13 digital *switching blocks*. Switching blocks $S_{6,1}$, $S_{5,1}$, and $S_{4,1}$, are called *segmenting switching blocks* and the remaining switching blocks are called *non-segmenting switching blocks*. Each switching block calculates its two output sequences as a function of its input sequence and one of 13 pseudo-random 1-b sequences, $d_{k,r}[n]$, $k = 1, 2, \ldots, 6$, and $r = 1, 2, \ldots, 6$, and 7. The $d_{k,r}[n]$ sequences are designed to

[1]Disabling the addition of $c[n]$ may also slow down the convergence of the HDC algorithm, because the samples for which $c[n]$ is disabled are not used in the correlation processes described by (9). For example, a sinusoid with a full-scale amplitude of 4.5Δ would cause the addition of $c[n]$ to be disabled 43% of the time. No reduction in convergence time occurs for signals with magnitudes below 3.5Δ.

[2]The use of notation $c_{k,r}[n]$ for the DEM encoder signals has been chosen to align with [13], [14] ($c_{k,r}[n]$ should not be confused with the calibration sequence $c[n]$).

[3]A 69-level version of the DEM DAC could have been implemented by combining the techniques presented in [13] and [15], but it would have been more complex.

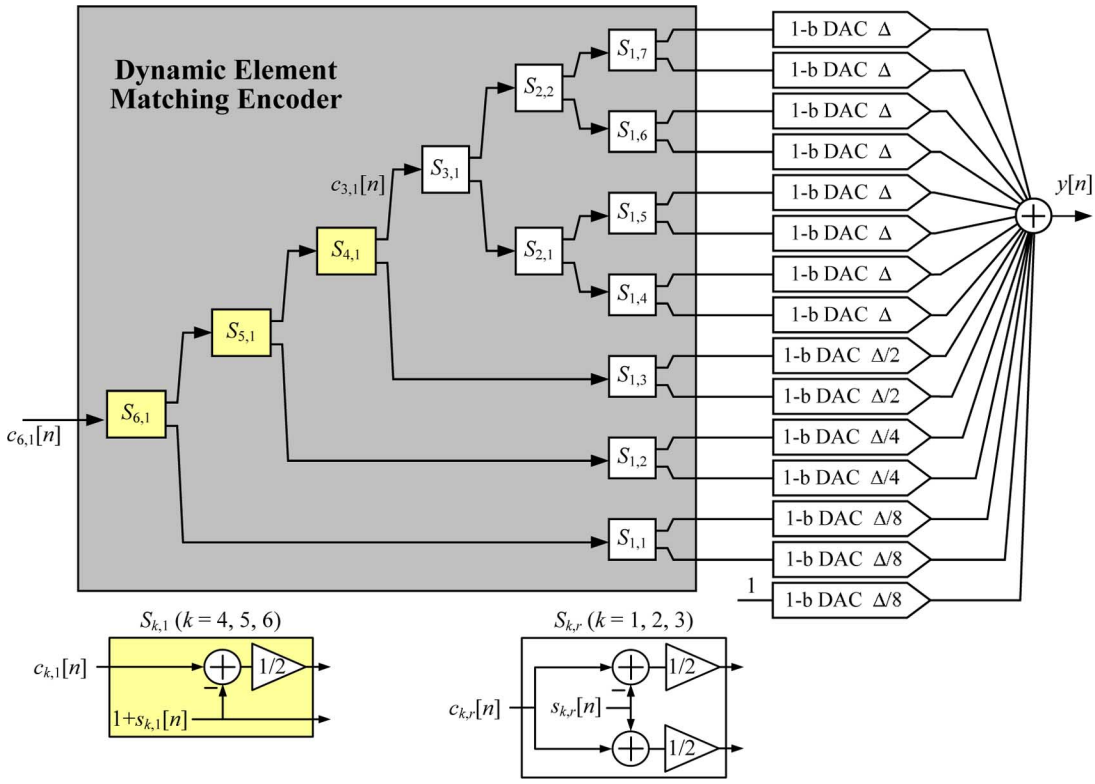

Fig. 8. 65-level segmented DAC with DEM encoder.

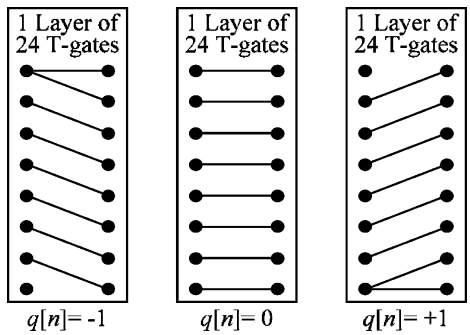

Fig. 9. The three configurations of the first layer of T-gates (only ON switches are shown).

well-approximate white random sequences that are independent from each other and $x[n]$, and each take on values of 0 and 1 with equal probability. The switching blocks function as shown in Fig. 8 with

$$s_{k,1}[n] = \begin{cases} 0, & \text{if } c_{k,1}[n] = odd, \\ 1, & \text{if } c_{k,1}[n] = even, d_{k,1}[n] = 1, \\ -1 & \text{if } c_{k,1}[n] = even, d_{k,1}[n] = 0. \end{cases} \quad (14)$$

for $k = 4$, 5, and 6, and

$$s_{k,r}[n] = \begin{cases} 0, & \text{if } c_{k,r}[n] = even, \\ 1, & \text{if } c_{k,r}[n] = odd, d_{k,r}[n] = 1, \\ -1 & \text{if } c_{k,r}[n] = odd, d_{k,r}[n] = 0. \end{cases} \quad (15)$$

for $k = 1$, 2, and 3, and $r = 1, 2 \ldots, 6,$ and 7.

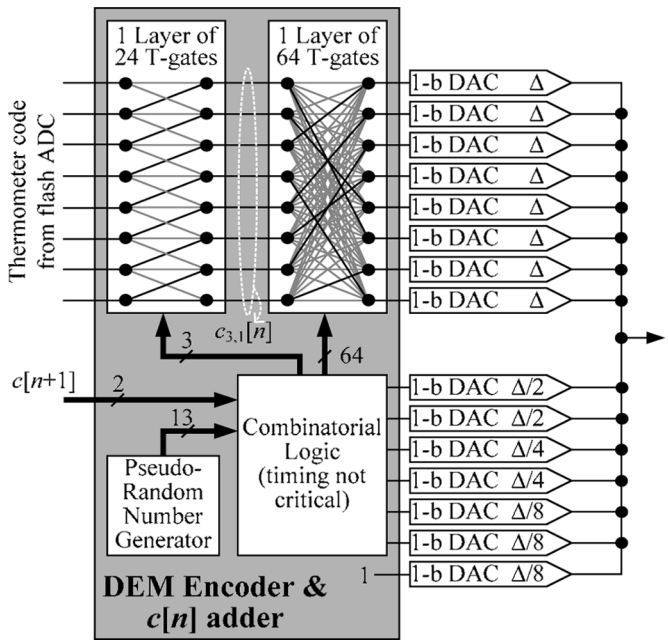

Fig. 10. Implementation of the DEM encoder and $c[n]$ adder.

In this design, the addition of $x_1[n]$ and $c[n]$ and the functionality of the segmented DEM encoder described above are implemented such that all time-critical operations are performed by a layer of 24 parallel T-gates followed by a layer of 64 parallel T-gates. Therefore, the total propagation time is equal to that of 2 cascaded T-gates. The way this is achieved is explained below.

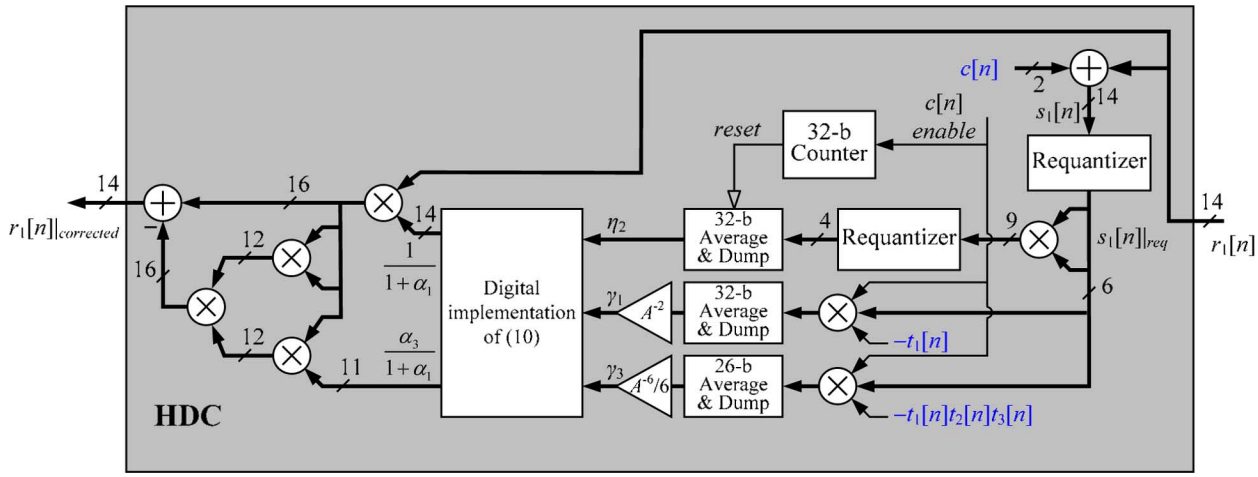

Fig. 11. Block diagram of the HDC logic in the first pipeline stage.

Note from (13) and (14) that the amplitude of $s_{6,1}[n]$ is chosen depending upon the parity of $c_{6,1}[n]$, which in turn depends only on $c[n]$. Therefore, the calculations performed by switching block $S_{6,1}$ do not involve the output of the flash ADC, $x_1[n]$, so they can be performed before $x_1[n]$ is available. Similar reasoning applies to switching blocks $S_{5,1}$, $S_{4,1}$, $S_{1,1}$, $S_{1,2}$, and $S_{1,3}$. Therefore, the input bits to the bottom 6 1-b DACs in Fig. 8 can be computed before the Flash ADC output is available.

By similar reasoning it can be verified that the upper output of $S_{4,1}$ is

$$c_{3,1}[n] = \frac{x_1[n]}{\Delta + 4 + q[n]} \tag{16}$$

where $q[n]$ is a function of $c[n]$, $s_{6,1}[n]$, $s_{5,1}[n]$, and $s_{4,1}[n]$, and can take on values of only -1, 0, and 1. A low-latency implementation of (16) is achieved by combining 24 parallel T-gates that can implement the three input-output connection configurations shown in Fig. 9. In this design $x_1[n]/\Delta + 4$ can take on values of $0, 1, 2, \ldots, 7$, and 8 and is provided by the flash ADC in the form of a thermometer code. Therefore, the mapping shown in Fig. 9 results in a thermometer code representation of $x_1[n]/\Delta + 4 + q[n]$. Since $q[n]$ is known before the flash ADC output is ready, the T-gate configuration is selected in advance, thereby minimizing latency.

Fig. 10 shows the implementation of the combined $x_1[n]+c[n]$ summer and the segmented DEM encoder. The first layer of 24 T-gates implements (16) as described above, and the second layer of 64 T-gates maps the combined operation of $S_{3,1}$, $S_{2,1}$, $S_{2,2}$, $S_{1,4}$, $S_{1,5}$, $S_{1,6}$, $S_{1,7}$. As demonstrated in [11] and [12] the configuration of such T-gates does not depend on the signal $c_{3,1}[n]$, so it is selected in advance. Standard logic is used to realize all components for which the timing is not critical. These components include the pseudo-random number generator (PRNG), switching blocks $S_{6,1}$, $S_{5,1}$, $S_{4,1}$, $S_{1,1}$, $S_{1,2}$, and $S_{1,3}$, and all the circuitry that drives the T-gates.

As described above, when $x_1[n] = \pm 4\Delta$ the addition of $c[n]$ must be disabled. To do this with minimal latency, the inputs to the bottom six 1-b DACs in Fig. 7 are computed for both cases (addition of $c[n]$ enabled and disabled) and then the correct choice is selected by a multiplexer. For the upper 8 1-b DACs, the T-gates in the first layer provide the disabling function: it can be verified from Fig. 9 that when the flash ADC output is full scale (all the thermometer bits are 1's or 0's), $q[n]$ has no effect on the signal.

B. HDC Digital Logic

The details of the HDC block in Fig. 6 are shown in Fig. 11. The HDC block implements the calculations described in Section II-C with some extra features to reduce complexity.

The signal $s_1[n]$ is requantized to 6 bits prior to the correlators, and its squared value is requantized to 4 bits prior to the η_2 average and dump operation to reduce the size of the HDC logic. *Dithered requantizers* are used to ensure that the resulting quantization noise is zero-mean and uncorrelated with $s_1[n]$ [16], which is sufficient to avoid corrupting the correlations. Although the quantization noise slows down the correlation process slightly, it has been found from simulation and approximate analysis that the increase in convergence time is negligible.

The average and dump blocks shown in Fig. 11 compute $A^2\gamma_1$, $6A^6\gamma_3$ and η_2 according to (10). They each average 2^P *valid* samples (i.e., samples for which $c[n]$ was enabled) where P is an integer between 28 and 34 (selectable via serial port control), and then output the average. Each time a new average is produced, the average and dump blocks are reset and start over. When new averages are ready, they are scaled as necessary to obtain γ_1, γ_3 and η_2, and further processed by digital logic that implements (11). Since the estimates are updated only once every 2^P valid samples, all the post processing only needs to produce new values at the same low rate, thus allowing a low-power and low-area realization. Four full speed multipliers and one adder implement (8).

C. Application of HDC and DNC to Multiple Pipeline Stages

In this design, HDC has been applied to the first three stages, as shown in Fig. 12. The calibration sequences $c_1[n]$, $c_2[n]$ and $c_3[n]$ are added and three HDC blocks, labeled HDC1, HDC2, and HDC3, are included in the first three stages, respectively. As explained in Section III-D, the coefficient estimation process

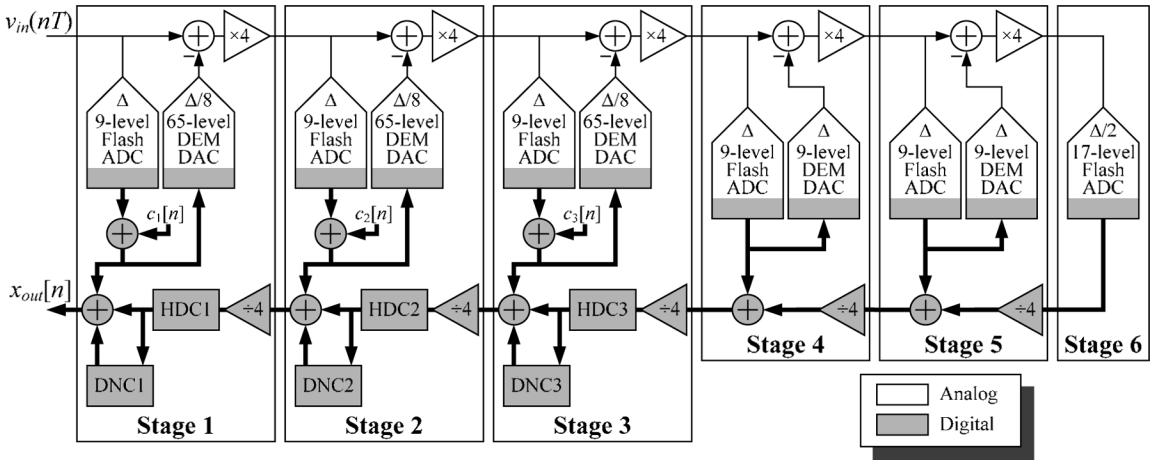

Fig. 12. Complete block diagram of the implemented 14-b pipelined ADC.

performed by HDC in a given stage is most accurate when the residue amplifier in that stage is the primary source of distortion. Therefore, the coefficient estimation process is implemented first in Stage 3, then in Stage 2, and then in Stage 1, at which point the cycle is repeated.

Fig. 12 also shows blocks that implement DNC in the first three pipeline stages. Each DNC block estimates and cancels the DAC noise introduced by the corresponding 65-level DAC. The implementation of DNC has been explained in [12], so further description of it is omitted from this paper.

HDC and DNC operate in the background during normal operation of the pipelined ADC, so they adapt to environmental changes without interrupting normal ADC operation. The convergence time is approximately 129 seconds (43 seconds per stage, limited by HDC convergence), so the DNC and HDC coefficients are updated every 129 seconds.

Therefore, the ADC does not operate at full accuracy for the first 129 seconds of operation. Although not implemented, a foreground calibration mode to address this issue can be implemented with no changes to HDC or DNC except for zeroing the input signal and using $4c_k[n]$ in place of $c_k[n]$ in each of the first three stages. While the ADC would not perform analog-to-digital conversion of the input signal while the foreground calibration mode is converging, the convergence is much faster than that of the normal background calibration mode. Simulations indicate that the foreground calibration mode would reduce the initial convergence time to less than a second. Thus, it would facilitate fast calibration at start-up, or after a long stand-by time, depending on the application. Once the ADC is calibrated the first time, HDC would continue to operate in the background to track environmental changes as described above.

D. Effect of Quantizer Nonlinearity On HDC

The estimation portion of HDC in a given pipeline stage measures distortion in that stage's digitized residue regardless of its source, but the correction portion of HDC is based on the assumption that all of the measured distortion came from that stage's residue amplifier. Therefore, the theory behind HDC implicitly assumes that the residue amplifier is the only significant source of nonlinearity in the pipelined ADC.

Nevertheless, under certain conditions the flash ADCs can be a significant source of nonlinearity in a pipelined ADC. Ideally, only the last stage's flash ADC quantization noise, i.e., $e_{\mathrm{ADC},6}[n]$, appears in the output of the pipelined ADC and the thermal noise level is high enough that it acts like dither and prevents $e_{\mathrm{ADC},6}[n]$ from introducing significant nonlinear distortion. However, due to non-zero α_1 and α_3, the quantization error from the first 5 stages is not perfectly canceled in practice, and this causes leakage of quantization error to the output. Even in the stages with HDC some leakage of quantization error always occurs, because the estimation process is never perfect.

To simplify the description of the problem, suppose the pipelined ADC has ideal components except that the residue amplifier in the second stage has a non-zero value of α_1 such that a fraction, λ_2, of quantization error, $e_{\mathrm{ADC},2}[n]$, leaks into the digitized residue, $r_1[n]$. In this case it follows from (10) that γ_1 and γ_3 of HDC1 contain terms $1/4\lambda_2\langle e_{\mathrm{ADC},2}[n]t_1[n]\rangle$ and $1/4\lambda_2\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle$, respectively. If either of these terms are non-zero, the estimates of the parameters α_1 and α_3 in stage 1 are corrupted. For example, it can be shown that when the pipelined ADC input stays in the range $-\Delta/16$ to $\Delta/16$, $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle = A^3\Delta/4$, whereas when the pipelined ADC input stays in the range $\Delta/16$ to $3\Delta/16$, $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle = -A^3\Delta/4$. In both cases even a small leakage of $\lambda_2 = 1 \times 10^{-4}$ causes the estimate of α_3 to have a magnitude of $0.139\ \mathrm{V}^{-2}$ (recall that $\alpha_3 = 0$ for this hypothetical example). Thus, the estimation error is almost 50% of the typical α_3 value of $-0.3\ \mathrm{V}^{-2}$ achieved by the op-amps used in the pipelined ADC prototype IC.

More generally, for DC and low-amplitude pipelined ADC input signals the correlation between $e_{\mathrm{ADC},2}[n]$ and $t_1[n]t_2[n]t_3[n]$ tends to be nonzero, which corrupts the estimates of α_3. This problem is negligible when the input signal amplitude is greater than -9 dBFS, because in such cases the signal at the input of the second stage's flash ADC is sufficiently busy that $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle$ is close to zero.

The problem described above is not unique to HDC. It affects all of the known residue amplifier distortion calibration techniques because they each use a pipelined ADC to measure the distortion from its own residue amplifiers. In each case, the distortion from all sources in the pipelined ADC is measured but

the distortion is corrected under the assumption that the residue amplifiers are the only significant distortion sources.

E. An Improved Calibration Sequence

One way to mitigate the problem is to use a calibration sequence consisting of 5 $t_i[n]$ sequences instead of 3 $t_i[n]$ sequences, i.e., $c[n] = t_1[n] + t_2[n] + t_3[n] + t_4[n] + t_5[n]$. The 2 extra sequences add enough dither to decorrelate $e_{\mathrm{ADC},2}[n]$ from $t_1[n]$ and $t_1[n]t_2[n]t_3[n]$, thus allowing successful convergence even for low-amplitude pipelined ADC input signals.

A drawback of this solution is that the two extra $t_i[n]$ sequences increase the magnitude of the calibration sequence by $\Delta/8$, so additional over range margin is used by the terms in the residue amplifier output associated with the calibration sequence. In this design, the drawback was found to be acceptable because the extra area and power consumption required to correspondingly reduce the flash ADC threshold errors, negligibly increased the overall circuit area and power consumption of the pipelined ADC prototype IC.

Unfortunately, a wiring mistake was made in the pipelined ADC prototype IC which caused the HDC calibration sequence in each HDC-enabled pipeline stage to be the sum of three rather than five $t_i[n]$ sequences. All five sequences are generated on chip for each HDC-enabled pipeline stage, but the wiring mistake prevented two of the five sequences from being used. As described above, the consequence of this mistake is that each stage's estimates of the α_1 and α_3 coefficients tend to be wrong for small-amplitude pipelined ADC input signals.

Normally, each HDC block continually updates its coefficients, but it can optionally freeze the coefficients after convergence. In order to test the pipelined ADC for small-amplitude input signals, the measurement results presented in Section V were obtained by allowing the HDC blocks to converge with a large-amplitude pipelined ADC input signal and then freezing the coefficients via serial port control. Measurements with frozen coefficients for numerous input signals, including small input signals, indicate that full performance is achieved in all cases as expected.

F. A Detection Method for Invalid Correlations

It can be shown that the dithering effect provided by adding the five $t_i[n]$ sequences completely removes any correlation between $e_{\mathrm{ADC},2}[n]$ and the sequences $t_1[n]$ and $t_1[n]t_2[n]t_3[n]$, in the case where $\alpha_1 = 0$. When $\alpha_1 \neq 0$, there are some small ranges of pipelined ADC input signals for which the quantization error $e_{\mathrm{ADC},2}[n]$ is still correlated with $t_1[n]t_2[n]t_3[n]$. For example, suppose $\alpha_1 = -0.06$. Then a pipelined ADC input signal that stays between 0.051Δ and 0.066Δ causes $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle = A^3\Delta/32$, and one that stays between 0.066Δ and 0.081Δ causes $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle = -A^3\Delta/32$, both of which would lead to invalid estimates of the distortion parameters.

As seen in the above example, the ranges of inputs for which $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle \neq 0$ come in doublets, and each side of the doublet has opposite correlations. Therefore, input signals that are sufficiently busy spend roughly equal time in each of the two sides of the doublet, so the effect of this undesired correlation tends to be small. Consequently the existence of these doublets does not seem to affect HDC accuracy significantly.

However, if necessary it is possible to detect invalid correlation results so as to avoid updating the distortion coefficients, until a new successful estimate is available. In the remainder of this section, a method to detect a bad estimate is described[4].

The output $x_2[n]$ of the Flash ADC of stage 2 can be correlated against $t_1[n]t_2[n]t_3[n]$ and the result can be used with the output of the second correlator of HDC1 to generate an estimate of the quantity

$$\langle s_1[n] \cdot t_1[n]t_2[n]t_3[n]\rangle - \frac{1}{4}\langle x_2[n] \cdot t_1[n]t_2[n]t_3[n]\rangle . \quad (17)$$

It follows from the reasoning described in Section II that

$$\frac{1}{4}\langle x_2[n] \cdot t_1[n]t_2[n]t_3[n]\rangle = -6A^6\alpha_3 + \frac{1}{4}\langle e_{\mathrm{ADC}2}[n] \cdot t_1[n]t_2[n]t_3[n]\rangle , \quad (18)$$

and

$$\langle s_1[n] \cdot t_1[n]t_2[n]t_3[n]\rangle = -6A^6\alpha_3 + \frac{\lambda_2}{4}\langle e_{\mathrm{ADC}2}[n] \cdot t_1[n]t_2[n]t_3[n]\rangle \quad (19)$$

where the last term in (19) is due to the leakage of quantization error. In practice $\lambda_2 \ll 1$ and $|\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle| < A^3\Delta/2$. Therefore, whenever the magnitude of the estimate of (17) is larger than $\lambda_{2-max}A^3\Delta/2$, where λ_{2-max} is an upper bound on λ_2, it indicates that $\langle e_{\mathrm{ADC},2}[n]t_1[n]t_2[n]t_3[n]\rangle$ is large enough to cause the HDC estimates to be corrupted. Furthermore, λ_{2-max} need not be a tight upper bound on λ_2. For example, in this system setting $\lambda_{2-max} = 0.01$ would work because it would ensure that the estimate of α_3 is precise within 10% assuming $\lambda_2 = 1 \times 10^{-3}$ and $\alpha_3 = -0.3V^{-2}$, which is sufficient accuracy to achieve the target ADC performance.

IV. Analog Circuit Details

Additional details of the analog and mixed-signal portions of the first three pipeline stages are shown in Fig. 13(a). The fourth and fifth stages have a similar structure, except no calibration sequence is added, and therefore a 9-level DEM DAC with a step size of Δ is used in place of the 65-level DEM DAC. Additional details of the last pipeline stage are shown in Fig. 13(b).

As shown in Fig. 13(a) the continuous time input signal is sampled by two separate passive sampling networks, the outputs of which are connected to the residue amplifier and the flash ADC, respectively [17]. The DAC is realized as a separate circuit connected to the input terminals of the residue amplifier.

A differential switched capacitor unit sampling cell with a simplified timing diagram is shown in Fig. 14. The sampling network of the residue amplifier consists of 8 such unit sampling

[4]The authors were not aware of the presence of such doublets until after the tape out, so the detection method described in this section was not implemented in the pipelined ADC prototype IC.

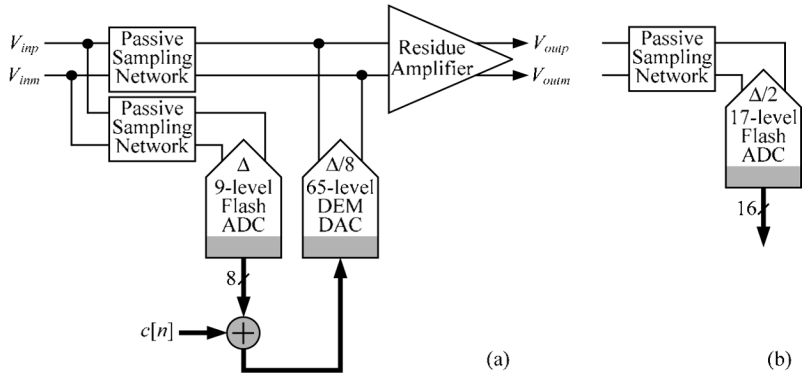

Fig. 13. Block diagram of the mixed-signal circuitry in (a) the first three pipeline stages, and (b) the last pipeline stage.

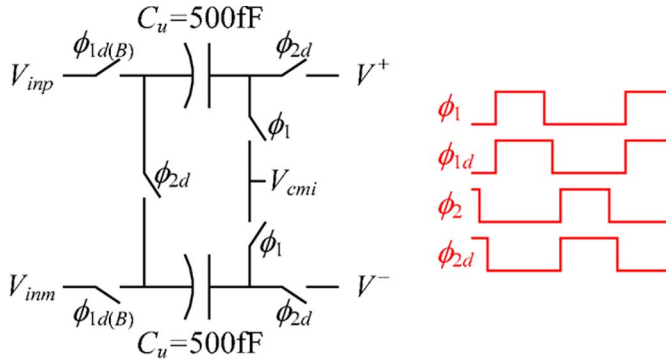

Fig. 14. Unit passive sampling network (bootstrap circuit for f1 d switches not shown).

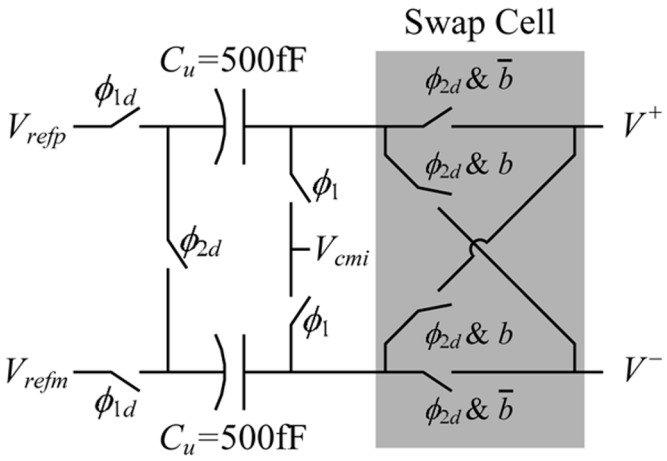

Fig. 15. 1-b DAC sampling network (weight Δ).

cells in parallel, whereas each of the 8 comparators of the 9-level flash ADC uses a quarter-size version of a single unit sampling cell. Both the capacitors and switches are scaled proportionally such that the two sampling paths have the same nominal time constant. The switches between the top plates of the capacitors and inputs of the op-amp provide isolation from the op-amp during the sampling phase to improve matching between the two sampling networks as described in [12], and ensure that the residue amplifier's α_i coefficients do not depend on the input signal. Bootstrapped switches of the type presented in [12] are used for the continuous-time input sampling switches of both sampling networks to achieve the necessary linearity.

A separate switched capacitor network has been used for the DAC to prevent signal-dependent loading of the voltage references. This benefit comes at the expense of a 3 dB increase in KT/C noise and a reduced residue amplifier feedback factor (1/10 versus 1/6) relative to a design in which the DAC and sampling network share the same capacitors.

The sampling network of each 1-b DAC with weight Δ is shown in Fig. 15. Scaled versions of the same cell have been implemented for the 1-b DACs with weights $\Delta/2$, $\Delta/4$ and $\Delta/8$ as required to implement the DAC in Fig. 8. The input bit b from the DEM encoder to each 1-b DAC controls the Swap Cell during ϕ_{2d}. Bootstrapped switches were not used for the DAC switches.

By design the dominant sources of noise in the pipelined ADC are KT/C noise and thermal noise from the op-amps in the first few stages. The 14-bit pipelined ADC architecture ensures that the quantization noise level is 16 dB below the targeted noise floor. The sampling network switch drivers were designed and verified by simulation to introduce noise that is similarly well below the targeted noise floor. Therefore, the capacitor sizes were determined and the op-amps were designed with the goal of meeting the target SNR specification of 70 dB.

The residue amplifier is shown in Fig. 16. It is based on a Miller compensated two-stage op-amp. Open loop op-amps and pseudo-differential op-amps were considered as possibilities for this design, but the two-stage op-amp ultimately was chosen because of its wide output dynamic range, which is particularly important given the 1.2 V supply voltage.

The simulated DC open-loop gain and unity gain frequency of the op-amp in the first pipeline stage's residue amplifier are 43 dB and 1.2 GHz, respectively. The corresponding loop gain of the residue amplifier is 23 dB at DC and has a unity gain frequency of 200 MHz. The current consumption of the op-amp is 4.8 mA from a 1.2 V supply.

During the amplification phase, ϕ_{2d}, the feedback capacitor C_f is connected to the op-amp, whereas during the ϕ_{1d} phase C_f is disconnected from the op-amp and discharged. During ϕ_{1d}, the op-amp is reset by shorting the differential outputs of both stages to reduce memory effects [18]. Switched capacitor common mode feedback circuitry (not shown in Fig. 16) controls the common mode voltage of the output stage by adjusting V_{cmfb}.

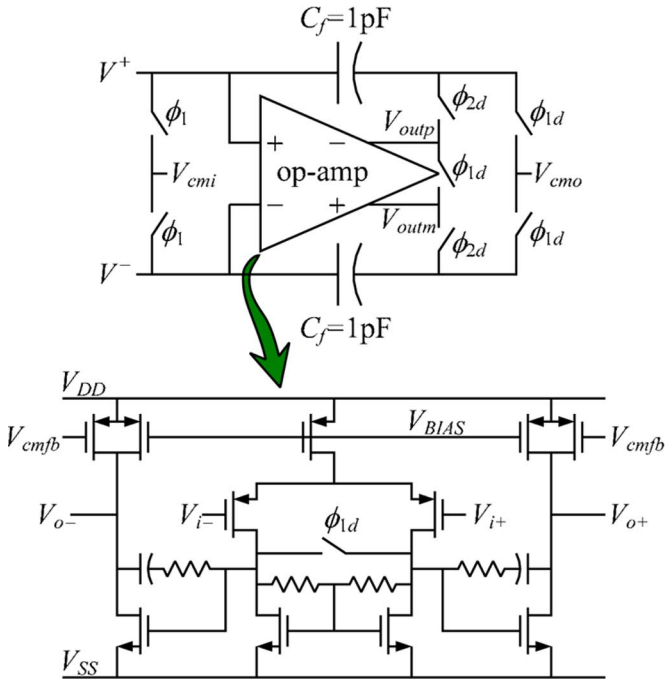

Fig. 16. Residue amplifier switched capacitor network and op-amp.

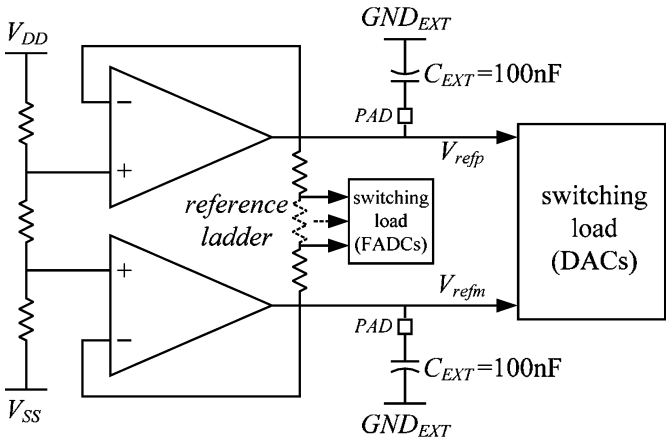

Fig. 17. Reference voltage generator.

The voltage references V_{refp} and V_{refm} are generated on chip as shown in Fig. 17. A set of resistors between the power supply and ground define the desired voltage reference values (nominally set to 950 mV and 265 mV, respectively), which are buffered by a pseudo-differential voltage follower and decoupled by external capacitors C_{EXT}[19]. The main drawback of this solution is the need for 2 extra pins for external decoupling. However the large external capacitors provide a low impedance over a wide frequency range, and this relaxes the performance requirements of the internal buffers which need only deliver the average current required by the switching load [20]. The total DC current consumption for the reference generation circuitry is 4 mA from a 1.2 V supply, including the current through the reference ladders.

The same reference voltages V_{refp} and V_{refm} are shared by all the DACs and flash ADCs in the pipelined ADC. The reference ladders that generate the threshold voltages for the flash

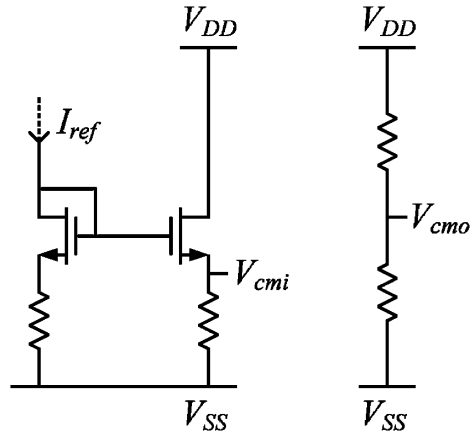

Fig. 18. Common mode voltage generators.

ADCs are connected between V_{refp} and V_{refm}. In this design, each flash ADC uses a dedicated reference ladder. The common mode voltages used for the switched capacitor circuits are generated as shown in Fig. 18.

Latched comparators of the type presented in [21] are used in the flash ADCs. It is a standard latch with preamplifier consisting of two resistively loaded differential pairs in series.

The phase generator has been designed with the strategy described in [12]. A dedicated phase is used as a sampling phase of the first stage only (ϕ_1 in Fig. 14), such that the sampling instant (falling edge of ϕ_1) happens before any other switching event [22]. This reduces the chance of corrupting the sampling process with disturbances such as from coupling effects. Care was taken to minimize sampling jitter by placing the clock generator close to the sampling network in the layout and by using a minimum number of inverters. The simulated jitter due to thermal noise of the sampling network is 100 fs.

To minimize design time the second through fifth pipeline stages are replicas of the first stage with only minor modifications. The only changes are that the residue amplifier, sampling network, and DAC have been scaled by 1/2 in stages 2 and 3 and by 1/4 in stages 4 and 5, and the op-amp has been scaled by 1/2 in the stages 3 and 4 and by 1/4 in the stage 5. More aggressive scaling would have reduced power and area consumption without sacrificing ADC accuracy. Power and area consumption also could have been reduced without sacrificing ADC accuracy if 1.5-b pipeline stages had been used after the first three stages [23]. However, neither of these design options were taken because they would have increased design time.

The pipelined ADC prototype IC is implemented in 90 nm CMOS technology with a deep nWell option, MiM capacitors, and both high and standard threshold voltage transistors. The circuit is partitioned into four power supply domains: (i) *analog*, (ii) *clock drivers & DEM*, (iii) *clock generator*, and (iv) *digital*, each of which is powered by a separate power supply line. The nominal power supply voltages of the four domains are 1.2 V, 1.2 V, 1.0 V, and 1.0 V, respectively. To minimize coupling from the substrate, all active components in the analog sections of the IC are in deep n-wells, the digital core and serial port interface (which were laid out with an automated place-and-route tool) are in a single deep n-well, and the capacitors associated

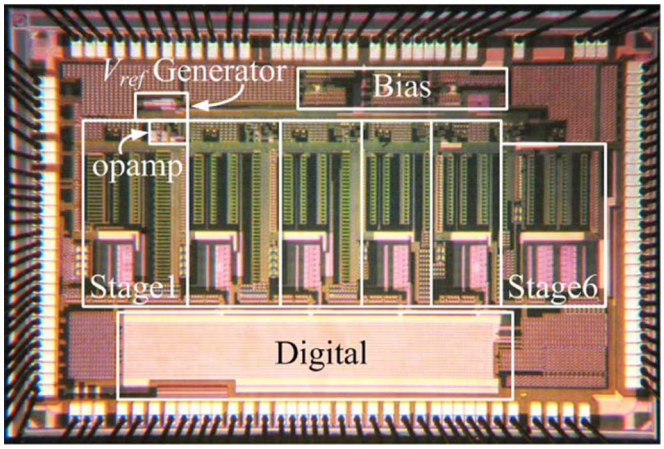

Fig. 19. Die photograph.

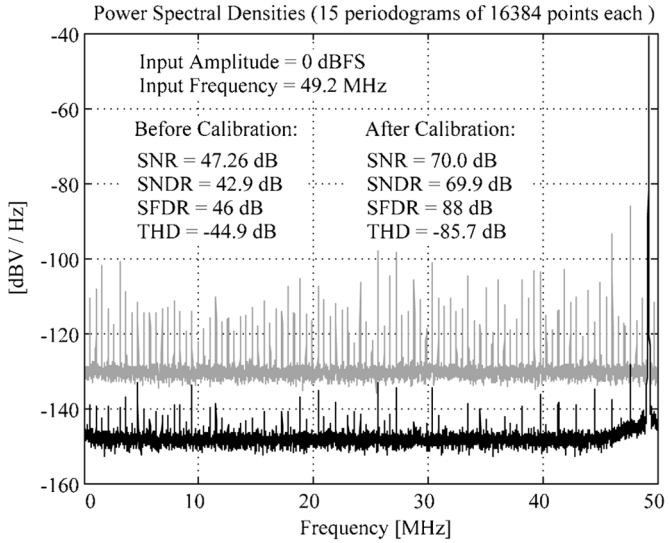

Fig. 20. Measured ADC output PSD plots before and after HDC/DNC calibration.

with the switched-capacitor portions of the IC were laid out above n-wells. On-chip decoupling capacitance is used to reduce power supply bounce. All pads have ESD protection circuitry. A die photograph is shown in Fig. 19. The IC is 2.15 mm by 3.35 mm and has an active area of 4 mm^2.

The IC is packaged in a 56-pin QFN package with exposed die paddle. All grounds are down-bonded to the exposed paddle. Critical supply pins and the pins that connect the voltage references to external decoupling capacitors are double-bonded to reduce inductance.

V. Measurement Results

Three randomly chosen copies of the pipelined ADC prototype IC have been tested. Each IC was soldered to one of three identical printed circuit test boards. Measurement results from the three test boards are reported in this section.

Each test board includes input signal conditioning circuitry, a 100 MHz low-jitter crystal oscillator and associated clock conditioning circuitry, voltage regulators, and digital circuitry to facilitate acquisition of the output data from and serial port communication with the pipelined ADC prototype IC. The input conditioning circuitry consists of a transformer followed by two passive *RC* filter stages to convert the single-ended input signal from an SMA connector to differential form and suppress out-of-band noise and distortion. The clock conditioning circuitry uses a transformer to convert the single-ended clock signal from the 100 MHz oscillator to differential form. The output swing of the 100 MHz oscillator is 3.3 V, so high-speed diodes are connected across the secondary terminals of the transformer to limit the amplitude of the differential clock signal to less than 1 V. Four voltage regulators provide the four power supplies of the pipelined ADC prototype IC. Five other voltage regulators provide power supplies for the other components on the test board.

Measurements were performed with a variety of single-tone and two-tone input signals. For each single-tone measurement, the output of a high-quality sinusoidal laboratory signal source was passed through a custom-made passive bandpass filter with a narrow bandwidth centered near the signal frequency to suppress noise and distortion from the signal source, and the output of the bandpass filter was connected to the test board. For each two-tone measurement, the outputs of two identical sinusoidal laboratory signal sources were added and the resulting signal was passed through a bandpass filter prior to the test board.

The measured performance from the three test boards was found to be nearly identical after calibration by HDC and DNC. Typical measurement results are shown in Figs. 20 and 21. Fig. 20 shows representative output power spectral density (PSD) plots from the pipelined ADC with a 49.2 MHz, 0 dBFS single-tone input signal. The grey plot was measured prior to calibration by HDC and DNC, and the black plot was measured after calibration by HDC and DNC. As indicated in the figure, the measured SNDR values of the ADC prior to and after calibration are 42.9 dB and 70 dB, respectively. Fig. 21 shows measured SNDR, SNR, and SFDR values from the pipelined ADC after calibration by HDC and DNC versus frequency and amplitude. The former were measured with -1 dBFS single-tone input signals ranging in frequency over the 50 MHz Nyquist band and the latter were measured with 19.2 MHz single-tone input signals ranging in amplitude from -69 dBFS to 0 dBFS. INL and DNL plots are shown in Fig. 22.

Fig. 23 shows plots of typical measured SFDR and SNR values from the pipelined ADC versus the number of values averaged by each of the HDC correlators for a 19.2 MHz, -1 dBFS single-tone input signal. The data suggests that full accuracy is achieved when 2^{31} or more values are averaged by the HDC correlators. Nevertheless, for all measurements other than those shown in Fig. 23 the HDC correlators were configured to average 2^{32} values, which corresponds to approximately 43 seconds of calibration time per stage at a sampling frequency of 100 MHz.

For all of the measurements described above, the analog, clock, and digital supply voltages of the pipelined ADC prototype IC were set to their targeted design values of 1.2 V, 1.0 V, and 1.0 V, respectively, but the power supply for the clock drivers and DEM was set to 1.35 V instead of its targeted design value of 1.2 V. When this supply is set to its targeted design value of 1.2 V, the peak SNDR decreases by

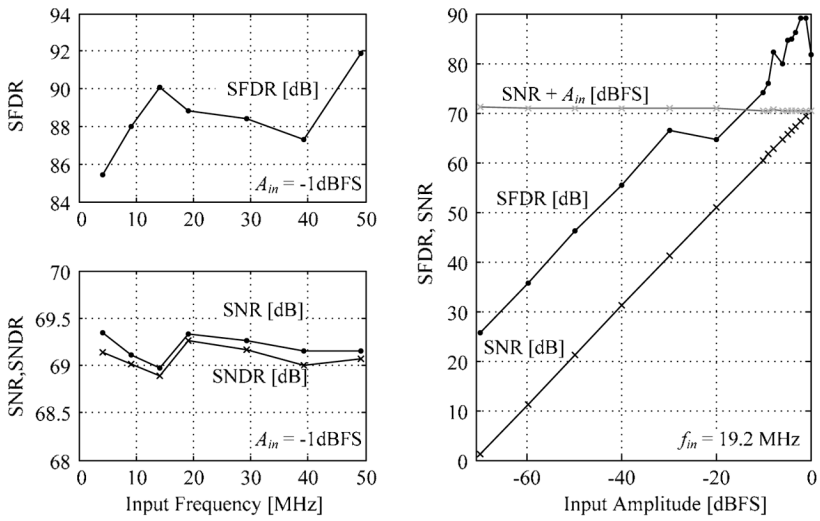

Fig. 21. Measured SFDR, SNR, and SNDR versus input frequency and input amplitude.

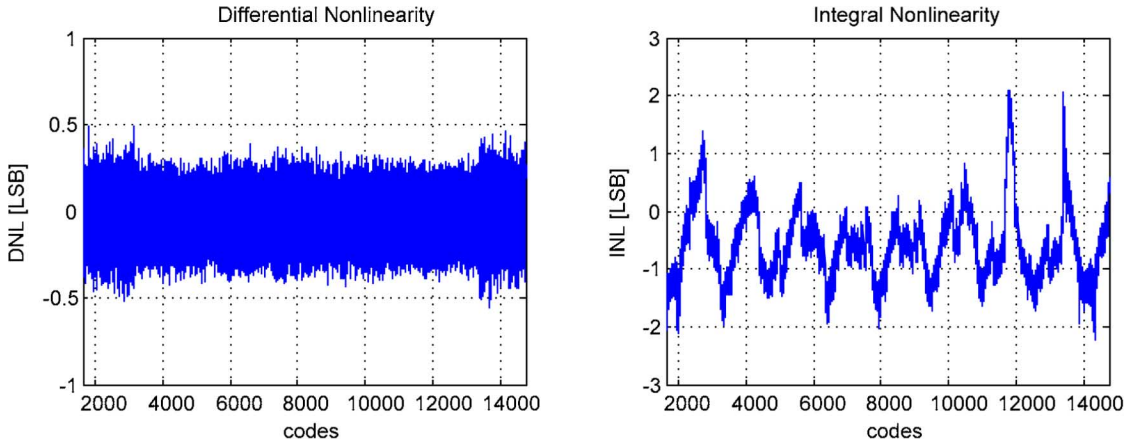

Fig. 22. Measured DNL and INL (14-bit level, 0.2 LSB precision, 99% confidence interval).

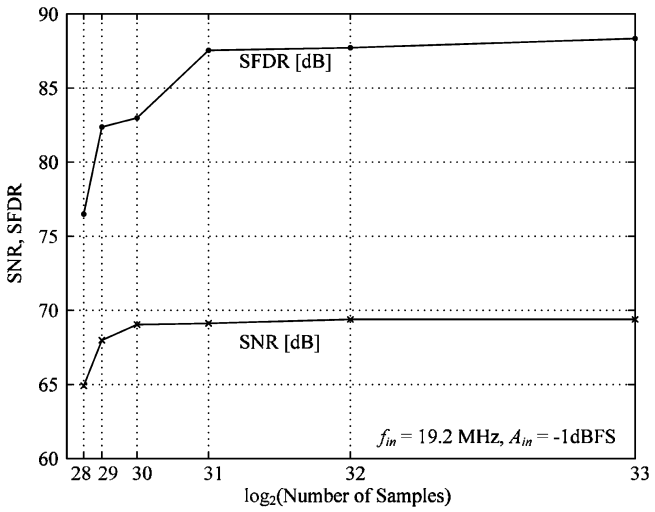

Fig. 23. Measured SNR and SFDR versus number of points averaged by HDC.

approximately 3 dB. Although not predicted by simulations, the authors believe that the clock drivers have insufficient strength to achieve full ADC performance at 1.2 V.

Table I shows worst-case measurement results for all three test boards under two different power supply voltage scenarios. The two power supply voltage scenarios are denoted $V_{\rm DD}$ *Test Case 1* and $V_{\rm DD}$ *Test Case 2*. In $V_{\rm DD}$ *Test Case 1* all power supplies, except that for the Clock Drivers and DEM, are set to their targeted design values as described above. In $V_{\rm DD}$ *Test Case 2* the analog power supply is reduced to 1.0 V, and the digital power supply is reduced to 0.7 V. Although the analog circuitry in the pipelined ADC was not designed to work at this reduced power supply voltage, it is based on simple circuit structures without cascode stages or gain boosting, so it tends to be robust with respect to low voltage operation, rather than achieving high-performance (which is not necessary because of HDC). As a result, at 1.0 V the measured worst-case reduction in SNDR is only 2.2 dB.

As mentioned above, the measured performance from the three test boards was found to be nearly identical after calibration by HDC and DNC. However, the α_1 and α_3 coefficients estimated by the HDC blocks (as read from the pipelined ADC prototype IC via the serial port interface) were found to vary significantly from chip to chip. For example, the estimate of α_3 by HDC in the first stage of the pipelined ADC varied by approx-

TABLE I
ADC PERFORMANCE SUMMARY

Design Details						
Architecture	14-bit Pipelined ADC					
Technology	90 nm CMOS					
Package	56 pin QFN					
Die Size Including Pads and ESD Protection	2.15 mm × 3.35 mm					
Active Area	4 mm^2					
Digital Calibration	on-chip					
Voltage References	on-chip					
Worst Case Measured Results Over Nyquist Band for f_s = 100 MHz						
Power Supplies	**V_{DD} Test Case 1**			**V_{DD} Test Case 2**		
	V_{DD}	Power Dissipation		V_{DD}	Power Dissipation	
Analog	1.2 V	93 mW	130 mW	1.0 V	62 mW	92 mW
Digital	1.0 V†	17 mW		0.7 V†	7 mW	
Clock Generator	1.0 V	1 mW		1.0 V	1 mW	
Clock Drivers & DEM	1.35 V‡	19 mW		1.35 V‡	22 mW	
Input and References						
Input Voltage Range	1.5 $V_{p\text{-}p}$ differential			1.25 $V_{p\text{-}p}$ differential		
Internal V_{ref+} / V_{ref-}	950 mV / 265 mV			775 mV / 225 mV		
Performance with HDC and DNC On						
Peak *SNR*	70 dB			68.3 dB		
SNDR at −1dBFS	68.8 dB			66.6 dB		
SFDR at −1dBFS	85 dB			75 dB		
2-tone *SFDR* at −1dBFS	86 dB			80 dB		
Maximum *INL*	3.6 LSB			3.8 LSB		
Maximum *DNL*	0.54 LSB			0.39 LSB		
Performance with HDC and DNC Off						
SNDR at −1dBFS	43.3 dB			47.3 dB		
SFDR at −1dBFS	52.3 dB			58 dB		
Performance with HDC on and DNC Off						
SNDR at −1dBFS	64.6 dB			64.3 dB		
SFDR at −1dBFS	85 dB			75 dB		

† The digital circuitry works reliably and full ADC performance is achieved provided this V_{DD} is at least 0.6V.
‡ When this V_{DD} is set to its targeted design value of 1.2V, the peak *SNDR* decreases by approximately 3dB. Although not predicted by simulations, the authors believe that the clock drivers have insufficient strength to achieve full ADC performance at 1.2V.

TABLE II
COMPARISON TO PRIOR WORK.

Reference or Part Number	f_s (MS/s)	*SNDR* (dBFS)	*SFDR* (dB)	V_{DD} (V)	P_{tot} (mW)	*FOM*1 (pJ/conv-step)	*FOM*2 (pJ·V/conv-step)
[7]	75	68	76	3	314	2.04	6.12
LTC2259	80	73	90	1.8	93	0.32	0.57
AD9233	80	70.5	90	1.8	248	1.13	2.03
ADS6123	80	72.3	89	3.3	318	1.18	3.89
LTC2260	105	73	90	1.8	112	0.29	0.53
AD9233	105	70.5	90	1.8	320	1.11	2.00
ADS6124	105	72.3	84	3.3	374	1.06	3.49
[26]	250	65.9	82	1.8	150	0.37	0.67
[10]	100	70	80	1.2	250	1.00	1.2
This work	100	69.8	85	1.2	130	0.52	0.62
This work	100	67.6	75	1.0	92	0.47	0.47

$$FOM1 = \frac{P_{tot}}{2^{ENOB} f_s} \quad \text{and} \quad FOM2 = FOM1 \times V_{DD} \quad \text{where} \quad ENOB = \frac{SNDR - 1.76\,\text{dB}}{6.02\,\text{dB}}$$

imately $\pm 30\%$ from chip to chip about a mean of $-0.15\ \text{V}^{-2}$. Therefore, HDC is at least partly responsible for the observed uniformity of the measurement results.

Table II shows relevant performance data from the pipelined ADC prototype IC along with those from published state-of-the-art ADCs with comparable bandwidths and SNDR values. Two commonly used figures of merit, *FOM*1 and *FOM*2, are included in the table. Although *FOM*1 is more widely referenced in the academic literature than *FOM*2, the latter is often considered more appropriate for ADCs that are SNR-limited because of low supply voltages [24], [25]. As indicated in the table, both figures of merit for the pipelined ADC prototype IC are better (lower) than those for the only other comparable published ADC that operates from a supply voltage below 1.8 V, and are better than those for most of the comparable published ADCs that operate from supply voltages at or above 1.8 V.

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