

A 12-b 18-GS/s RF Sampling ADC With an Integrated Wideband Track-and-Hold Amplifier and Background Calibration

Ahmed M. A. Ali[✉], Senior Member, IEEE, Huseyin Dinc, Member, IEEE,
Paritosh Bhoraskar, Senior Member, IEEE, Scott Bardsley, Chris Dillon,
Matthew McShea, Joel Prabhakar Periathambi, and Scott Puckett

Abstract—We discuss a 12-b 18-GS/s analog-to-digital converter (ADC) implemented in 16-nm FinFET process. The ADC is composed of an integrated high-speed track-and-hold amplifier (THA) driving up to eight interleaved pipeline ADCs that employ open-loop inter-stage amplifiers. Up to 10 GS/s, the THA operates at the full sampling rate using a non-interleaved single sample network, thereby eliminating the interleaving sampling time and bandwidth mismatch. Above 10 GS/s, the THA is programmed to use two ping-ponged, or an optional (2 + 1) randomized, sample networks to spread the residual post-calibration interleaving spurs in the noise floor. The THA enables an input bandwidth of 18 GHz and employs dither injection and optional pseudorandom chopping. In the pipeline stages, dither-based background calibration detects and corrects gain, settling, memory, and kick-back errors. New dither-based background calibration algorithms are employed to detect and correct the arbitrary non-linearity in the form of integral non-linearity (INL) breaks and harmonic distortion up to the fifth order in the THA and in the references, DACs, and inter-stage open-loop amplifiers of the pipeline ADCs. Moreover, new dither-based background calibration is implemented to detect and correct the chopping non-idealities, memory errors, interleaving mismatches, and order-dependent randomization errors. Compared to the fastest state-of-the-art with similar performance, this ADC achieves 80% higher sample rate and 2.4x higher input bandwidth, and incorporates a THA that supports a 3.3x higher non-interleaved sample rate.

Index Terms—Analog-to-digital converter (ADC), background calibration, DAC calibration, digital assistance, interleaved, non-linear calibration, pipeline, reference calibration, RF sampling, sample-and-hold, sample-and-hold amplifier (SHA), track-and-hold, track-and-hold amplifier (THA).

I. INTRODUCTION

ANALOG-TO-DIGITAL converters (ADCs) with high sample rate, high input bandwidth, and low power consumption are needed in communication, instrumentation, and other applications to enable direct RF sampling, more integration, greater flexibility, and lower cost. By removing the

Manuscript received May 11, 2020; revised July 12, 2020 and August 25, 2020; accepted August 28, 2020. Date of publication September 30, 2020; date of current version November 24, 2020. This article was approved by Guest Editor John P. Keane. (*Corresponding author: Ahmed M. A. Ali.*)

The authors are with Analog Devices, Inc., Greensboro, NC 27409 USA (e-mail: ahmed.ali@analog.com).

Color versions of one or more of the figures in this article are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2020.3023882

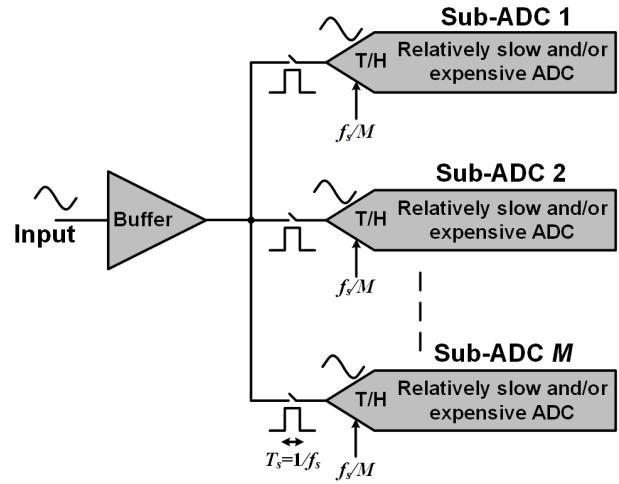


Fig. 1. Conventional architecture of an interleaved ADC with the sampling rate f_s . The input buffer drives the RF signal into the distributed samplers (T/H's) of the sub-ADCs.

mixers of heterodyne and homodyne receivers and positioning the ADC closer to the antenna, the RF signal can be directly digitized, which moves the majority of the signal processing to the digital domain. Moreover, supporting a Nyquist bandwidth that is greater than 8 GHz enables the whole signal band of interest in many applications to be in a single Nyquist zone, thereby eliminating the need for complicated anti-aliasing filtering and frequency planning.

The state-of-the-art interleaved RF converters enable up to 10-GS/s sample rate with 12–14 b of resolution [1]–[4], 5 GHz of Nyquist bandwidth, and 7.4 GHz of input bandwidth, which are inadequate for some applications. They typically lack a frontend track-and-hold amplifier (THA) or a sample-and-hold amplifier (SHA), employing an input buffer driving interleaved sub-ADCs with interleaved samplers as shown in Fig. 1. The sub-ADCs are often optimized in the analog domain for performance and/or power. This results in either relatively low-speed or high-power sub-ADCs.

To increase the sample rate in a conventional architecture, the number of interleaved sub-ADCs needs to increase, which increases their load, and hence, the input capacitance of the ADC input buffer reduces the input bandwidth and increases the power consumption. Moreover, increasing the

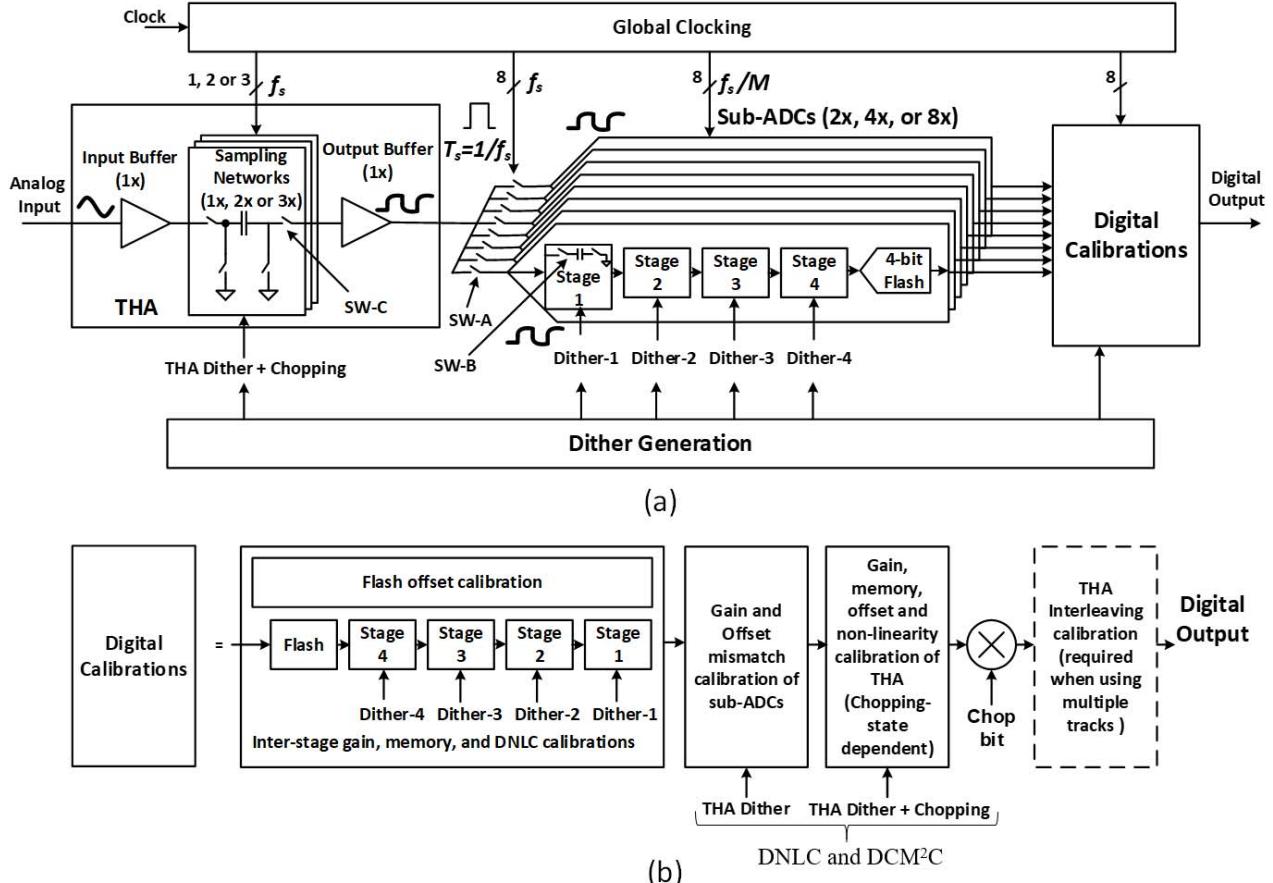


Fig. 2. (a) Conceptual diagram of the ADC architecture. The THA samples the input RF signal and provides a “held” signal to the sub-ADCs. (b) Digital calibrations. The two THA calibration blocks before un-chopping represent the DNLC and DCM²C algorithms.

number of interleaved sub-ADCs, while using an SHA-less architecture, degrades the interleaving spurs due to sampling time and bandwidth mismatch. Randomization of the interleaved sub-ADCs helps alleviate the impact of the interleaving spurs but that degrades the noise and increases the power consumption in a manner that gets progressively worse as the input frequency and number of sub-ADCs increase [1].

In this work [5], we describe a 12-b 18-GS/s ADC comprising a THA driving as many as eight interleaved sub-ADCs. To increase the sample rate and lower the power consumption, we employ fast, low-power, pipeline sub-ADCs that utilize open-loop amplifiers with background calibration to correct the non-linearity in the inter-stage amplifiers, DACs, and references.

Moreover, to decouple the RF sampling problem from the challenge of driving the quantizer, the ADC has an integrated fast THA that employs dither injection and optional pseudo-random chopping. This enables robust and input-independent background calibration of the THA’s and ADC’s non-idealities, as well as offset, gain, and non-linearity mismatches between the sub-ADCs, thereby substantially reducing the power overhead of adding a THA to the ADC.

In this article, we discuss the architecture in Section II and the analog design considerations of some of the blocks

in Section III. Section IV covers the background calibration algorithms employed in this work with emphasis on the new dither-based non-linear calibration (DNLC) and the dither-based chopping, memory, and core mismatch calibration (DCM²C). Section IV summarizes the measured results and comparison with the state-of-the-art and Section V concludes this article.

II. ARCHITECTURE

The architecture employed in this work is shown in Fig. 2. It consists of eight interleaved pipeline sub-ADCs with open-loop Gm-R amplifiers [10] that can sample up to 3 GS/s each. Each sub-ADC consists of four 3-bit stages followed by a 4-bit flash. The sub-ADCs are programmable to operate in 8-, 4-, or 2-way interleaved modes. As shown in Fig. 3(a), each stage has a one-bit calibration dither sequence injected in the multiplying digital-to-analog converter (MDAC) for calibration and multi-bit linearization dither injected in both the MDAC and flash for linearization/dithering of any residual errors to improve the accuracy and robustness of the calibrations [6], [7]. Since the flash ADC consists of eight comparators (instead of 7), this creates \pm half a sub-range of additional range beyond the full scale that can be used for the THA and linearization dithers without compromising the dynamic range of the ADC [6], [7], as shown in Fig. 3(b).

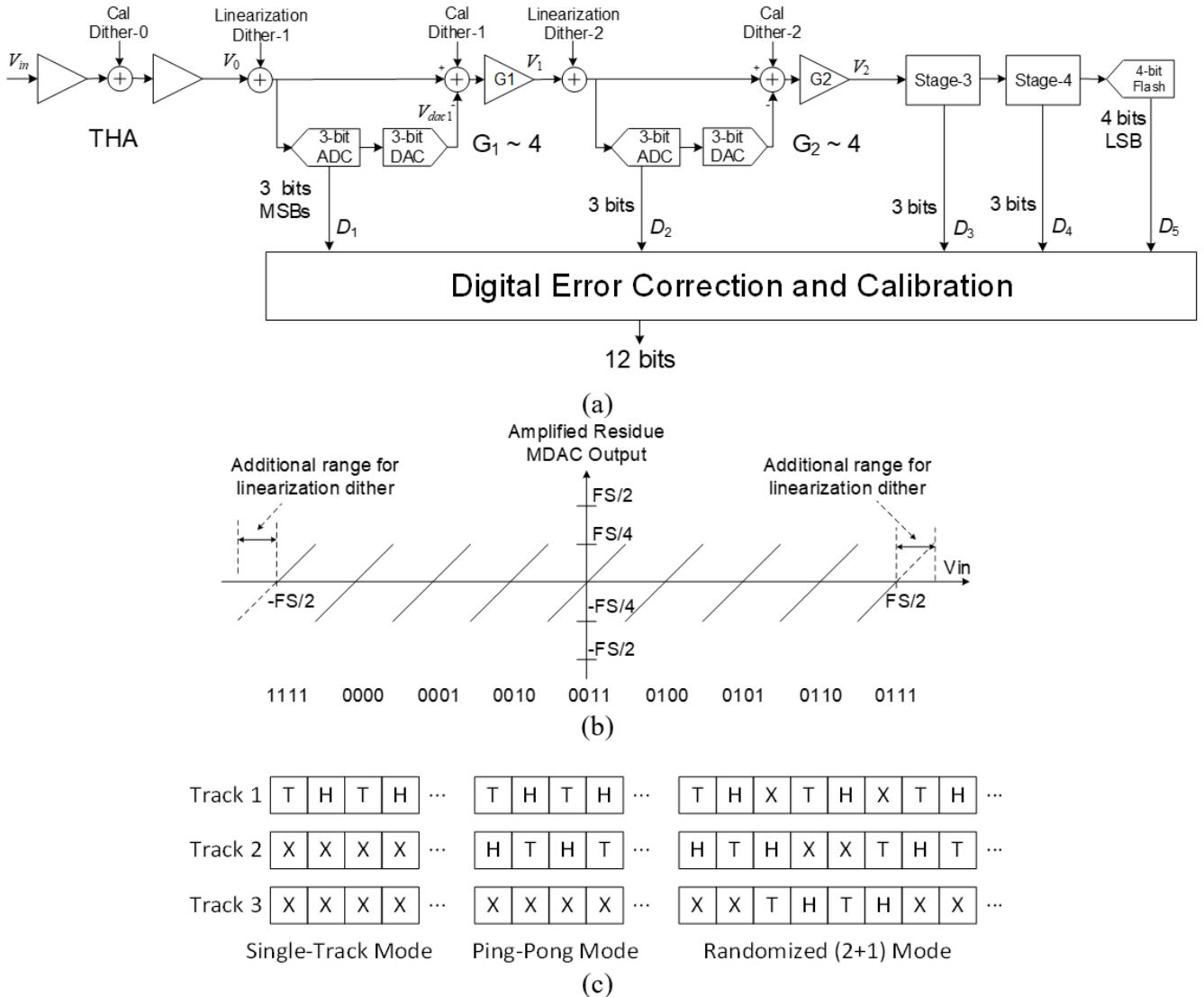


Fig. 3. (a) Simplified block diagram of one of the pipeline sub-ADCs driven by the common THA showing the calibration and linearization dither injections. (b) Residue of a pipeline stage showing the additional range used by the linearization dither and the calibration dither of the preceding stage. “FS” is the full scale of the ADC. (c) Illustration of different modes of the THA. “T” is the sample/track phase, “H” is the hold phase, and “X” is an unused phase. The three “tracks” refer to the three sample networks of the THA.

Background calibrations are implemented for the pipeline inter-stage gain, settling, memory, flash, and residual charge injection (“kick-back”) errors [3], [6], [7].

In addition, we employ new background calibrations that can detect and correct non-linearity in the form of arbitrary integral non-linearity (INL) breaks and harmonic distortion up to the fifth order that are due to the inter-stage amplifier, DAC, reference, or other causes. This non-linearity calibration algorithm is collectively called DNLC and it enables substantial improvement in performance, enhancement of speed, and reduction in power of the MDAC amplifier and reference, as discussed in Section IV.

To improve the input bandwidth relative to the prior art, enhance the RF sampling performance, and alleviate the timing/bandwidth mismatch problem, a fast THA is implemented to drive the sub-ADCs. The THA employs an open-loop design

that consists of an input buffer, one or more reconfigurable sampling network(s), and an output buffer that drives the sub-ADCs. As shown in Fig. 3(c), up to 10 GS/s, a single sampling network (referred to as “track” in this work) can be utilized, which results in the THA operating at the full sample rate, thereby eliminating the timing/bandwidth mismatch problem completely. Above 10 GS/s, two sample networks (i.e., tracks) are required to operate in ping-pong mode, with the third network to operate in an optional randomized (2 + 1) mode. This converts the eight-way interleaving timing mismatch problem in a traditional architecture into a two-way mismatch problem, with the option to randomize and, hence, spread the residual interleaving spurs after calibration into the noise floor. The mismatches between the eight sub-ADCs result in only offset and gain mismatch errors. When operating in ping-pong or randomized (2 + 1) modes, the THA requires background

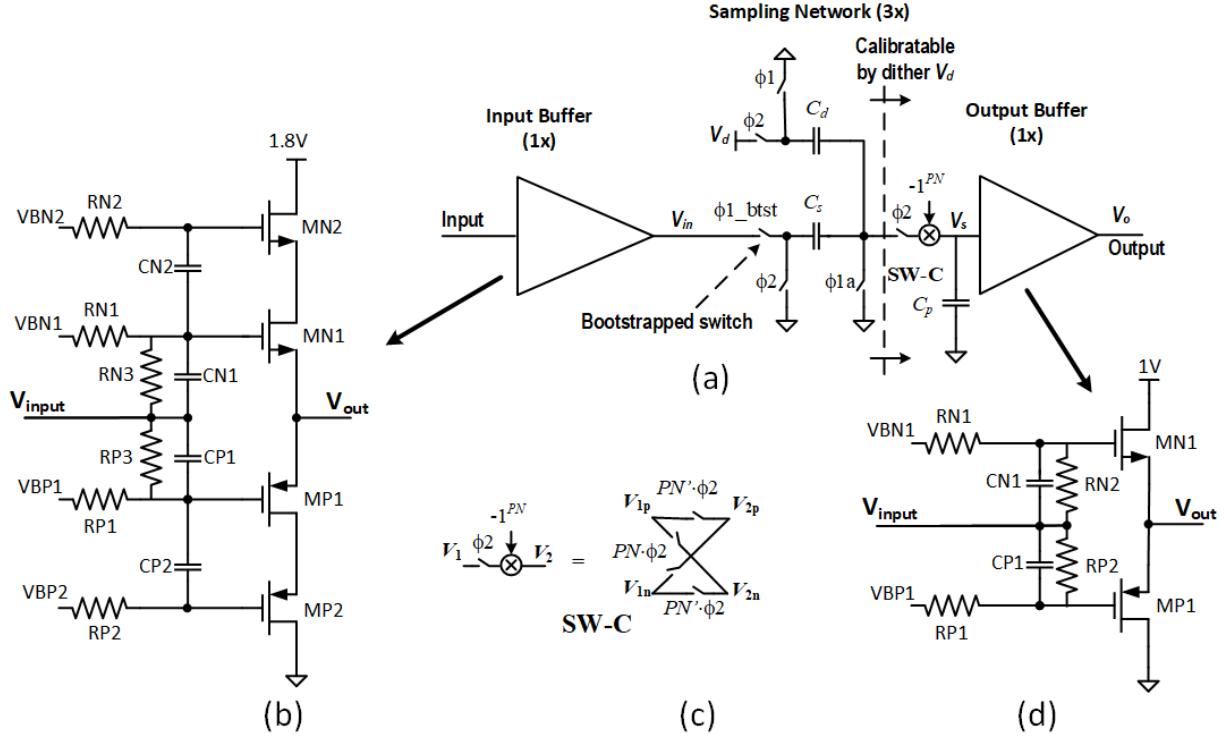


Fig. 4. Simplified diagrams of (a) THA, (b) input buffer, (c) chopping switch SW-C, and (d) output buffer.

calibration for offset, gain, and timing mismatches between the different sample networks of the THA, as shown in the dotted box in Fig. 2(b). The randomization is similar to the one employed in [1]. As shown in Fig. 3(c), whenever a certain “track” is used to sample the input, the next sampling track is pseudorandomly selected from the other two tracks. However, since ping-pong interleaving creates only one timing interleaving spur within a Nyquist band, the benefit of randomizing this spur may not be compelling enough to justify the additional complexity of randomization. In this work, the ping-pong mode is the preferred mode of operation.

Since the sampling clock jitter degrades the ADC noise as the input frequency increases, a low-jitter clock is critical for RF sampling. The ADC is clocked by a differential low-noise clock receiver that is driven by an off-chip low-jitter clock source. The output of the clock receiver generates the clock signals for the THA, sub-ADCs, and the digital block [1]. Good design and layout practices are employed to isolate the clock from noise coupling and the number of gates in the sampling clock path is minimized to reduce the sampling jitter.

The THA employs optional pseudorandom chopping in the hold phase to de-sensitize the offset mismatch calibration against the input signal characteristics [8]. Dither is also injected in the THA to calibrate the non-linearity of the THA output buffer, switches, and the subsequent sub-ADC, using the previously mentioned DNLC algorithm, and, thus, reduce the power consumption, size, and complexity of this THA compared to traditional THAs. This dither is also used to calibrate the gain and non-linearity mismatches between the eight sub-ADCs, and the chopping-dependent gain and

memory errors in the THA. These calibrations are collectively called DCM²C and are described in Section IV.

The calibration dither injected in a stage is used to calibrate the stage amplifier non-linearity, the memory/kick-back errors of the same stage, and the DAC/reference errors and non-linearity of the following stage. Therefore, the dither injected in the THA is used to calibrate the non-linearity of the THA buffer, the DAC/reference errors of stage 1, and so on.

To summarize, this architecture has three main pillars.

- 1) Fast and low-power ADC cores that use simple analog circuits and rely on digital calibration to enhance their performance and reduce their power consumption and area.
- 2) Fast and low-power THA that improves the input bandwidth, RF sampling, and interleaving mismatch performance.
- 3) Digital background calibration algorithms that enable efficient and robust detection and correction of discrete-time non-linearities, interleaving mismatches, memory, and chopping non-idealities. These calibrations enable an enhancement in performance and reduction of power.

III. CIRCUIT IMPLEMENTATION

A. Track-and-Hold Amplifier

The THA consists of an input buffer, as many as three sample networks, and an output open-loop buffer or amplifier, as shown in Fig. 4(a). The input buffer of the THA, which is

shown in Fig. 4(b), is a push-pull follower optimized for low-distortion RF sampling with bootstrapped drains to increase the output impedance of the source follower transistors and improve their linearity. Each sampling network employs bottom plate sampling with an advanced clock (ϕ_{1a}) driving the sampling switch and, hence, determining the sampling instant. A bootstrapped clock (ϕ_{1_btst}) drives the input switch to improve its linearity. In the hold phase, the dither is injected on the dither capacitance, and the series switch SW-C is turned on. This switch is shown in Fig. 4(c) and it multiplexes the three sampling networks onto the same output buffer, performs chopping, and improves the isolation between the eight-way interleaved sub-ADCs and the sampling switches. Since multiple sampling networks share the same output buffer, the charge stored on the summing node of the buffer may not be fully reset and, hence, can cause degradation in noise and linearity due to the memory errors across sampling networks and within the same network. These errors are detected and corrected by the THA memory calibration. Moreover, the two chopping paths can be mismatched, which requires calibration as well. These calibrations will be discussed in Section IV.

The output buffer provides low output impedance to drive the load capacitance of the eight sub-ADCs and their routing network, and isolates the THA sampling switches from the eight-way sub-harmonic coupling. The output buffer is shown in Fig. 4(d) and is composed of a push-pull source follower. Unlike the input buffer that requires a supply of at least 1.8 V to support the drain bootstrapping transistors, the output buffer's supply can be as low as 1 V, which reduces its power consumption but degrades its linearity.

The THA drives the eight sub-ADCs through a routing network that has two series switches as shown in Fig. 2. The first switch SW-A is physically close to the THA and is clocked by pulses whose widths are equal to the period of the high speed clock (f_s), while the second switch SW-B is inside the sub-ADC's stage 1 and is clocked by the slow clock (f_s/M). Using two series switches helps reduce the capacitive load on the output buffer of the THA by disconnecting the routing of the unused sub-ADCs. It also reduces the load on the MDAC's reference buffer and enables sharing the capacitance between the sampling and the DAC operations in the MDAC of stage 1. This capacitance sharing improves the speed and noise and lowers the power consumption of the pipeline stage.

In Fig. 4(a), the non-idealities of the THA can be illustrated by applying charge conservation to the summing node, which gives

$$V_s[n] = -\frac{V_{in}[n]C_s}{C_t} + \frac{\alpha_m V_s[n-1]C_p}{C_t} + \frac{V_d[n]C_d}{C_t} \quad (1)$$

where $V_s[n]$ is the summing node voltage of the n th sample, $V_{in}[n]$ is the input voltage, $V_d[n]$ is the dither voltage, $V_s[n-1]$ is the $(n-1)$ th summing node voltage, α_m is the memory coefficient, C_s is the sampling capacitance, C_p is the parasitic capacitance, C_d is the dither capacitance, and $C_t = C_s + C_d + C_p$ is the total capacitance. We should note that the previous summing node voltage $V_s[n-1]$ can represent

the previous sample of the same network or from another network in the case of ping-pong or randomized operation. It also embodies the cumulative residual memory of all the previous samples. That is, this discrete-time filter is an infinite impulse response (IIR) filter.

When chopping is employed, the ideal chopping function can be represented as

$$f_{ch_id}(V[n]) = D_{ch}[n] \cdot V[n] = (-1)^{PN[n]} \cdot V[n] \quad (2)$$

where $D_{ch}[n]$ is the chopping code that can be 1 or -1 , PN is the same chopping code represented as 0 or 1, and PN' is its inverse. Practically, due to mismatches, the chopping function deviates from the ideal function in (2). Incorporating chopping in (1) gives

$$V_s[n] = f_{ch}\left(-\frac{V_{in}[n]C_s}{C_{tch}} + \frac{V_d[n]C_d}{C_{tch}}\right) + \frac{\alpha_{mch} V_s[n-1]C_{pch}}{C_{tch}} \quad (3)$$

where $f_{ch}(V[n])$ is the non-ideal chopping function, and C_{pch} , C_{tch} , and α_{mch} are the chopping-dependent parasitic capacitance, total capacitance, and memory coefficient, respectively. The summing node voltage is the output of the sampling network, which gets buffered by the output buffer of the THA and digitized by the sub-ADCs. If the non-linear output of the buffer is $V_o[n]$, the input and, hence, the calibrated/corrected output can be deduced from the output by re-arranging (3) and normalizing to get

$$V_{in}[n] = -f_{ch}^{-1}(f_{NL}^{-1}(V_o[n])) + \alpha_{mtch} f_{ch}^{-1}(f_{NL}^{-1}(V_o[n-1])) + V_d[n] \quad (4)$$

where f_{NL} is a non-linear function that represents the transfer function of the output buffer and the cumulative non-linear effects of the whole down-stream signal path, and α_{mtch} is the normalized chopping-dependent memory coefficient. The chopping-dependent gain and offset terms are absorbed in the inverse chopping function f_{ch}^{-1} . Note that the correction of the IIR memory term is eliminated by a single-tap finite impulse response (FIR) correction as shown in (4) because the correction is applied to the output, not the input. The non-idealities that require calibration are represented by the inverse nonlinear function f_{NL}^{-1} , the inverse chopping function f_{ch}^{-1} , and the chopping-dependent memory coefficient α_{mtch} . By estimating these parameters, using the DNLC and DCM²C algorithms, the non-idealities of the THA can be corrected in the digital domain as will be illustrated in Section IV.

B. Pipeline Sub-ADCs

As shown in Fig. 3, each sub-ADC consists of four 3-bit stages and a 4-bit backend flash. Each MDAC employs eight capacitances that are shared between the sampling and DAC operations, and dither capacitances to inject the calibration and linearization dither signals as shown in Fig. 5(a). The calibration dither is injected in the hold phase and the capacitance is connected to ground in the sample phase. Alternatively, it can be connected to the input in the sample phase to "kick"

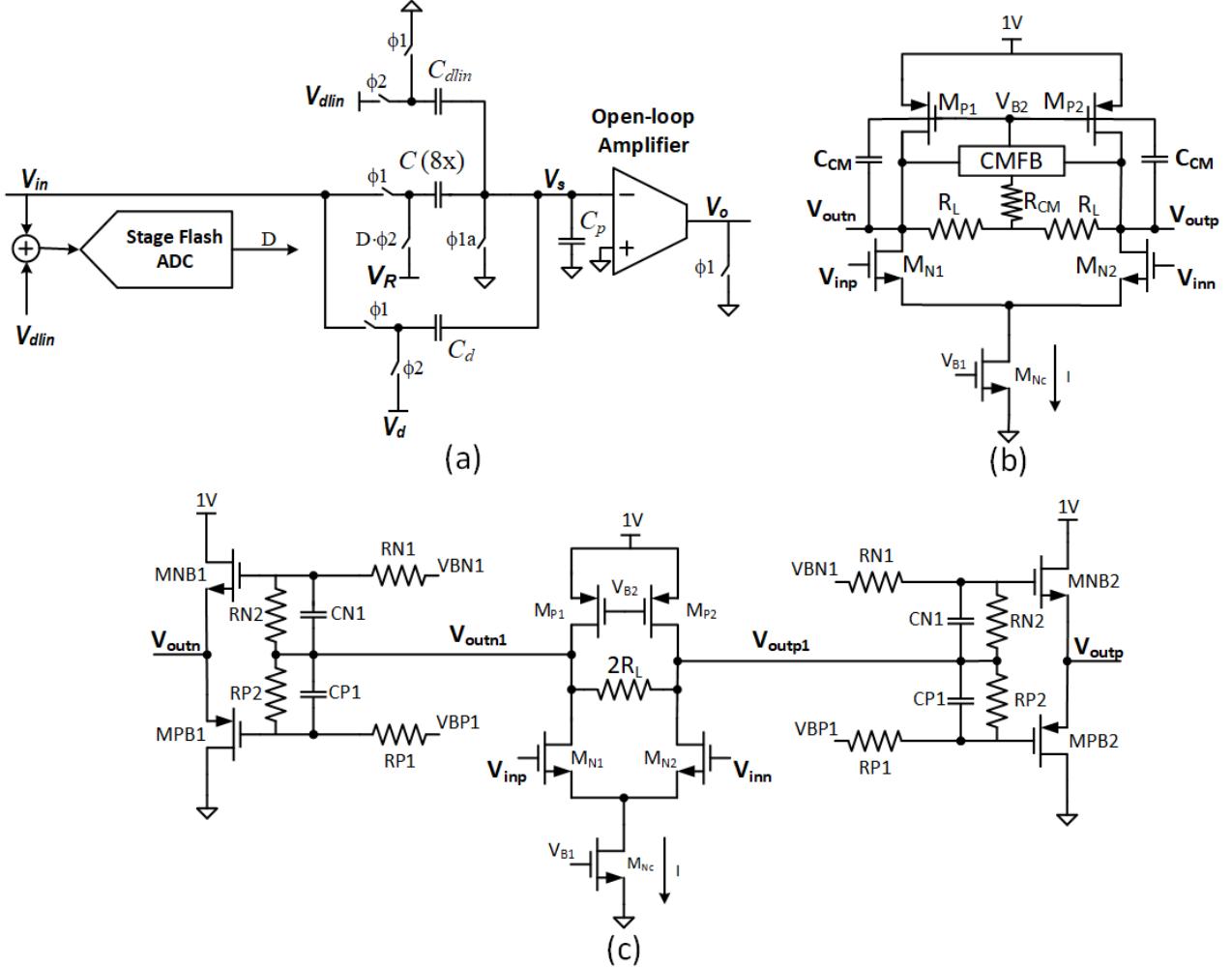


Fig. 5. Simplified diagrams of (a) pipeline stage, (b) inter-stage amplifier with the CMFB loop, and (c) inter-stage amplifier of the backend stages.

the input in a manner similar to the DAC kick-back and, hence, enable dither-based kick-back calibration of DAC code-dependent charge injection [6], [7]. This kick-back connectivity increases the load on the previous driving amplifier and, hence, is employed only in the output of the first stage, where the kick-back errors are significant.

The MDAC amplifier consists of a simple differential Gm-R amplifier, as shown in Fig. 5(b), whose third-order harmonic distortion to a single-tone sine wave is in the order of about 40 dB. Its common-mode feedback (CMFB) combines a switched-capacitor fast loop using the capacitors \$C_{CM}\$, with a slow feedback loop to ensure dc accuracy [7]. In the backend stages, the load is dominated by the parasitics, so a differential-pair buffered by a push-pull follower is used to improve the settling and reduce the power consumption, as shown in Fig. 5(c). The reference buffer is implemented as a stacked source follower [13]. The non-linearity of the amplifier, reference, DAC, and switches is background calibrated thereby detecting and correcting any arbitrary non-linearity in the stage.

To demonstrate the non-idealities of the circuit in Fig. 5(a), we apply charge conservation on the summing node

to obtain

$$V_{s1}[n] = \frac{C_1}{C_{t1}} V_{DAC1}[n] - \frac{C_1 + C_{d1}}{C_{t1}} V_{in1}[n] + \frac{C_{d1}}{C_{t1}} V_{d1}[n] + \frac{C_{dlin1}}{C_{t1}} V_{dlin1}[n] + \frac{\alpha_{m1} C_{p1}}{C_{t1}} V_{s1}[n-1] \quad (5)$$

where the suffix “1” indicates the components of stage 1, \$C_1\$ is the MDAC-1 capacitance, \$C_{d1}\$ is the calibration dither capacitance in MDAC-1, \$C_{dlin1}\$ is linearization dither capacitance, \$C_{p1}\$ is the parasitic capacitance on the summing node, \$C_{t1}\$ is the total capacitance on the summing node, and \$V_{DAC1}\$ is the DAC voltage, which is given by [7]

$$\begin{aligned} \frac{C_1}{C_1 + C_{d1}} V_{DAC1} &= f_{DAC1/Ref1}(D_{i1}, V_{in1}) \\ &= \sum_{i=1}^8 \frac{D_{i1} C_{i1}}{C_1 + C_{d1}} V_{R1}(D_{i1}, V_{in1}) \end{aligned} \quad (6)$$

where \$D_{i1}\$ is the \$i\$th bit of flash 1 thermometer code, \$C_{i1}\$ are the individual DAC capacitances whose sum is equal to \$C_1\$, and \$V_{R1}\$ is the code-dependent and input-dependent reference voltage of stage 1. The function \$f_{DAC1/Ref1}\$ represents the input-referred code-dependent DAC non-idealities and reference

non-linearity, which can be in the form of INL breaks and harmonic distortion due to the reference settling errors, charge injection, or other causes.

Note the difference between the DAC errors due to capacitance mismatches [the C_{i1} terms in (6)] versus those due to the reference errors [the V_{R1} terms in (6)]. Although the capacitance mismatch terms can be randomized by capacitance shuffling, the reference errors do not necessarily depend on the capacitance mismatch but rather on the total charge stored on the capacitance during the sample phase and on the DAC code, which determines the total number of capacitances connected to the positive or negative references. These charge injection and reference settling errors can exist in the absence of capacitor mismatches and can cause both INL breaks and harmonic distortion. This is more pronounced when the same capacitances are shared between the input sampling and the DAC operation, which is the case in this work.

If the output of the stage is given by $V_{o1}[n]$, we can obtain the input, or corrected output, from the output, by re-arranging and normalizing the terms in (5), while taking into account the reference/DAC non-linearity due to DAC errors, capacitance mismatch, or code-dependent reference settling errors to obtain

$$V_{in1}[n] = G_1 f_{NL1}^{-1}(V_{o1}[n]) - \alpha_{mt1} f_{NL1}^{-1}(V_{o1}[n-1]) + G_{d1} V_{d1}[n] + G_{dlin1} V_{dlin1}[n] + f_{DAC1/Ref1}(D_{i1}[n], V_{in1}[n]) \quad (7)$$

where f_{NL1} is the non-linear transfer function of the amplifier, which captures the collective input-referred non-linearity of all the blocks and circuits down-stream, G_1 , G_{d1} , and G_{dlin1} are the normalized gain terms for the residue, calibration dither, and linearization dither, respectively, and α_{mt1} is the normalized memory term.

The two non-linear functions f_{NL1}^{-1} and $f_{DAC1/Ref1}$ are detected and corrected by the DNLC background calibration algorithm as will be discussed in Section IV. In addition, the gain and memory components of the output voltage are detected by the inter-stage gain and memory calibration [3], [6], [7], [9].

IV. BACKGROUND CALIBRATION

As shown in Fig. 2, background calibration is employed to detect and correct the inter-stage gain, memory, kick-back, settling, and flash errors in the pipeline stages [3], [6], [7], [9]. In addition, dither-based non-linearity background calibration of harmonic distortion and arbitrary INL breaks (DNLC) is implemented for the THA and the first two stages of the sub-ADCs. Furthermore, for the THA, dither-based background calibration of the chopping, memory, and interleaving core mismatch errors (DCM²C) is employed.

Examples of calibration of harmonic distortion of pipeline inter-stage amplifiers in the literature are [10], [11]. As is usually the case, different algorithms have different tradeoffs. The calibration discussed in [10] utilizes dither injection in the flash of the pipeline stage to detect and correct the third-order non-linearity. Injecting the dither in the flash, instead of the MDAC, obviates the need to subtract the dither from the digital output. However, the calibration does not extend to reference and DAC non-linearities.

In [11] and [12], three calibration dither sequences are injected in the MDAC to calibrate the third-order distortion by detecting the resulting cross correlation between them in the digital domain. The use of cross correlation between multiple dither sequences removes the need for the presence of an input signal, which is an advantage. However, that non-linear calibration algorithm does not extend to correcting INL breaks due to arbitrary DAC and reference errors. A separate calibration algorithm was needed to calibrate the DAC errors due to capacitor mismatches only, but not DAC reference errors [11]. That additional algorithm requires randomly shuffling the DAC capacitances (i.e., dynamic element matching) to decorrelate the errors from the input and, hence, correct them. Since reference settling errors, as shown in (6) above, manifest themselves as DAC errors that can cause both INL breaks and low-order harmonic distortion even in the absence of capacitance mismatches, those INL breaks are not necessarily randomized by shuffling and may not be corrected by the algorithm in [11].

In this section, we discuss the new calibration algorithms: the DNLC and DCM²C. These algorithms utilize the same analog infrastructure employed to enable the calibration of the inter-stage gain and memory errors [6] to substantially expand the scope of the calibrated errors using a single calibration dither sequence without adding additional analog complexity. The DNLC represents a new comprehensive framework to calibrate arbitrary non-linearities in the discrete-time domain including harmonic distortion up to the fifth order and arbitrary INL breaks due to DAC and reference errors. The DCM²C represents a framework to calibrate memory, chopping, gain, and offset mismatches in an interleaved switched capacitor THA or pipeline stage with a shared buffer/amplifier in the context of interleaved sequential or randomized operation. For more details about the other calibrations implemented in this work, the reader can refer to [1], [3], [6], and [7].

A. Dither-Based Non-Linearity Calibration

The DNLC concept is based on the fact that a single-bit dither when added to the input signal can effectively expose non-linear behavior. After subtracting the dither from the output, unlike a linear system where superposition applies, a non-linear system gives different outputs depending on the dither polarity. That is,

$$f(x + V_d) - \widehat{V}_d \neq f(x - V_d) + \widehat{V}_d \quad (8)$$

where x is the input, $f()$ is a non-linear function, V_d is a 1-bit dither sequence, and \widehat{V}_d is the dither estimate at the output.

To quantify this non-linearity, correlation-based algorithms can be employed. However, applying correlation using all the digital samples would typically detect the overall gain that minimizes the squared error between the corrected output and the actual output. Instead, since non-linearity implies a transfer characteristic that has input-dependent gain or different gains for different segments of the transfer characteristics, detection of this non-linearity needs to incorporate segment-based (or threshold-based) correlation.

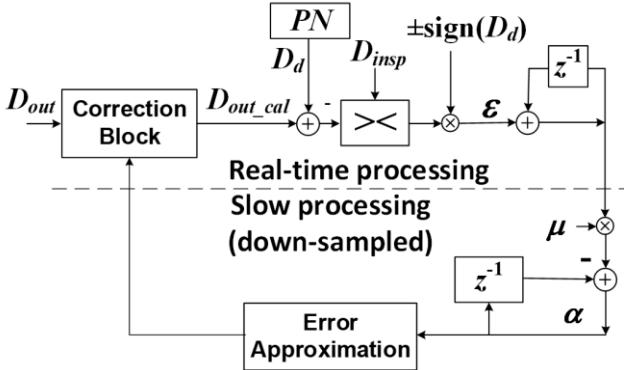


Fig. 6. Conceptual block diagram of the DNLC estimation.

To achieve this goal, we use thresholded correlation over half-bounded segments (intervals) in the digital domain to estimate the error, as shown conceptually in Fig. 6. This is a distinguishing aspect of this algorithm compared to the prior art and it enables the use of a single dither sequence for correlation instead of multiple dither sequences [11], [15]. In order for these thresholded correlations to effectively extract the non-linearity, the threshold points (hereby called “inspection points”) need to be selected in a way that exposes the non-linearity under investigation, based on the digital code after the dither estimate is subtracted. They also need to be adaptively updated by the algorithm to continue satisfying this condition as the calibration progresses and the conditions change.

The correlation can be implemented using real-time multiplication of the samples’ digital code with the dither or using normalized counting, similar to the sign-sign least mean square (LMS) algorithm, as shown conceptually in Fig. 6. The latter is used in this work to simplify the calculations, lower power consumption, and to localize the estimates around the inspection points, while being less sensitive to remote points. The block marked by “><” in Fig. 6 represents the determination of whether the sample satisfies the condition of being above or below the inspection point D_{insp} . In a full-multiplication implementation, the output of this block is the full digital code of the samples that satisfy the inspection condition and 0 for the samples that do not satisfy the inspection condition. Alternatively, in the normalized counting implementation, the output of the “><” block is 1 if the sample satisfies the inspection condition and 0 otherwise.

After correlation, the error ϵ is accumulated, and after multiplication by the step size μ in the slow-processing domain, it generates the calibration coefficient α . The error approximation block estimates the correction coefficients that need to be fed back and applied to the output samples at the full rate. The details of the error approximation and correction will be discussed in the remainder of this section.

This comprehensive framework shown in Fig. 6 is employed to detect and calibrate the non-linearities in the form of INL breaks and harmonic distortion of the whole ADC and within the sub-ranges of the ADC as illustrated conceptually in an exaggerated manner in Fig. 7 and as will be discussed in the remainder of this section.

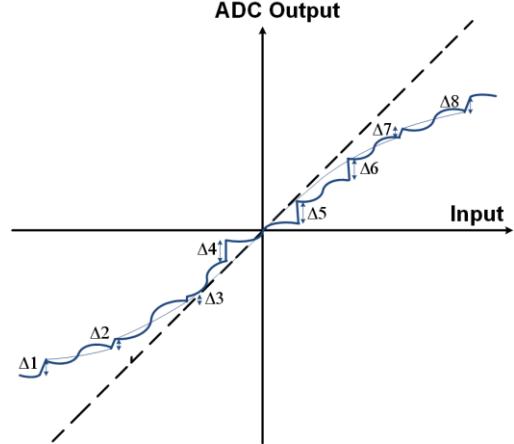


Fig. 7. Conceptual and exaggerated demonstration of an arbitrary non-linearity that is calibratable by the DNLC algorithm. The transfer characteristic shows breaks at the boundaries of the stage sub-ranges (INL breaks Δ_i), harmonic distortion within each sub-range, and harmonic distortion (compression) in the whole transfer characteristic.

1) INL Breaks: Breaks in the INL or transfer characteristic of a multistep ADC (such as pipeline and pipeline-SAR ADCs) typically happen at the sub-range boundaries of the stage DACs. Regardless of whether they are caused by capacitor mismatches, charge injection, reference settling errors, or otherwise, the DNLC algorithm detects and corrects those breaks in the background. If the input is in the vicinity of the break before dither is added, the addition of the calibration dither causes the signal to cross the INL break and, thus, experience different gains and, hence, different correlations/counts, depending on the dither polarity. Therefore, the input samples that are in the vicinity of the INL breaks, before the dither addition, qualify as valid threshold/inspection points for exposing and correcting these breaks. The algorithm adaptively locates these inspection points in the background after the dither estimate is subtracted in the digital domain to expose the breaks between neighboring sub-ranges. If there are nine sub-ranges, eight inspection points are created (D_{insp_1} to D_{insp_8}) as shown in Fig. 8. The correlation/counting is done over open segments up to the key inspection/threshold points. Using the average count differences based on the dither bit sign with the proper normalization, the algorithm shifts the sub-ranges as shown in Fig. 6 until the breaks are eliminated with the desired accuracy, while adaptively updating the inspection points to stay within the vicinity of the INL breaks, which is a key condition for robust error detection. For the error between the i th and $(i+1)$ th sub-ranges, the estimation of the parameter α_{DAC_i} shown conceptually in Fig. 6 can be represented by

$$\alpha_{DAC_i}[n+1] = \alpha_{DAC_i}[n] - \mu (\text{sign}(D_d)|_{D_{out_cal} - D_d < D_{insp_i}}) \quad (9)$$

where the term $(x|_y)$ is equal to x if y is true and 0 otherwise, μ is the algorithm step size, D_d is the digital dither bit, D_{insp_i} is the i th inspection point, and D_{out_cal} is the calibrated digital output, which is given by

$$D_{out_cal} = \alpha_1 D_{out} + \sum_{i=1}^{2^N_k} \alpha_{DAC_i}|_{(D_k=i+1)} \quad (10)$$

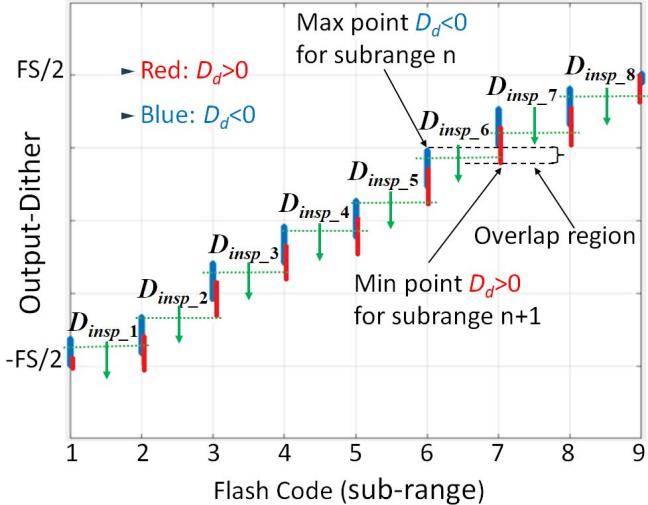


Fig. 8. Inspection points ($D_{\text{insp},1}$ to $D_{\text{insp},8}$) for the calibration of INL breaks shown as y-axis values for different sub-range transitions.

where D_{out} is the uncalibrated digital output, α_1 is the gain coefficient, N_k is the number of bits of the k th stage ($N_k = 3$ in this case), the term $(x|_y)$ is equal to x if y is true and 0 otherwise, $(D_k = i + 1)$ is true if the flash code of the k th stage (D_k) indicates that the sample is in the $(i + 1)$ th sub-range, and $\alpha_{\text{DAC},i}$ is an additive parameter used to shift the $(i + 1)$ th sub-range relative to the i th sub-range to correct the break in the transfer characteristic. Therefore, (9) and (10) continuously estimate the INL breaks and shift the sub-ranges to correct the errors to the desired accuracy.

In order to adaptively locate the inspection points, the algorithm identifies the minimum and maximum points of each sub-range based on the dither polarity such that

$$D_{\text{insp},i} \in \left\{ \left\{ (D_{\text{out}_{\text{cal}}} - D_d) \mid |_{D_d < 0 \text{ AND } D_k=i} \right\} \right. \\ \left. \cup \left\{ (D_{\text{out}_{\text{cal}}} - D_d) \mid |_{D_d > 0 \text{ AND } D_k=i+1} \right\} \right\} \quad (11)$$

where $\{x|_y\}$ is the set of samples whose values are equal to x if y is true and is the empty set {} if y is false. The sets/regions shown in Fig. 8 and described by (11) represent ranges of values that are valid for the inspection/threshold points to detect the break between sub-ranges i and $i + 1$. The boundaries can be detected in the digital domain using digital peak and trough detectors of each sub-range for each dither state [3], [7]. That is, the overlap region between the maximum point of sub-range i when the dither is negative and the minimum (trough) point of sub-range $i + 1$ when the dither is positive. These sub-range boundaries are obtained as part of the flash offset calibration implemented in this work and described in [3] and [7] and, hence, do not require substantial additional hardware.

2) *Harmonic Distortion:* In addition to the INL breaks, the DNLC algorithm concurrently detects and corrects any overarching harmonic distortion up to the fifth-order distortion. This is accomplished by using the correlations/counts both above and below inspection/threshold points, whose magnitudes are large enough to detect the specific harmonic, by exposing the differences in the local non-linear

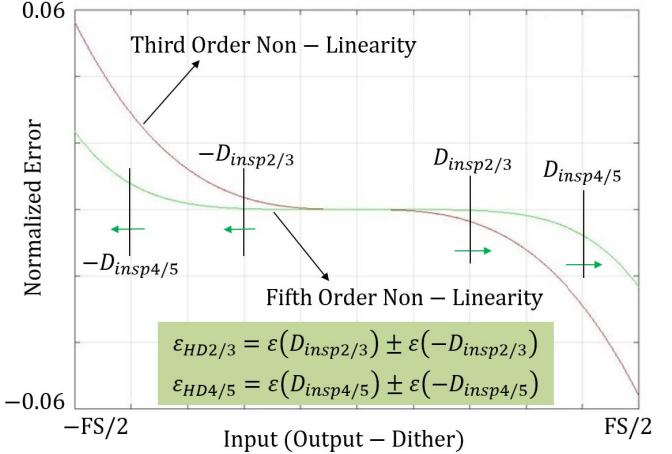


Fig. 9. Inspection points for the calibration of the harmonic distortion shown as x-axis values on a plot of the normalized distortion error versus the input or (Output - Dither).

(compressed) gain relative to the gain near zero obtained using counts with zero as the threshold. Overall, four threshold/inspection points (two symmetric pairs: $\pm D_{\text{insp}2/3}$ and $\pm D_{\text{insp}4/5}$) are needed to detect up to the fifth order.

The inspection points' symmetry distinguishes between even- and odd-order harmonics. Moreover, the inspection points for the 2nd/3rd-order distortion ($\pm D_{\text{insp}2/3}$) are smaller in magnitude than those for the fourth/fifth order ($\pm D_{\text{insp}4/5}$) to expose the sharper compression of the higher order distortions shown in Fig. 9. This sharp compression of the fourth-/fifth-order distortion that tends to rapidly disappear as the amplitude decreases necessitates a large inspection point, preferably high in the upper quarter of the dynamic range, to ensure correct estimation of the non-linearity, as shown in Fig. 9. In general, larger inspection points lead to relatively larger error measures ε that are easier to detect but may have lower signal activity (i.e., hits) because of their large magnitude, which leads to higher percentage of samples being thrown out.

Although the inspection points for the INL breaks must be adaptively adjusted as the convergence progresses, and sub-range boundaries move, to continue satisfying their respective conditions, the inspection points for the harmonic distortion do not need such adaptation. However, if the inspection points are located at relatively large amplitudes that the number of useful samples is small or, even worse, non-existent for a long period of time, the algorithm can slowly move them to smaller magnitudes where the signal activity can adequately exercise the inspection points, while satisfying the symmetry conditions.

It is interesting to note that the odd/even symmetries of the inspection points capture the fundamental characteristics of the non-linearities in order to detect the various non-idealities of the real circuit correctly. These fundamental characteristics do not change depending on the symmetry (or lack thereof) of the real circuit's characteristics or of the input signal. For example, the presence of an offset in the analog transfer characteristics or in the input signal breaks the symmetry of the circuit and the output signal but does not change the fundamental symmetric

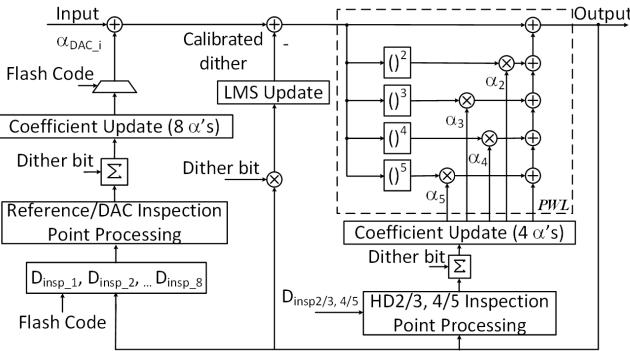


Fig. 10. Conceptual block diagram of the DNLC algorithm.

nature of the non-linearity and, hence, does not cause problems with the algorithm. In that case, the signal would exercise an asymmetric portion of the non-linearity but the algorithm still detects that non-linear behavior correctly, as long as the inspection points are symmetric and are exercised adequately and, hence, generates a corrected linearized output signal with an offset as expected.

The estimation of the harmonic distortion coefficients (α_j) is shown conceptually in Fig. 6 and can be represented as

$$\alpha_j[n+1] = \alpha_j[n] - \mu_j \times \varepsilon_{HDj} \quad (12)$$

where j is the order of distortion and can range from 2 to 5. As shown in Fig. 9, the errors $\varepsilon_{HDj/k}$ can be given by

$$\varepsilon_{HDj/k} = \varepsilon(D_{inспj/k}) \pm \varepsilon(-D_{inспj/k}) \quad (13)$$

where j/k can be 2/3 or 4/5 for the second-/third- and fourth-/fifth-order distortion, respectively. The addition in (13) is used for the even-order distortion, which has even symmetry, and the subtraction is used for the odd-order distortion, which has odd symmetry. As shown in Fig. 6, this error calculation can be done using full multiplication or counting. When using counting, it can be represented as

$$\begin{aligned} \varepsilon_{HDj/k} &= \text{sign}(D_d)|D_{out_cal} - D_d| - D_{inспj/k} \\ &\quad \pm \text{sign}(D_d)|D_{out_cal} - D_d| + D_{inспj/k}. \end{aligned} \quad (14)$$

Once the coefficients α_j are estimated, the algorithm uses a polynomial fit to estimate the errors at a much lower rate, while the correction is done at the full rate using additive piecewise linear segments to reduce the power consumption

$$\begin{aligned} D_{out_cal} &= \alpha_1 D_{out} + \text{PWL}(\alpha_2 D_{out}^2 + \alpha_3 D_{out}^3 + \alpha_4 D_{out}^4 \\ &\quad + \alpha_5 D_{out}^5 + \text{higher order terms}) \end{aligned} \quad (15)$$

where D_{out} is the uncalibrated digital output, D_{out_cal} is the calibrated digital output, PWL is a piecewise linear approximation of the polynomial function, and the higher order terms are added to cancel the high-order non-linear terms introduced by the correction itself.

3) *DNLC Algorithm:* The overall DNLC algorithm detects and corrects both the INL breaks and harmonic distortion up to the fifth order and is represented conceptually in Fig. 10

and can be expressed as

$$D_{out_cal} = \alpha_1 D_{out} + \sum_{i=1}^{2^N_k} \alpha_{DAC_i} |_{(D_k=i+1)} + \text{PWL} \left(\sum_{j=2}^{j_{\max}} \alpha_j D_{out}^j \right) - D_d \quad (16)$$

where α_1 is the gain coefficient, α_{DAC_i} is the DAC coefficient of the i th sub-range, D_k is the flash code of the k th stage and N_k is its number of bits, α_j is the coefficient of the j th-order distortion, j_{\max} is the highest power included in the polynomial, and D_d is the dither.

In Fig. 10, the “Inspection Point Processing” blocks determine whether the samples satisfy the inspection point conditions as represented by the “ $><$ ” block in Fig. 6. The outputs of these blocks are the whole digital code of the sample (in the full-multiplication implementation) or the sign bit of the sample (in the counting implementation). The “ Σ ” blocks perform the correlation with the dither and accumulation, and the “Update” blocks perform the multiplication with the step size μ and the update of the α calibration coefficients, as shown in Fig. 6.

The convergence of the DNLC algorithm requires about 2^{30} and 2^{26} samples to achieve the desired performance for the THA and the first stage’s residue, respectively. Since the correlation of the DNLC algorithm uses a single dither sequence as shown in Fig. 10, this dither sequence can be m -times larger compared to algorithms that rely on cross-correlations between m dither sequences occupying the same dynamic range budget for the total calibration dither, where m has to be equal to or higher than the order of the harmonic distortion to be calibrated [11]. This helps the convergence time/accuracy and sensitivity to higher order and backend non-idealities [6], [12], [15].

Since the DNLC algorithm is dither based, it is relatively independent of the input signal’s distribution. However, if the input signal is absent or too small to adequately exercise some inspection points or INL breaks, the calibration coefficients corresponding to those calibrations and sub-range boundaries will not be updated. While the linearization dither can generate enough activity to keep the 2nd-/3rd-harmonic distortion portion of the DNLC active in the absence of an input signal, its amplitude may not be large enough for the fourth/fifth harmonic distortion of the THA or to be in the vicinity of all the DAC sub-range boundaries in the first stage. Therefore, the updates to those coefficients of the algorithm will automatically freeze until an input signal creates enough activity in the vicinity of the corresponding inspection points.

B. Dither-Based Chopping, Memory, and Core Mismatch Calibration

Fig. 11 shows a conceptual simplified diagram of the estimation of the memory, offset, and gain parameters of the THA in the digital domain. These parameters represent the cumulative effect of the THA circuit as well as all the blocks that follow, including the sub-ADCs. While the offset is estimated by low-pass filtering, the memory and gain are estimated by correlating with the previous and present dither

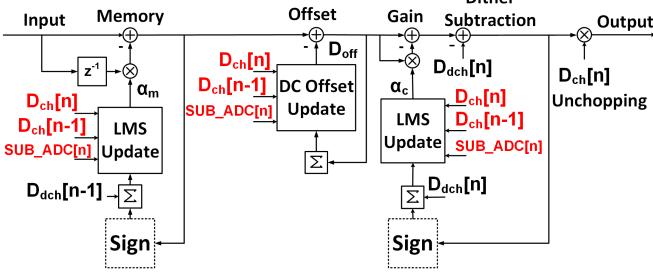


Fig. 11. Conceptual block diagram of the DCM^2C algorithm. The “Sign” blocks are optional. D_{dch} is the product of the dither bit D_d and the chopping bit D_{ch} . The correlation, accumulation, and update blocks are shown dependent on the present and past chopping states, and the present sub-ADC, but they can also depend on the present/past track.

samples, respectively. The memory error is corrected using a single-tap FIR filter. Calibrating the chopping non-idealities is achieved by binning the estimations and corrections based on the chopping bit as shown in Fig. 11, where the samples are automatically sorted by the algorithm during the correlation, accumulation, update, and correction steps into bins based on the chopping state for that particular sample. This ensures the estimation and correction of the offset, gain, and memory mismatches between the two chopping paths before un-chopping in the digital domain. In addition, by binning the estimation and correction based on the previous chopping state and sample network used, the algorithm detects and corrects order-dependent errors in the THA. Moreover, by binning further based on which sub-ADC is used, the algorithm can detect and correct the offset, gain, and memory for every sub-ADC individually and, therefore, calibrate the mismatches between the interleaved sub-ADCs. This interleaving calibration and the DCM^2C algorithm are chopping- and dither-based and, therefore, can be independent of the input signal.

As shown in Fig. 11, the offset $D_{\text{off},i,j,k}$ can be estimated conceptually as follows:

$$D_{\text{off},i,j,k}[n+1] = D_{\text{off},i,j,k}[n] + \mu_{\text{off}} \cdot (D_s[n] - D_{\text{off},i,j,k}[n]). \quad (17)$$

The gain error coefficient $\alpha_{c,i,j,k}$ can be estimated, as shown conceptually in Fig. 11, using the sign-sign LMS as follows:

$$\begin{aligned} \alpha_{c,i,j,k}[n+1] &= \alpha_{c,i,j,k}[n] + \mu_c \cdot D_d[n] \cdot D_{\text{ch}}[n] \\ &\quad \cdot \text{sign}(D_s[n] - \alpha_{c,i,j,k}[n] \cdot D_s[n] - D_d[n] \cdot D_{\text{ch}}[n]). \end{aligned} \quad (18)$$

Similarly, for the memory coefficient $\alpha_{m,i,j,k}$

$$\begin{aligned} \alpha_{m,i,j,k}[n+1] &= \alpha_{m,i,j,k}[n] + \mu_m \cdot D_d[n-1] \cdot D_{\text{ch}}[n-1] \\ &\quad \cdot \text{sign}(D_s[n] - \alpha_{m,i,j,k}[n] \cdot D_s[n-1]) \end{aligned} \quad (19)$$

where $D_s[n]$ is the digital code corresponding to the summing node voltage of the THA, $D_d[n]$ is the dither code, $D_{\text{ch}}[n]$ is the chopping code, μ_{off} , μ_c , and μ_m are the step sizes, and $D_{\text{off},i,j,k}$, $\alpha_{c,i,j,k}$, and $\alpha_{m,i,j,k}$ are the offset, gain, and memory coefficients that depend on the chopping state i , the track used j , and the sub-ADC used k . The “sign” functions/blocks are optional and their outputs are the sign bit of the digital code, as implemented in this work. However, the whole digital code

can be used instead if a full-multiplication implementation is preferred to eliminate the dependence on the input signal. By binning these coefficients further based on the previous state, they can capture dependence on the previous sub-ADC, track, or chopping state.

The convergence of the offset, gain, and memory calibration of the DCM^2C algorithm requires about 2^{30} samples. It is interesting to note that the THA’s DNLC correction can influence the gain estimated by the DCM^2C algorithm. As the DNLC converges with the desired accuracy, the gain parameter converges accordingly, such that both algorithms converge simultaneously. Moreover, since the non-linearity correction can be sub-ADC dependent, correcting for the non-linearity mismatch by binning the DNLC calibration based on the sub-ADC used corrects the non-linearity interleaving mismatches and improves the core gain mismatch calibration accuracy at the expense of convergence time.

When binning is employed to account for the present and previous chopping states, tracks, and sub-ADCs, as shown in Fig. 11, the convergence time can increase. However, since not all state combinations are unique, the total number of bins can be reduced. For example, since the states of the THA and the sub-ADCs are independent, the binning can be combined. That is, the same samples can be used in more than one bin. Therefore, when using a single track with chopping and four sub-ADCs, we have four states for the present and previous chopping states or four states for the sub-ADCs, instead of 16 unique states. This increases the convergence time by a factor of 4 (instead of 16) to about 2^{32} . Similarly, for the ping-pong THA with chopping driving eight sub-ADCs, we have eight THA states or eight sub-ADC states, which increase the convergence time by a factor of 8 (instead of 64) to about 2^{33} . This represents a convergence time of less than 1 s at the sampling rates covered by this work.

For all the calibrations including both the DNLC and DCM^2C algorithms, it is important to desensitize the convergence of a stage to the non-idealities in the subsequent stages. This is achieved in part by the calibration of the backend non-idealities. In addition, additional/linearization dither, whose amplitude is equal to \pm half a sub-range as shown in Fig. 3, helps improve the calibration’s accuracy and robustness in the presence of residual backend non-idealities [6], [14].

V. RESULTS

The ADC is implemented in 16-nm FinFET process. The die photograph is shown in Fig. 12, which shows the THA with three tracks, eight sub-ADCs, the clocking, biasing, and digital clocks. The area of the sub-ADC is about 0.06 mm^2 and the total area is about 2.6 mm^2 . It can operate in 1-, 2-, 4-, or 8-way interleaved modes. In addition, the THA can be configured in a single track, ping-pong, or randomized 2 + 1 modes with chopping and randomization enabled or disabled.

To demonstrate the impact of the THA and sub-ADC calibrations, Fig. 13(a) shows a measured INL without any calibrations where the errors are in the order of 100–150 LSBs. Fig. 13(b) shows an INL with all the calibrations turned on except the non-linear calibration of the THA. We can observe

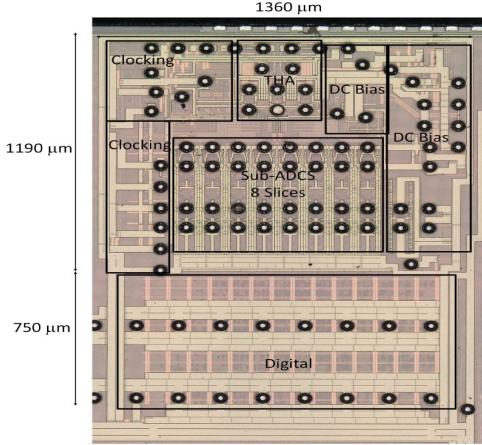


Fig. 12. Die photograph.

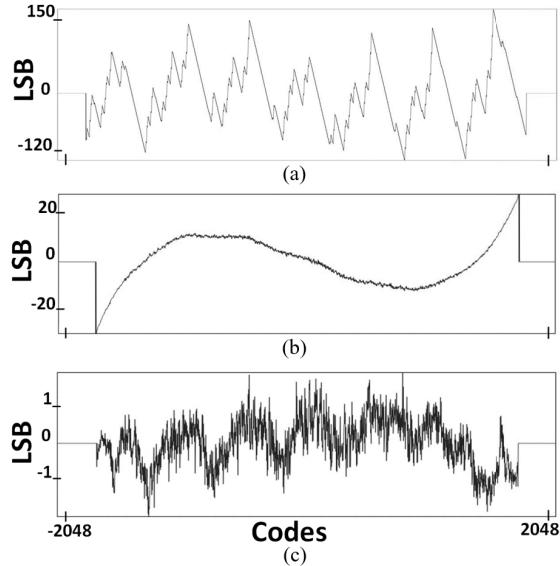


Fig. 13. Measured INL (a) without calibration, showing INL breaks and harmonic distortion, (b) with all calibrations except non-linear correction of the THA, and (c) with all calibrations and non-linear correction of the THA.

a large third-order distortion due to the non-linearity of the THA. Fig. 13(c) shows an INL with all the calibrations and the non-linear correction of the THA, where the INL is corrected to the order of about 2 LSBs.

Figs. 14 and 15 show the performance versus sample rate and input frequency, respectively. Up to 10 GS/s, the THA can operate at the full sample rate using a non-interleaved single track. Up to 18 GS/s, the THA operates in the ping-pong mode.

Fig. 16 shows an approximate normalized magnitude response to demonstrate the ADC input bandwidth of 18 GHz. Fig. 17 shows an output spectrum at 10 GS/s with the THA operating at the full sample rate driving four sub-ADCs each operating at 2.5 GS/s. Fig. 18 shows an output spectrum at 18 GS/s with an input frequency of 10 GHz and with the THA in the ping-pong mode driving eight sub-ADCs each operating at 2.25 GS/s.

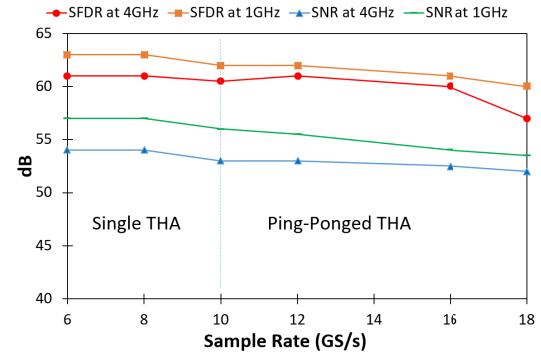


Fig. 14. Measured performance versus sample rate.

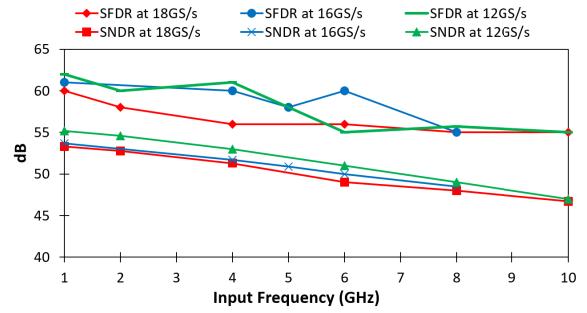


Fig. 15. Measured performance versus input frequency.

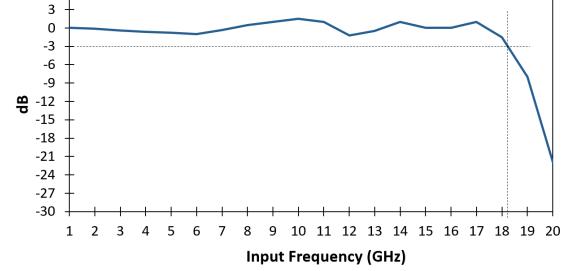


Fig. 16. Measured ADC input bandwidth of approximately 18 GHz.

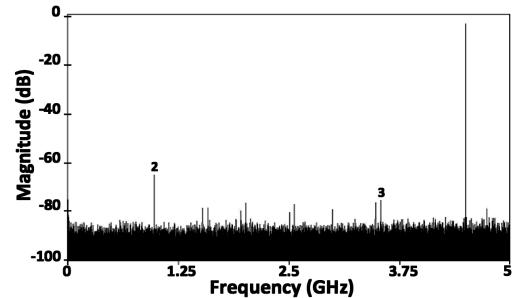


Fig. 17. Output spectrum at 10 GS/s and 4.5-GHz input frequency using a single full-rate THA driving four sub-ADCs.

To demonstrate the effect of chopping and randomization, Fig. 19 shows a spectrum, with residual and uncalibrated interleaving spurs, and without chopping or randomization. Fig. 20 shows the effect of chopping in the THA. It is interesting to note the offset spurs in Fig. 19 highlighted by

TABLE I
COMPARISON OF THIS WORK WITH THE STATE-OF-THE-ART

	This Work				[1]	[2]	[3]	[4]
Sampling Rate (Fs)	18 GS/s	10 GS/s	10 GS/s	8 GS/s	5 GS/s	5 GS/s	5 GS/s	5 GS/s
Resolution (bits)	12	12	12	10	14	13	-	-
Input BW (GHz)	18	18	7.4	4	5	-	-	-
Power (W)	1.3	0.75	2.9	0.3	2.3	0.64	-	-
Noise Floor (dBFS/Hz)	-157	-157	-157	-154	-157	-156	-	-
Fin (GHz)	4	8	2.5	4	4	2	2.5	2.5
SNDR at Fin (dB)	52	48	55	53.5	55	58	57	57
SFDR at Fin (dB)	56	54	65	65	64	70	61.9	-
Schreier FOM (dB): FOMS_HF=SNDR+10log(Fs/(2*Power))	150.4	146.4	153	151.5	147.4	150.2	148.4	152.9
Walden FOM (fJ/step): FOMW_HF=Power/(Fs*10^(SNDR-1.76)/20)	222	351.9	163.2	194	631.2	162.9	708.7	221.6
THA or input buffer	THA		THA		Buffer	None	Buffer	Buffer
Sampling time and BW mismatch	2-way or optional randomized (2+1)		Full-speed or 2-way or optional randomized (2+1)		8-way or optional randomized (7+1)	16-way	2-way	8-way
Sub-ADC	Pipeline		Pipeline		Pipeline	SAR	Pipeline	Pipe-SAR
Area	2.6		2.6		7.4	0.184 (analog only)	14.4	1.1
Process Technology	16nm FinFET		16nm FinFET		28nm	28nm FDSOI	28nm	16nm FinFET

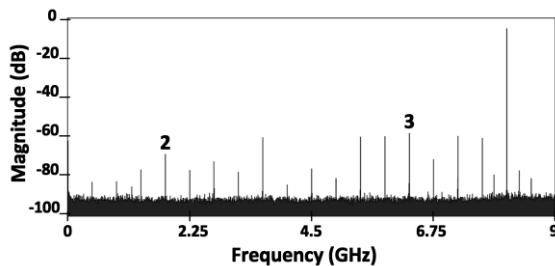


Fig. 18. Output spectrum at 18 GS/s and 10-GHz input frequency using ping-pong THA driving eight sub-ADCs.

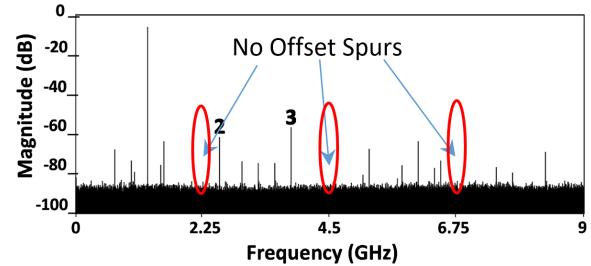


Fig. 20. Output spectrum at 18 GS/s and 1.3-GHz input frequency using ping-pong THA driving eight sub-ADCs with chopping ON.

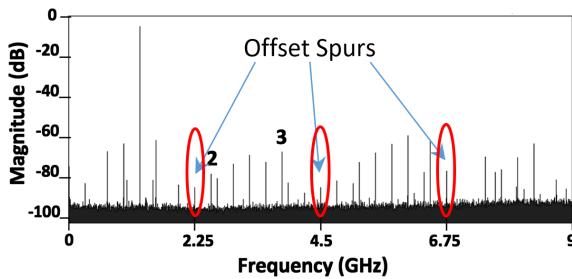


Fig. 19. Output spectrum at 18 GS/s and 1.3-GHz input frequency using ping-pong THA driving eight sub-ADCs without chopping or randomization.

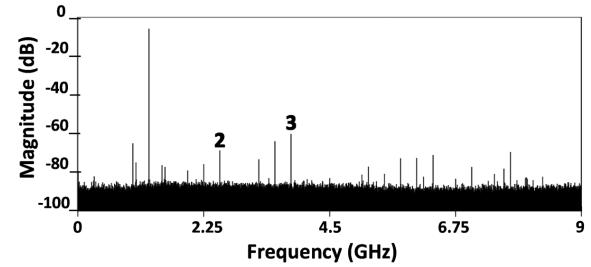


Fig. 21. Output spectrum at 18 GS/s and 1.3-GHz input frequency with THA randomization ON.

the ellipses, because they do not scale down with reducing the input amplitude. Those spurs are eliminated in Fig. 20 because of the pseudorandom chopping. Fig. 21 shows the effect of randomization in the THA, which spreads the interleaving spurs

due to the THA interleaving mismatches in the noise floor. In addition, it randomizes the interaction between the tracks and the sub-ADCs, which helps reduce some of the other spurs as well. However, any residual spurs due to the interleaving mismatch errors between the sub-ADCs will still exist.

The power consumption is about 1.3 W at 18 GS/s. The THA consumes about 220 mW, each sub-ADC consumes about 60 mW, and the clocking and the digital consume about 600 mW. Approximate comparison with the state-of-the-art is shown in Table I. This ADC is 80% faster with an input bandwidth that is $2.4\times$ larger than the fastest prior art with similar performance. It also compares well in terms of figures-of-merit at similar sampling rate and input frequency. In addition, this ADC has an integrated THA that eliminates the timing and bandwidth mismatch up to 10 GS/s and improves it substantially above 10 GS/s from eight-way mismatch to two-way mismatch.

VI. CONCLUSION

We presented a 12-b 18-GS/s interleaved pipeline ADC with an integrated wideband THA implemented in 16-nm FinFET process. The THA can sample at the full rate of the ADC up to 10 GS/s and operates in ping-pong or an optional randomized (2 + 1) mode up to 18 GS/s. The interleaved sub-ADCs can operate in 8-, 4-, or 2-way interleaved modes. The ADC has an input bandwidth of 18 GHz and employs optional pseudorandom chopping and dither injection to calibrate the offset and gain mismatch between the sub-ADCs. Digital background calibration algorithms were developed and implemented to linearize the THA and pipeline stages, thereby correcting for INL breaks and harmonic distortion. Chopping and order-dependent non-idealities are also calibrated.

ACKNOWLEDGMENT

The authors would like to acknowledge the contributions of P. Gulati, M. Kumar, R. Bunch, S. Dabaghv, S. Prabhu, S. Pasad, L. Noonan, C. Block, T. Freeman, J. Vanhoy, E. Otte, V. Sarma, H. Zhu, S. Hattangady, U. Mehta, R. Shumovich, W. Yang, B. Luu, D. Rey-Losada, F. Murden, L. Singer, D. Kelly, B. Babjak, J. Brunsilius, A. Morgan, R. Sneed, and J. Dispirito and the support of K. Tam, D. Robertson, R. Stop, T. Montalvo, C. Petersen, S. Harston, J. Bankman, S. Devarajan, and the others who supported or contributed to this work. They would also like to thank the anonymous reviewers and the Guest Editor for the constructive feedback that helped improve the quality of this article.

REFERENCES

- [1] S. Devarajan *et al.*, “16.7 a 12b 10GS/s interleaved pipeline ADC in 28nm CMOS technology,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 288–289.
- [2] J. P. Keane *et al.*, “16.5 an 8GS/s time-interleaved SAR ADC with unresolved decision detection achieving 58dBFS noise and 4GHz bandwidth in 28nm CMOS,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2017, pp. 284–285.
- [3] A. M. A. Ali *et al.*, “A 14-bit 2.5GS/s and 5GS/s RF sampling ADC with background calibration and dither,” in *Proc. IEEE Symp. VLSI Circuits (VLSI-Circuits)*, Jun. 2016, pp. 206–207.
- [4] B. Vaz *et al.*, “A 13Bit 5GS/S ADC with time-interleaved chopping calibration in 16NM FinFET,” in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. 99–100.
- [5] A. M. A. Ali *et al.*, “16.1 a 12b 18GS/s RF sampling ADC with an integrated wideband Track-and-Hold amplifier and background calibration,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 250–252.
- [6] A. M. A. Ali *et al.*, “A 14 bit 1 GS/s RF sampling pipelined ADC with background calibration,” *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2857–2867, Dec. 2014.

- [7] A. M. A. Ali, *High Speed Data Converters*. London, U.K.: Institution of Engineering and Technology (IET), 2016.
- [8] B. Setterberg *et al.*, “A 14b 2.5GS/s 8-way-interleaved pipelined ADC with background calibration and digital dynamic linearity correction,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 466–467.
- [9] J. P. Keane, P. J. Hurst, and S. H. Lewis, “Digital background calibration for memory effects in pipelined analog-to-digital converters,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 3, pp. 511–525, Mar. 2006.
- [10] B. Murmann and B. E. Boser, “A 12-bit 75-MS/s pipelined ADC using open-loop residue amplification,” *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2040–2050, Dec. 2003.
- [11] A. Panigada and I. Galton, “A 130 mW 100MS/s pipelined ADC with 69dB SNDR enabled by digital harmonic distortion correction,” in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 162–163.
- [12] A. Panigada and I. Galton, “Digital background correction of harmonic distortion in pipelined ADCs,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 9, pp. 1885–1895, Sep. 2006.
- [13] H. Dinc and A. M. A. Ali, “Reference buffer with wide trim range,” U.S. Patent 9 397 682 B2, Jul. 19, 2016.
- [14] S. G. Bardsley *et al.*, “Pipelined converter systems with enhanced linearity,” U.S. Patent 7 719 452 B2, May 18, 2010.
- [15] N. Rakuljic and I. Galton, “Suppression of quantization-induced convergence error in pipelined ADCs with harmonic distortion correction,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 3, pp. 593–602, Mar. 2013.
- [16] B. Murmann and B. E. Boser, “Digital domain measurement and cancellation of residue amplifier nonlinearity in pipelined ADCs,” *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2504–2514, Dec. 2007.
- [17] E. Siragusa and I. Galton, “A digitally enhanced 1.8-V 15-bit 40-MSample/s CMOS pipelined ADC,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.
- [18] A. M. A. Ali, “Track and hold circuits for high speed and interleaved ADCS,” U.S. Patent 10 608 654 B2, May 2, 2019.
- [19] A. M. A. Ali and P. Gulati, “Background calibration of reference, DAC, and quantization non-linearity in ADCS,” U.S. Patent 10 547 319 B2, May 2, 2019.
- [20] A. M. A. Ali and P. Gulati, “Background calibration of non-linearity of samplers and amplifiers in ADCS,” U.S. Patent 2019 024 555 A1, Aug. 8, 2019.
- [21] A. M. A. Ali *et al.*, “Calibrating time-interleaved switched-capacitor track-and-hold circuits and amplifiers,” U.S. Patent 20 190 305 791 A1, Oct. 3, 2019.
- [22] A. M. A. Ali and B. S. Puckett, “Background calibration of random chopping non-idealities in data converters,” U.S. Patent 20 190 273 505 A1, Feb. 1, 2019.
- [23] A. M. A. Ali, “Low power amplifier structures and calibrations for the low power amplifier structures,” U.S. Patent 20 190 296 756 A1, Sep. 5, 2019.



Ahmed M. A. Ali (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees (Hons.) in electrical engineering from Ain Shams University, Cairo, Egypt, in 1991 and 1994, respectively, and the Ph.D. degree in electrical engineering from the University of Pennsylvania, Philadelphia, PA, USA, in 1999.

His past industrial experience includes Texas Instruments, Warren, NJ, USA, Anacad, Ulm, Germany, and Cairo, Egypt, and Siemens AG, Erlangen, Germany. He was an Adjunct Assistant Professor with the University of Pennsylvania. He is currently a fellow with Analog Devices, Inc., Greensboro, NC, USA, where he has led the design and development of several industry firsts in the high-speed data converter field. He has authored the book entitled *High Speed Data Converters* (Institution of Engineering and Technology (IET), 2016). He has co-authored more than 30 articles and holds more than 50 patents. His research interests include analog IC design, high-linearity sampling, digitally assisted converters, and signal processing.

Dr. Ali received the S. J. Stein Award from the University of Pennsylvania. He was a recipient of the George Stephenson Foundation Award, the Catalyst Foundation Fellowship Award, the University of Pennsylvania Fellowship, and several industry and academic awards. He was an IEEE SSCS Distinguished Lecturer. He currently serves on the ISSCC Data Converter Sub-Committee and as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS.



Huseyin Dinc (Member, IEEE) received the B.S. degree in electrical engineering from Middle East Technical University, Ankara, Turkey, in 2000, the M.S. degree from Texas A&M University, College Station, TX, USA, in 2002, and the Ph.D. degree from the Georgia Institute of Technology, Atlanta, GA, USA, in 2011.

Since 2008, he has been with Analog Devices, Inc., Greensboro, NC, USA, working on high-speed pipelined analog-to-digital converters. He was granted a scholarship by the Scientific and Technical Research Council of Turkey (TUBITAK) to pursue graduate studies in USA. His technical interests include high-speed data converters, digitally assisted analog circuit design, and low-distortion and low-noise circuits.



Paritosh Bhoraskar (Senior Member, IEEE) received the B.Tech. degree in electrical engineering from IIT Bombay, Mumbai, India, in 2005 and the M.S. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA, in 2007.

He is currently a Senior Design Engineer with Analog Devices, Inc., Greensboro, NC, USA, where he has been working on high-speed high-performance A/D converter design and development and holds several patents in this area. His research interests include high-speed data converters, digitally assisted analog techniques, and analog circuit design in deep-submicrometer CMOS process.



Scott Bardsley received the B.S.E.E. degree from the University of Florida, Gainesville, FL, USA, in 1985.

He attended the Florida Institute of Technology, Melbourne, FL. From 1985 to 1999, he worked with Harris Semiconductor, Melbourne, as a Product Engineer on radiation hardened military products until 1992 and then a Design Engineer with the Mixed-Signal Product Development Group, working on a variety of products including analog-to-digital converters (ADCs), synthesizers, modems, and wireless LAN radios. Since 1999, he has been with the High Speed Converter Group, Analog Devices, Inc., Greensboro, NC, USA, where he has worked on high-speed 12- and 14-bit pipeline ADC converters in both BiCMOS and CMOS technologies. He holds 17 patents in the area of mixed-signal and pipeline ADC design.



Chris Dillon received the B.S.E.E. degree from North Carolina State University, Raleigh, NC, USA, in 1997.

After graduating, he began to work as a Mixed-Signal Design Engineer with High Speed Converter Group, Analog Devices, Inc., Greensboro, NC, USA. He has spent most of his career designing and developing a wide range of analog high-performance circuits for high-speed high-resolution A/D converter products. He has co-developed many industry first A/D converters pushing the state-of-the-art of speed, resolution, and dynamic performance. He holds seven U.S. patents in the analog circuit design and more pending.



Matthew McShea received the B.S. degree in electrical engineering from the University of Kansas, Lawrence, KS, USA, in 2000, the M.S. degree in electrical engineering from the University of Colorado, Boulder, CO, USA, in 2005, and the M.S. degree in system design and management from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2019.

He has worked with the semiconductor industry for 20 years designing complex systems and leading digital and embedded software teams with Lucent Technologies, Westminster, CO, Avaya, Westminster, RF Micro Devices, Greensboro, NC, USA, and Analog Devices Inc., Greensboro.



Joel Prabhakar Periathambi received the bachelor's degree in electronics and communication engineering from the Madras Institute of Technology, Anna University, Chennai, India, in 2008 and the master's degree in electrical engineering from North Carolina State University, Raleigh, NC, USA, in 2013.

He joined Analog Devices Inc., Greensboro, NC, USA, as a Digital IC Design Engineer, in 2013, where he works on the register transfer level (RTL) design and verification of digital calibration. His interests include RTL design, verification, and physical design flow.



Scott Puckett received the B.S. degree in mathematics from Southern College, Collegedale, TN, USA, in 1991 and the B.S.E.E., M.S., and Ph.D. degrees from the University of Tennessee, Knoxville, TN, in 1995, 1998, and 2001, respectively.

He currently works as a Mixed-Signal Design Engineer with Analog Devices, Inc., Greensboro, NC, USA.