BANDHAN HALDER

bandhanhalder.office@gmail.com
+8801823307328
House: 47,Mirpur,Dhaka

PROFILE

I am an aspiring VLSI engineer with a strong academic foundation in VLSI design, further enhanced by my VLSI 2 coursework. I am a detail-oriented and analytical problem solver with demonstrated leadership and technical skills, as evidenced by my successful projects. I am seeking a challenging position in the VLSI industry, where I can apply my knowledge and project experience to contribute to innovative semiconductor solutions while advancing my career in this dynamic field.

EDUCATION

Ahsanullah University of Science & Technology (AUST) (2024)
Bachelor of Science in Electrical & Electronic Engineering
Thesis: ***Analysis of Structural & Electrical Properties of Samarium Doped Bismuth Ferrite***

- CGPA: 3.686/4.00
- 4 Students Scholarship within 8 semesters

Government Science College (2019)
Higher Secondary Certificate

- GPA: 5.00/5.00

Dhanmondi Govt. Boys' High School (2017)
Secondary School Certificate

- GPA: 5.00/5.00

TECHNICAL SKILLS

- **Programming Languages**: C, C++
- **Software**: Cadence virtuoso, Innovus Origin, Matlab, PsPice, Autocad, Code Blocks, Proteus.
- **Operating System:** Windows, Linux (Bash Command & Scripting)

PROJECT EXPERIENCE

10T SRAM Cell
Build schematic and layout using paper reference & Calculated power and Area of the cell using Cadence Virtuoso with no LVS and DRC error. Delivered a functional SRAM cell design with improved area utilization and compliance with all design rules.

Advanced Home Automation & Security
Designed a full chip from RTL code to stream out using ModelSim, Genus, Innovus.

ADDITIONAL PROJECT

Phase Frequency Detector
It is used to compare the phase and frequency of two input signals and generate an output that represents the phase and frequency difference between them. Softwares used are Cadence Virtuoso & ADE L.

LEADERSHIP EXPERIENCE

Project Lead, 10T SRAM Design
Directed a team of 4 members in designing a 10T,6T,5T,4T SRAM cell using Cadence Virtuoso (90nm technology). Conducted power and area analysis, ensuring compliance with DRC and LVS requirements. Delivered the project within the stipulated academic timeline.

Team Leader, Advanced Home Automation Full Chip Design
Led a team of 4 members in the end-to-end development of a full-chip design from RTL to GDSII. Coordinated team efforts using tools like ModelSim, Genus, and Innovus. Ensured project success on 45nm technology, achieving functional and timing goals. Ensured task allocation and adherence to deadlines, resulting in a successful project demo.

ADDITIONAL INFORMATION

- Completed industrial attachment at Neural Semiconductor & Bangladesh Satellite Company Limited (BSCL).
- Completed course on **VLSI 1&2, Digital Electronics**, **Fabrication and Processing, Electronics 1&2,** Signal & Systems, Programming Language.