**ECEN 454 – Lab1: Introduction to Cadence Schematic Capture & Simulation**

Faizan Bangash

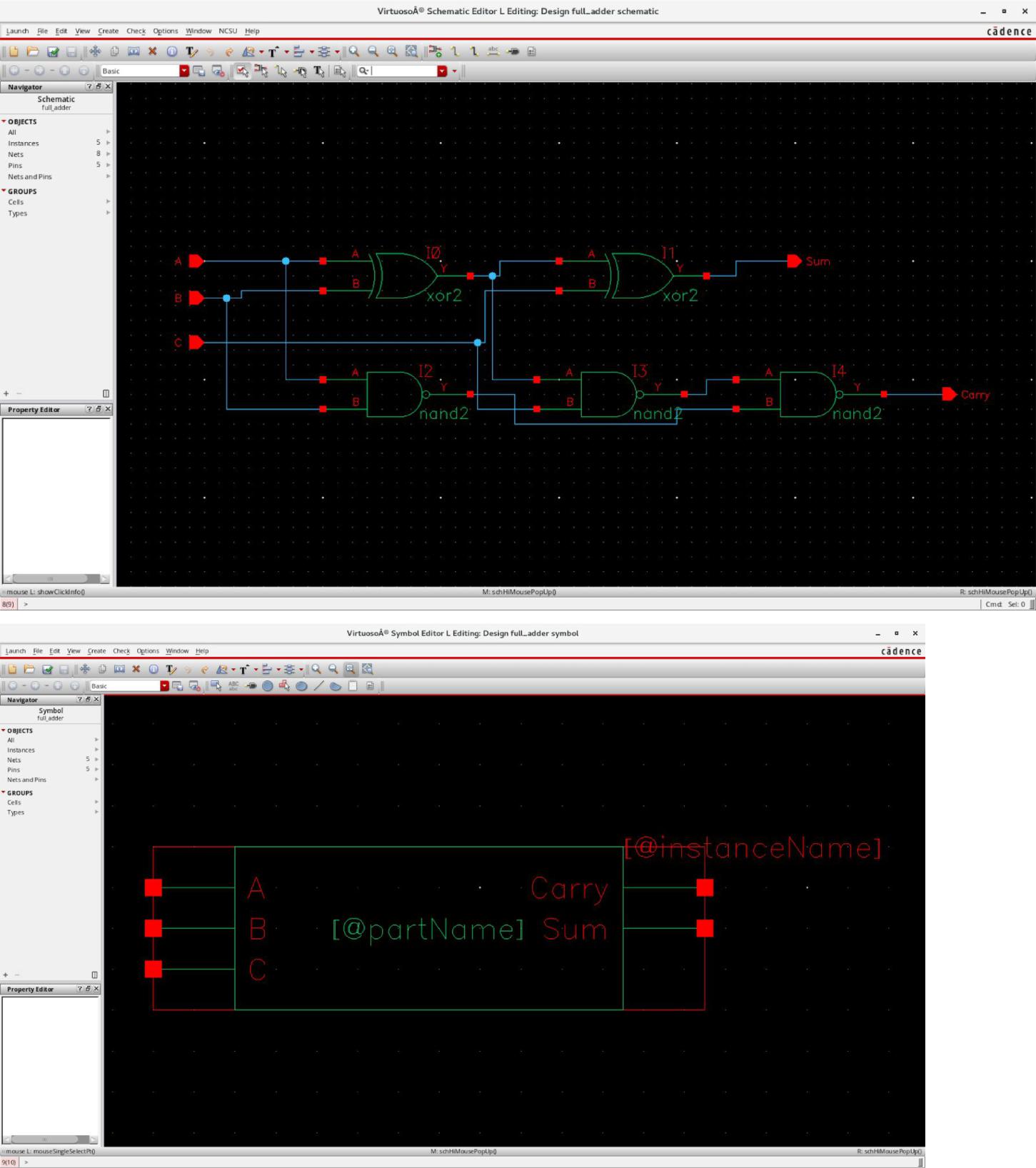
Section 506

TA: Lin Huang

DUE: 11 September 2018

**1-bit Full Adder:**

* **Schematic/Symbol:**



* + **Testfixture:**
* Verilog stimulus file.
* Please do not create a module in this file.
* Default verilog stimulus.

initial

begin

A=1'b0; B=1'b0; C=1'b0;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b0; B=1'b0; C=1'b1;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b0; B=1'b1; C=1'b0;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b0; B=1'b1; C=1'b1;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b1; B=1'b0; C=1'b0;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b1; B=1'b0; C=1'b1;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b1; B=1'b1; C=1'b0;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); #50 A=1'b1; B=1'b1; C=1'b1;

$monitor($time, "A=%b, B=%b, C=%b, Sum=%b, Carry=%b", A,B,C,Sum,Carry); end

* **Simout:**

TOOL: ncxlmode 10.20-s073: Started on Sept 07, 2018 at 18:04:43 CST /softwares/Linux/cadence/INCISIV102/tools.lnx86/bin/ncxlmode

+delay\_mode\_path

+typdelays

-l

simout.tmp

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/full\_adder\_run1/testfixture.template -f /home/ugrads/b/bangashfaizan1/Cadence/lab-1/full\_adder\_run1/verilog.inpfiles

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/nand2/functional/verilog.v

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/xor2/functional/verilog.v ihnl/cds0/netlist

+nostdout

+nocopyright

+ncvlogargs+" -neverwarn -nostdout -nocopyright "

+ncelabargs+" -neg\_tchk -nonotifier -sdf\_NOCheck\_celltype -access +r -pulse\_e 100 -pulse\_r 100 -neverwarn -timescale 1ns/1ns -nostdout -nocopyright"

+ncsimargs+" -neverwarn -nocopyright -gui -input

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/full\_adder\_run1/.simTmpNCCmd "

+mpssession+virtuoso30559

+mpshost+hera3.ece.tamu.edu SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

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Relinquished control to SimVision...

ncsim>

ncsim> source /softwares/Linux/cadence/INCISIV102/tools/inca/files/ncsimrc ncsim> database -open shmWave -shm -default -into shm.db Created default SHM database shmWave

ncsim> probe -create -shm test -all -depth 1

Created probe 1

ncsim> run

0A=0, B=0, C=0, Sum=0, Carry=0

50A=0, B=0, C=1, Sum=1, Carry=0

100A=0, B=1, C=0, Sum=1, Carry=0

150A=0, B=1, C=1, Sum=0, Carry=1

200A=1, B=0, C=0, Sum=1, Carry=0

250A=1, B=0, C=1, Sum=0, Carry=1

300A=1, B=1, C=0, Sum=0, Carry=1

350A=1, B=1, C=1, Sum=1, Carry=1

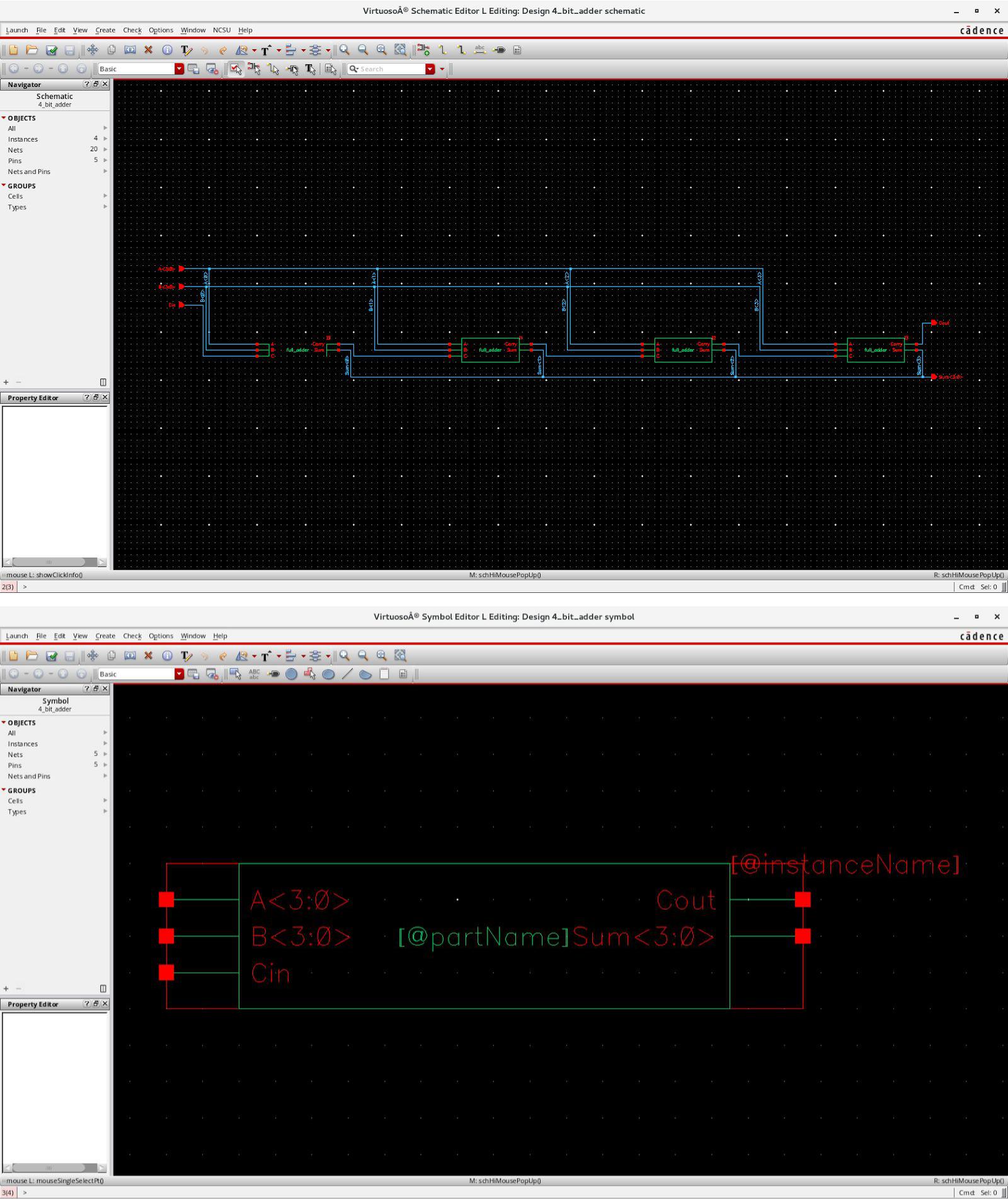
ncsim> ^C

ncsim> exit

TOOL: ncxlmode 10.20-s073: Exiting on Sept 07, 2018 at 18:26:52 CST (total: 00:22:09)

**4-bit Adder:**

* **Schematic/Symbol:**



* + **Testfixture:**

// Verilog SumtimuluSum file.

* Please do not create a module in this file.
* Default verilog SumtimuluSum.

initial

begin

A[3:0] = 4'b0000;

B[3:0] = 4'b0000;

Cin = 1'b0;

$monitor($time, "A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin ,Sum, Cout); #50

A[3:0] = 4'b1111;

B[3:0] = 4'b1111;

Cin = 1'b0;

$monitor($time, "A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin ,Sum, Cout); #50

A[3:0] = 4'b1010;

B[3:0] = 4'b1010;

Cin = 1'b1;

$monitor($time, "A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin ,Sum, Cout); #50

A[3:0] = 4'b0101;

B[3:0] = 4'b0101;

Cin = 1'b1;

$monitor($time, "A=%b, B=%b, Cin=%b, Sum=%b, Cout=%b", A, B, Cin ,Sum, Cout);

end

* **Simout:**

TOOL: ncxlmode 10.20-s073: Started on Sept 07, 2018 at 19:39:52 CST /softwares/Linux/cadence/INCISIV102/tools.lnx86/bin/ncxlmode

+delay\_mode\_path

+typdelays

-l

simout.tmp

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_adder\_run1/testfixture.template -f /home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_adder\_run1/verilog.inpfiles

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/nand2/functional/verilog.v

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/xor2/functional/verilog.v ihnl/cds0/netlist

ihnl/cds1/netlist

+nostdout

+nocopyright

+ncvlogargs+" -neverwarn -nostdout -nocopyright "

+ncelabargs+" -neg\_tchk -nonotifier -sdf\_NOCheck\_celltype -access +r -pulse\_e 100 -pulse\_r 100 -neverwarn -timescale 1ns/1ns -nostdout -nocopyright"

+ncsimargs+" -neverwarn -nocopyright -gui -input

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_adder\_run1/.simTmpNCCmd "

+mpssession+virtuoso7325

+mpshost+lin19-324cvlb.ece.tamu.edu SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

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Relinquished control to SimVision...

ncsim>

ncsim> source /softwares/Linux/cadence/INCISIV102/tools/inca/files/ncsimrc ncsim> database -open shmWave -shm -default -into shm.db Created default SHM database shmWave

ncsim> probe -create -shm test -all -depth 1

Created probe 1

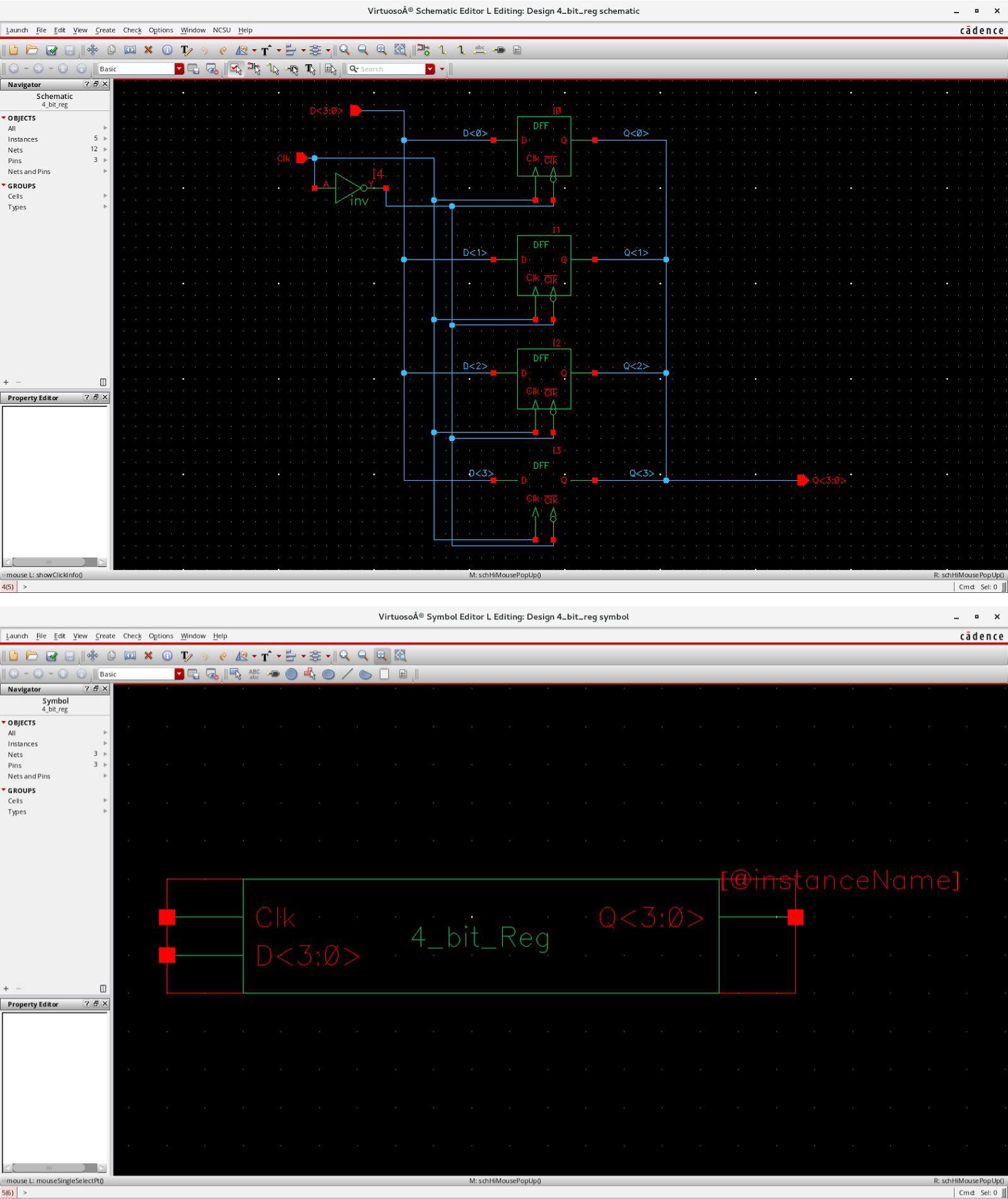
ncsim> run

0A=0000, B=0000, Cin=0, Sum=0000, Cout=0 50A=1111, B=1111, Cin=0, Sum=1110, Cout=1 100A=1010, B=1010, Cin=1, Sum=0101, Cout=1 150A=0101, B=0101, Cin=1, Sum=1011, Cout=0

ncsim>

**4-bit Register:**

* **Schematic/Symbol:**



**-**

* + **Testfixture:**
* Verilog stimulus file.
* Please do not create a module in this file.
* Default verilog stimulus.

initial

begin

Clk = 1'b0;

D[3:0] = 4'b0000;

$monitor($time, "D=%b, Clk=%b, Q=%b", D, Clk, Q);

#50

Clk = 1'b1;

#50

D = 4'b0001;

#50

Clk = 1'b1;

D = ~D;

#50

Clk = 1'b0;

#50

D = 4'b1000;

#50

D = 4'b0100;

#50

Clk = 1'b0;

D = ~D;

#50

Clk = 1'b1;

#50

D = 4'b1000;

#50

D = 4'b0100;

#50

D = 4'b1111;

#50

Clk = 1'b0;

#50

Clk = 1'b1;

#50

Clk = 1'b0;

#50

Clk = 1'b0;

#50

Clk = 1'b1;

#50

Clk =1'b0;

#50

D = 4'b0000;

#50

Clk = 1'b0;

end

* **Simout:**

TOOL: ncxlmode 10.20-s073: Started on Sept 10, 2018 at 14:26:53 CST /softwares/Linux/cadence/INCISIV102/tools.lnx86/bin/ncxlmode

+delay\_mode\_path

+typdelays

-l

simout.tmp

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_reg\_run1/testfixture.template -f /home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_reg\_run1/verilog.inpfiles

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/inv/functional/verilog.v

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/Dlatch/behavioral/verilog.v ihnl/cds0/netlist

ihnl/cds1/netlist

+nostdout

+nocopyright

+ncvlogargs+" -neverwarn -nostdout -nocopyright "

+ncelabargs+" -neg\_tchk -nonotifier -sdf\_NOCheck\_celltype -access +r -pulse\_e 100 -pulse\_r 100 -neverwarn -timescale 1ns/1ns -nostdout -nocopyright"

+ncsimargs+" -neverwarn -nocopyright -gui -input

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/4\_bit\_reg\_run1/.simTmpNCCmd "

+mpssession+virtuoso2216

+mpshost+lin18-324cvlb.ece.tamu.edu SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

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Relinquished control to SimVision...

ncsim>

ncsim> source /softwares/Linux/cadence/INCISIV102/tools/inca/files/ncsimrc ncsim> database -open shmWave -shm -default -into shm.db Created default SHM database shmWave

ncsim> probe -create -shm test -all -depth 1

Created probe 1

ncsim> run

0D=0000, Clk=0, Q=xxxx

50D=0000, Clk=1, Q=0000

100D=0001, Clk=1, Q=0000

150D=1110, Clk=1, Q=0000

200D=1110, Clk=0, Q=0000

250D=1000, Clk=0, Q=0000

300D=0100, Clk=0, Q=0000

350D=1011, Clk=0, Q=0000

400D=1011, Clk=1, Q=1011

450D=1000, Clk=1, Q=1011

500D=0100, Clk=1, Q=1011

550D=1111, Clk=1, Q=1011

600D=1111, Clk=0, Q=1011

650D=1111, Clk=1, Q=1111

700D=1111, Clk=0, Q=1111

800D=1111, Clk=1, Q=1111

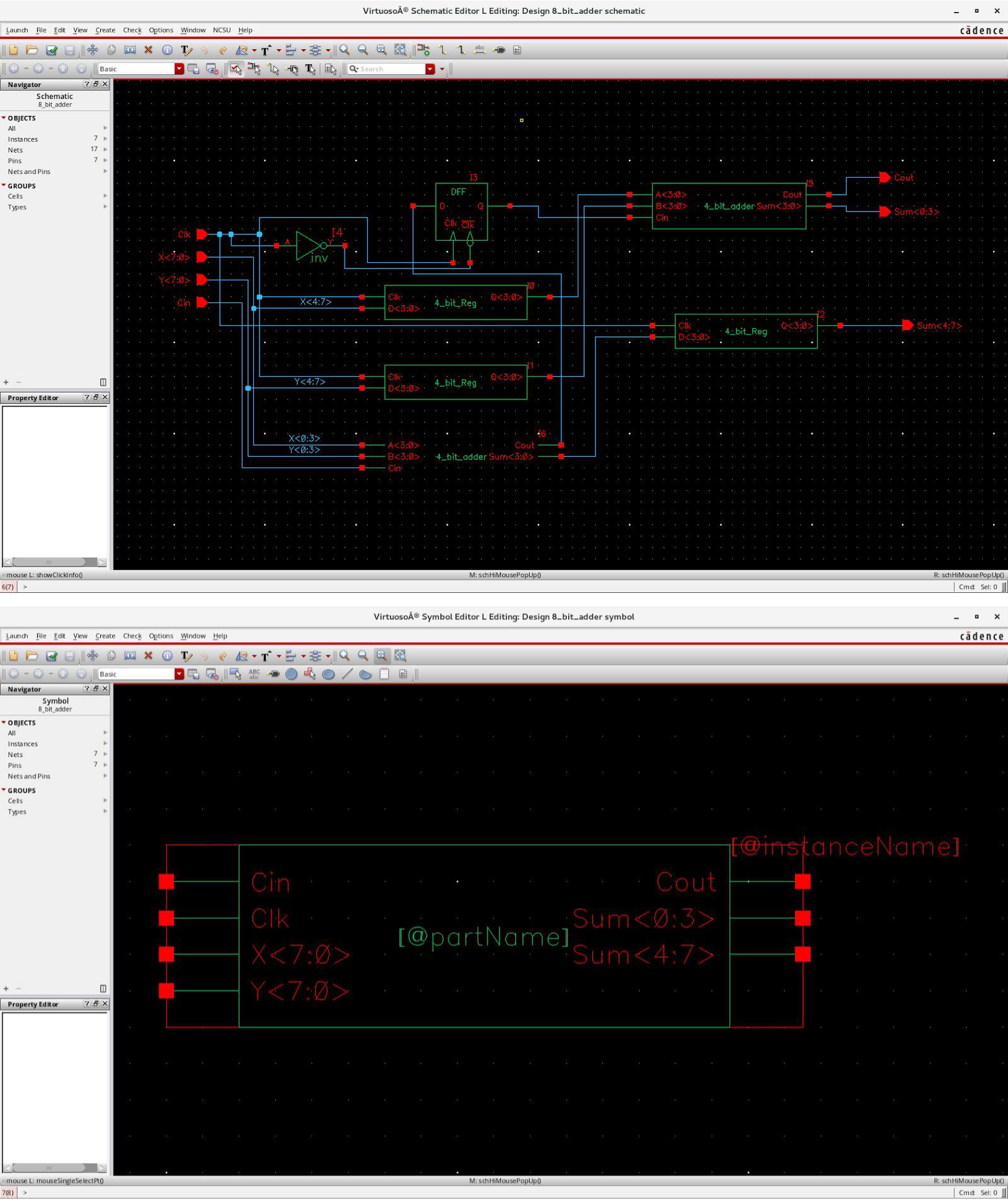
850D=1111, Clk=0, Q=1111

900D=0000, Clk=0, Q=1111

ncsim>

**8-Bit Adder:**

* **Schematic/Symbol:**



* + **Testfixture:**
* Verilog stimulus file.
* Please do not create a module in this file.
* Default verilog stimulus.

initial

$monitor ($time, "Cin=%b, Clk=%b, X=%b, Y=%b, Sum=%b, Cout=%b", Cin, Clk, X, Y, Sum, Cout);

initial

begin

Cin = 1'b0;

Clk = 1'b0;

X[7:0] = 8'b00000000;

Y[7:0] = 8'b00000000;

#50

Cin=1'b0;

Clk=1'b1;

X[7:0]=8'b00000000;

Y[7:0]=8'b00000000;

#50

Cin=1'b0;

Clk=1'b0;

X[7:0]=8'b01111110;

Y[7:0]=8'b11100111;

#50

Cin=1'b0;

Clk=1'b1;

X[7:0]=8'b01111110;

Y[7:0]=8'b11100111;

#50

Cin=1'b1;

Clk=1'b0;

X[7:0]=8'b11111111;

Y[7:0]=8'b00000000;

#50

Cin=1'b1;

Clk=1'b1;

X[7:0]=8'b11111111;

Y[7:0]=8'b00000000;

#50

Cin=1'b0;

Clk=1'b0;

X[7:0]=8'b10101010;

Y[7:0]=8'b01010101;

#50

Cin=1'b0;

Clk=1'b1;

X[7:0]=8'b10101010;

Y[7:0]=8'b01010101;

#50

Cin=1'b1;

Clk=1'b0;

X[7:0]=8'b10101010;

Y[7:0]=8'b01010101;

#50

Cin=1'b1;

Clk=1'b1;

X[7:0]=8'b10101010;

Y[7:0]=8'b01010101;

#50

Cin=1'b0;

Clk=1'b0;

X[7:0]=8'b11001100;

Y[7:0]=8'b00110011;

#50

Cin=1'b0;

Clk=1'b1;

X[7:0]=8'b11001100;

Y[7:0]=8'b00110011;

#50

Cin=1'b1;

Clk=1'b0;

X[7:0]=8'b11001100;

Y[7:0]=8'b00110011;

#50

Cin=1'b1;

Clk=1'b1;

X[7:0]=8'b11001100;

Y[7:0]=8'b00110011;

end

* **Simout:**

TOOL: ncxlmode 10.20-s073: Started on Sept 10, 2018 at 20:31:51 CST /softwares/Linux/cadence/INCISIV102/tools.lnx86/bin/ncxlmode

+delay\_mode\_path

+typdelays

-l

simout.tmp

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/8\_bit\_adder\_run1/testfixture.template -f /home/ugrads/b/bangashfaizan1/Cadence/lab-1/8\_bit\_adder\_run1/verilog.inpfiles

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/nand2/functional/verilog.v

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/xor2/functional/verilog.v /softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/inv/functional/verilog.v

/softwares/Common/ncsu-cdk-1.6.0.beta/lib/NCSU\_Digital\_Parts/Dlatch/behavioral/verilog.v ihnl/cds0/netlist

ihnl/cds1/netlist

ihnl/cds2/netlist

ihnl/cds3/netlist

ihnl/cds4/netlist

+nostdout

+nocopyright

+ncvlogargs+" -neverwarn -nostdout -nocopyright "

+ncelabargs+" -neg\_tchk -nonotifier -sdf\_NOCheck\_celltype -access +r -pulse\_e 100 -pulse\_r 100 -neverwarn -timescale 1ns/1ns -nostdout -nocopyright"

+ncsimargs+" -neverwarn -nocopyright -gui -input

/home/ugrads/b/bangashfaizan1/Cadence/lab-1/8\_bit\_adder\_run1/.simTmpNCCmd "

+mpssession+virtuoso7325

+mpshost+lin19-324cvlb.ece.tamu.edu SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib

|

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

SOFTINCLUDE $SYSTEM\_CDS\_LIB\_DIR/cds.lib |

ncxlmode: \*W,DLCVAR (/home/ugrads/b/bangashfaizan1/cds.lib,1): cds.lib Invalid environment variable ''.

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Relinquished control to SimVision...

ncsim>

ncsim> source /softwares/Linux/cadence/INCISIV102/tools/inca/files/ncsimrc ncsim> database -open shmWave -shm -default -into shm.db Created default SHM database shmWave

ncsim> probe -create -shm test -all -depth 1

Created probe 1

ncsim> run

0Cin=0, Clk=0, X=00000000, Y=00000000, Sum=xxxxxxxx, Cout=x 50Cin=0, Clk=1, X=00000000, Y=00000000, Sum=00000000, Cout=0 100Cin=0, Clk=0, X=01111110, Y=11100111, Sum=00000000, Cout=0 150Cin=0, Clk=1, X=01111110, Y=11100111, Sum=01100101, Cout=1 200Cin=1, Clk=0, X=11111111, Y=00000000, Sum=01100101, Cout=1 250Cin=1, Clk=1, X=11111111, Y=00000000, Sum=00000000, Cout=1 300Cin=0, Clk=0, X=10101010, Y=01010101, Sum=00000000, Cout=1 350Cin=0, Clk=1, X=10101010, Y=01010101, Sum=11111111, Cout=0 400Cin=1, Clk=0, X=10101010, Y=01010101, Sum=11111111, Cout=0 450Cin=1, Clk=1, X=10101010, Y=01010101, Sum=00000000, Cout=1 500Cin=0, Clk=0, X=11001100, Y=00110011, Sum=00000000, Cout=1 550Cin=0, Clk=1, X=11001100, Y=00110011, Sum=11111111, Cout=0 600Cin=1, Clk=0, X=11001100, Y=00110011, Sum=11111111, Cout=0 650Cin=1, Clk=1, X=11001100, Y=00110011, Sum=00000000, Cout=1

ncsim> ^C

ncsim> exit

TOOL: ncxlmode 10.20-s073: Exiting on Sept 10, 2018 at 20:34:23 CST (total: 00:02:32)