***ECEN 454: Lab 3***

***Cell Characterization using Spectre***

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**Section 506**

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**Cell18 File:**

//Spice netlist for an inverter

simulator lang=spectre

subckt IV (input output VDD VSS)

parameters wp=0.6u lp=0.2u wn=0.3u ln=0.3u

M1 output input VDD VDD tsmc18P w=wp l=lp

M2 output input VSS VSS tsmc18N w=wn l=ln

ends IV

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//Spice netlist for NAND2

simulator lang=spectre

subckt NAND2 (inputA inputB output VDD VSS) parameters wp=0.65u lp=0.2u wn=0.3u ln=0.2u M1 output inputA VDD VDD tsmc18P w=wp l=lp M2 output inputB VDD VDD tsmc18P w=wp l=lp M3 output inputA W1 VSS tsmc18N w=wn l=ln M4 W1 inputB VSS VSS tsmc18N w=wn l=ln

ends NAND2

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//Spice netlist for XOR

simulator lang=spectre

subckt XOR (inputA inputB out VDD VSS) parameters wp=1.4u lp=0.2u wn=0.35u ln=0.2u M1 W1 inputA VDD VDD tsmc18P w=wp l=lp M2 W2 inputB VDD VDD tsmc18P w=wp l=lp M3 W3 W4 VDD VDD tsmc18P w=wp l=lp M4 out W1 W2 VDD tsmc18P w=wp l=lp

M5 out inputA W3 VDD tsmc18P w=wp l=lp

M6 W4 inputB VDD VDD tsmc18P w=wp l=lp

M7 out W1 W5 VSS tsmc18N w=wn l=ln

M8 out inputA W6 VSS tsmc18N w=wn l=ln

M9 W4 inputB VSS VSS tsmc18N w=wn l=ln

M10 W5 W4 VSS VSS tsmc18N w=wn l=ln

M11 W6 inputB VSS VSS tsmc18N w=wn l=ln

M12 W1 inputA VSS VSS tsmc18N w=wn l=ln ends XOR

**-------------------------------------------------------- Inverter --------------------------------------------------------**

**Delay\_Table.spi -**

;Spice netlist for an inverter and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

vpwl (IV\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

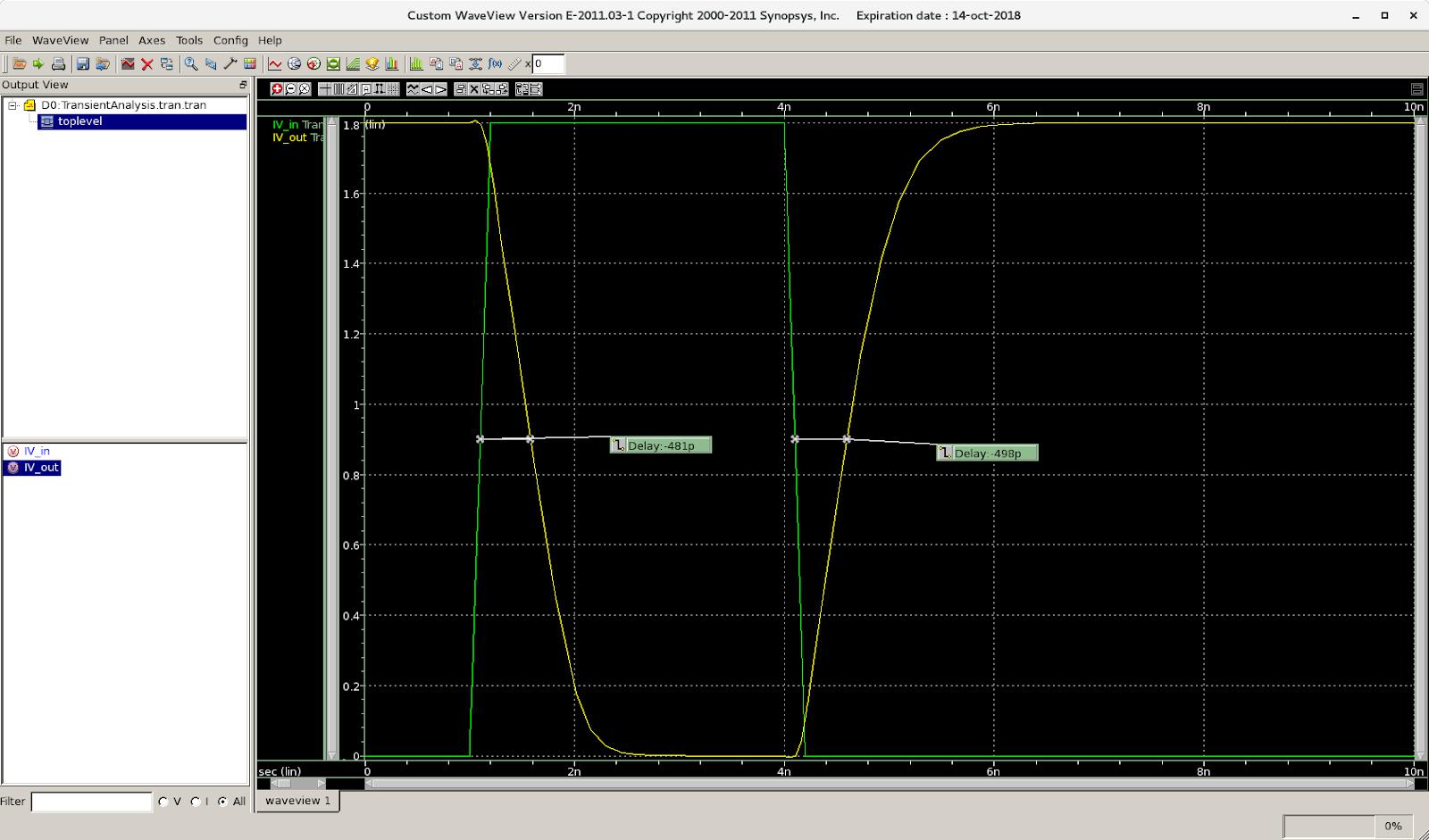
X1 (IV\_in IV\_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

;R1 (IV\_out 1) resistor r=1

C1 (IV\_out 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save IV\_in IV\_out

**Transient Lines -**



**Transient Delay Table -**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cap (f) | Delay 1 (ps) |  | Delay (ps) |  | % error |
|  |  |  |  |  |  |
| 1 |  | -27.1 |  | -45.2 | 5.00692 |
|  |  |  |  |  |  |
| 5 |  | -57.7 |  | -74.5 | 2.4416 |
|  |  |  |  |  |  |
| 10 |  | -85.8 |  | -101 | 1.62741 |
|  |  |  |  |  |  |
| 18 |  | -122 |  | -136 | 1.08527 |
|  |  |  |  |  |  |
| 23 |  | -144 |  | -157 | 8.63737 |
|  |  |  |  |  |  |
| 29 |  | -171 |  | -184 | 7.32394 |
|  |  |  |  |  |  |
| 38 |  | -210 |  | -223 | 6.00462 |
|  |  |  |  |  |  |
| 47 |  | -249 |  | -265 | 6.22568 |
|  |  |  |  |  |  |
| 56 |  | -288 |  | -302 | 4.74576 |
|  |  |  |  |  |  |
| 61 |  | -310 |  | -327 | 5.33752 |
|  |  |  |  |  |  |
| 69 |  | -347 |  | -363 | 4.57047 |
|  |  |  |  |  |  |
| 77 |  | -382 |  | -397 | 3.85671 |
|  |  |  |  |  |  |
| 85 |  | -416 |  | -430 | 3.30965 |
|  |  |  |  |  |  |
| 93 |  | -451 |  | -466 | 3.27652 |
|  |  |  |  |  |  |
| 100 |  | -481 |  | -498 | 3.47293 |
|  |  |  |  |  |  |

**Sim\_Cap.spi -**

;Spice netlist for an inverter and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

acinput (IV\_in 0) vsource dc=0 mag=1

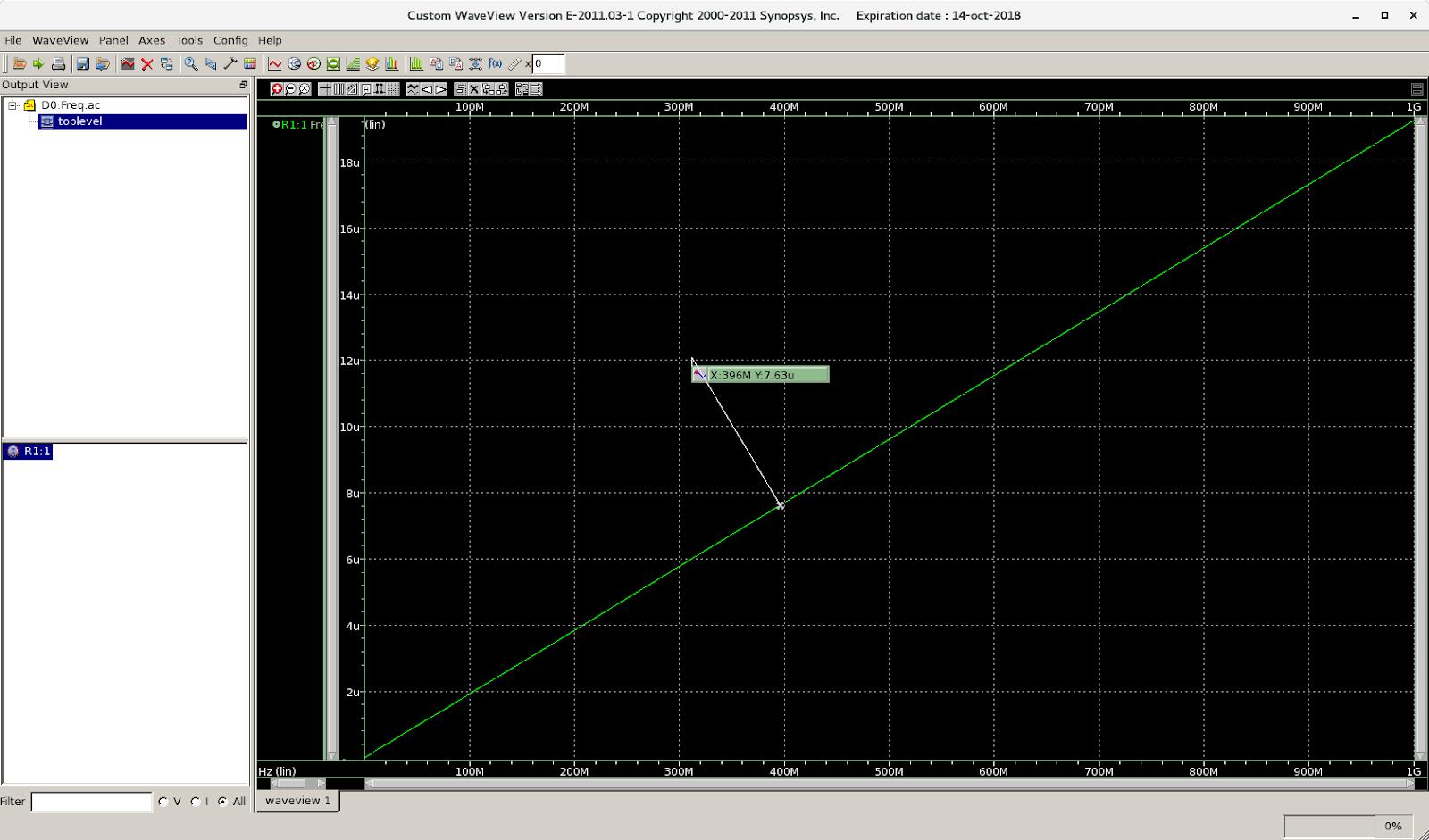
R1 (IV\_in IV\_in1) resistor r=0

X1 (IV\_in1 IV\_out vdd gnd) IV wp=0.9u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9

save R1:currents

**Sim Cap Line -**



**Sim Cap Table -**

|  |  |
| --- | --- |
| Frequency(M) | Current(uA) |
|  |  |
| 80.1 | 1.54 |
|  |  |
| 146 | 2.81 |
|  |  |
| 224 | 4.31 |
|  |  |
| 306 | 5.88 |
|  |  |
| 380 | 7.31 |
|  |  |
| 479 | 9.21 |
|  |  |
| 569 | 11 |
|  |  |
| 646 | 12.4 |
|  |  |
| 742 | 14.3 |
|  |  |
| 819 | 15.8 |
|  |  |
| 916 | 17.6 |
|  |  |

**-------------------------------------------------------- NAND2 --------------------------------------------------------**

**Delay\_Table.spi -**

;Spice netlist for an NAND2 and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

vpwl (NAND2\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

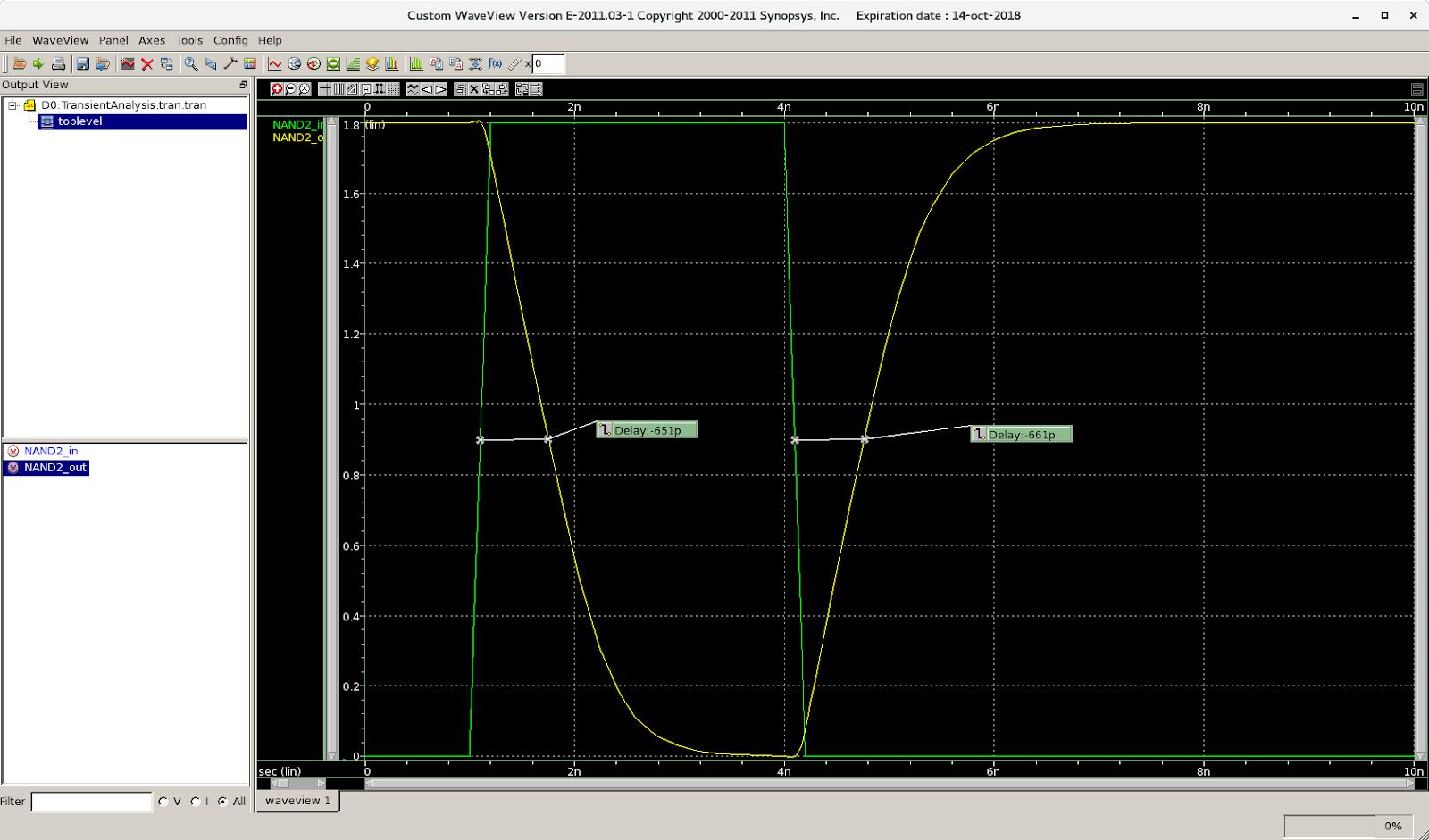
X1 (vdd NAND2\_in NAND2\_out vdd gnd) NAND2 wp=0.65u lp=0.2u wn=0.3u ln=0.2u

;R1 (NAND2\_out 1) resistor r=1

C1 (NAND2\_out 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save NAND2\_in NAND2\_out

**Transient Lines -**



**Transient Delay Table -**

|  |  |  |  |
| --- | --- | --- | --- |
| Load Cap (fF) | Delay 1 (ps) | Delay 2 (ps) | %error |
|  |  |  |  |
| 1 | -33.8 | -65.3 | 6.35721 |
|  |  |  |  |
| 5 | -67.4 | -95.9 | 3.49051 |
|  |  |  |  |
| 10 | -101 | -126 | 2.20264 |
|  |  |  |  |
| 16 | -138 | -161 | 1.53846 |
|  |  |  |  |
| 21 | -169 | -191 | 1.22222 |
|  |  |  |  |
| 28 | -212 | -233 | 9.41382 |
|  |  |  |  |
| 39 | -280 | -298 | 6.22837 |
|  |  |  |  |
| 46 | -322 | -341 | 5.73152 |
|  |  |  |  |
| 52 | -359 | -375 | 4.35967 |
|  |  |  |  |
| 57 | -390 | -405 | 3.77358 |
|  |  |  |  |
| 68 | -457 | -470 | 2.80475 |
|  |  |  |  |
| 76 | -505 | -521 | 3.11891 |
|  |  |  |  |
| 84 | -553 | -566 | 2.32351 |
|  |  |  |  |
| 91 | -596 | -609 | 2.15768 |
|  |  |  |  |
| 100 | -651 | -661 | 1.52439 |
|  |  |  |  |

**Sim\_Cap.spi**

;Spice netlist for an inverter and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

acinput (NAND2\_in 0) vsource dc=0 mag=1

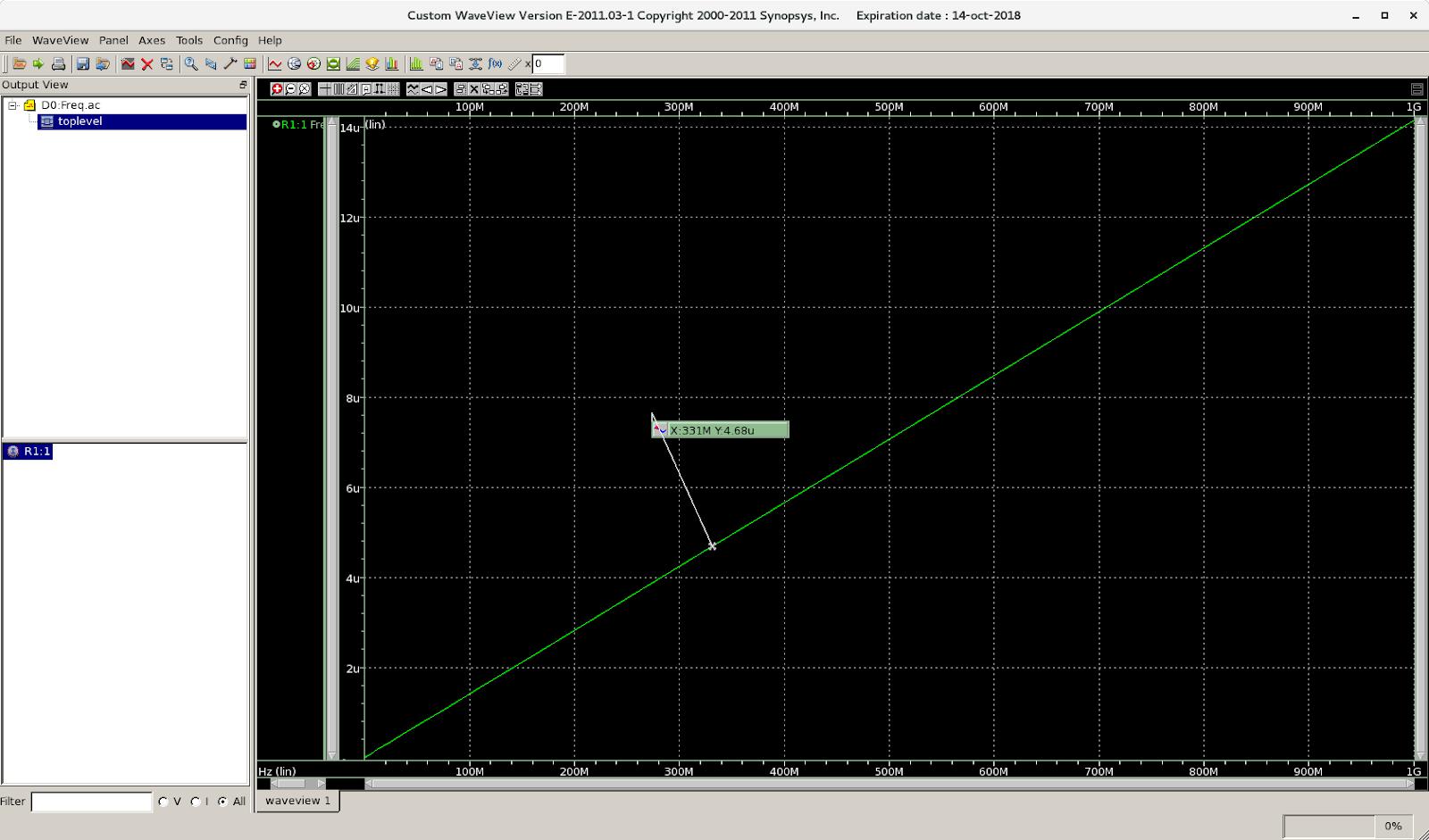
R1 (NAND2\_in NAND2\_in1) resistor r=0

X1 (vdd NAND2\_in1 NAND2\_out vdd gnd) NAND2 wp=0.65u lp=0.2u wn=0.3u ln=0.2u

Freq ac start=1e+1 stop=1e+9

save R1:currents

**Sim Cap Line -**



**Sim Cap Table -**

|  |  |
| --- | --- |
| Frequency(M) | Current(uA) |
|  |  |
| 101 | 1.43 |
|  |  |
| 186 | 2.63 |
|  |  |
| 292 | 4.13 |
|  |  |
| 364 | 5.14 |
|  |  |
| 449 | 6.35 |
|  |  |
| 522 | 7.39 |
|  |  |
| 615 | 8.7 |
|  |  |
| 740 | 10.5 |
|  |  |
| 837 | 11.8 |
|  |  |
| 891 | 12.6 |
|  |  |
| 947 | 13.4 |
|  |  |

**-------------------------------------------------------- XOR ------------------------------------------------------------**

**Delay\_Table.spi -**

;Spice netlist for an XOR and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

vpwl (XOR\_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

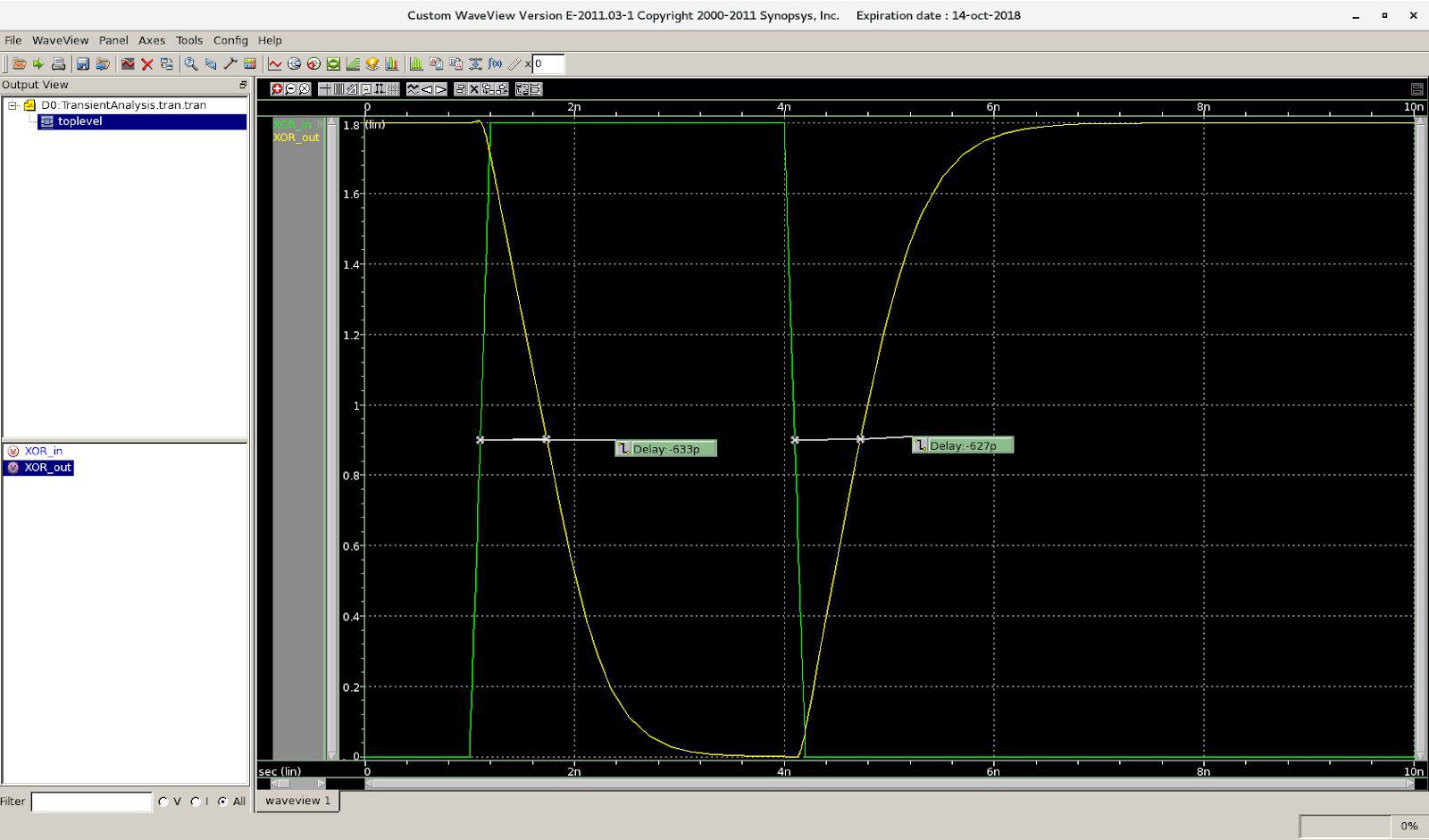
X1 (vdd XOR\_in XOR\_out vdd gnd) XOR wp=1.4u lp=0.2u wn=0.35u ln=0.2u

;R1 (XOR\_out 1) resistor r=1

C1 (XOR\_out 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps save XOR\_in XOR\_out

**Transient Lines -**



**Transient Delay Table -**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Cap (f) | Delay 1 (ps) |  | Delay (ps) |  | % error |
|  |  |  |  |  |  |
| 1 |  | -71.9 |  | -77.3 | 7.23861 |
|  |  |  |  |  |  |
| 5 |  | -98.2 |  | -104 | 5.73689 |
|  |  |  |  |  |  |
| 10 |  | -128 |  | -132 | 3.07692 |
|  |  |  |  |  |  |
| 18 |  | -148 |  | -236 | 4.58333 |
|  |  |  |  |  |  |
| 23 |  | -174 |  | -279 | 4.63476 |
|  |  |  |  |  |  |
| 29 |  | -236 |  | -237 | 0.422833 |
|  |  |  |  |  |  |
| 38 |  | -286 |  | -286 | 0.0 |
|  |  |  |  |  |  |
| 47 |  | -337 |  | -336 | 0.297177 |
|  |  |  |  |  |  |
| 56 |  | -387 |  | -386 | 0.258732 |
|  |  |  |  |  |  |
| 61 |  | -415 |  | -413 | 0.483092 |
|  |  |  |  |  |  |
| 69 |  | -460 |  | -457 | 0.654308 |
|  |  |  |  |  |  |
| 77 |  | -504 |  | -503 | 0.19861 |
|  |  |  |  |  |  |
| 85 |  | -549 |  | -545 | 0.731261 |
|  |  |  |  |  |  |
| 93 |  | -594 |  | -588 | 1.011523 |
|  |  |  |  |  |  |
| 100 |  | -633 |  | -627 | 0.952381 |
|  |  |  |  |  |  |

**Sim\_Cap.spi -**

;Spice netlist for an inverter and a capacitor

simulator lang=spectre

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/model18.spi"

include "~/Desktop/ecen-454/lab3/cellcharacs/spectre/cell18.spi"

vgnd (gnd 0) vsource dc=0

vvdd (vdd 0) vsource dc=1.8

acinput (XOR\_in 0) vsource dc=0 mag=1

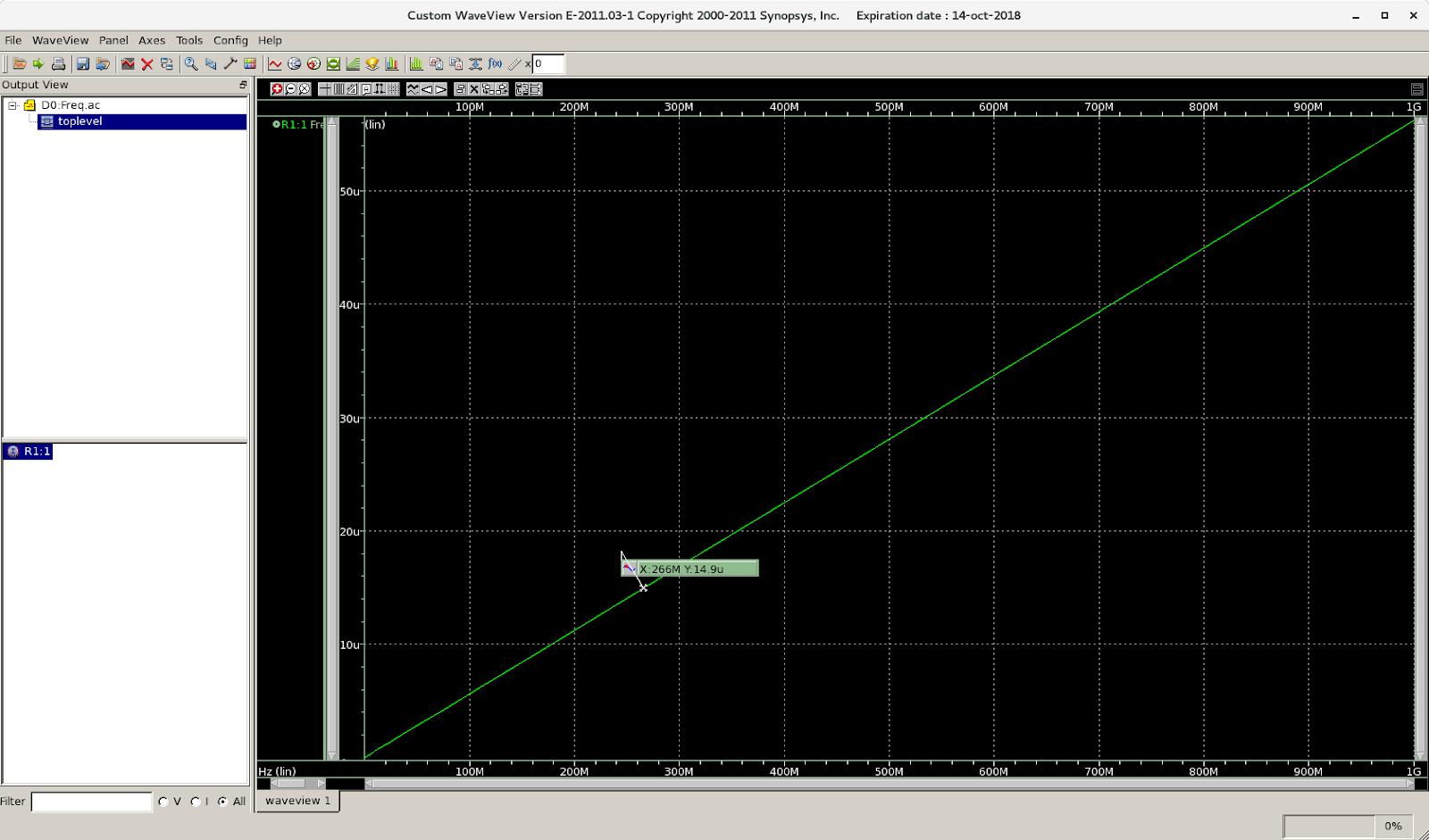
R1 (XOR\_in XOR\_in1) resistor r=0

X1 (vdd XOR\_in1 XOR\_out vdd gnd) XOR wp=1.4u lp=0.2u wn=0.35u ln=0.2u

Freq ac start=1e+1 stop=1e+9

save R1:currents

**Sim Cap Lines -**



**Sim Cap Table -**

|  |  |
| --- | --- |
| Frequency(M) | Current(uA) |
|  |  |
| 75.9 | 4.27 |
|  |  |
| 158 | 8.91 |
|  |  |
| 235 | 13.2 |
|  |  |
| 342 | 19.2 |
|  |  |
| 472 | 26.5 |
|  |  |
| 548 | 30.8 |
|  |  |
| 649 | 36.5 |
|  |  |
| 737 | 41.4 |
|  |  |
| 805 | 45.2 |
|  |  |
| 861 | 48.4 |
|  |  |
| 938 | 52.7 |
|  |  |