**Lab 4**

**Design and Simulation of 1-bit Adder**

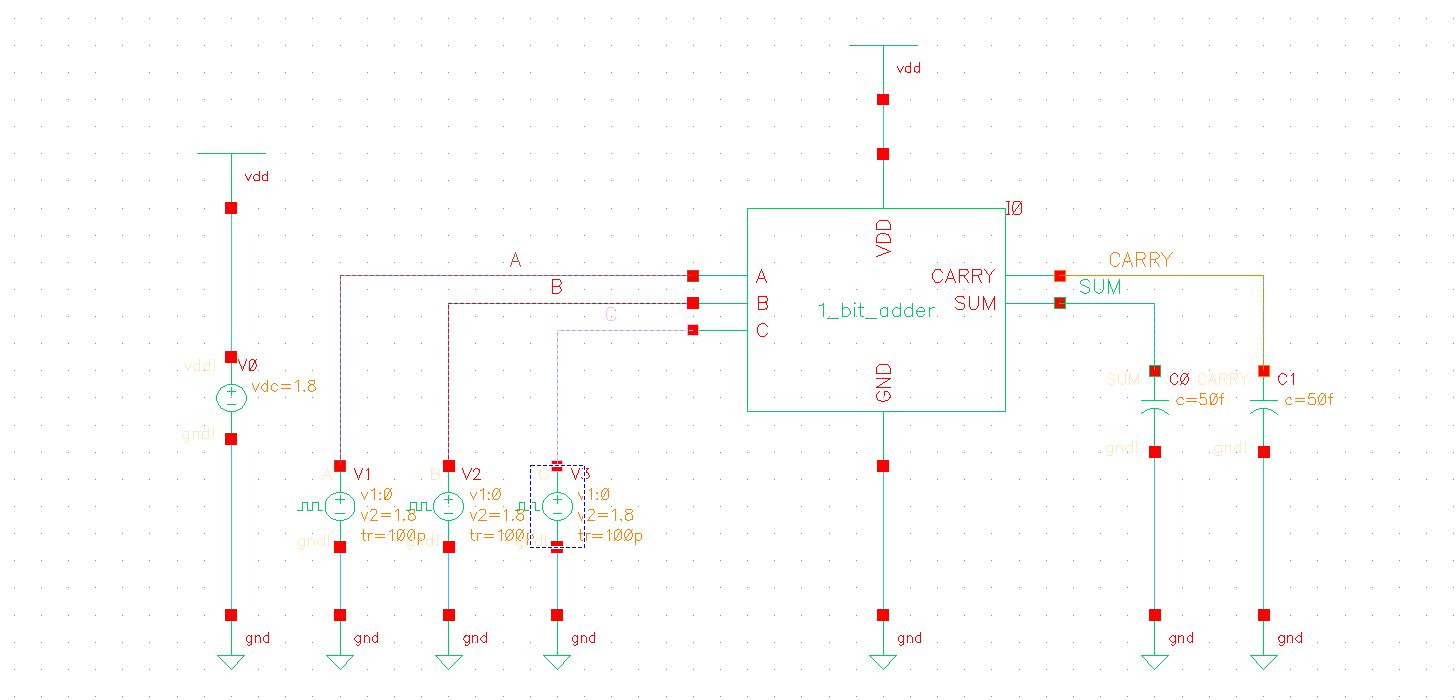
**Faizan Bangash**

**Section 506**

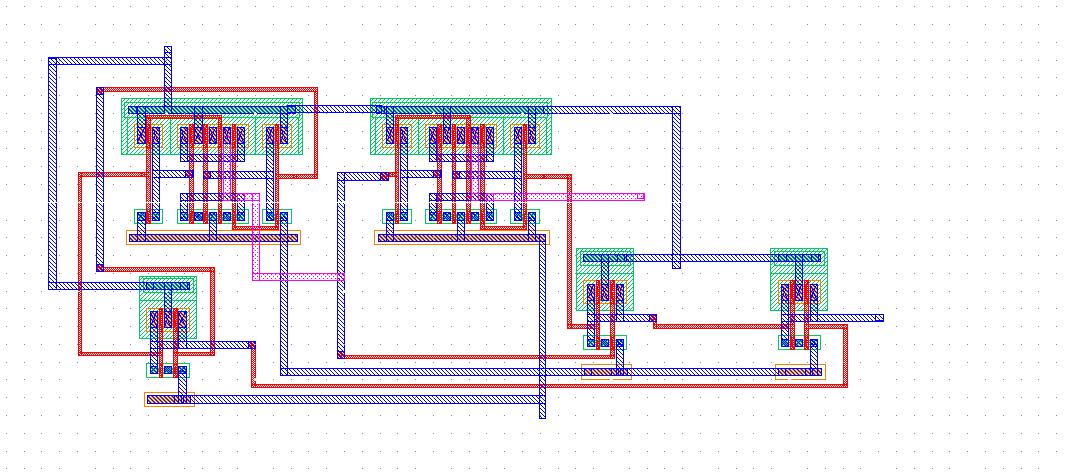
**TA: Lin Huang**

**DUE: 02 October 2018**

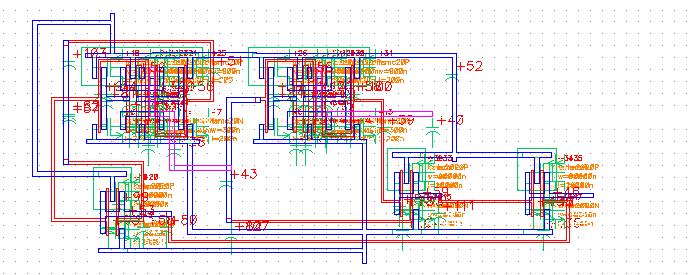
**1-Bit Adder Schematic**

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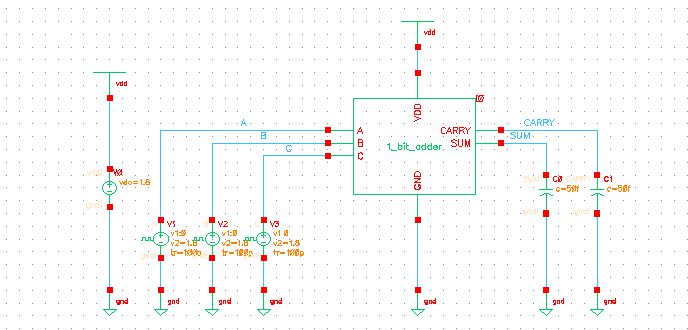
**1-Bit Adder Layout**

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**1-Bit Adder Extracted**

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**1-Bit Adder Simulate Schematic**

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**1-Bit Adder LVS**

@(#)$CDS: LVS version 6.1.7-64b 09/26/2018 18:10 (sjfhw313) $

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /home/ugrads/b/bangashfaizan1/cadence/lab4/LVS/layout/netlist

count

25 nets

7 terminals

18 pmos

18 nmos

Net-list summary for /home/ugrads/b/bangashfaizan1/cadence/lab4/LVS/schematic/netlist

count

25 nets

7 terminals

18 pmos

18 nmos

Terminal correspondence points

N22 N6 A

N21 N2 B

N19 N7 C

N24 N8 CARRY

N18 N9 GND

N20 N5 SUM

N23 N3 VDD

Devices in the netlist but not in the rules:

pcapacitor

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

layout schematic

instances

un-matched 0 0

rewired 0 0

size errors 0 0

pruned 0 0

active 36 36

total 36 36

nets

un-matched 0 0

merged 0 0

pruned 0 0

active 25 25

total 25 25

terminals

un-matched 0 0

matched but

different type 0 0

total 7 7

Probe files from /home/ugrads/b/bangashfaizan1/cadence/lab4/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/ugrads/b/bangashfaizan1/cadence/lab4/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

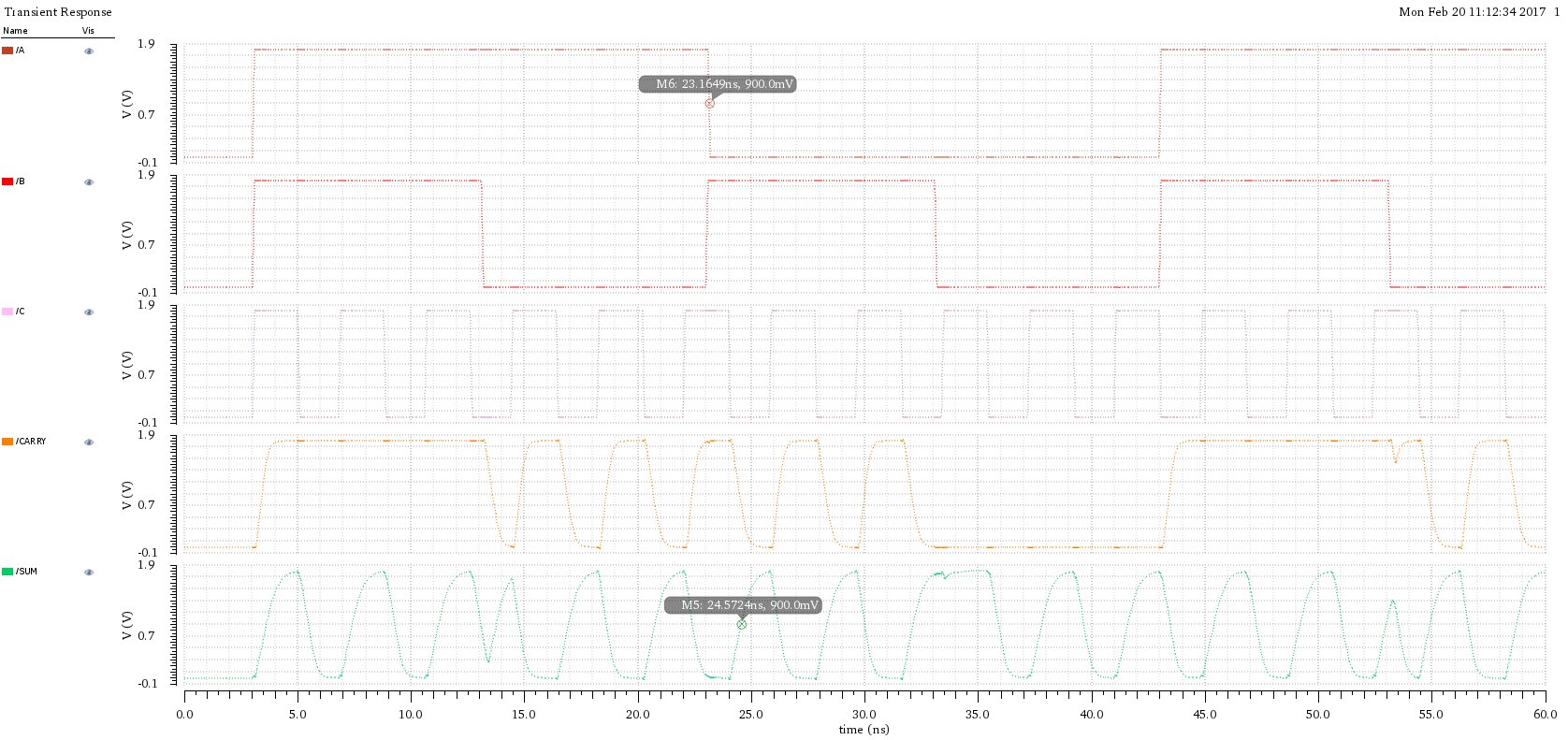
prunenet.out:

prunedev.out:

audit.out:

**1-Bit Adder Rise and Delay**

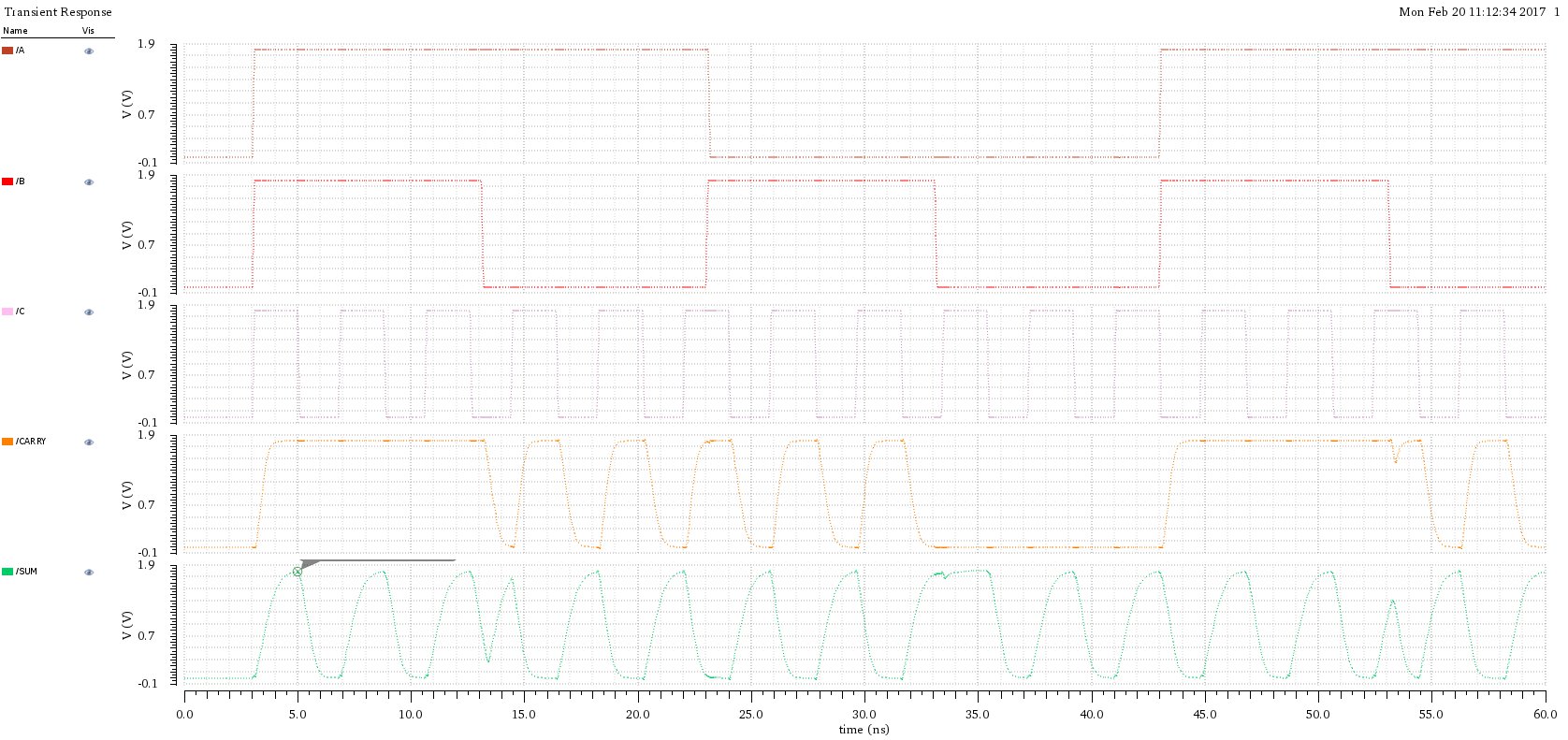
|  |  |  |
| --- | --- | --- |
| Fall(ns) | Rise(ns) | %error |
| 23.1649 | 24.5724 | 6.076003 |



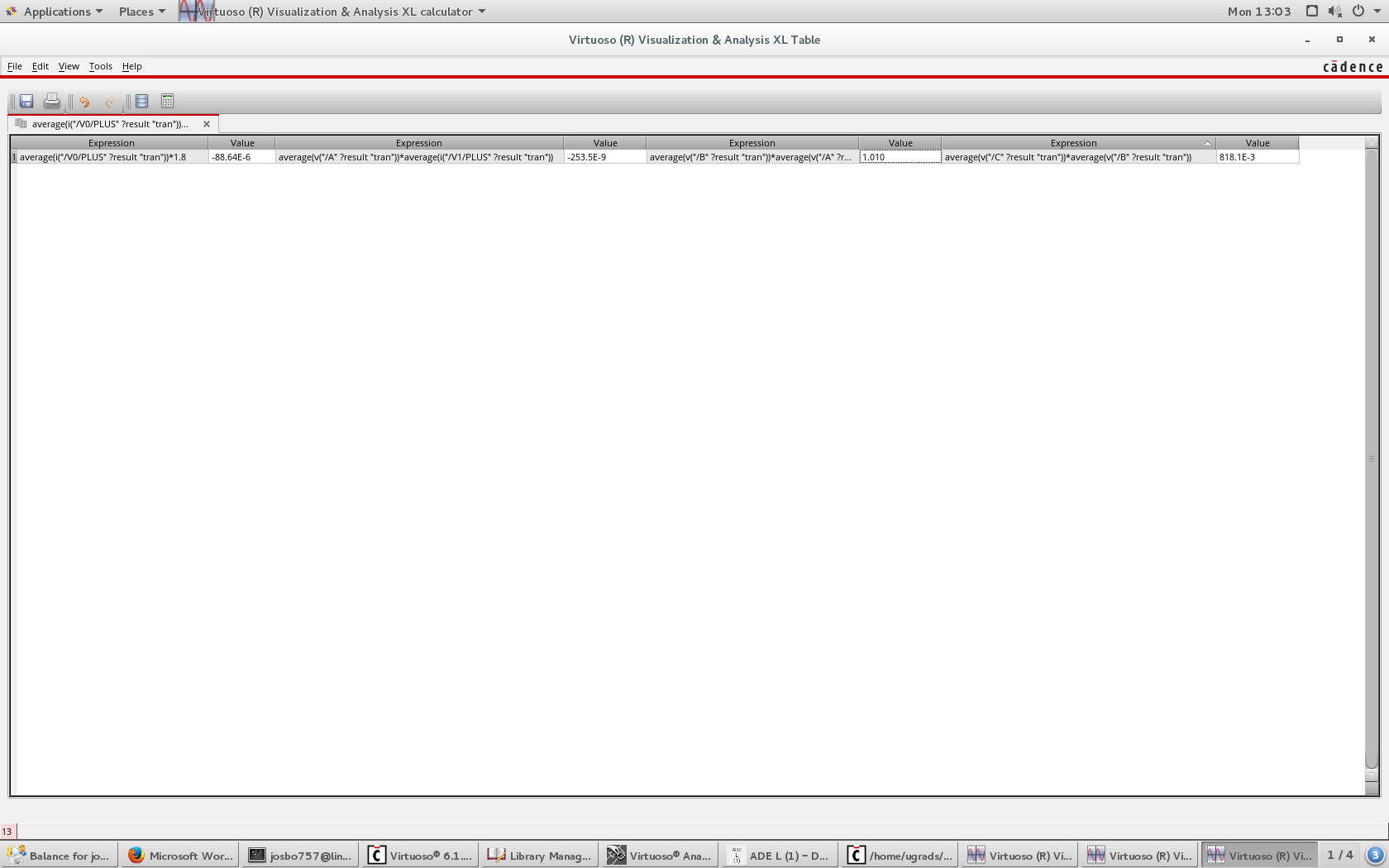
**1-Bit Threshold (Max Frequency)**

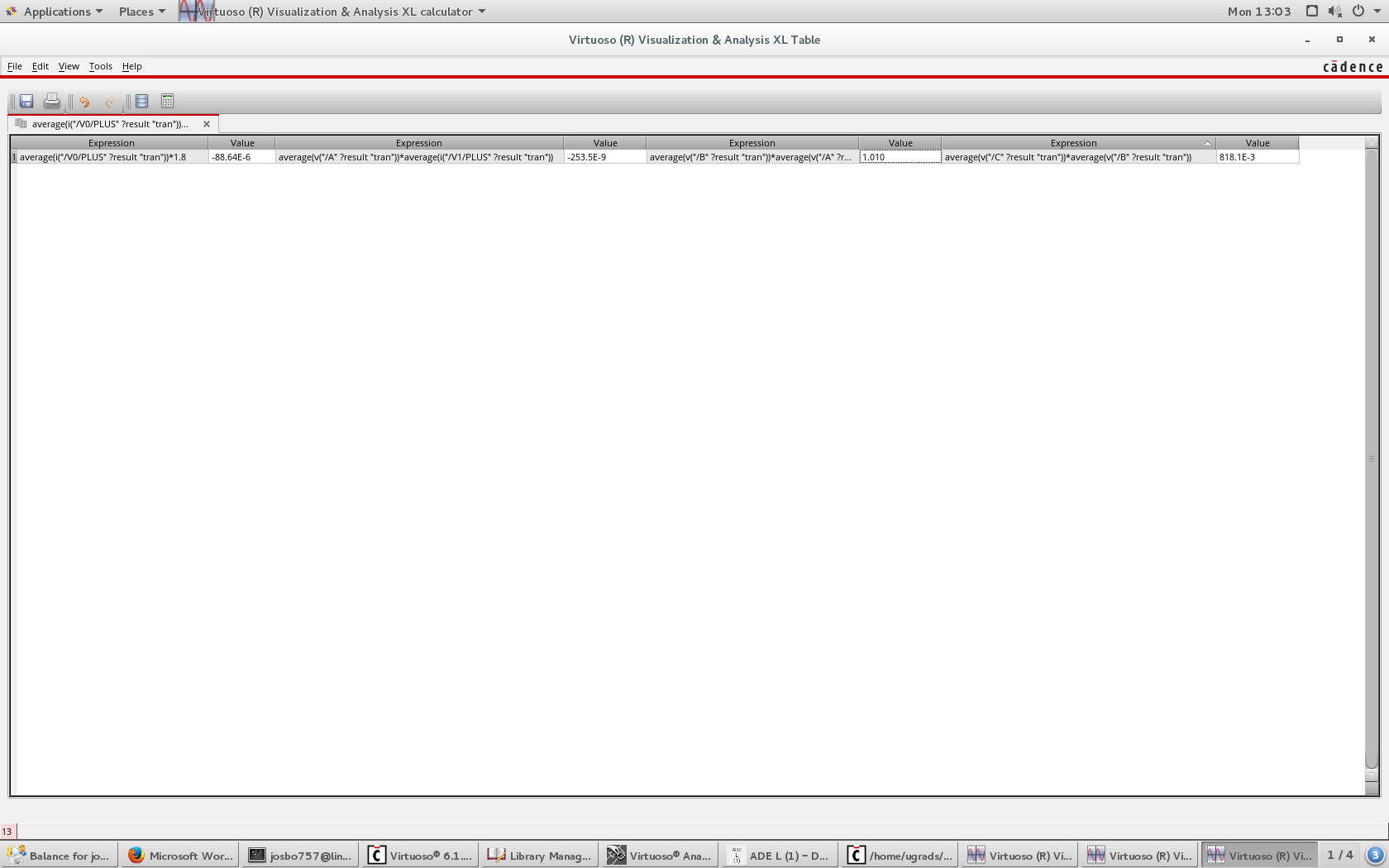
T = 2 ns

F= 500MHz



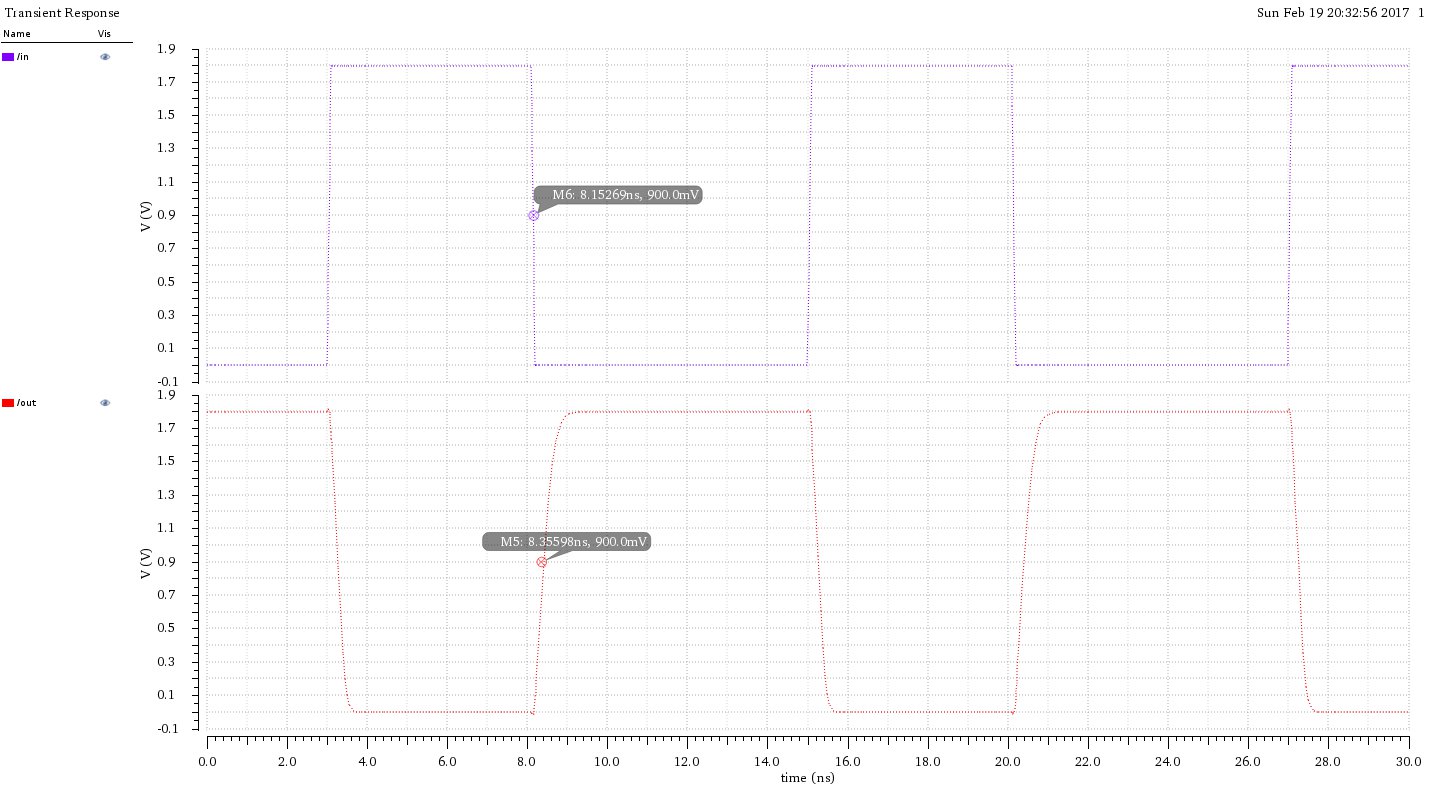
**1-Bit Adder Power Dissipation**

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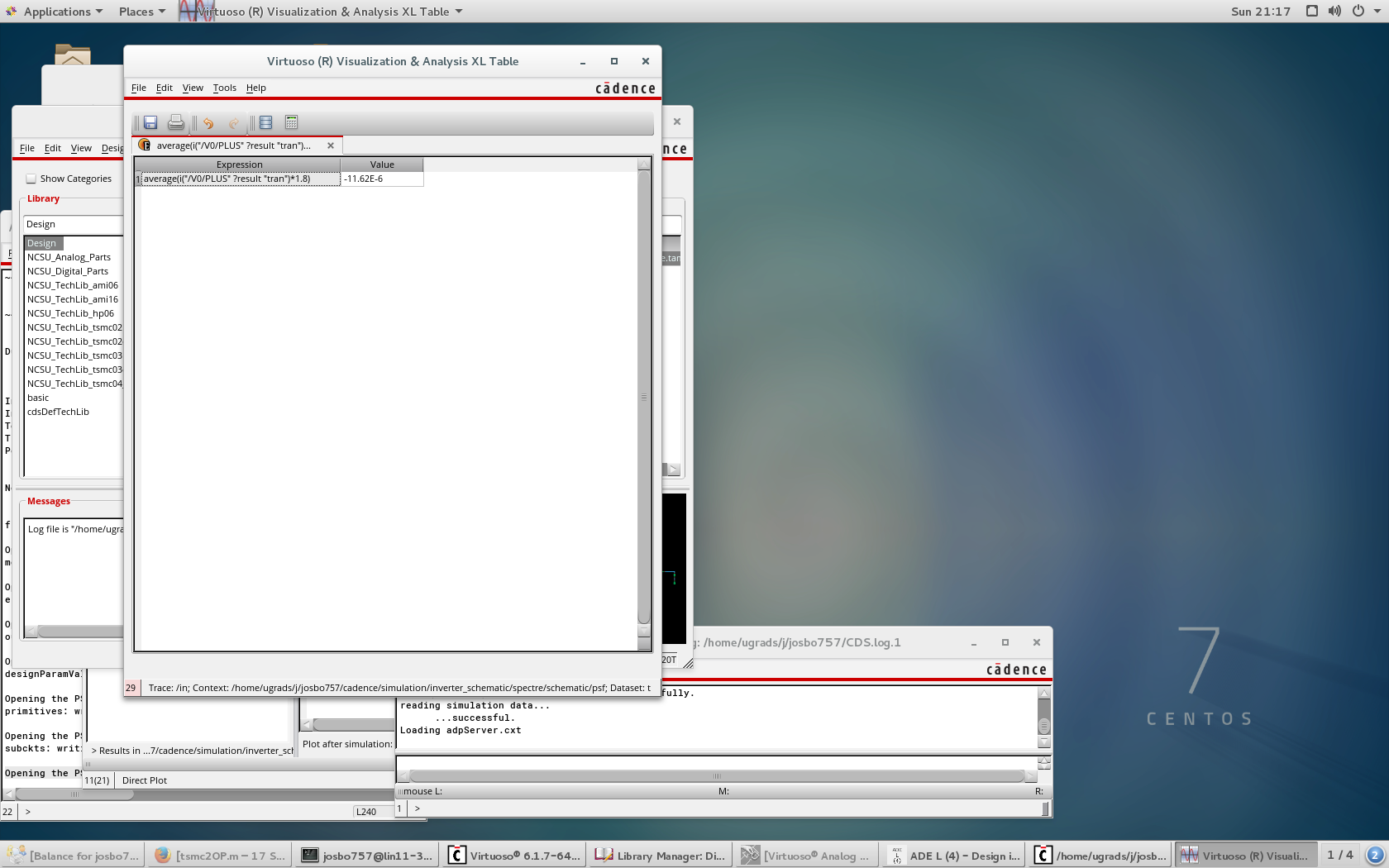
****

**Inverter Adder Rise and Delay**

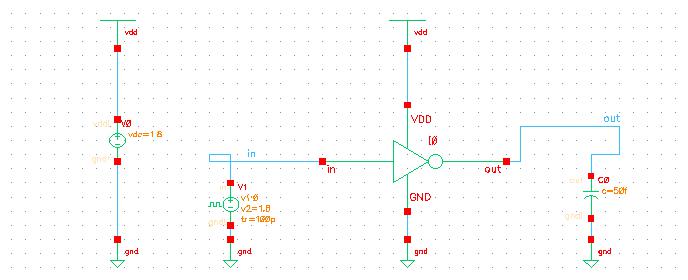
|  |  |  |
| --- | --- | --- |
| Fall(ns) | Rise(ns) | %error |
| 8.15269 | 8.35598 | 2.493533 |

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**Inverter Power Dissipation**

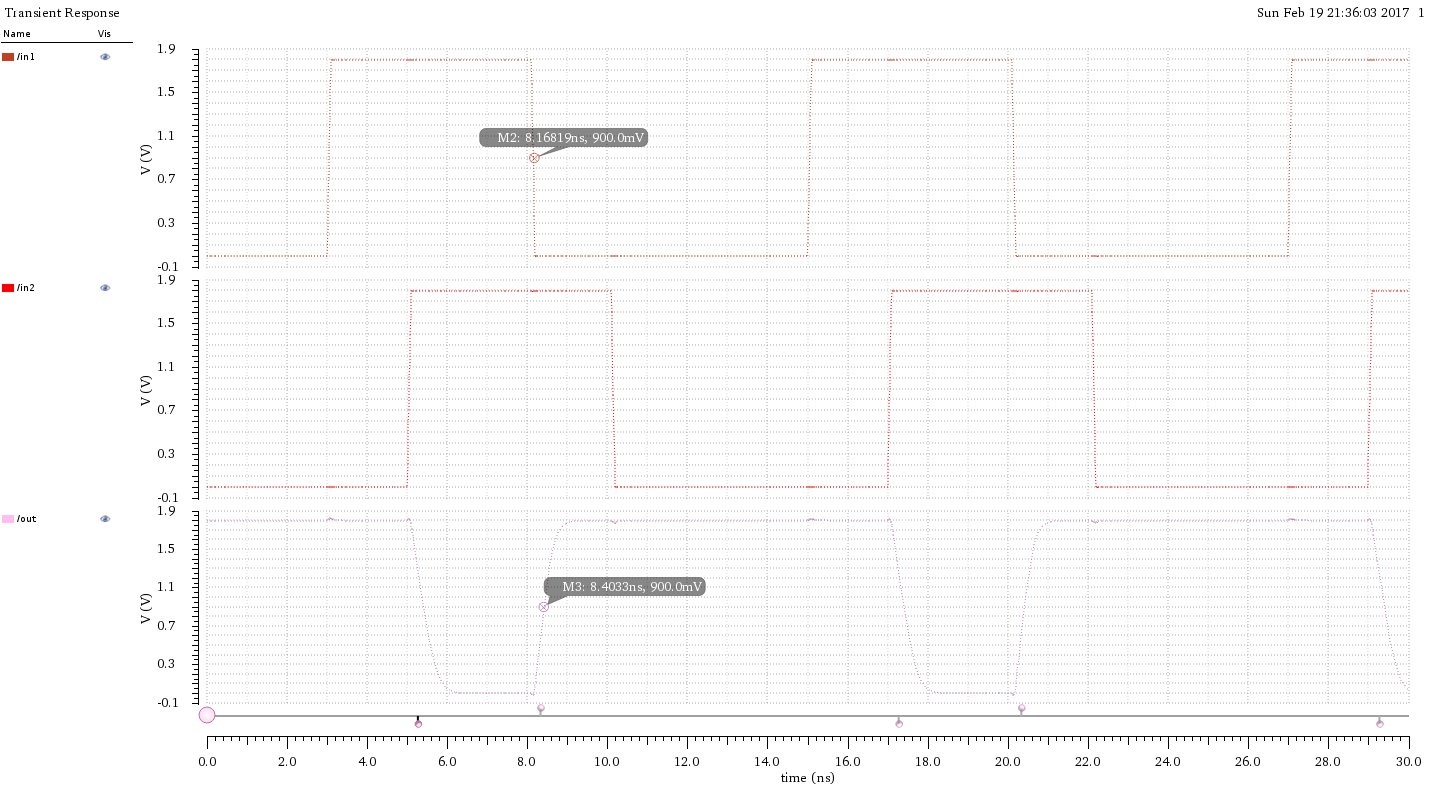


**Inverter Simulate Schematic**

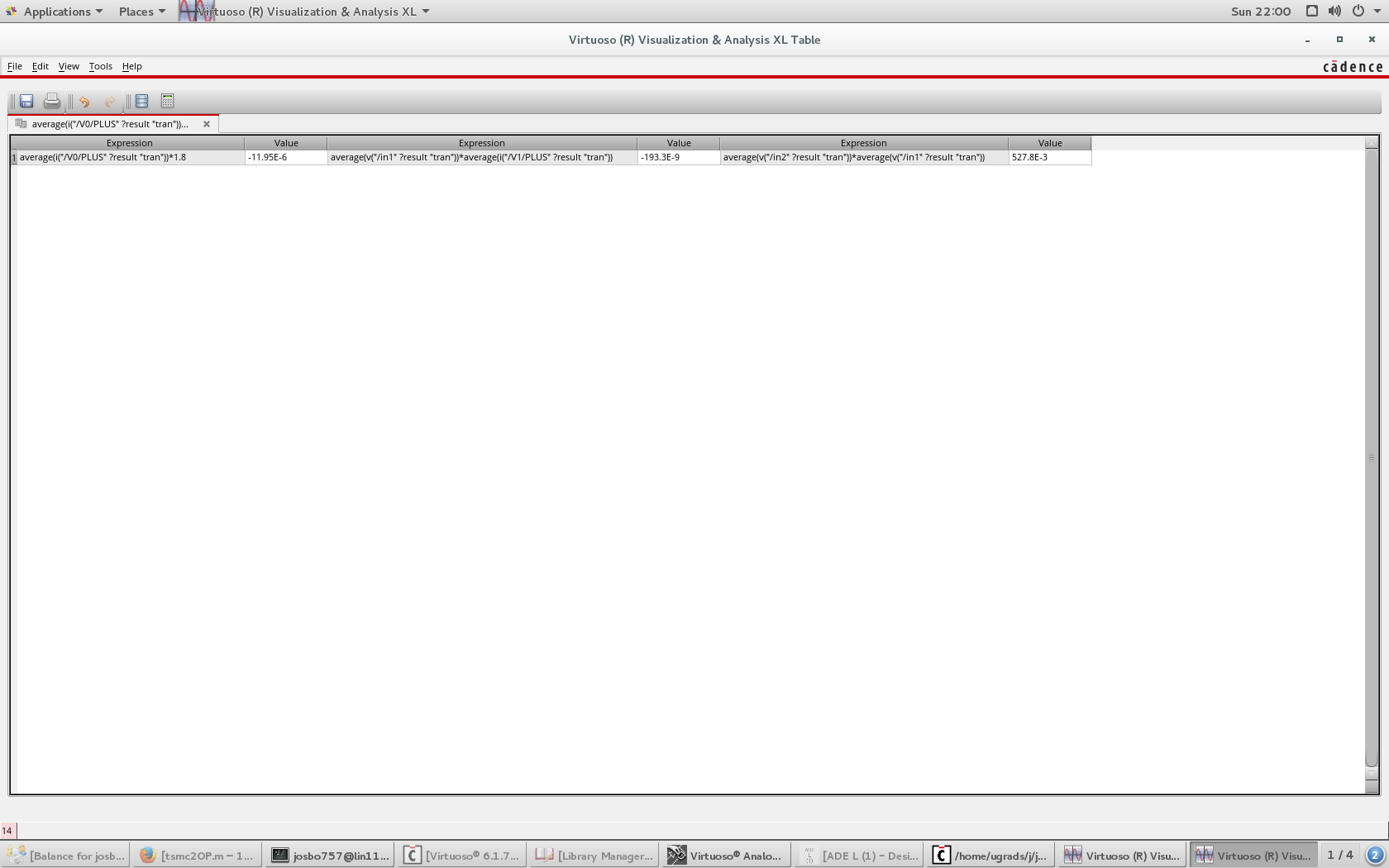
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**NAND2 Adder Rise and Delay**

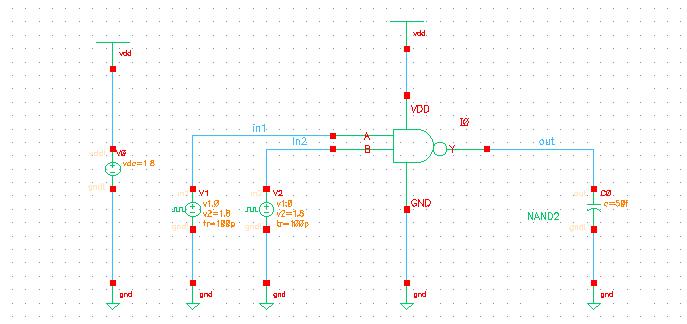
|  |  |  |
| --- | --- | --- |
| Fall(ns) | Rise(ns) | %error |
| 8.16819 | 8.4033 | 2.878361 |



**NAND2 Power Dissipation**

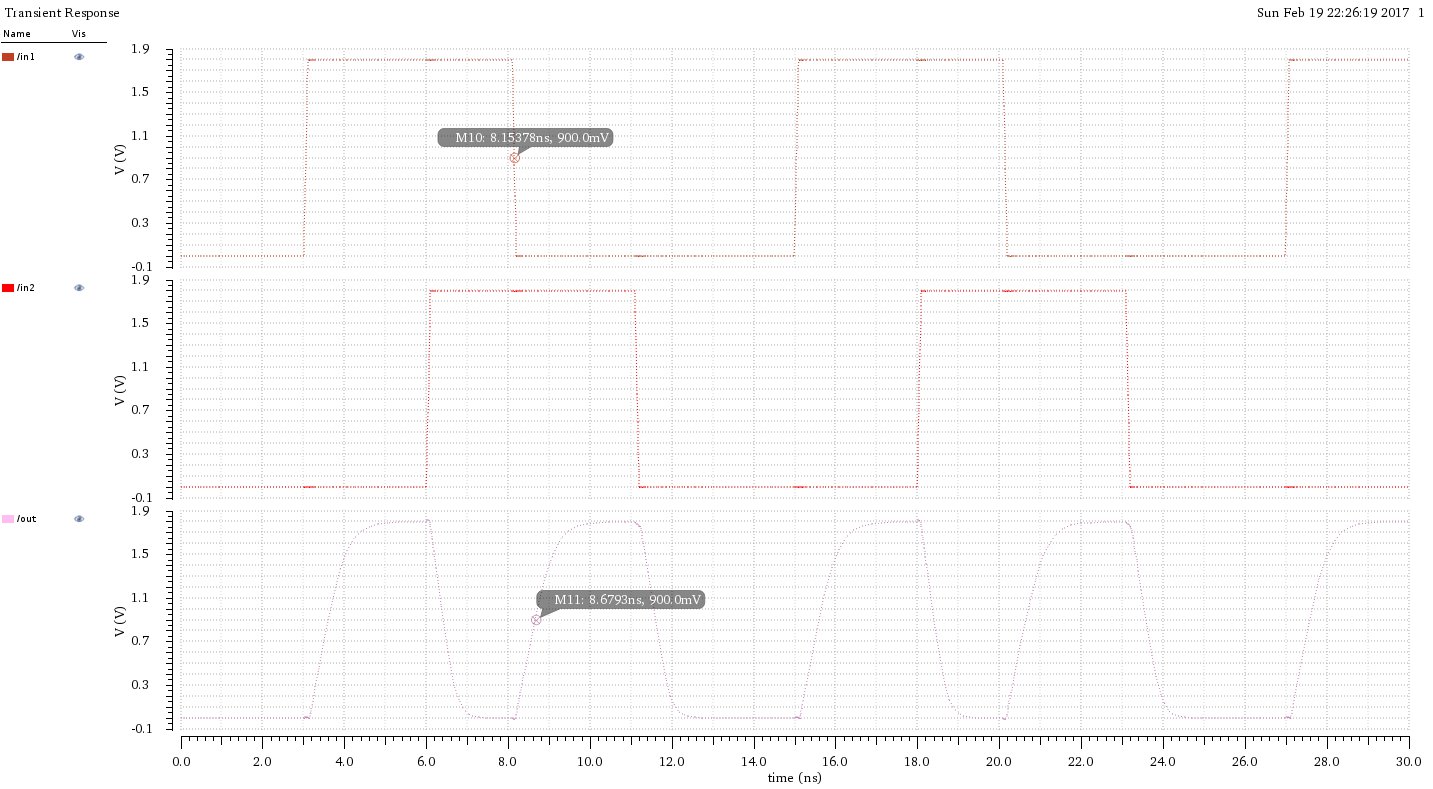
****

**NAND 2 Simulate Schematic**

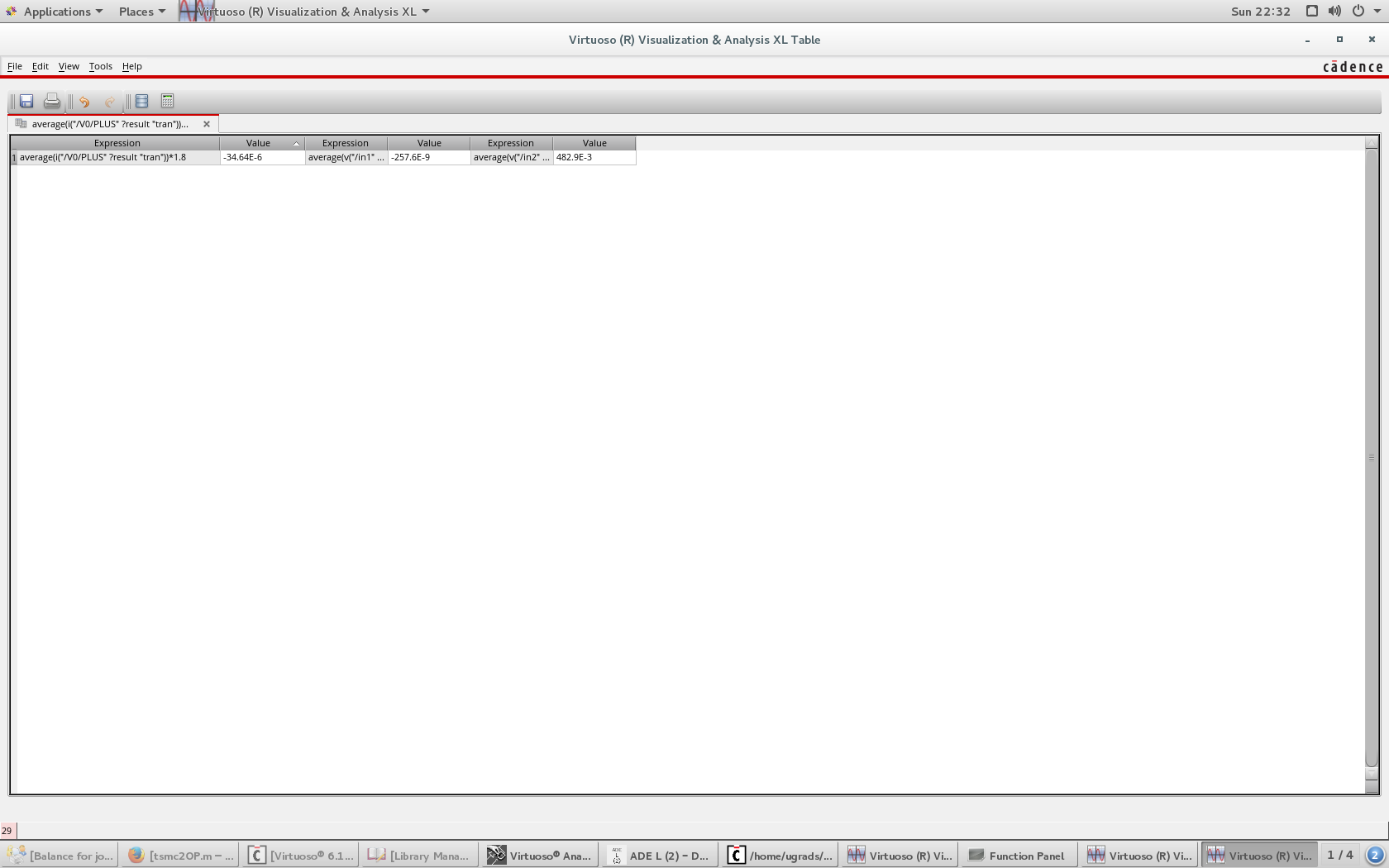
****

**XOR2 Adder Rise and Delay**

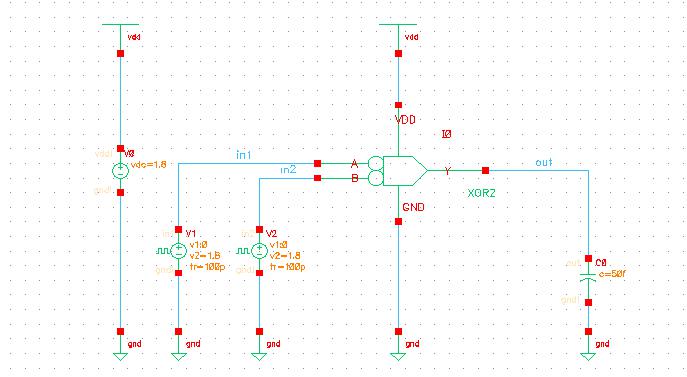
|  |  |  |
| --- | --- | --- |
| Fall(ns) | Rise(ns) | %error |
| 8.15378 | 8.6793 | 6.445109 |



**XOR2 Power Dissipation**



**XOR2 Simulate Schematic**

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