**Lab 5**

**Design and Simulation of 4-bit Adder**

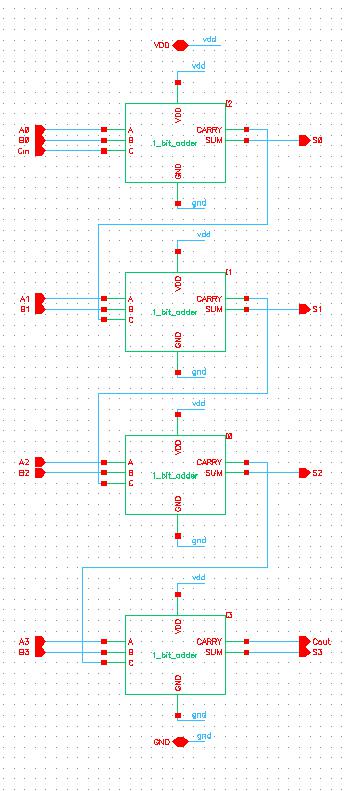
**Faizan Bangash**

**Section 506**

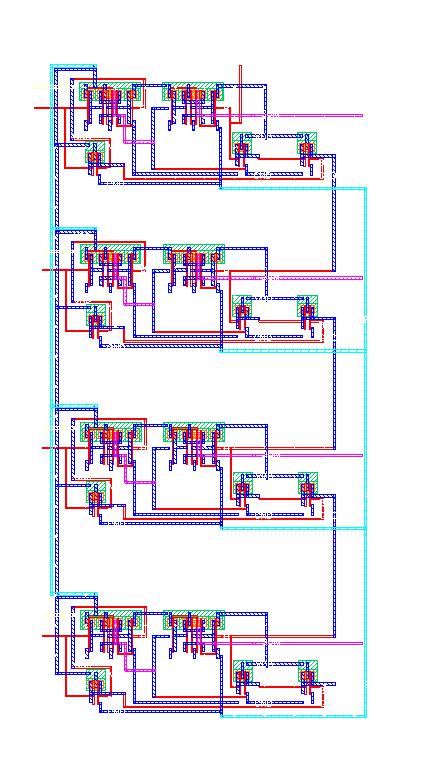
**TA: Lin Huang**

**DUE: 09 October 2018**

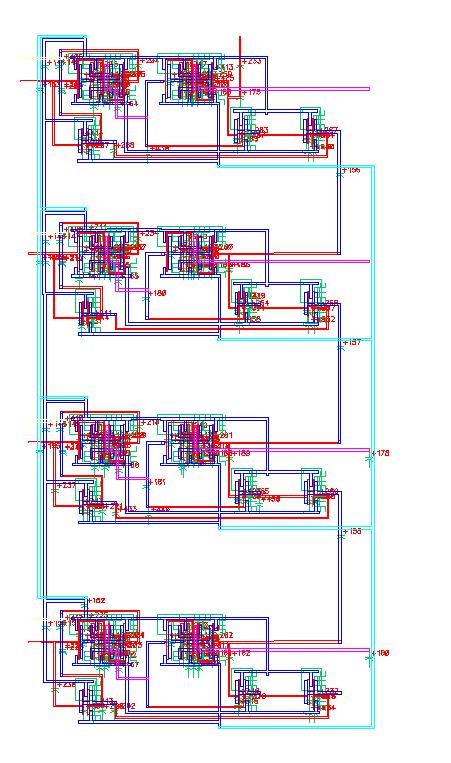
**4-Bit Adder Schematic**

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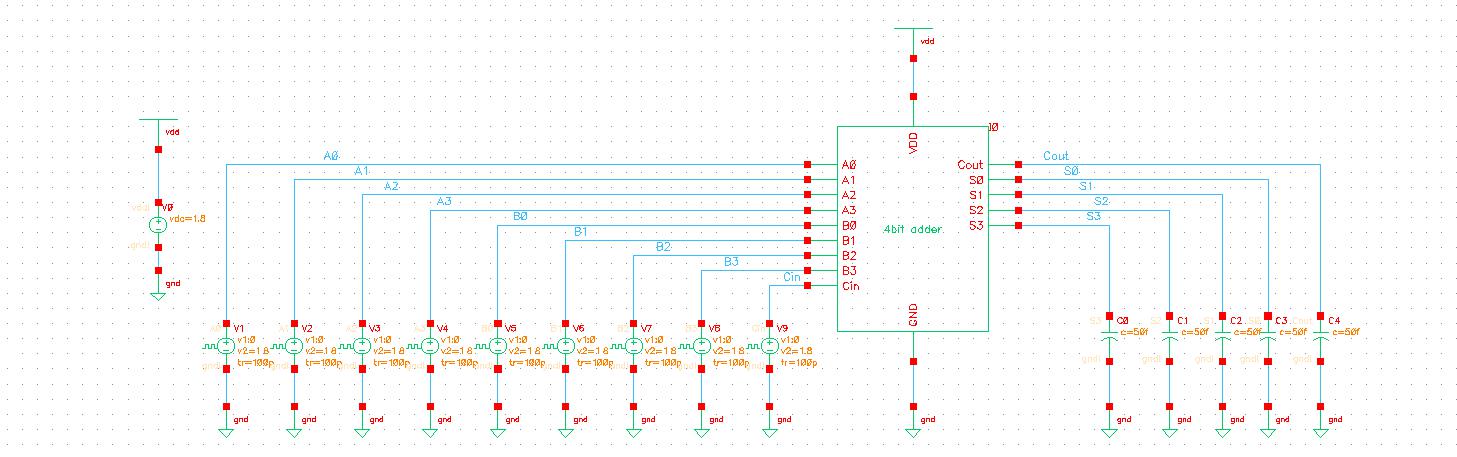
**4-Bit Adder Layout**

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**4-Bit Adder Extracted**

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**4-Bit Adder Simulate Schematic**

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# LVS Result:

Command line: /softwares/Linux/cadence/IC615/tools.lnx86/dfII/bin/32bit/LVS -dir /homes/ugrad/b/bangashfaizan1/cadence/lab5/LVS -l -s -t

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab5/LVS/layout/netlist

count

91 nets

16 terminals

72 pmos

72 nmos

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab5/LVS/schematic/netlist

count

91 nets

16 terminals

72 pmos

72 nmos

Terminal correspondence points

N82 N16 A<0>

N79 N14 A<1>

N76 N1 A<2>

N75 N8 A<3>

N90 N18 B<0>

N87 N4 B<1>

N86 N7 B<2>

N85 N6 B<3>

N81 N5 C

N89 N10 CARRY

N78 N11 GND

N84 N9 SUM<0>

N83 N0 SUM<1>

N80 N15 SUM<2>

N77 N12 SUM<3>

N88 N3 VDD

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

layout schematic

instances

un-matched 0 0

rewired 0 0

size errors 0 0

pruned 0 0

active 144 144

total 144 144

nets

un-matched 0 0

merged 0 0

pruned 0 0

active 91 91

total 91 91

terminals

un-matched 0 0

matched but

different type 0 0

total 16 16

Probe files from /homes/ugrad/b/bangashfaizan1/cadence/lab5/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /homes/ugrad/b/bangashfaizan1/cadence/lab5/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

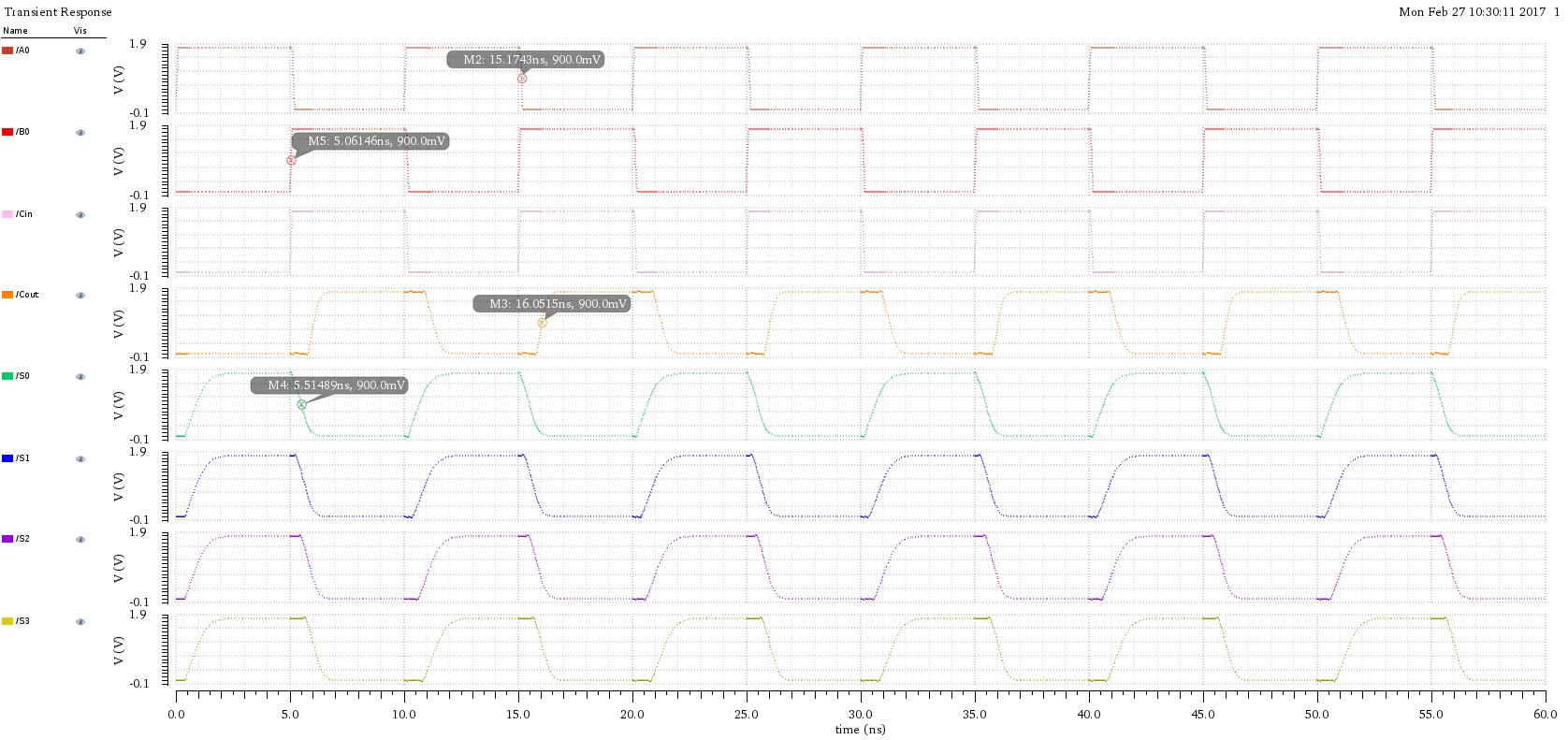
prunenet.out:

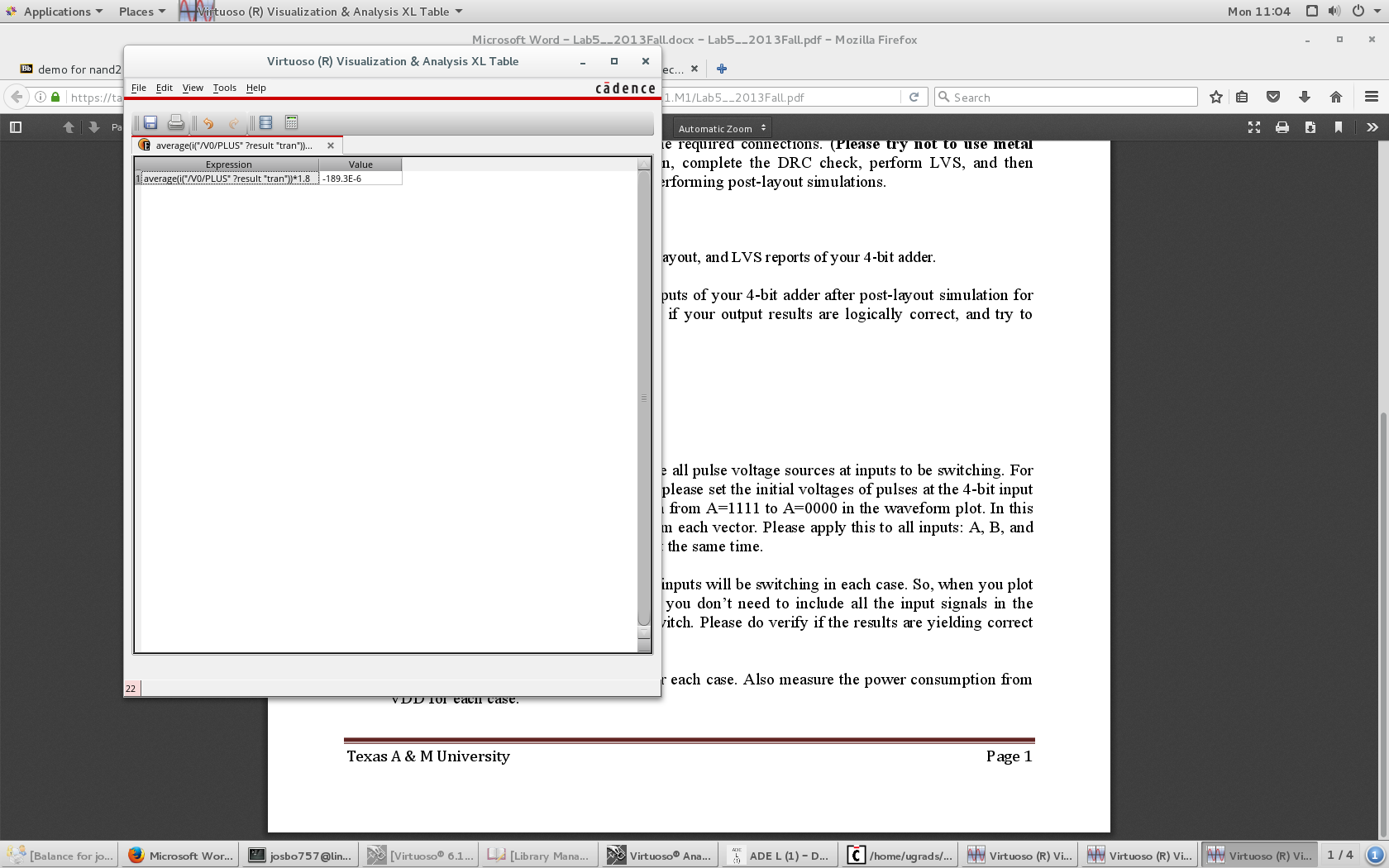
prunedev.out:

audit.out:

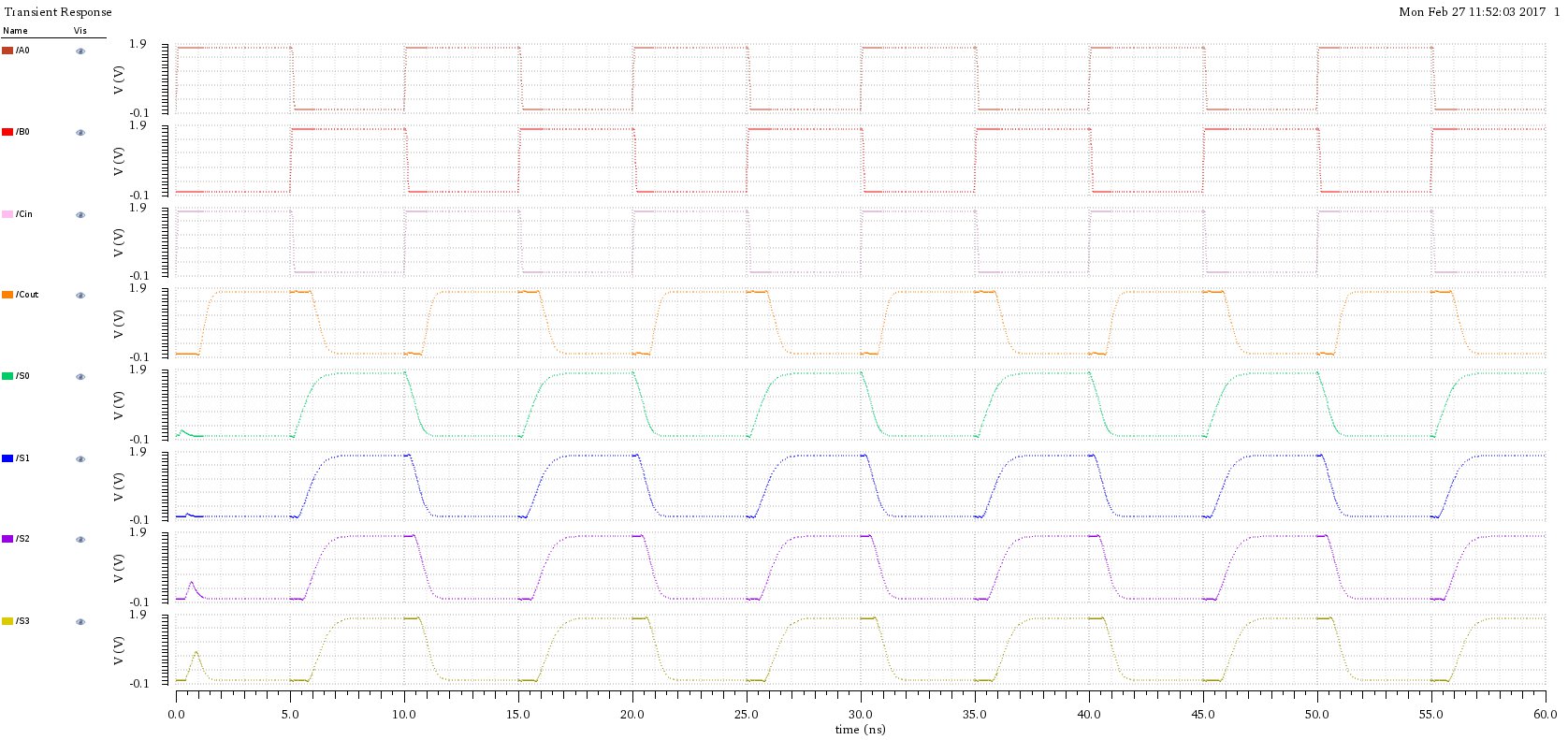
**4-Bit Adder (Rise and Delay), Waveforms and Power Consumption**

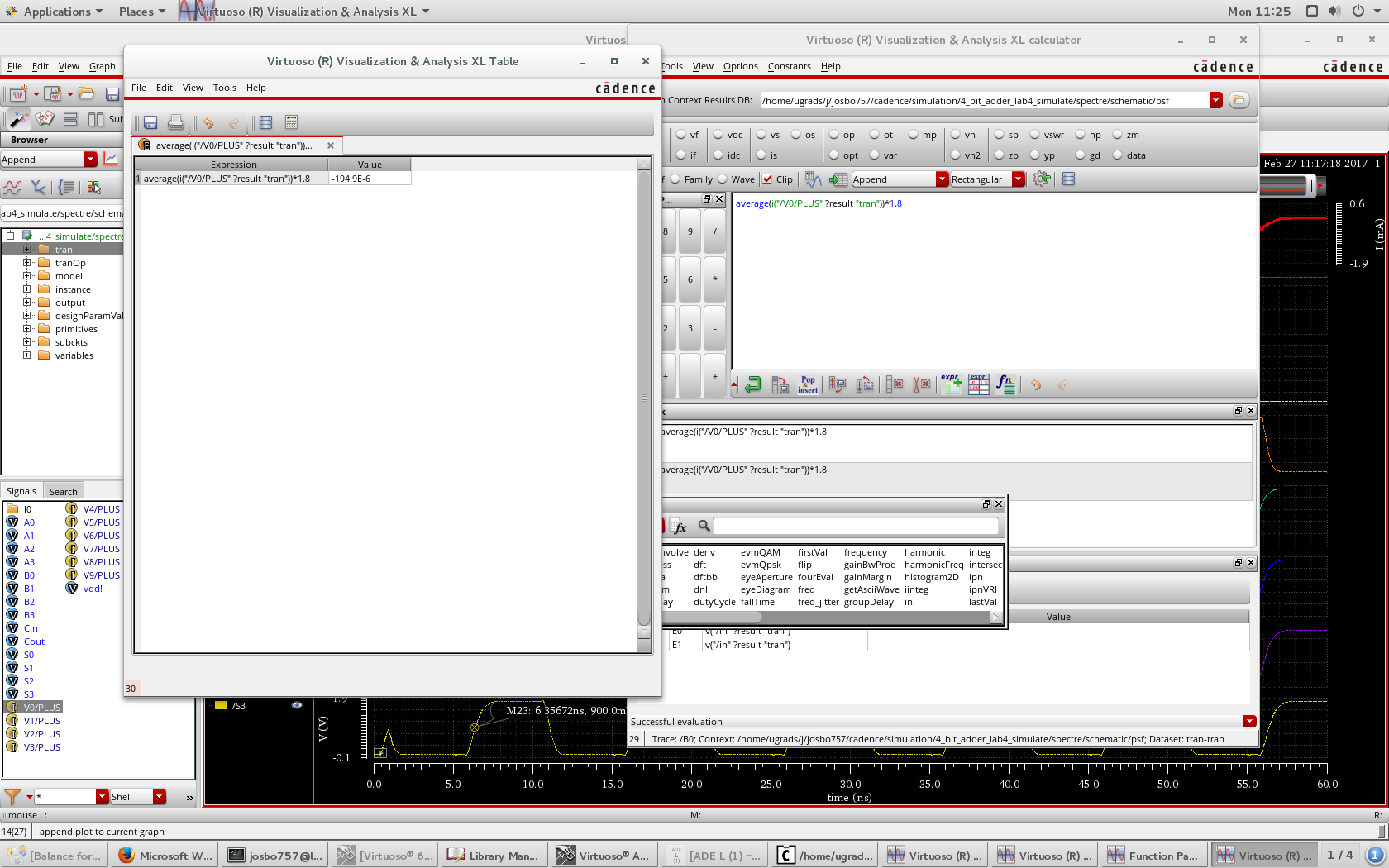
|  |  |  |  |
| --- | --- | --- | --- |
| A=0000 | B=1111 | Cin=1 |  |
|  | Fall(ns) | Rise(ns) | Delay(ps) |
| Cout | 15.1743 | 16.0515 | 877.2 |
| S0 | 5.51489 | 5.0614 | 454.5 |
| S1 | 5.51489 | 5.0614 | 453.5 |
| S2 | 5.51489 | 5.0614 | 453.5 |
| S3 | 5.51489 | 5.0614 | 453.5 |



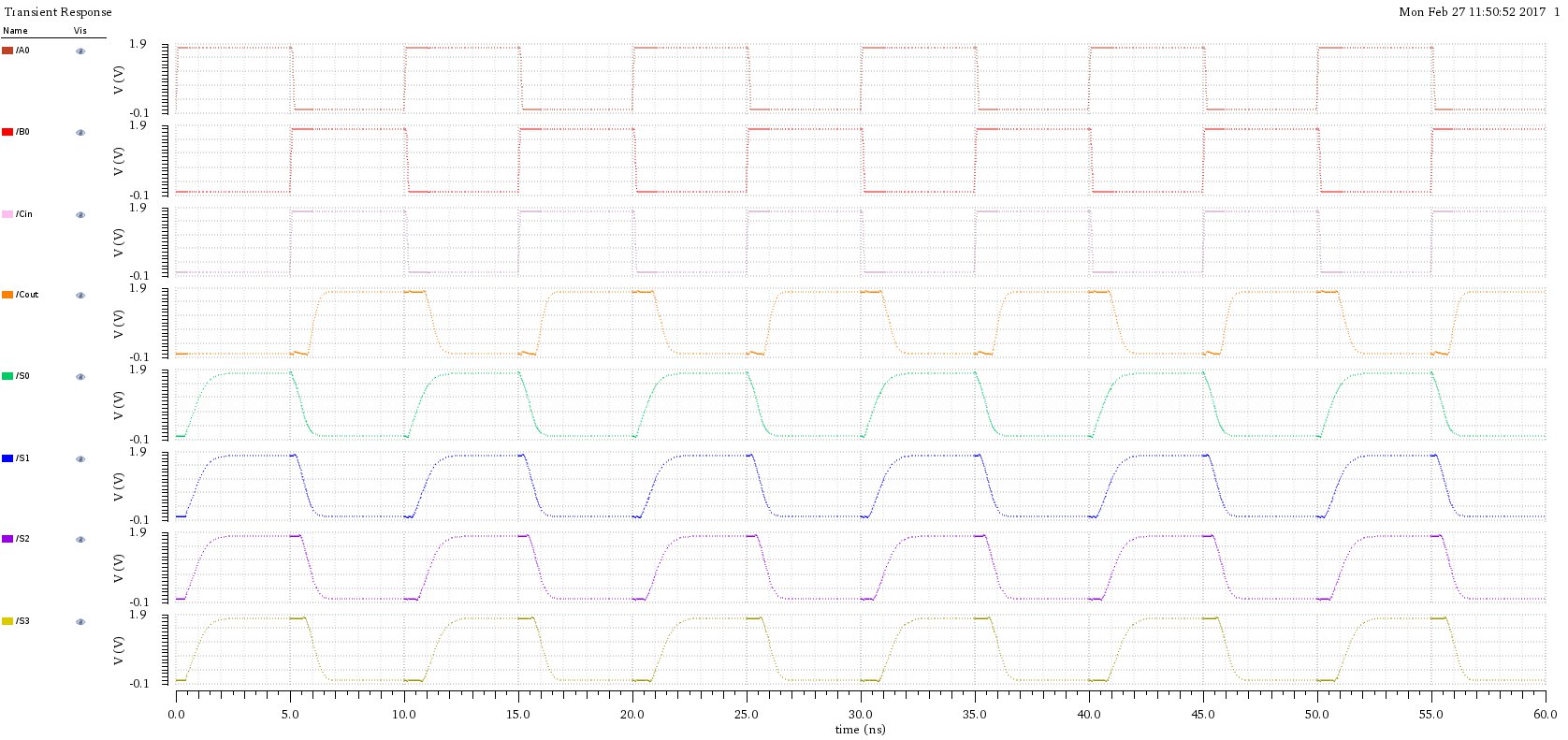


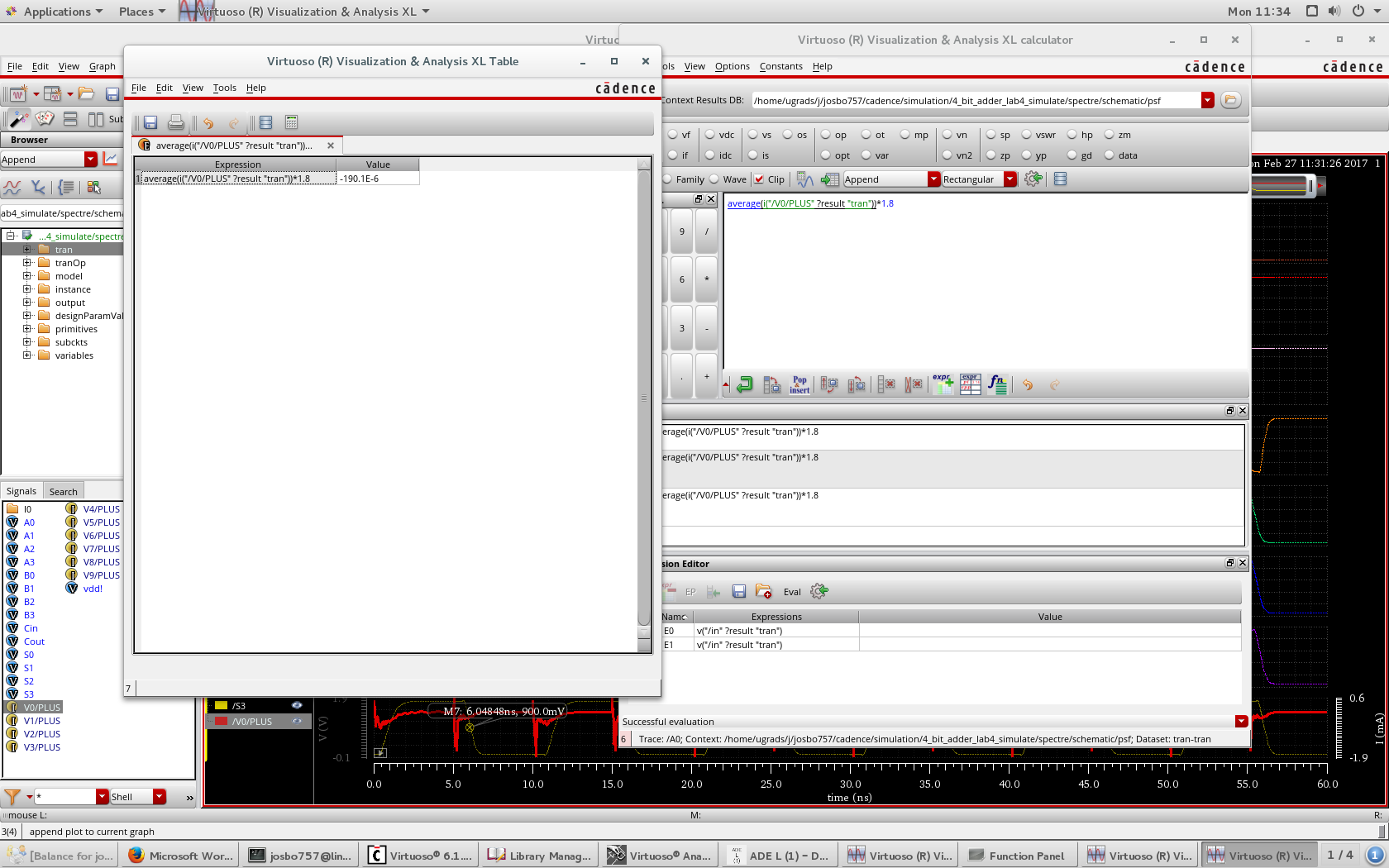
|  |  |  |  |
| --- | --- | --- | --- |
| A=1010 | B=0101 | Cin=0 |  |
|  | Fall(ns) | Rise(ns) | Delay(ps) |
| Cout | 6.25772 | 5.06104 | 1196.68 |
| S0 | 5.13979 | 5.67495 | 535.16 |
| S1 | 5.13979 | 5.92553 | 785.74 |
| S2 | 5.13979 | 6.04923 | 909.44 |
| S3 | 5.13979 | 6.35672 | 1216.93 |

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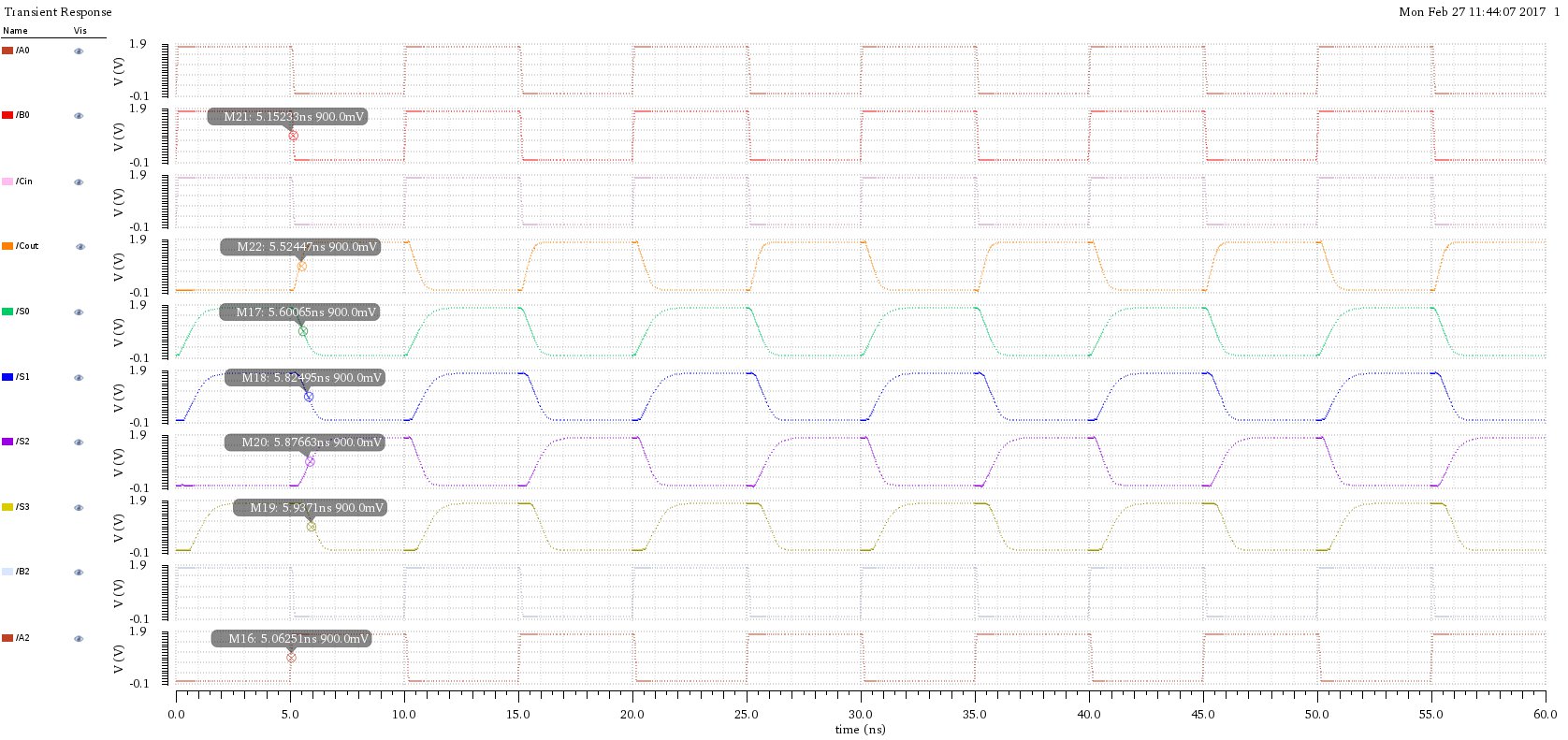
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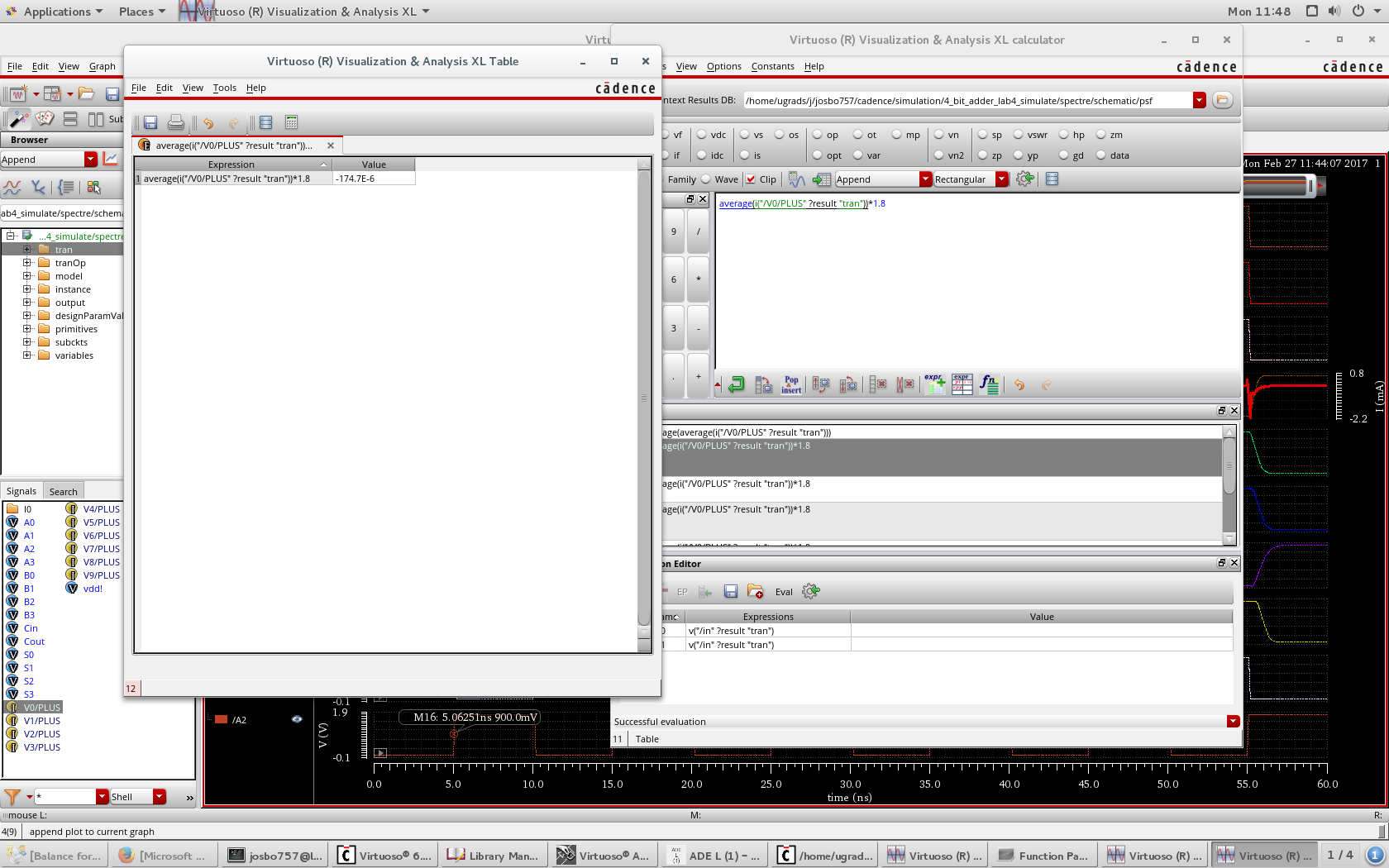
|  |  |  |  |
| --- | --- | --- | --- |
| A=1010 | B=0101 | Cin=1 |  |
|  | Fall(ns) | Rise(ns) | Delay(ps) |
| Cout | 5.14606 | 6.03209 | 886.03 |
| S0 | 5.52157 | 5.06001 | 461.56 |
| S1 | 5.65691 | 5.06001 | 596.90 |
| S2 | 5.71644 | 5.06001 | 656.43 |
| S3 | 6.04848 | 5.06001 | 988.47 |

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|  |  |  |  |
| --- | --- | --- | --- |
| A=1100 | B=1000 | Cin=0 |  |
|  | Fall(ns) | Rise(ns) | Delay(ps) |
| Cout | 5.15233 | 5.4388 | 286.47 |
| S0 | 5.60065 | 5.06521 | 535.44 |
| S1 | 5.82495 | 5.06521 | 759.74 |
| S2 | 5.15233 | 5.87663 | 724.30 |
| S3 | 5.9371 | 5.06521 | 871.89 |

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