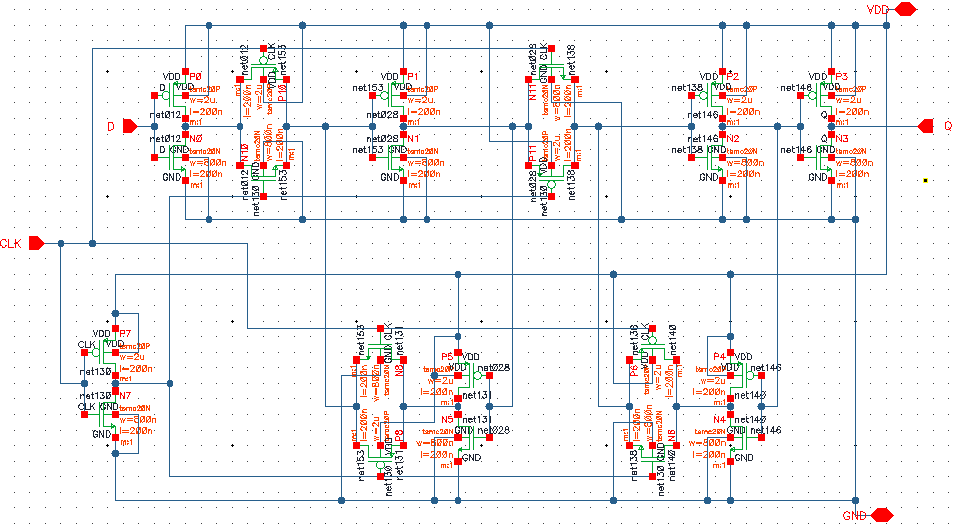
**Lab 7- – Design & Characterization of a Flip-flop**

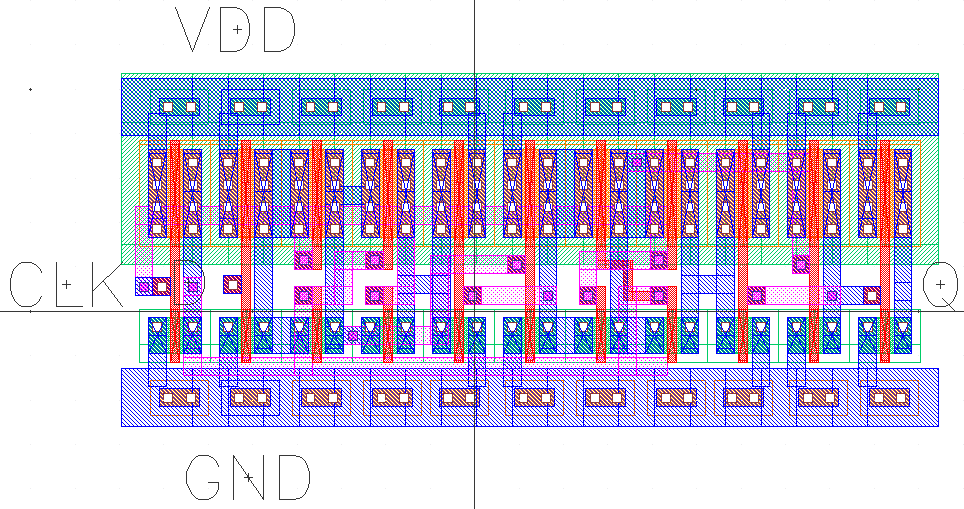
**Faizan Bangash**

**Section 506**

**TA: Lin Huang**

**DUE: 23 October 2018**

 Flip Flop Transistor level schematic



Flip Flop Layout

@(#)$CDS: LVS version 6.1.5 10/19/2018 15:04 (sjfdl054) $

Command line: /softwares/Linux/cadence/IC615/tools.lnx86/dfII/bin/32bit/LVS -dir /homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS -l -s -t

/homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/layout

/homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/layout/netlist

count

13 nets

5 terminals

11 pmos

11 nmos

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/schematic/netlist

count

13 nets

5 terminals

11 pmos

11 nmos

Terminal correspondence points

N10 N0 CLK

N11 N11 D

N8 N6 GND

N9 N7 Q

N12 N5 VDD

Devices in the netlist but not in the rules:

pcapacitor

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

**The net-lists match.**

layout schematic

instances

un-matched 0 0

rewired 0 0

size errors 0 0

pruned 0 0

active 22 22

total 22 22

nets

un-matched 0 0

merged 0 0

pruned 0 0

active 13 13

total 13 13

terminals

un-matched 0 0

matched but

different type 2 2

total 5 5

Probe files from /homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

? Terminal CLK's type in the schematic: input, in the layout: inputOutput

? Terminal D's type in the schematic: input, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:

Probe files from /homes/ugrad/b/bangashfaizan1/cadence/lab7/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

? Terminal CLK's type in the layout: inputOutput, in the schematic: input

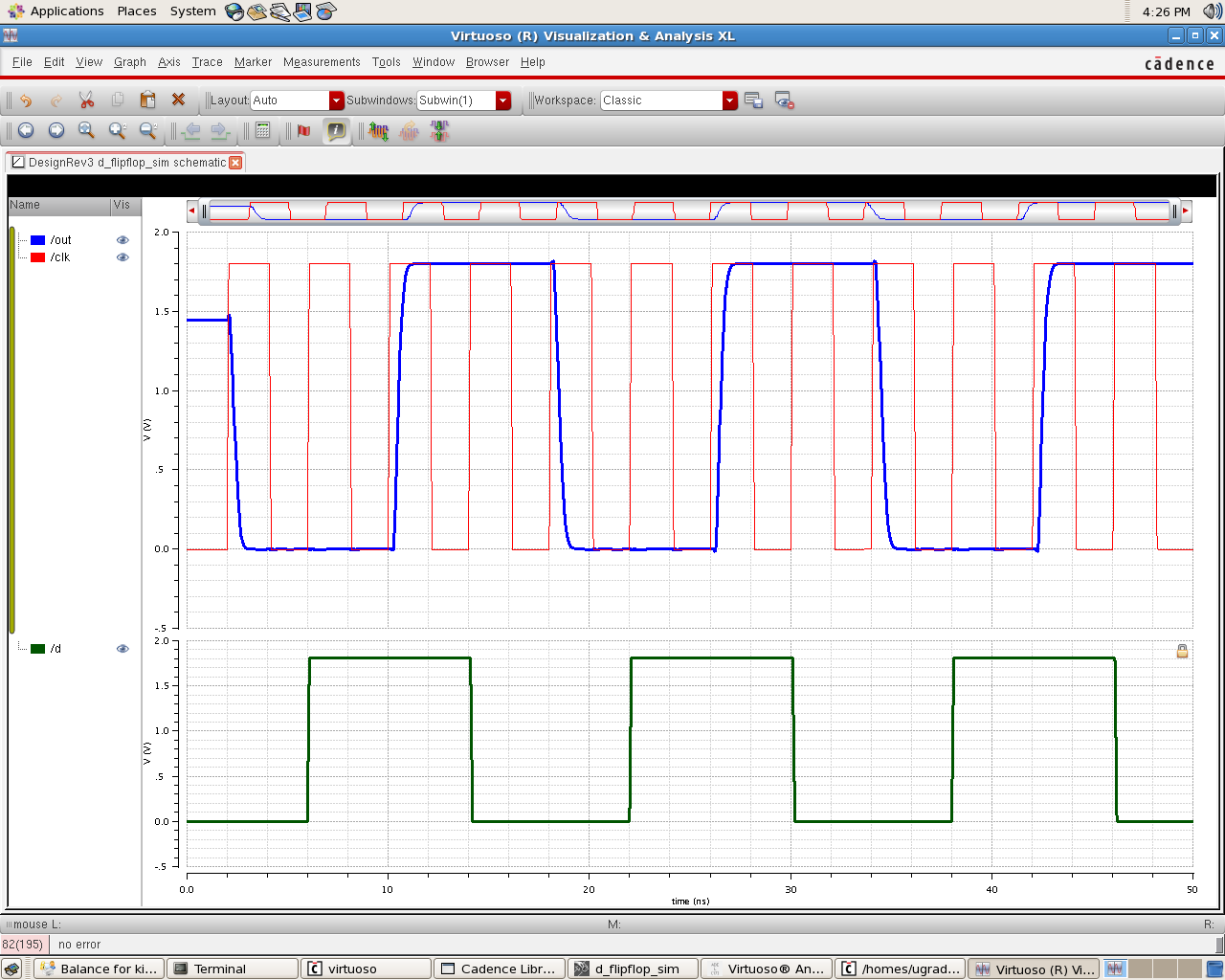
? Terminal D's type in the layout: inputOutput, in the schematic: input

prunenet.out:

prunedev.out:

audit.out:

LVS report

****

Flip Flop simulation verifying proper functionality

|  |  |  |  |
| --- | --- | --- | --- |
| output capacitance | rise time (in ps) | fall time (in ps) | %diff |
| 1 | 249.6 | 195.5 | -27.6726 |
| 2 | 253.1 | 199.6 | -26.8036 |
| 5 | 262.4 | 210.9 | -24.4192 |
| 10 | 276.1 | 228.3 | -20.9374 |
| 25 | 311 | 273.9 | -13.5451 |
| 50 | 363.3 | 343.1 | -5.8875 |
| 75 | 414.2 | 411.1 | -0.75407 |
| **100** | **465** | **478.9** | **2.902485** |

Flip Flop Capacitance Delay Simulation

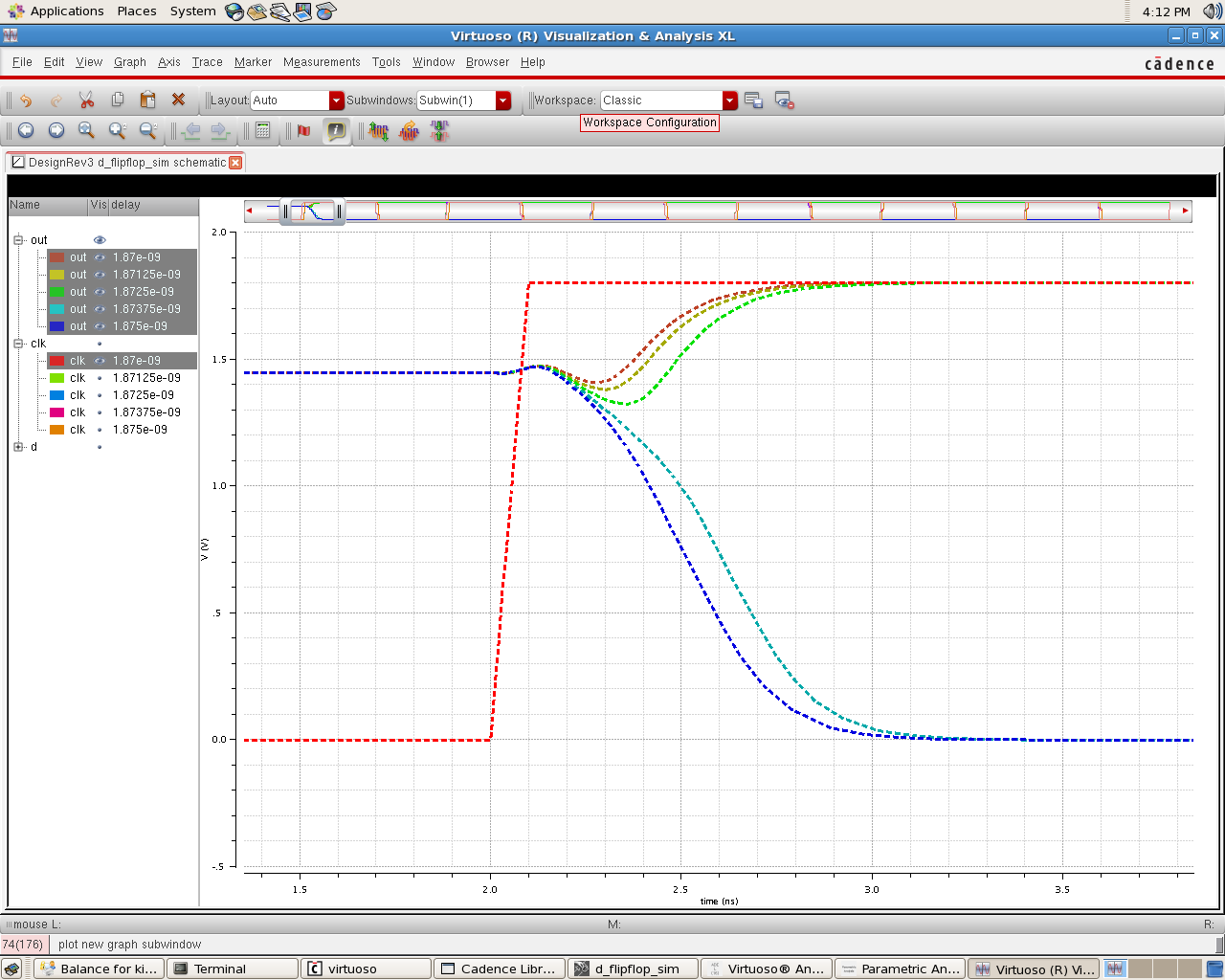
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Frquency (MHz) | V-Sin Current (µA) | | Capacitance (C=i/2pif) in fF | |
| 49 | 2.243 | 7.29 | |
| 101 | 4.615 | 7.27 | |
| 201 | 9.189 | 7.28 | |
| 301 | 13.765 | 7.28 | |
| 400 | 19.287 | 7.67 | |
| 502 | 22.917 | 7.27 | |
| 600 | 27.391 | 7.27 | |
| 700 | 31.97 | 7.27 | |
| 800 | 36.509 | 7.26 | |
| 900 | 41.072 | 7.26 | |
| 950 | 43.357 | 7.26 | |
| **AVERAGE** | **-----** | **7.263 fF** | |

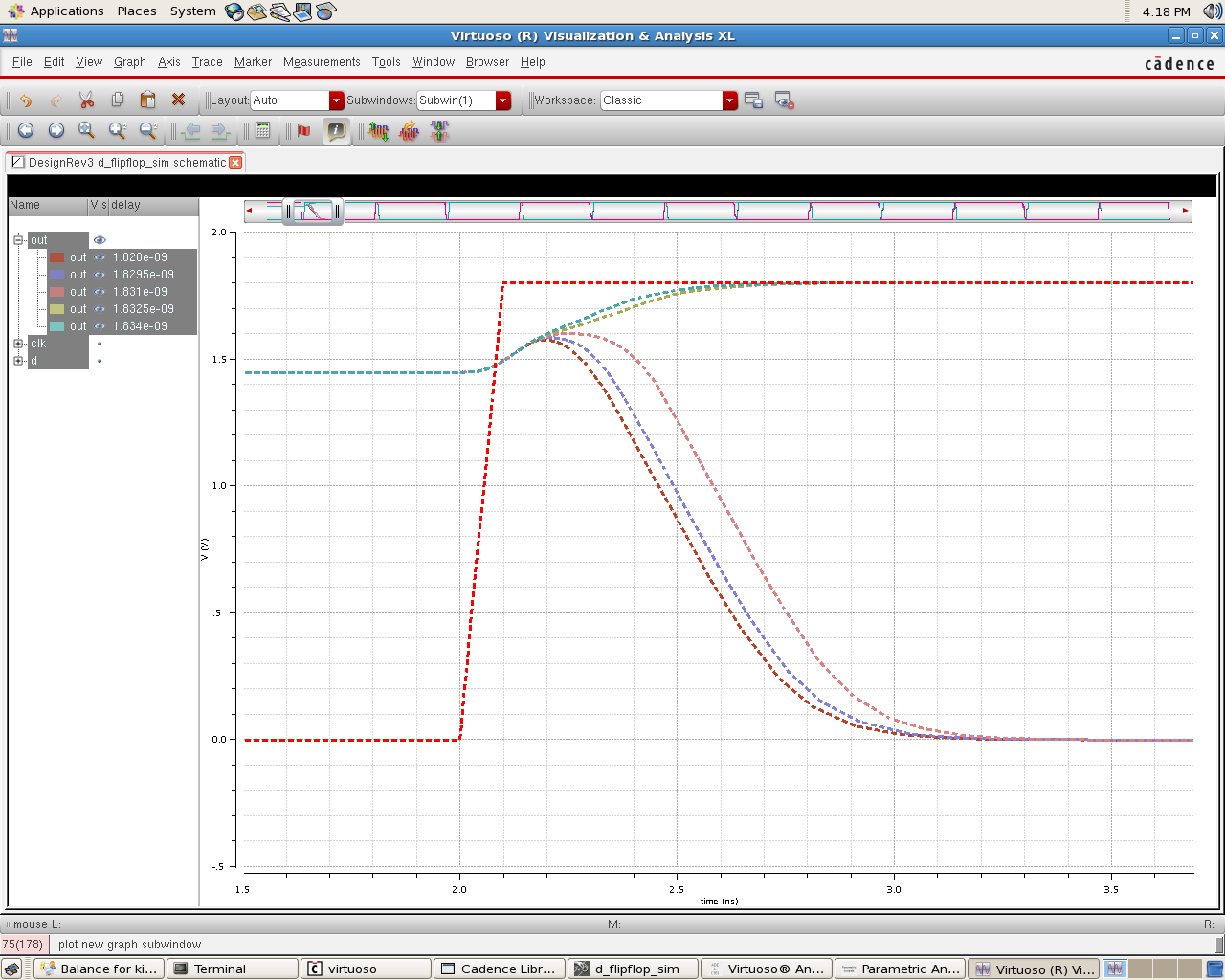
Current vs FrequencySimulation and GIC Calculation

**Setup Time**

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The setup time of a rising and falling D Flip-Flop is found and illustrated in the following two figures:

  
D-Flip Flop rising setup time

  
D-Flip Flop falling setup time