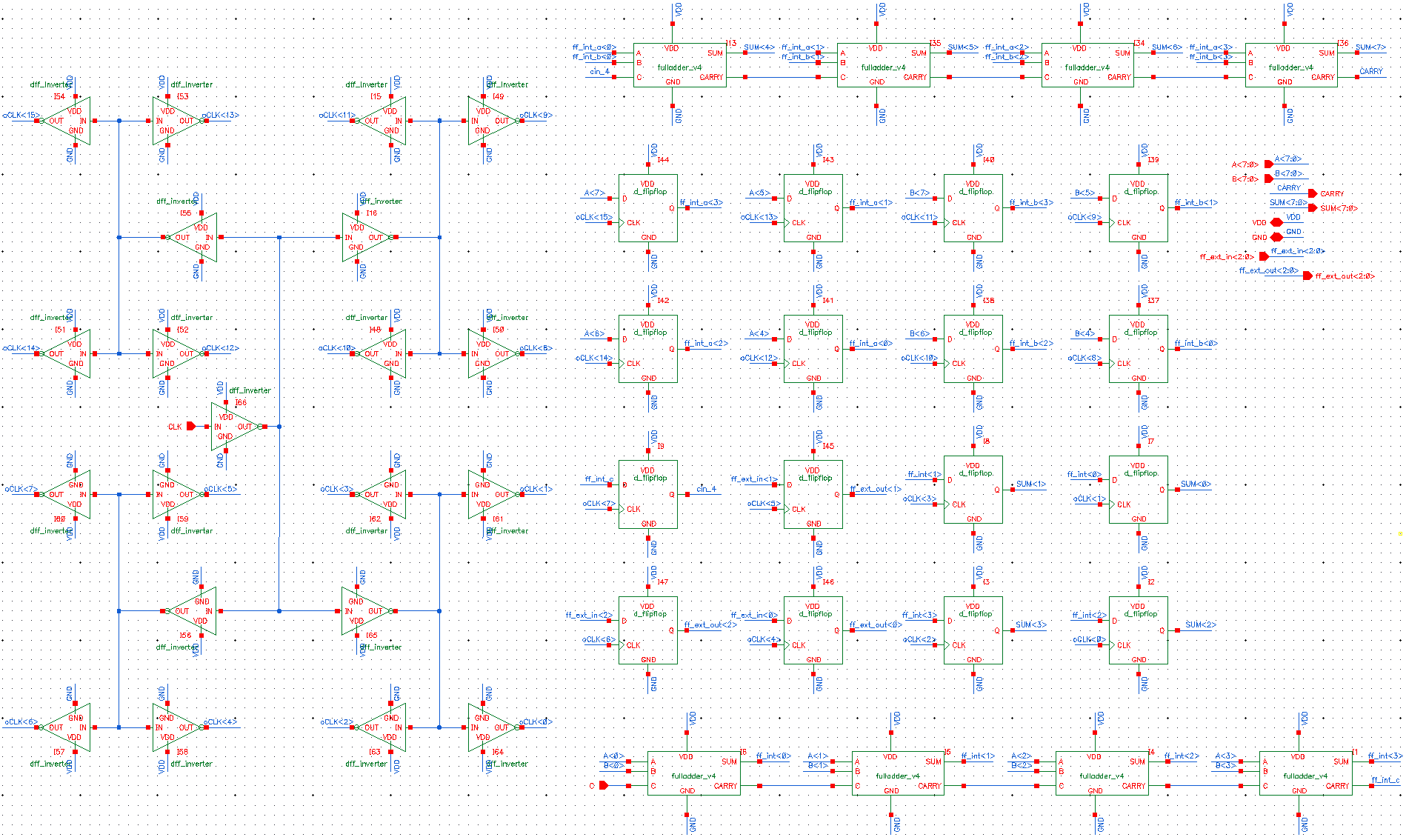
**Lab8: Design of 8-bit pipelined Adder with buffered H-clock tree**

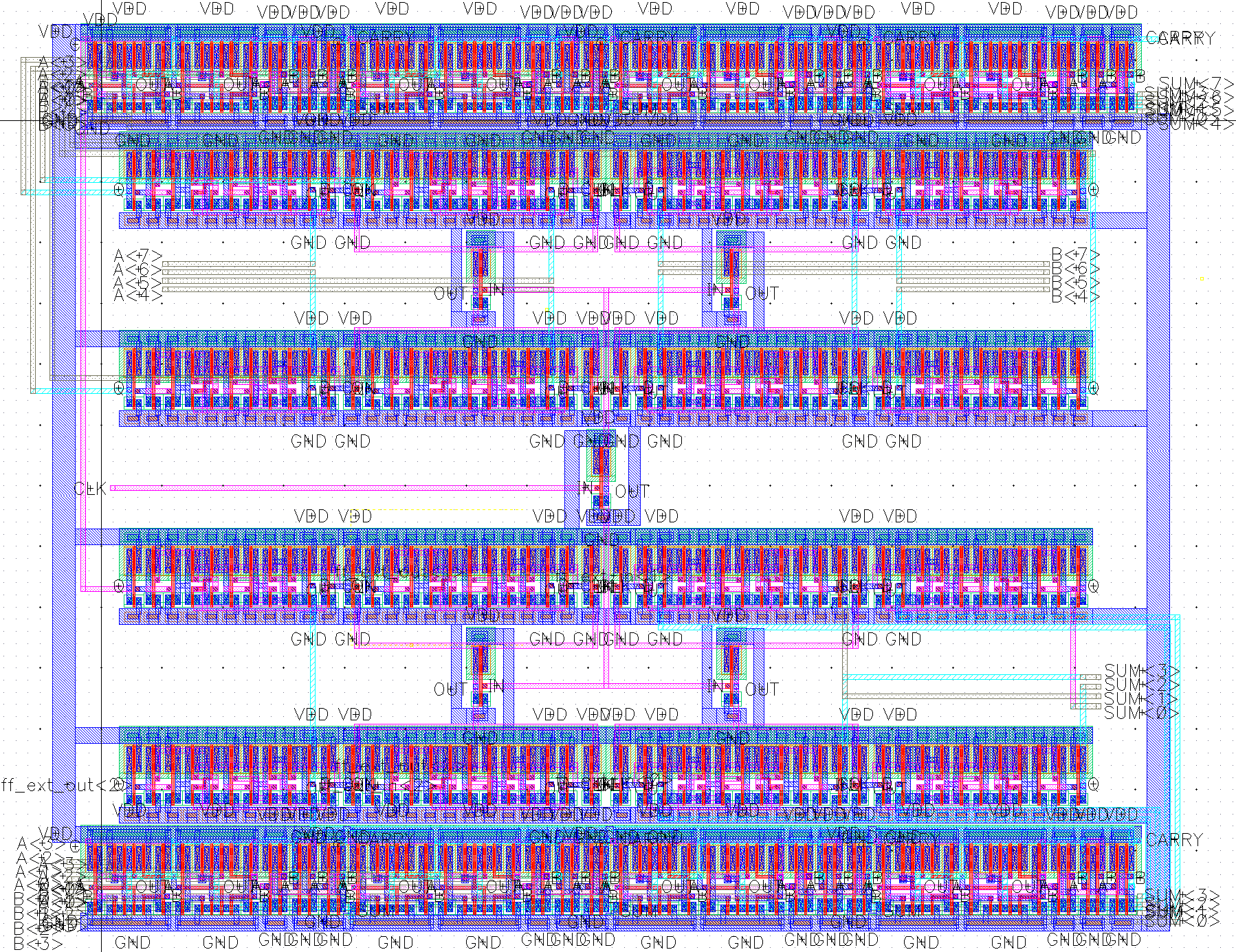
**Faizan Bangash**

**Section 506**

**TA: Lin Huang**

**DUE: 06 November 2018**

8-Bit Pipelined Adder Schematic



8-Bit Pipelined Adder Physical Layout. The physical circuit size was found to be  
**74.65 µm x 95.241 µm, or 7.11 nm2**.

D

Q

D

Q

Q

Q

D

D

Command line: /softwares/Linux/cadence/IC615/tools.lnx86/dfII/bin/32bit/LVS -dir /homes/ugrad/b/bangashfaizan1/cadence/lab9/LVS -l -s -t /homes/ugrad/b/bangashfaizan1/cadence/lab9/LVS/layout /homes/ugrad/b/bangashfaizan1/cadence/lab9/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab9/LVS/layout/netlist

count

348 nets

35 terminals

341 pmos

341 nmos

Net-list summary for /homes/ugrad/b/bangashfaizan1/cadence/lab9/LVS/schematic/netlist

count

348 nets

35 terminals

341 pmos

341 nmos

Terminal correspondence points

N328 N19 A<0>

N321 N67 A<1>

N316 N64 A<2>

N313 N65 A<3>

N344 N10 A<4>

N340 N9 A<5>

N337 N8 A<6>

N335 N7 A<7>

N347 N44 B<0>

N342 N66 B<1>

N339 N13 B<2>

N336 N6 B<3>

N332 N21 B<4>

N327 N15 B<5>

N320 N17 B<6>

N315 N14 B<7>

N326 N27 C

N346 N20 CARRY

N325 N75 CLK

N318 N0 GND

N333 N28 SUM<0>

N329 N26 SUM<1>

N322 N25 SUM<2>

N317 N60 SUM<3>

N314 N5 SUM<4>

N345 N4 SUM<5>

N341 N1 SUM<6>

N338 N3 SUM<7>

N343 N47 VDD

N334 N57 ff\_ext\_in<0>

N330 N36 ff\_ext\_in<1>

N323 N39 ff\_ext\_in<2>

N331 N45 ff\_ext\_out<0>

N324 N33 ff\_ext\_out<1>

N319 N70 ff\_ext\_out<2>

Devices in the netlist but not in the rules:

pcapacitor

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

**The net-lists match.**

layout schematic

instances

un-matched 0 0

rewired 0 0

size errors 0 0

pruned 0 0

active 682 682

total 682 682

nets

un-matched 0 0

merged 0 0

pruned 0 0

active 348 348

total 348 348

terminals

un-matched 0 0

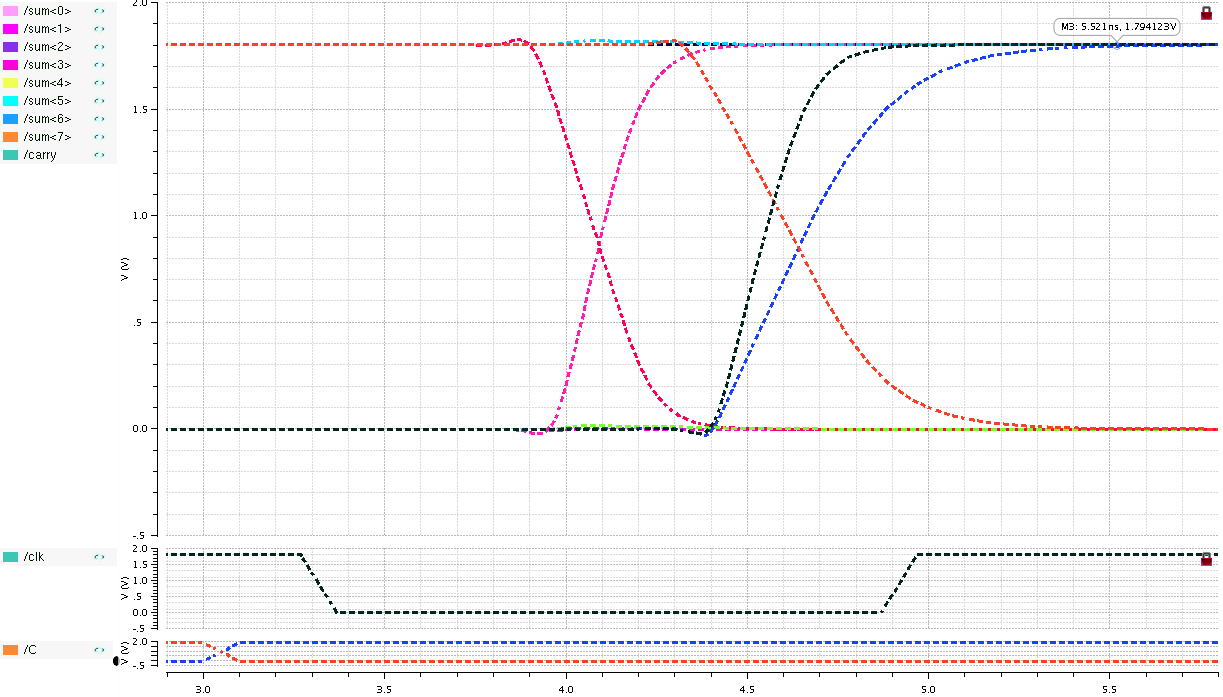
matched but

different type 0 0

total 35 35

**8bit\_adder\_si.spi**

**Verification and Evaluation**

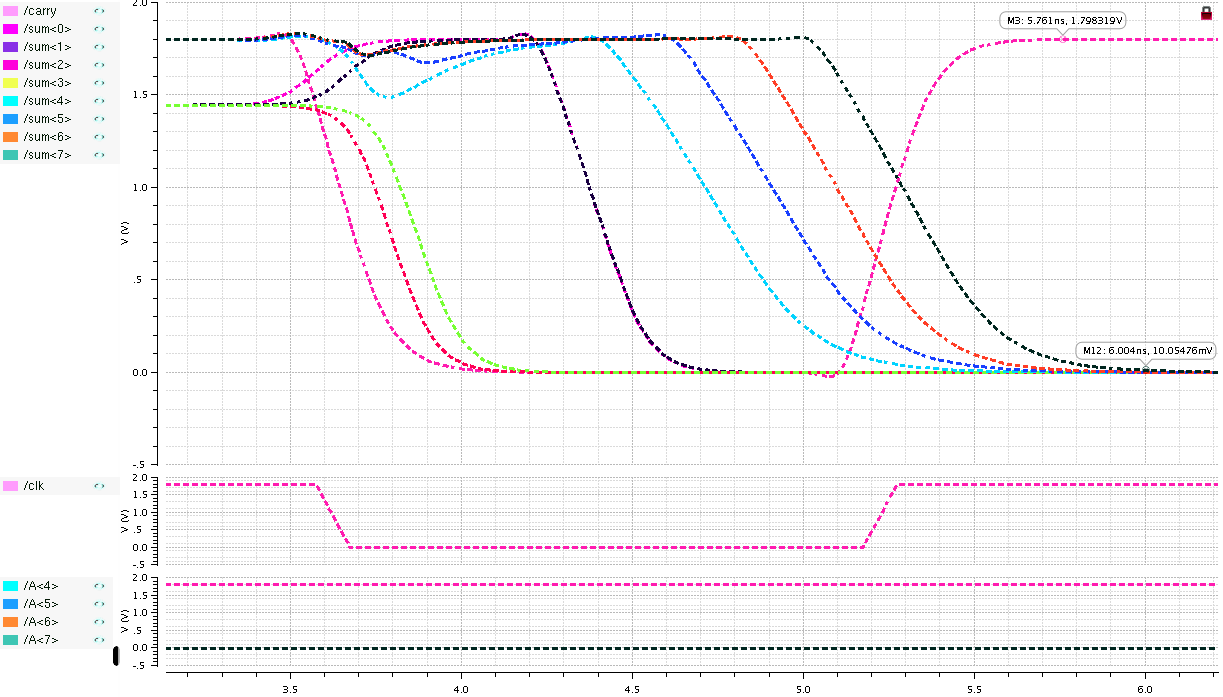


Adder with input combination 0111 1110 + 1110 0111 + 0

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | *t* = 0 | CLK Pulse (setup) | 99% Output | Best Possible CLK Period | Maximum Frequency |
| Time | 3 ns | 3269 ps | 5521 ps | 5521 – 3000 = 2521 ps | 396.7 MHz |

|  |  |  |
| --- | --- | --- |
| VDD | I (avg) | PWR (avg) |
| 1.8 V | -1.1 mA | 1.98 mW |

Timing and power characteristics for this input vector



Adder with input combination 1111 1111 + 0000 0000 + 1

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | *t* = 0 | CLK Pulse (setup) | 99% Output | Best Possible CLK Period | Maximum Frequency |
| Time | 3 ns | 3575 ps | 6004 ps | 6004 – 3000 = 3004 ps | 332.9 MHz |

|  |  |  |
| --- | --- | --- |
| VDD | I (avg) | PWR (avg) |
| 1.8 V | -1.65 mA | 2.97 mW |

Timing and power characteristics for this input vector