**Lab 12: The Traffic Light Controller Lab**

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ECEN 248 – 302

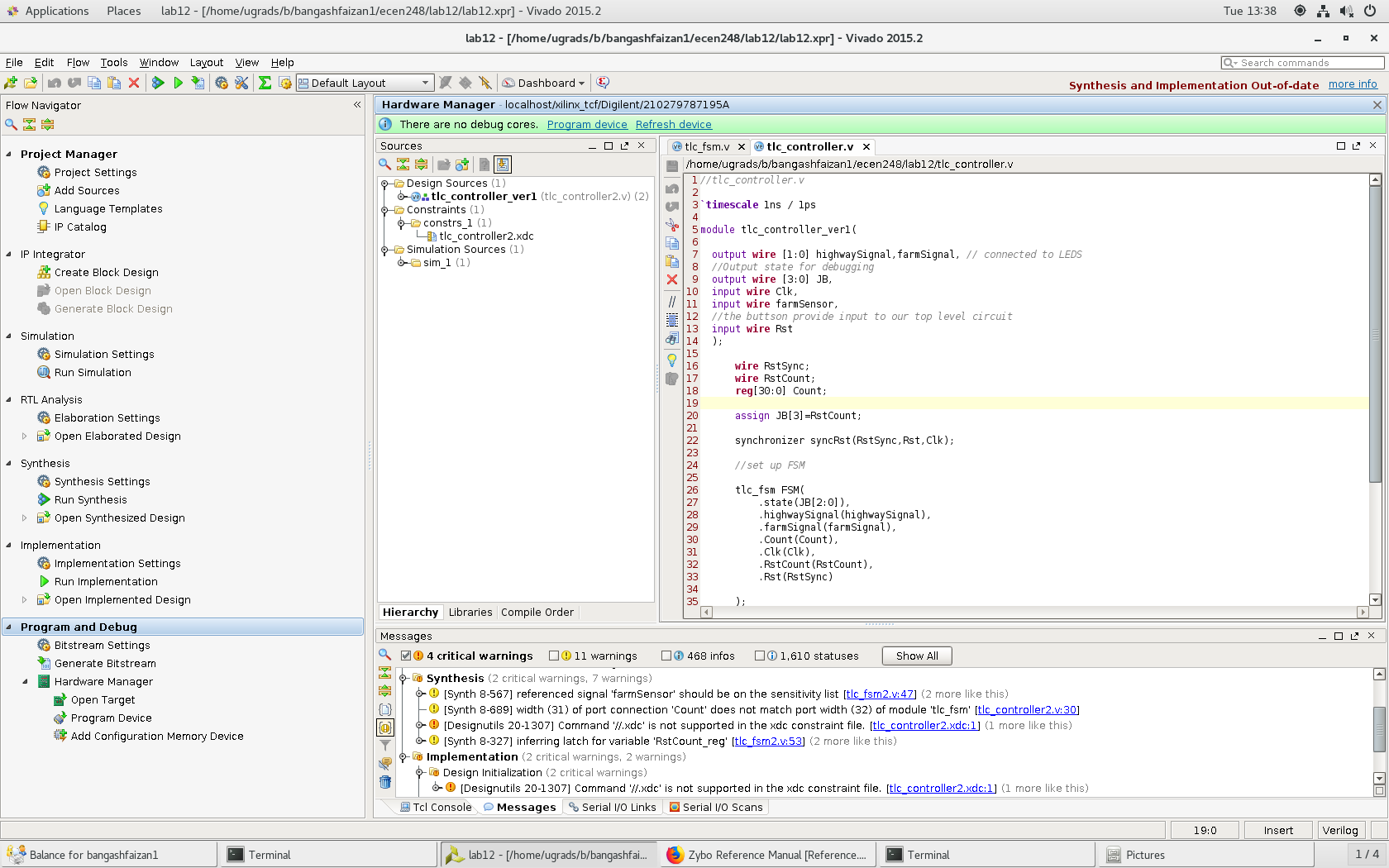
August 3rd, 2018.

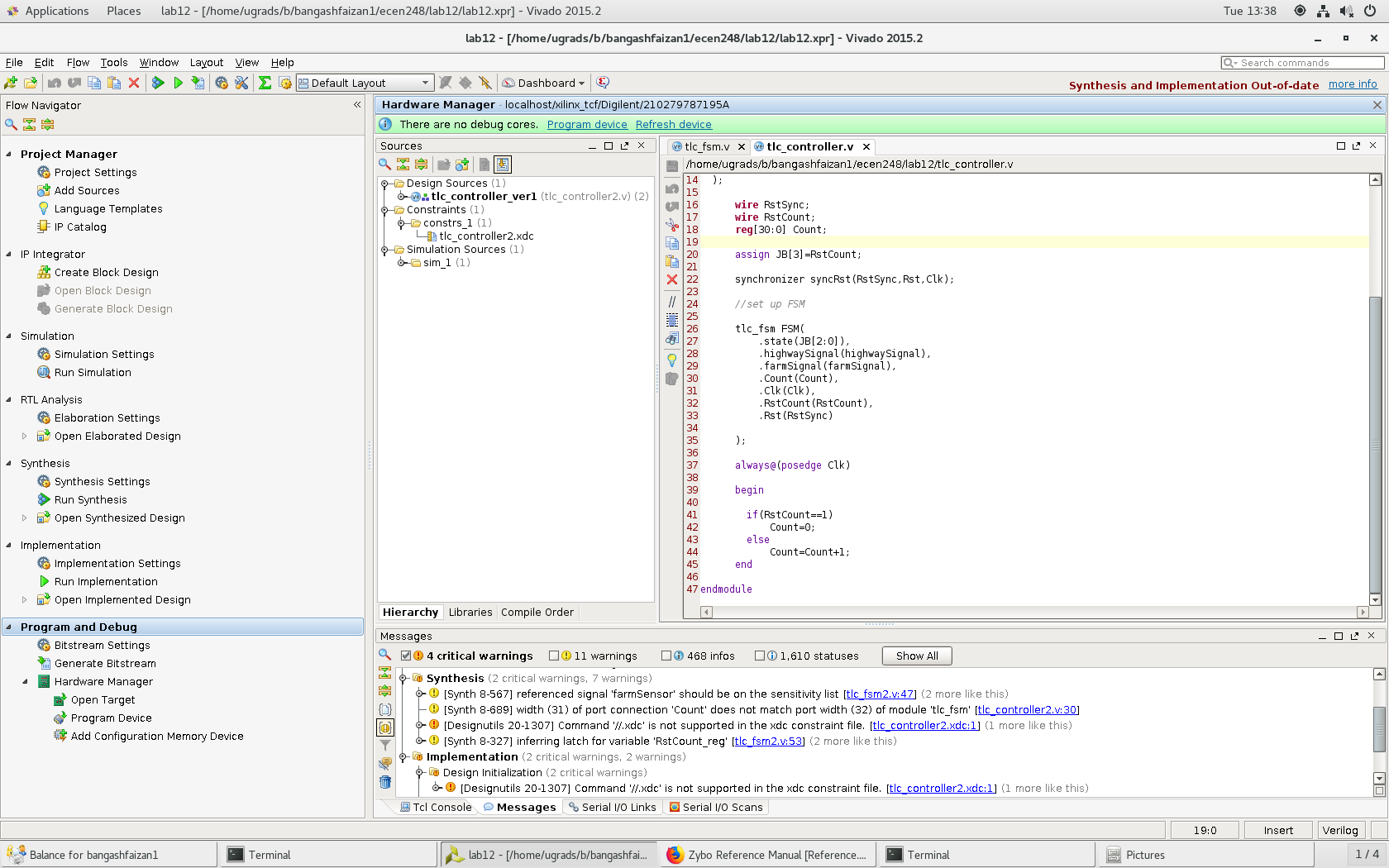
**Objectives –**

In this lab, we will design a FSM over a real world scenario as well as implementing it into verilog code. Using a circuit that is able to retain memory, we constructed a rudimentary traffic light system which we later modified by adding a sensor for a more realistic application. This lab brushed up on multiple verilog skills as well as how to implement a project on a ZYBO board.

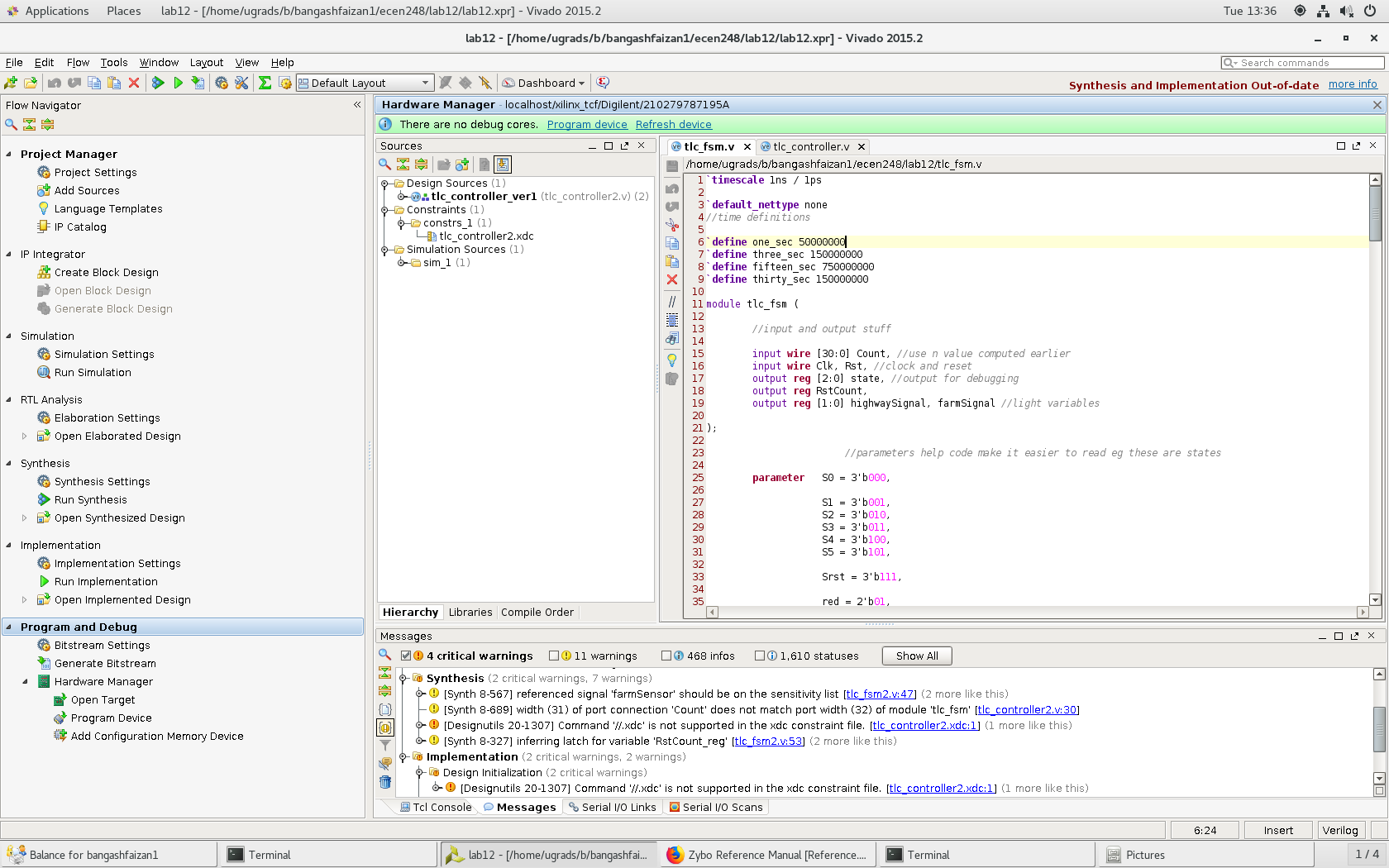
**Design** –

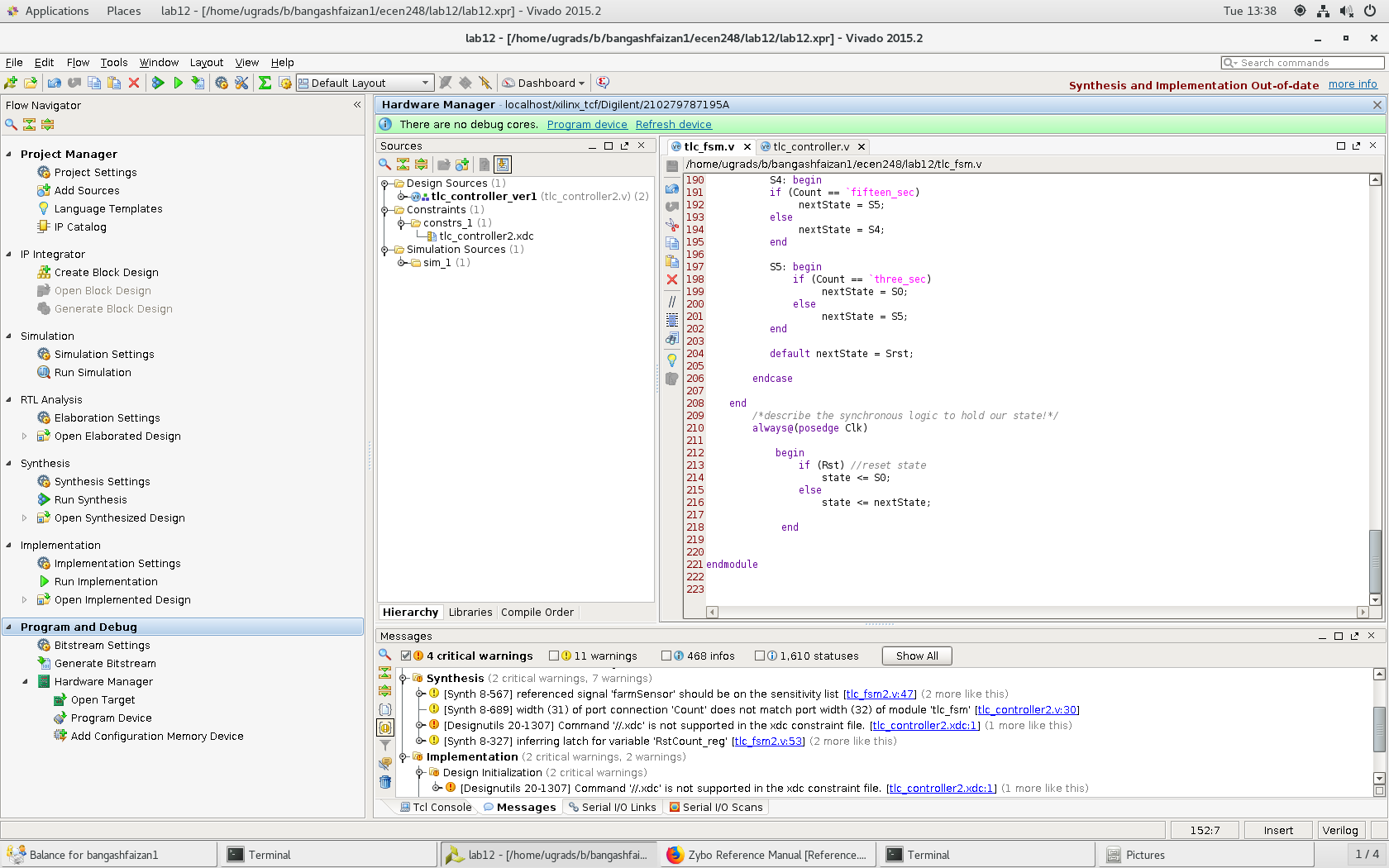
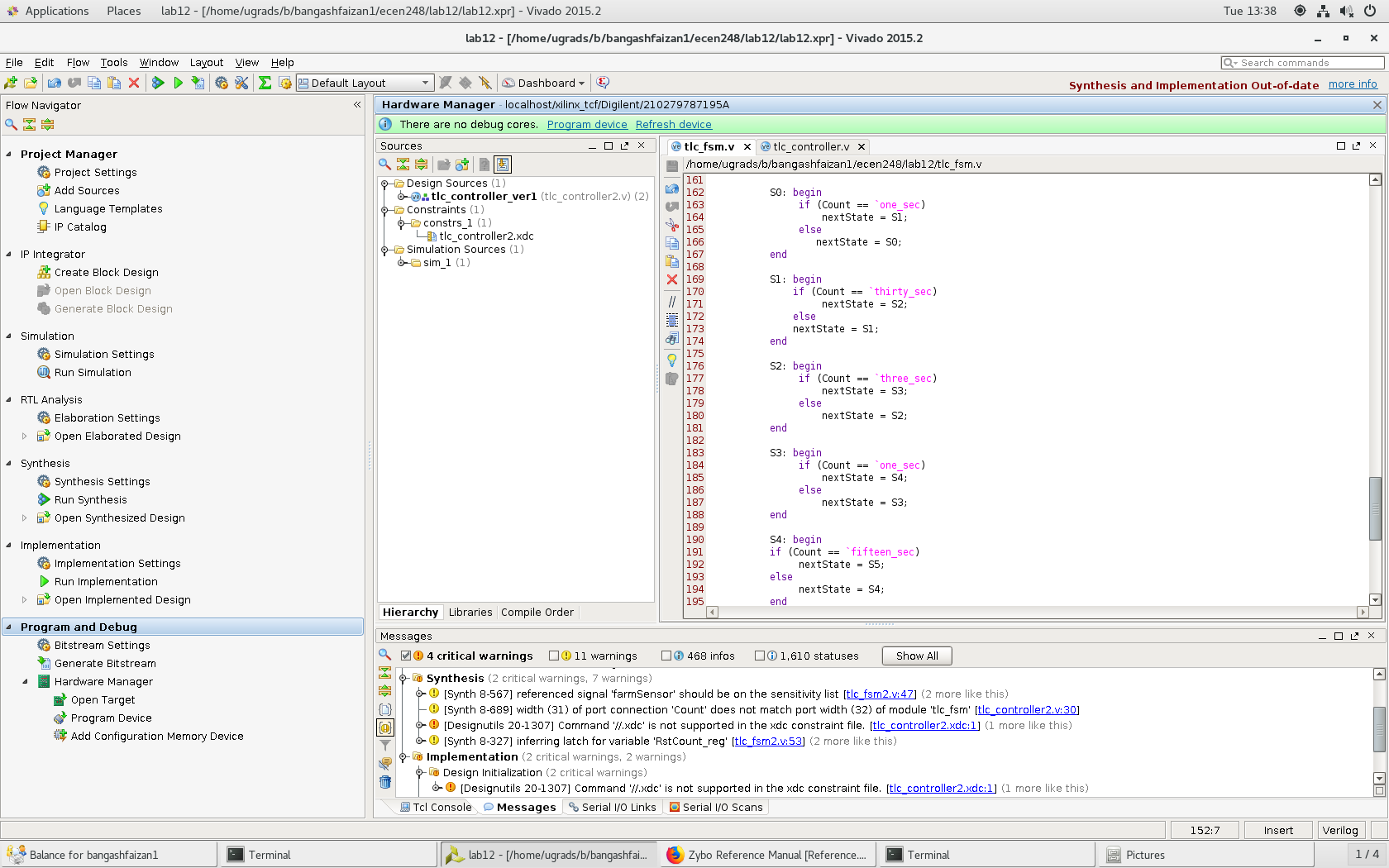
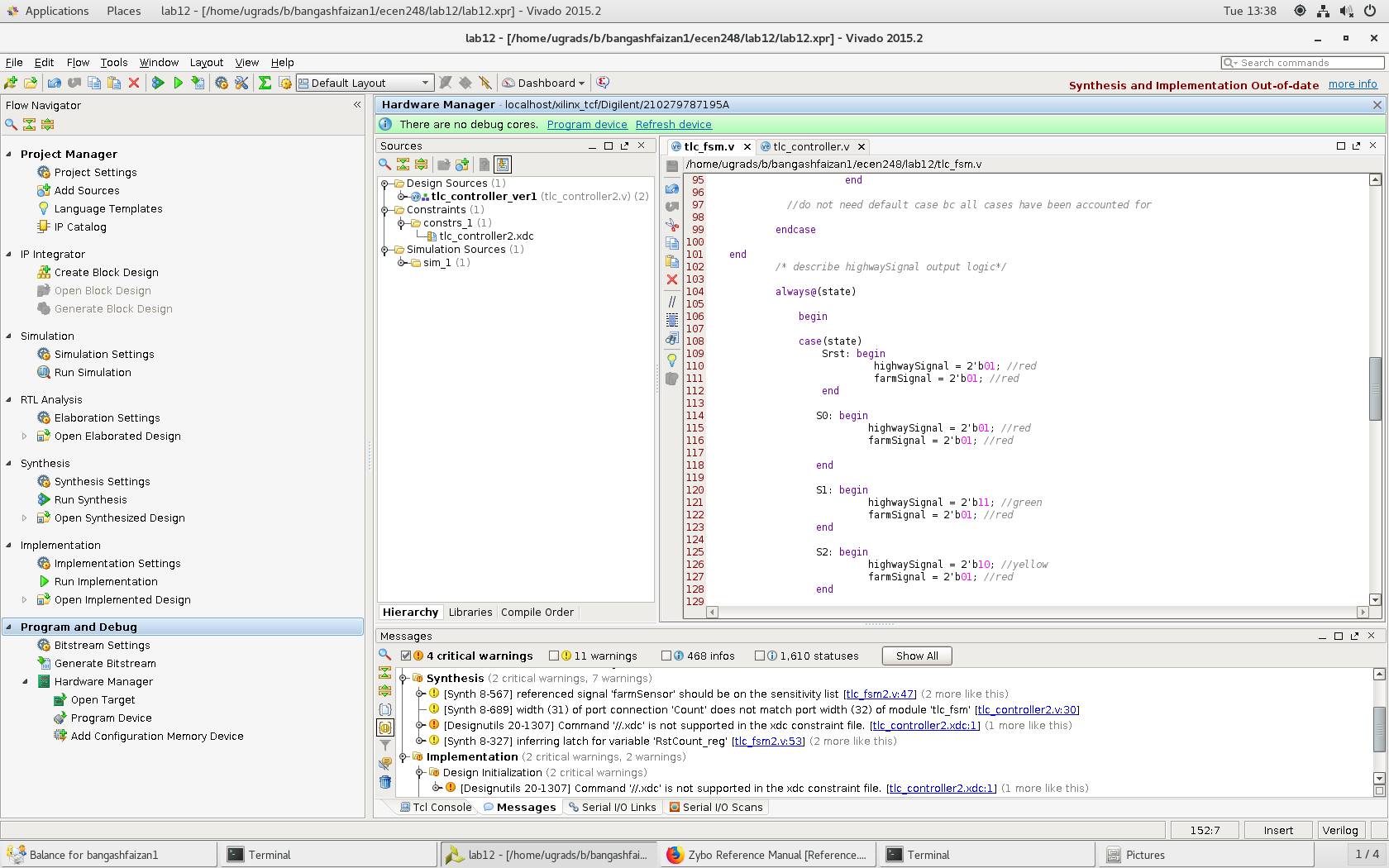
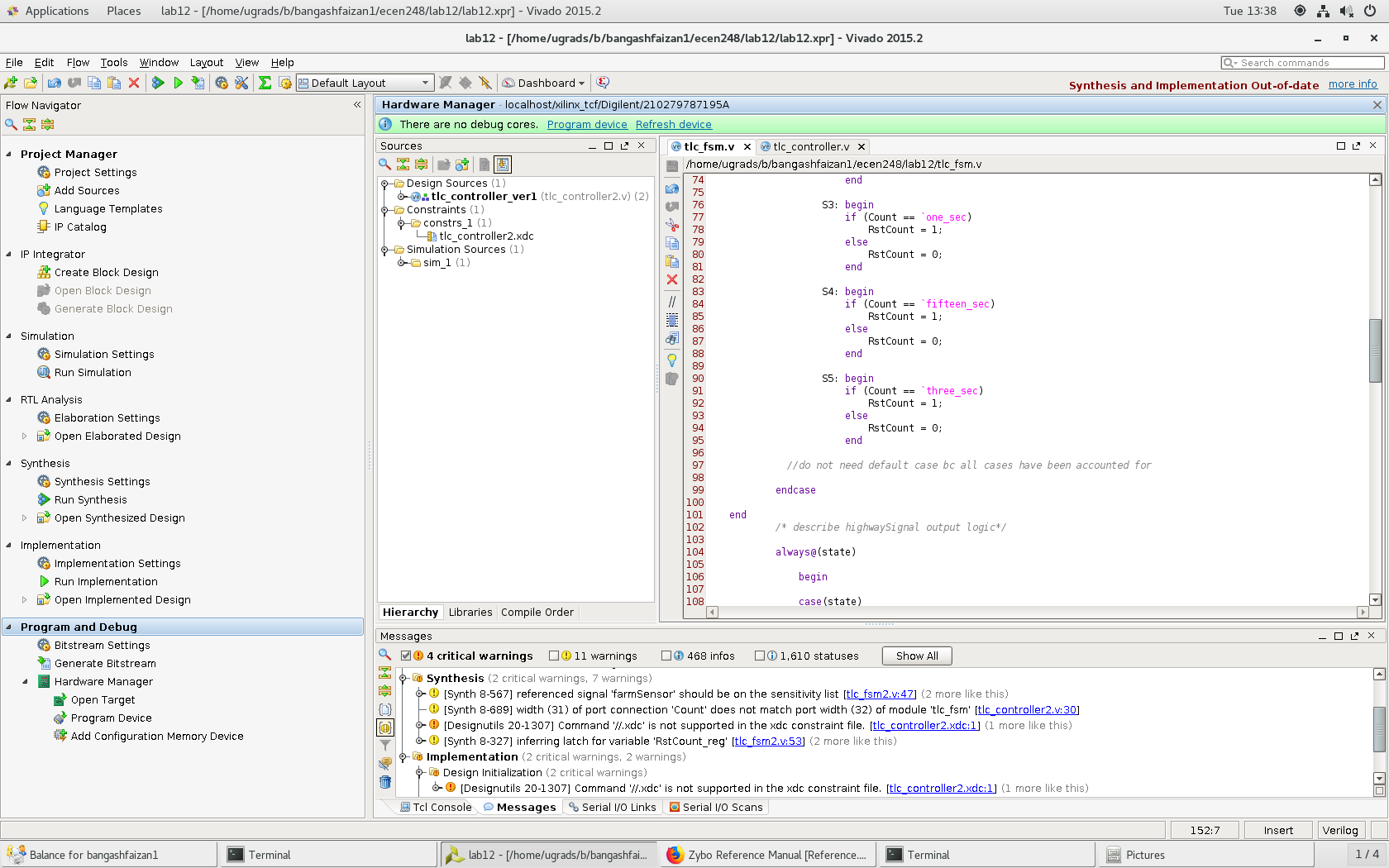
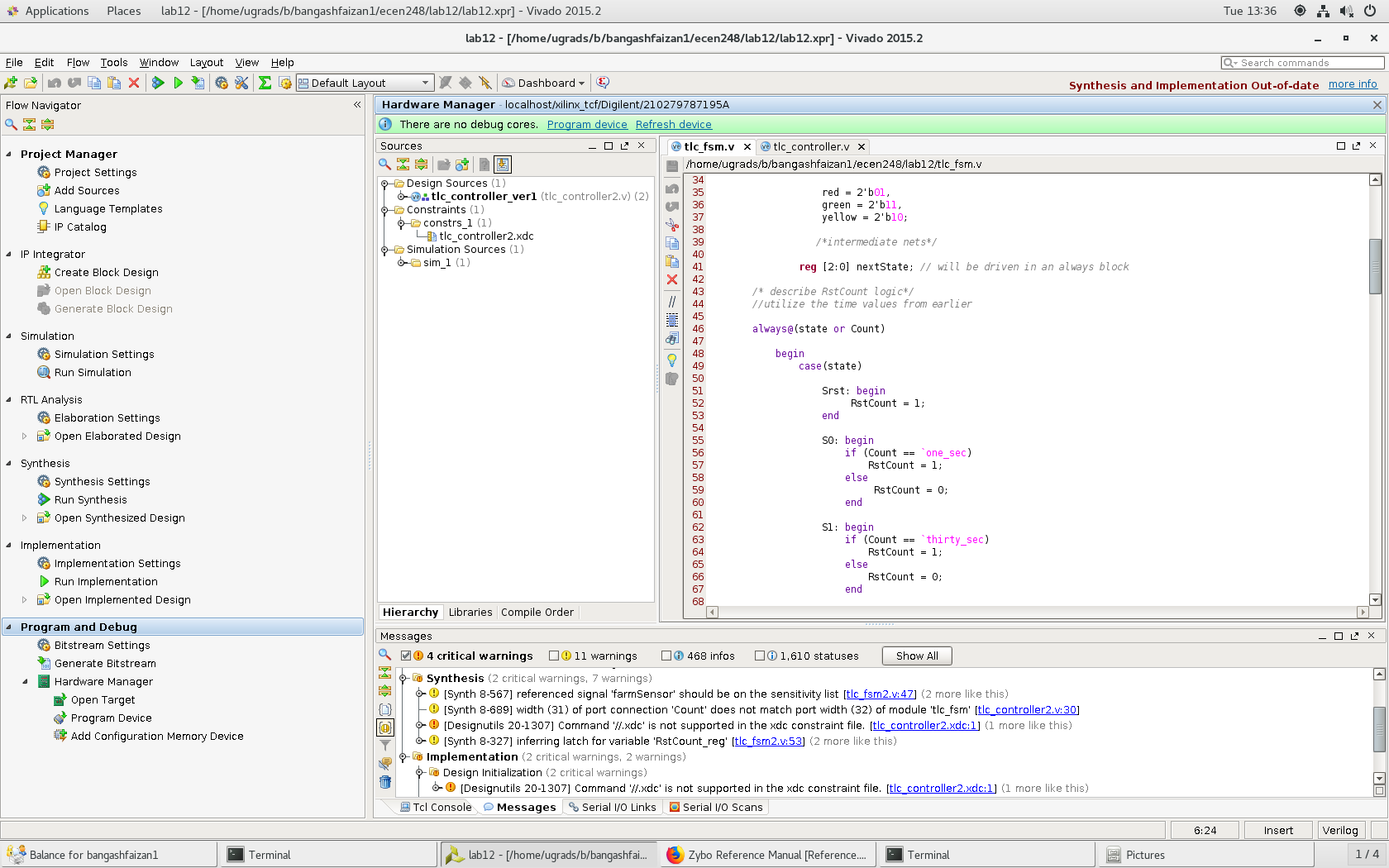
In the first part of the lab, we tested the pre-lab code to ensure that it works. We did this by implementing it onto the ZYBO board as well as making the tlc\_controller.v file that will set up and run the simulation. Seen below is the code for the 1st experiment.





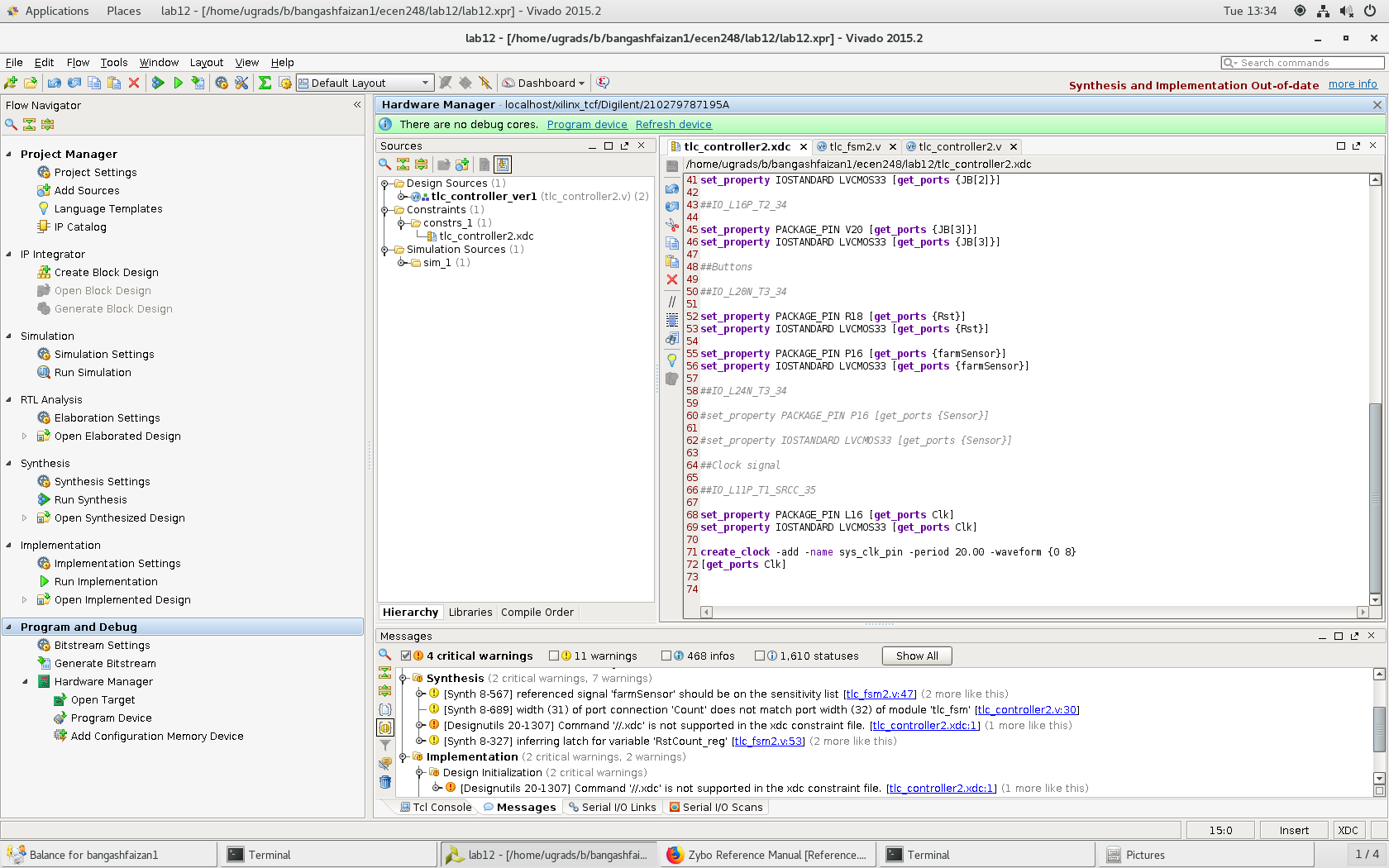
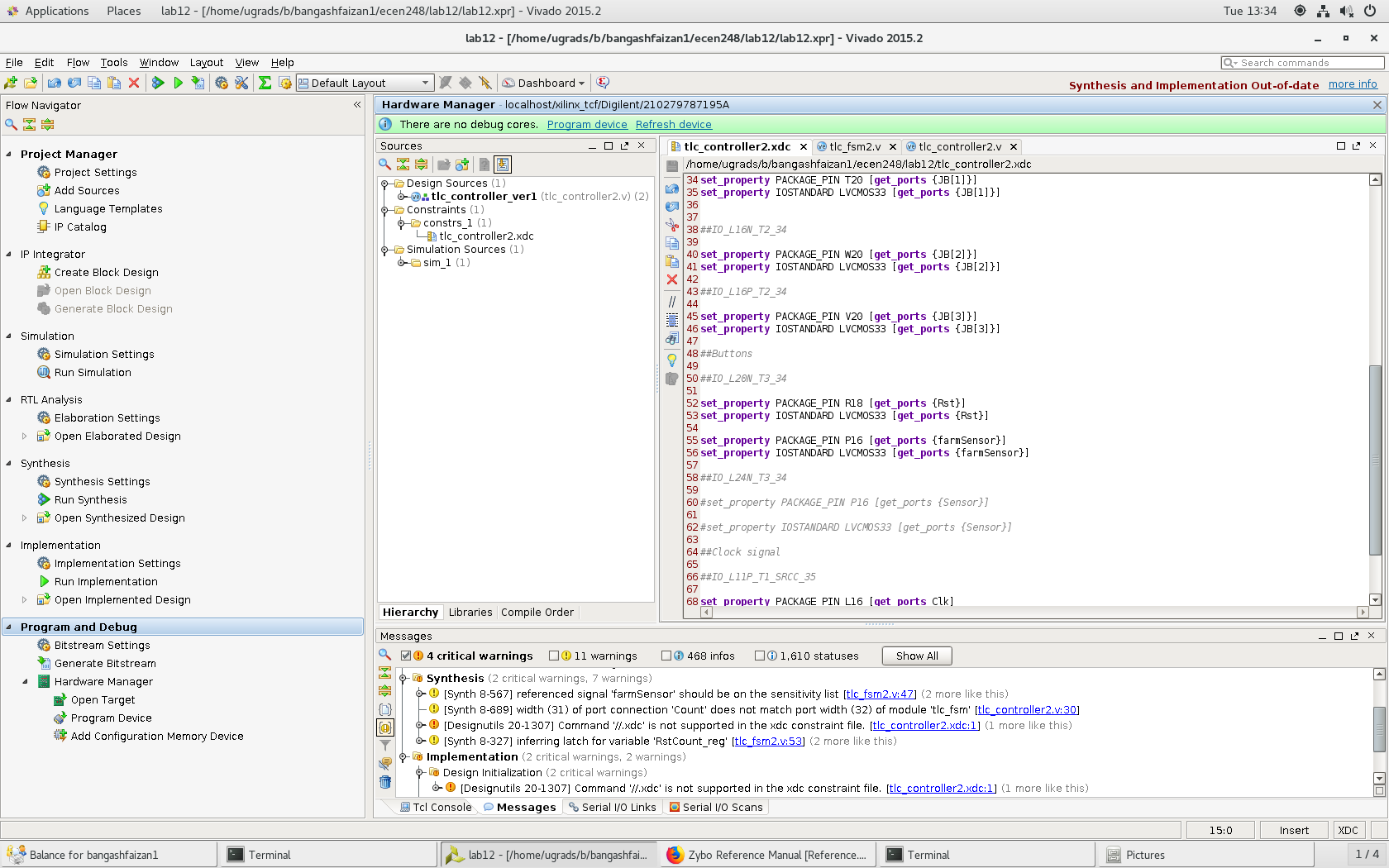
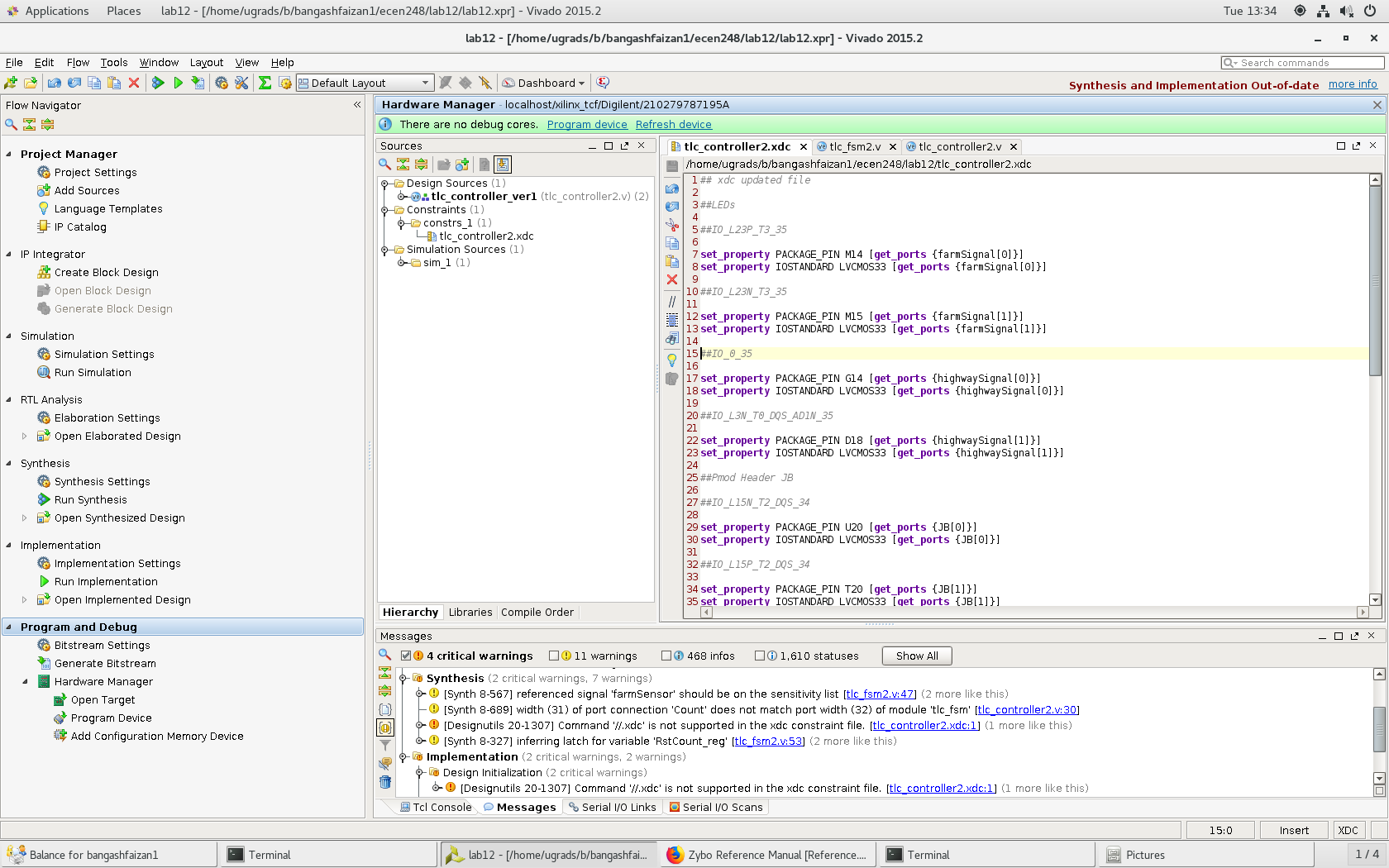
//tlc\_controller



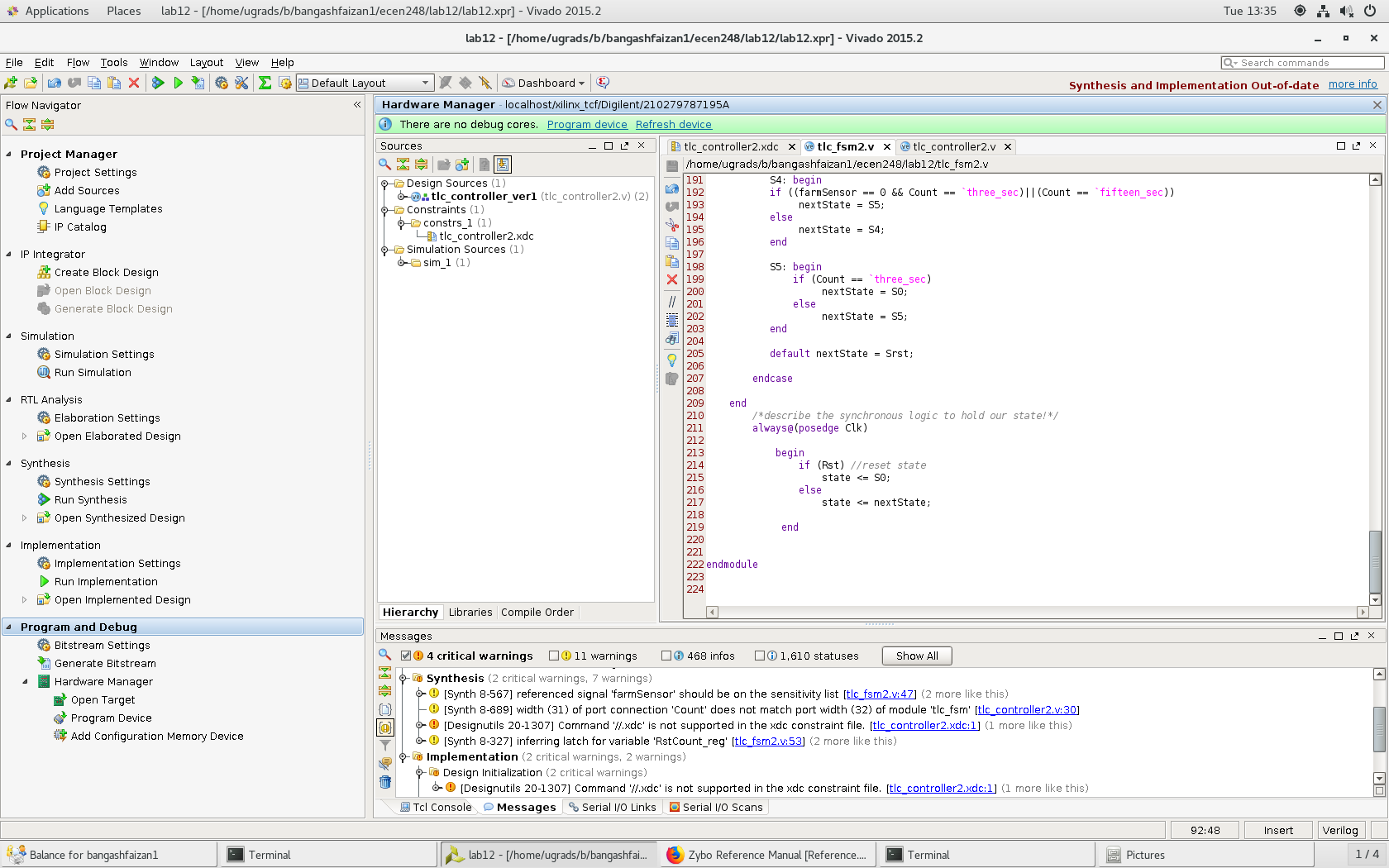
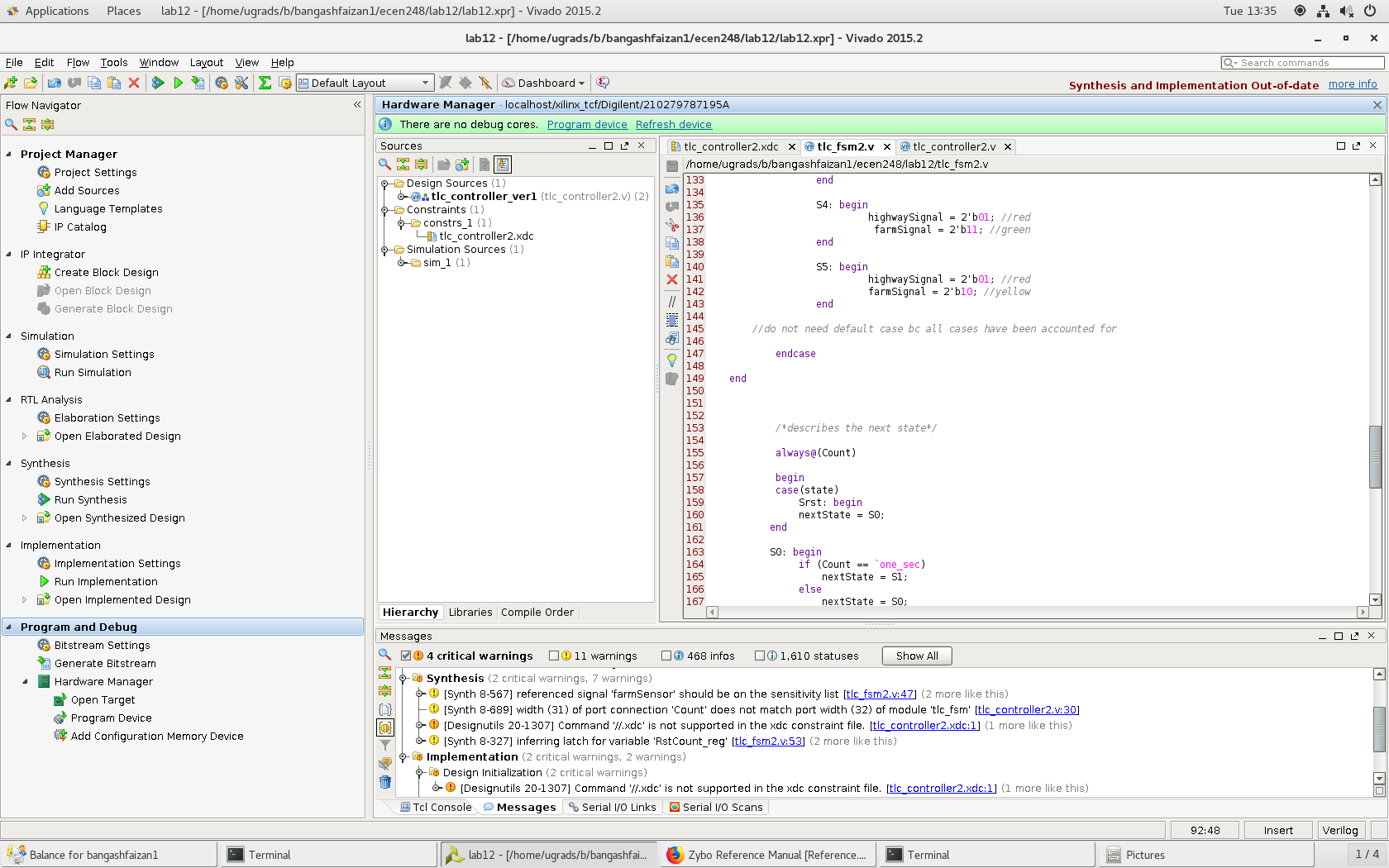
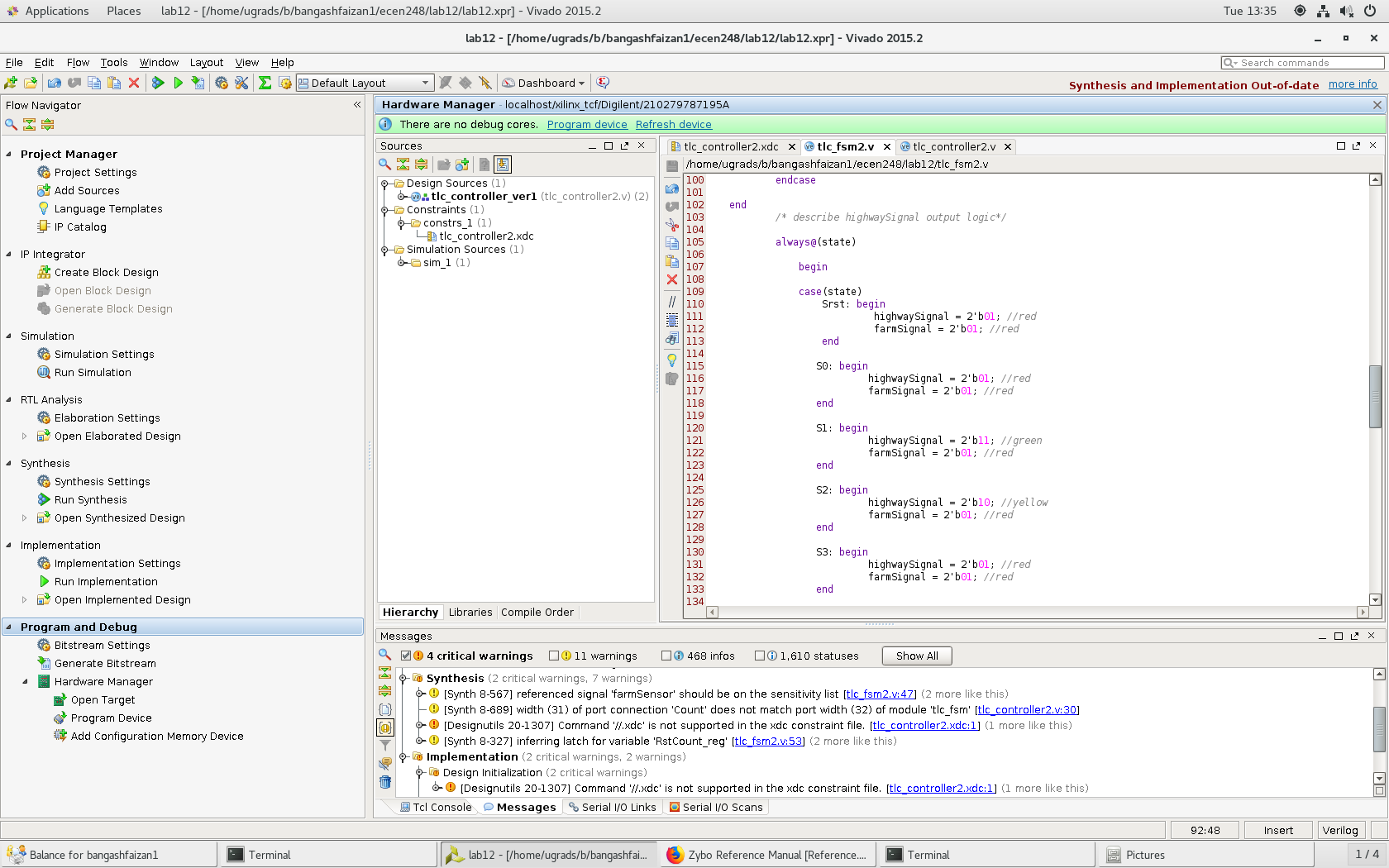
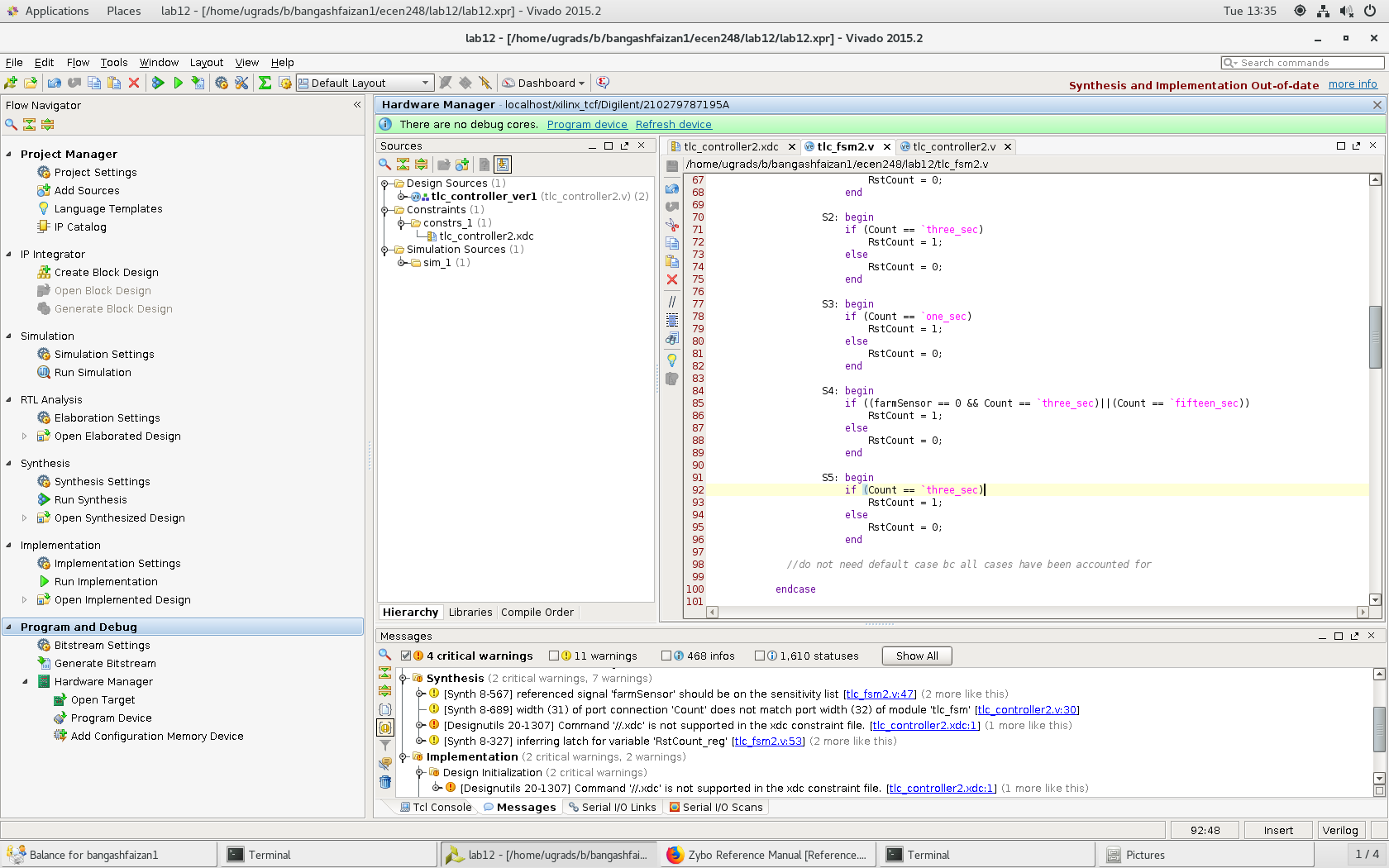
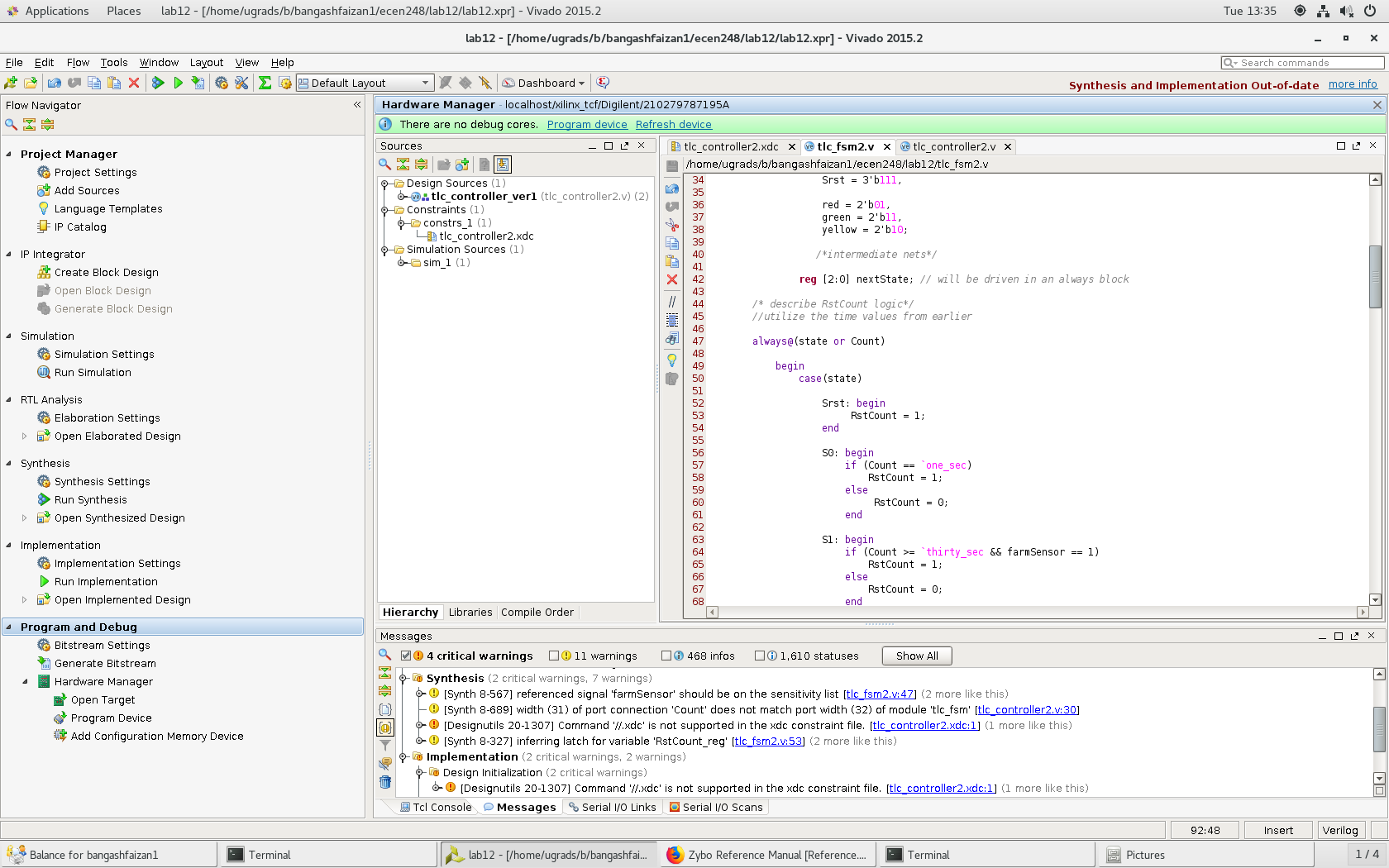
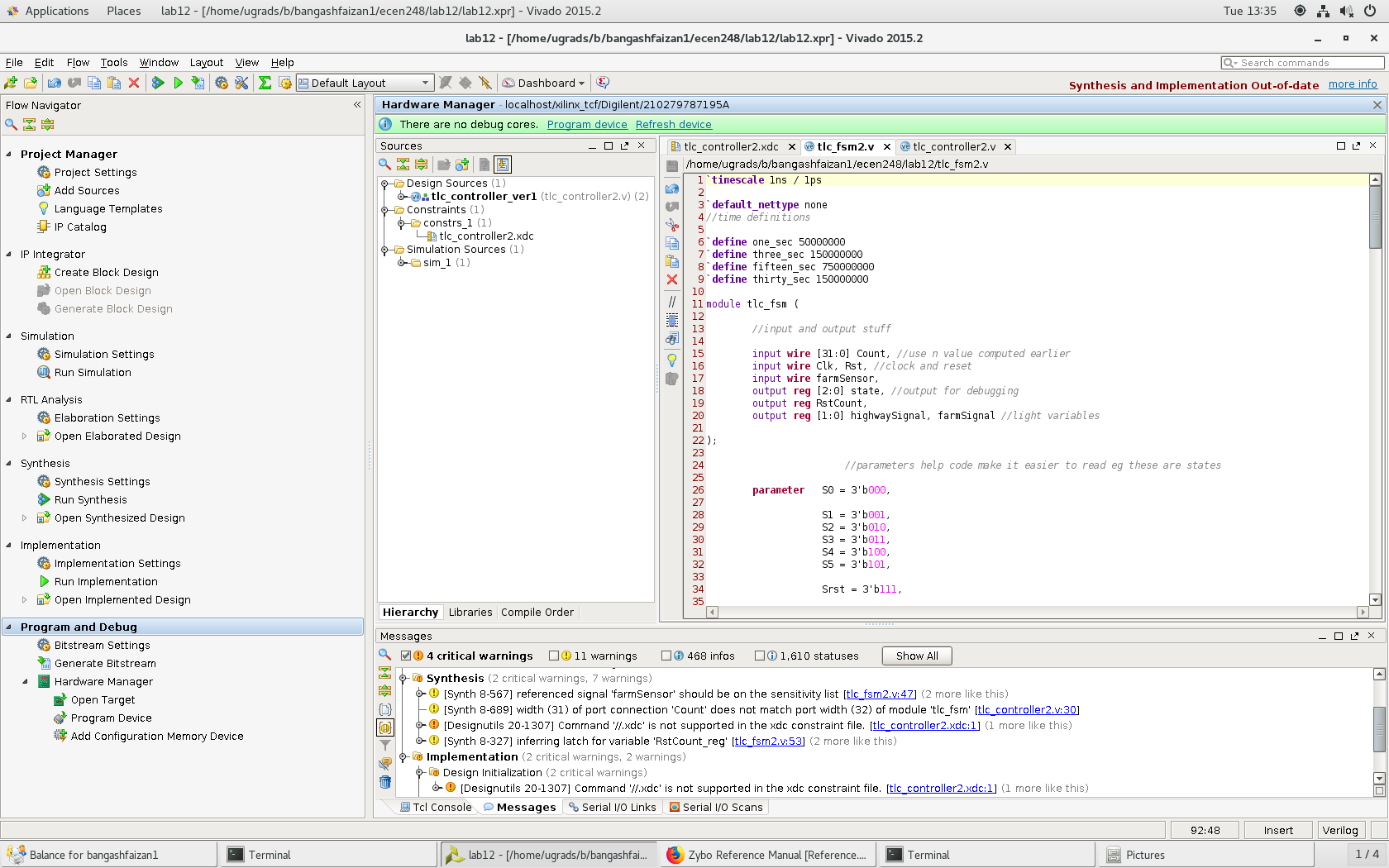


//tlc\_fsm.v

Following the code testing and debugging in experiment 1, we implement the farm sensor and it’s logic for experiment 2. We also had to change the .xdc file to allow for the farm sensor button. The code for the .xdc file can be seen below followed by the updated tlc\_fsm.v file.



//.xdc updated file



//updated tlc\_fsm.v file

**Results –**

Overall, the lab went very smoothly. I was able to follow the FSM and get the code in just a few tries. The only issue I had was implementing the farm sensor logic. I was failing to do the new logic in a few spots which was causing my code to get stuck on a green light. However, after adding the new logic checks to move on to the next state, the program worked perfectly.

**Conclusion –**

The circuit that was implemented followed the state diagram that was given. Using the “count” and “farmSensor” the circuit is able to hold memory and show various lighting conditions for a traffic light. This lab gave me a better understanding of sequential circuits in verilog as well as how memory works in a circuit.

**Questions:**

1. Include the source code with comments for all modules that you wrote or modified in lab. You do not need to include code that was provided! Remember that code without comments will not be accepted!
   1. The code is included in the design section of the lab report.
2. Include the state diagram for the modified traffic light controller FSM.