**Lab 4: Rudimentary Adder Circuits**

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**Objectives –**

In this lab, I worked with half adder, the full adder to create the 2 bit ripple adder. This lab is intended to teach me the basics of how digital numerical computations are physically created and how it can be used to demonstrate optimization and logic simplification.

**Design –**

Here are the designs from the pre-lab that I used for the various adders.

For the half adder in this lab, there were two outputs, a carry and a sum. Additionally, there were two inputs, A and B.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Input | | | Output | |
| Type: | X | Y | Carry (c) | Sum (s) |
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 2 | 1 | 0 | 0 | 1 |
| 3 | 1 | 1 | 1 | 0 |

Truth table for the half adder

|  |  |  |
| --- | --- | --- |
| X Y | 0 | 1 |
| 0 | 0 | 0 |
| 1 | 0 | 1 |

k-map for the carry output

|  |  |  |
| --- | --- | --- |
| X  Y | 0 | 1 |
| 0 | 0 | 1 |
| 1 | 1 | 0 |

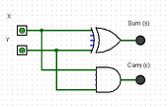
k-map for the sum output

From the k-maps, we can see that the boolean equations for each equation are the follow:

Carry=XY

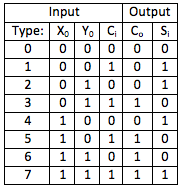
Sum=X’Y+XY’ or X xor Y

Gate levels schematic for the half adder.



Gate schematic for half adder

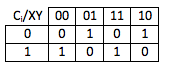
Full adder has 3 inputs- the X,Y and the Carry-in (). From here, there are two outputs again- a Carry-out () and the Sum.



Truth table for the full adder



Carry out k-map for full adder



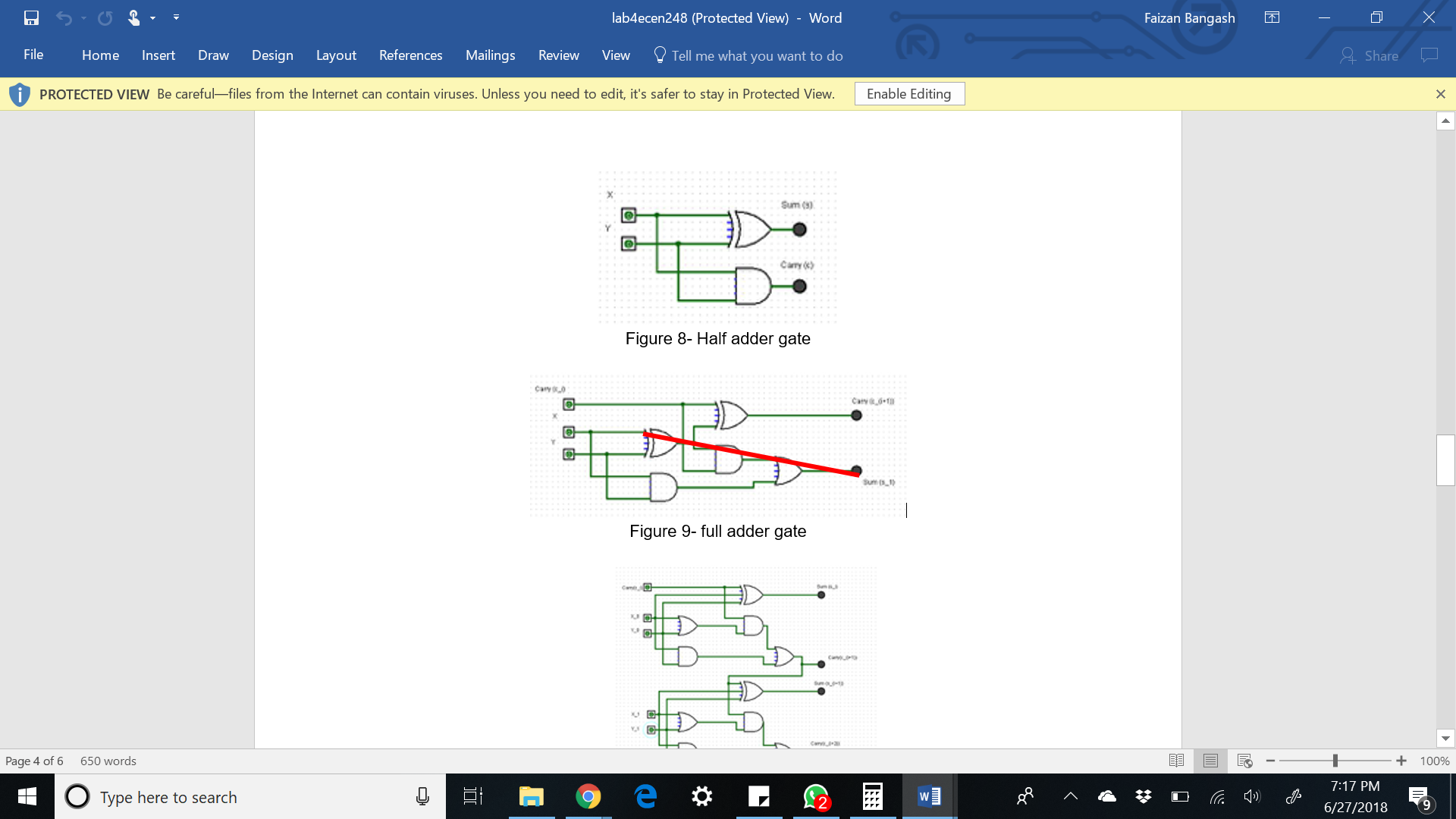
Sum k-map for full adder

Using the two k-maps derived from the truth table, we can get the final boolean equations for the full adder

Carry= XY+Y+X

Sum= X’Y’+’XY’+XY+ XY’’ or X xor Y xor

Using the boolean equation, we can get the gate level schematic

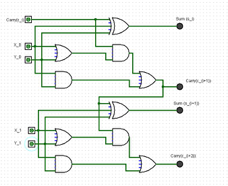


Gate schematic for full adder

For the full adder in figure 9, the maximum delay is 3 units and is highlighted in the red path. This is the worst-case scenario in the circuit. Lastly, I combined two full adders to get the 2-bit ripple carry adder.

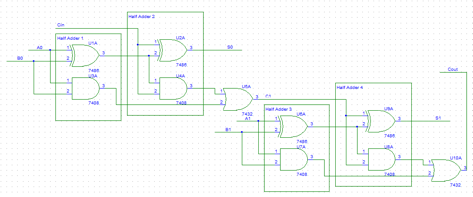
Truth table for 2-bit ripple adder

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A1 | B1 | A2 | B2 | Cin | Cout | S1 | S0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |



Gate schematic for the 2 bit ripple adder using 2 full adders

Down below is 2 bit ripple adder using half adders only:



**Results –**

My pre-lab designs were accurate therefore I completed the lab the successfully and the circuits outputted the result as expected. The circuits performed all the addition that they were all intended for. As mentioned above the worst-case propagation delay for my full adder design is 3 units.

**Conclusion –**

In this lab, I first implemented a half adder, which adds an input bit a to an input bit b, and displays the result and carry-out. Then for 2nd part, I set up a full adder, which adds the same input bits a and b with optional carry in. Then for the last part, I created a 2-bit carry ripple adder, was unbelievably technically interesting, as I had to link two full adders to obtain the results. However, setting up the 2-bit carry ripple helped me understand the difficult circuit schematics. This lab also taught me how to have more logic gates on the board at once and how to properly organize them to prevent confusion.