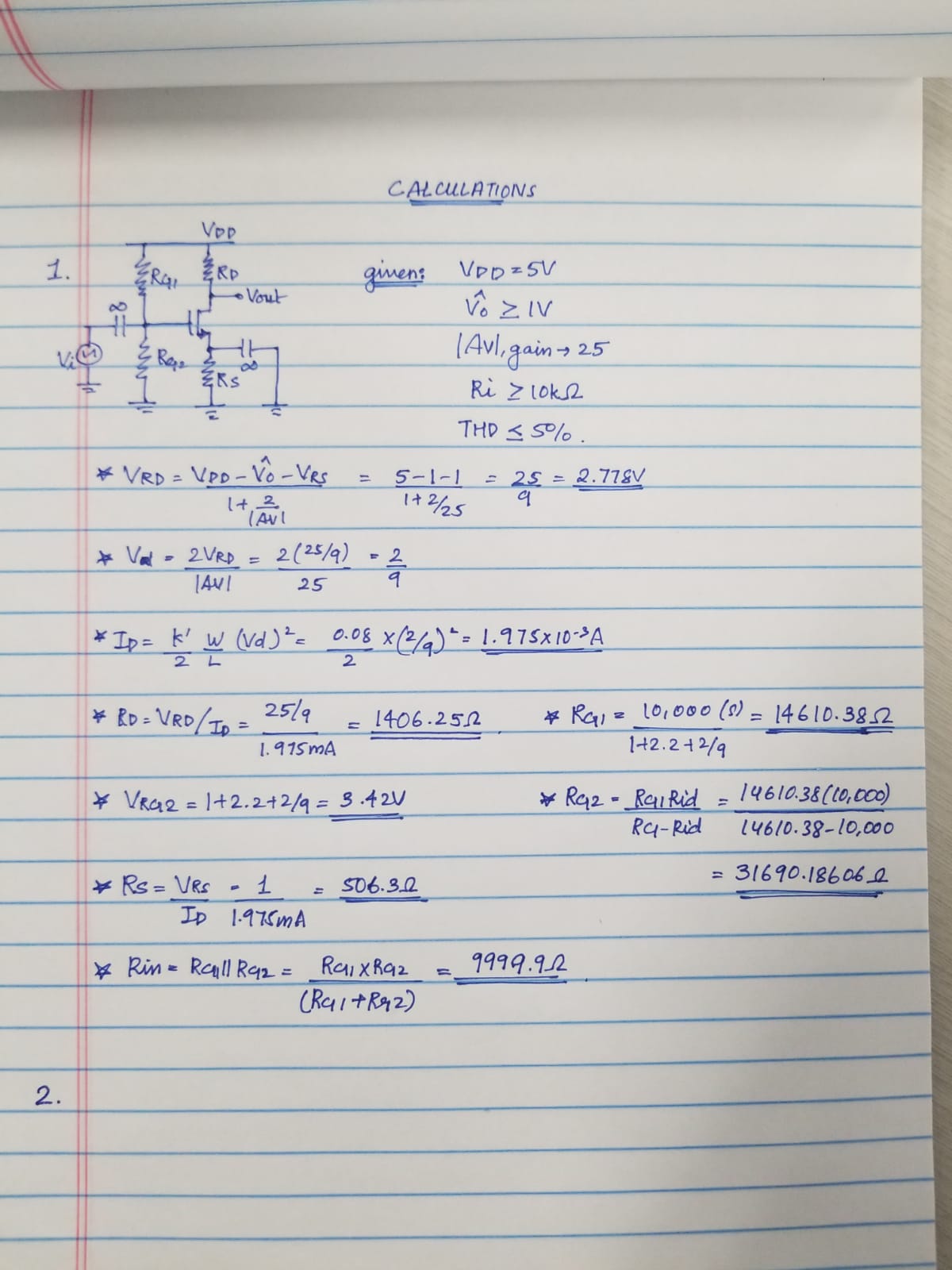
**Lab 11: MOSFET Amplifier Configurations**

**Faizan Bangash**

**Ecen 325-504**

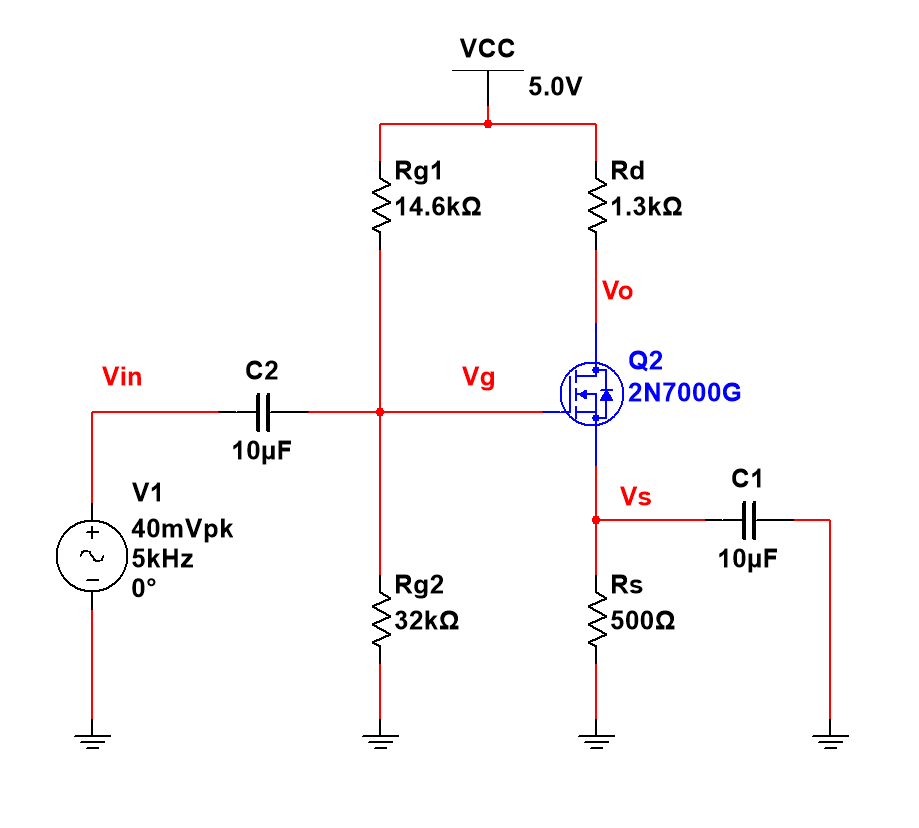
**Date: November 28, 2018**

**Calculations**

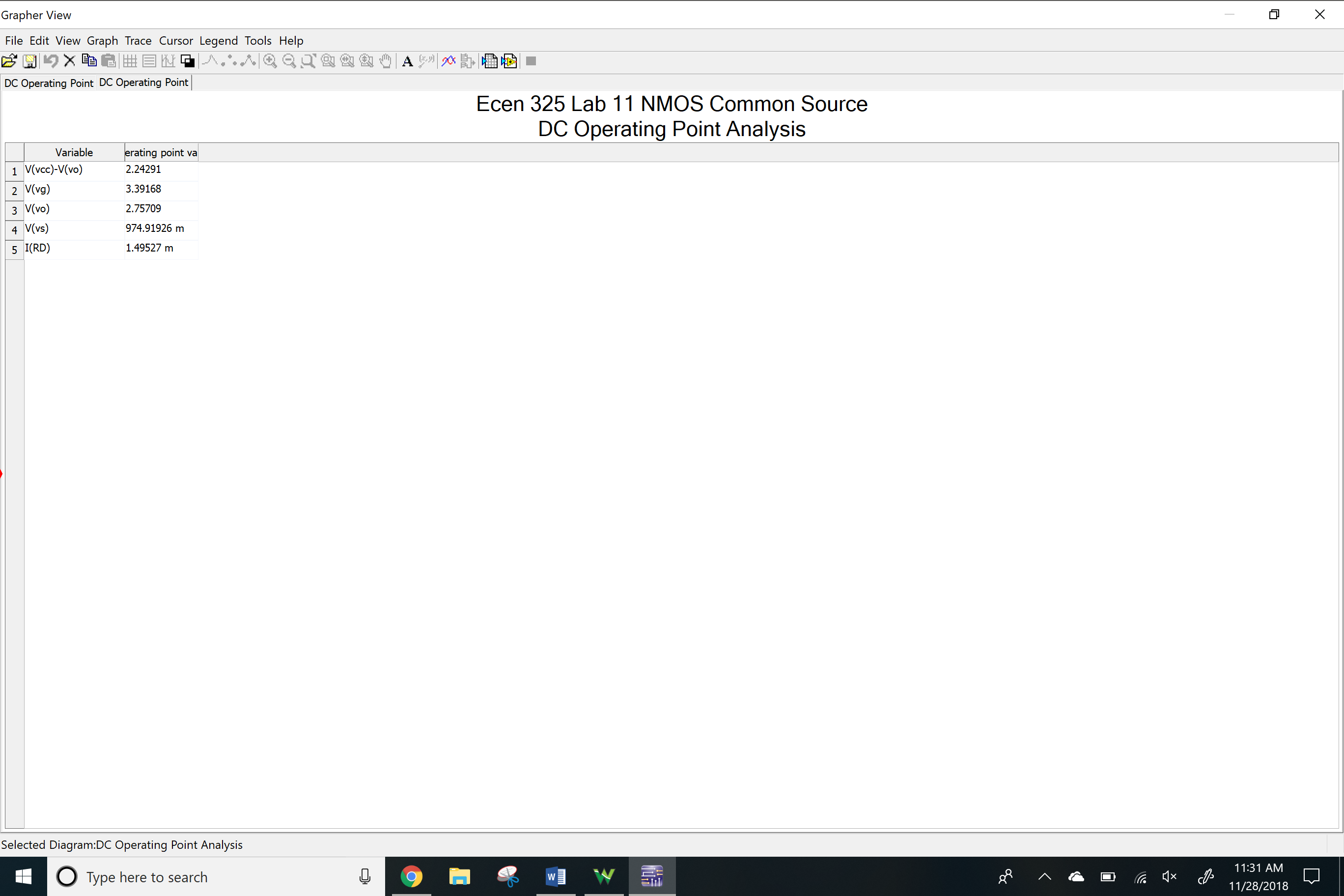
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**Simulations**

NMOS Common Source

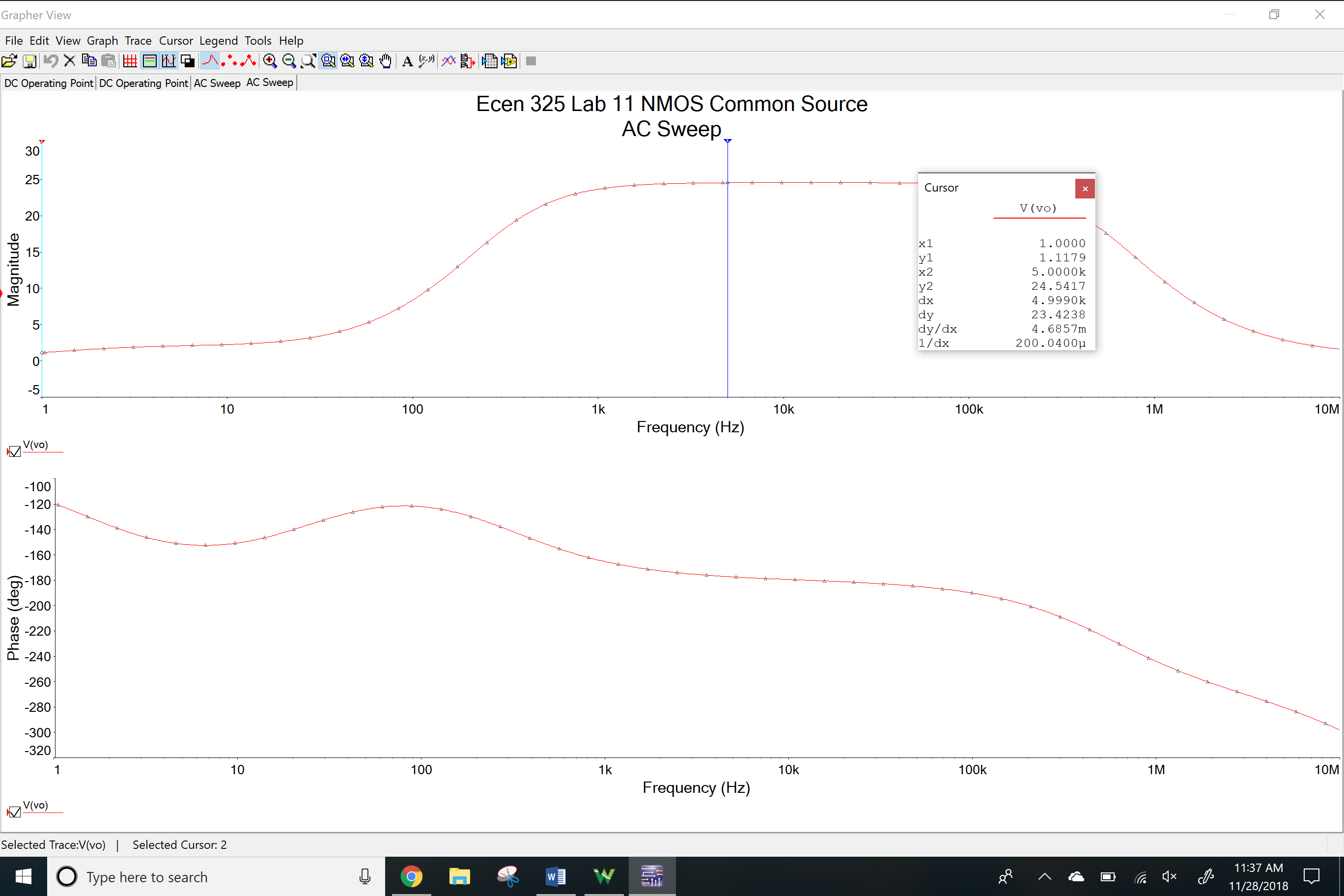


DC Operating Point

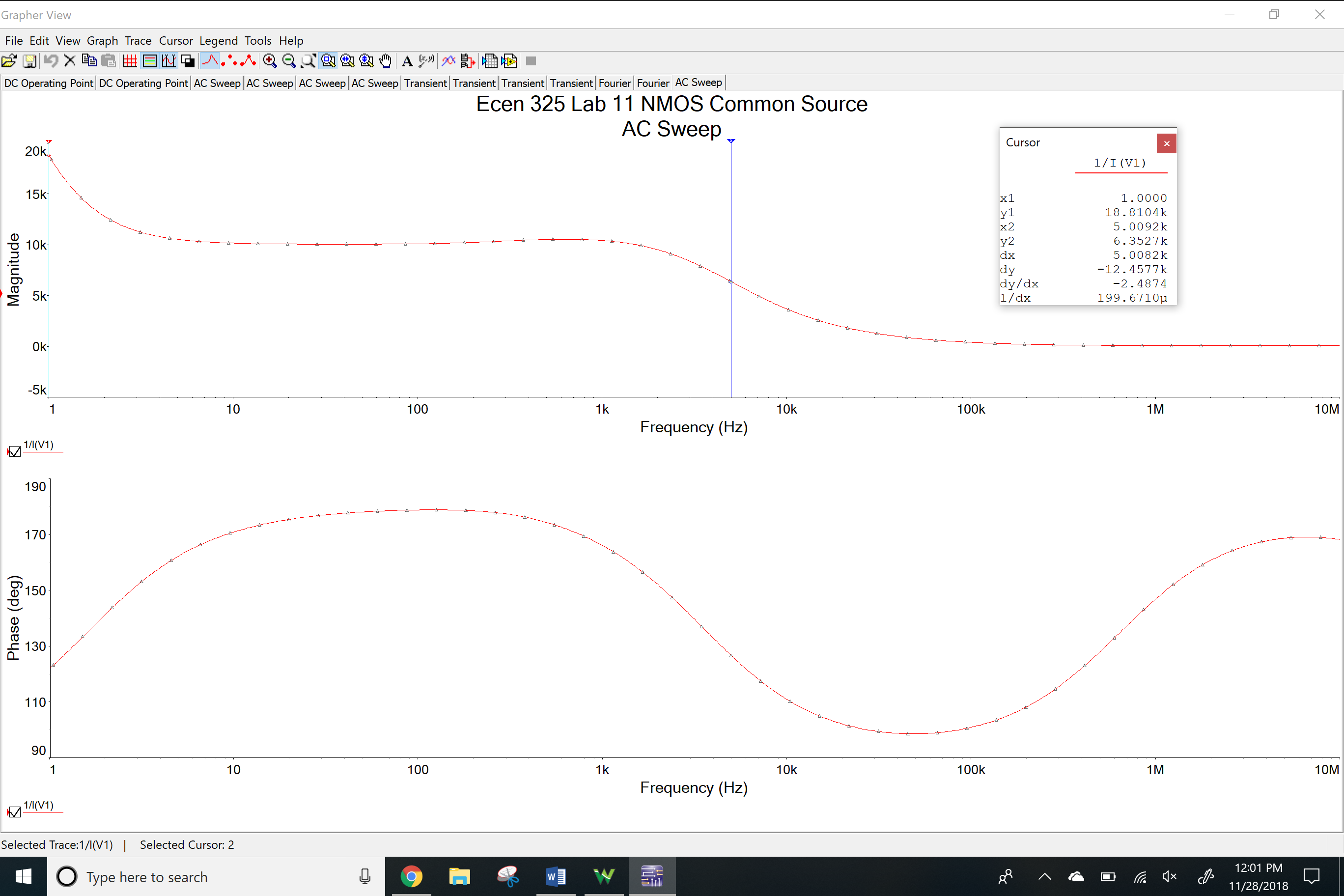


AC Simulation

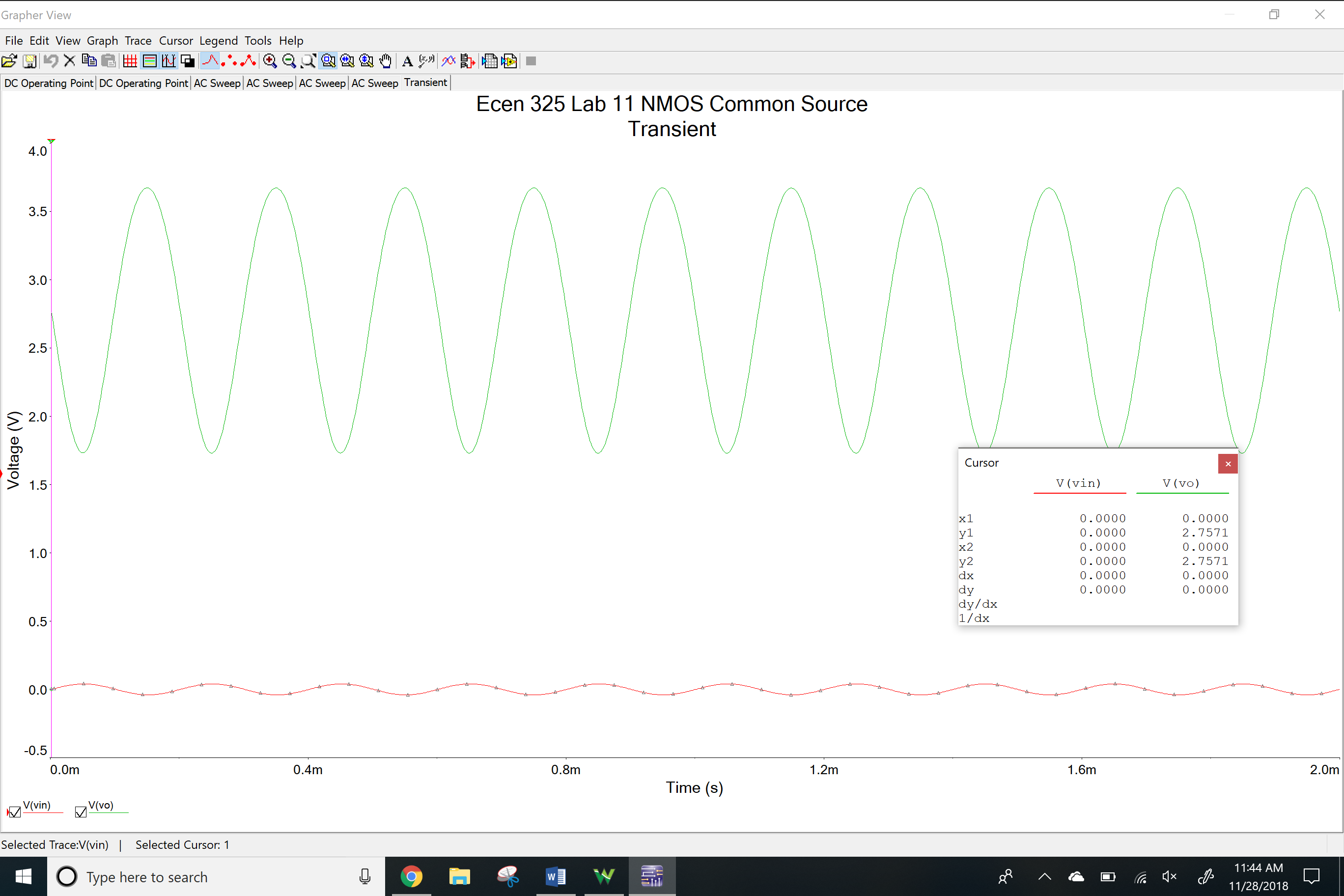
Av



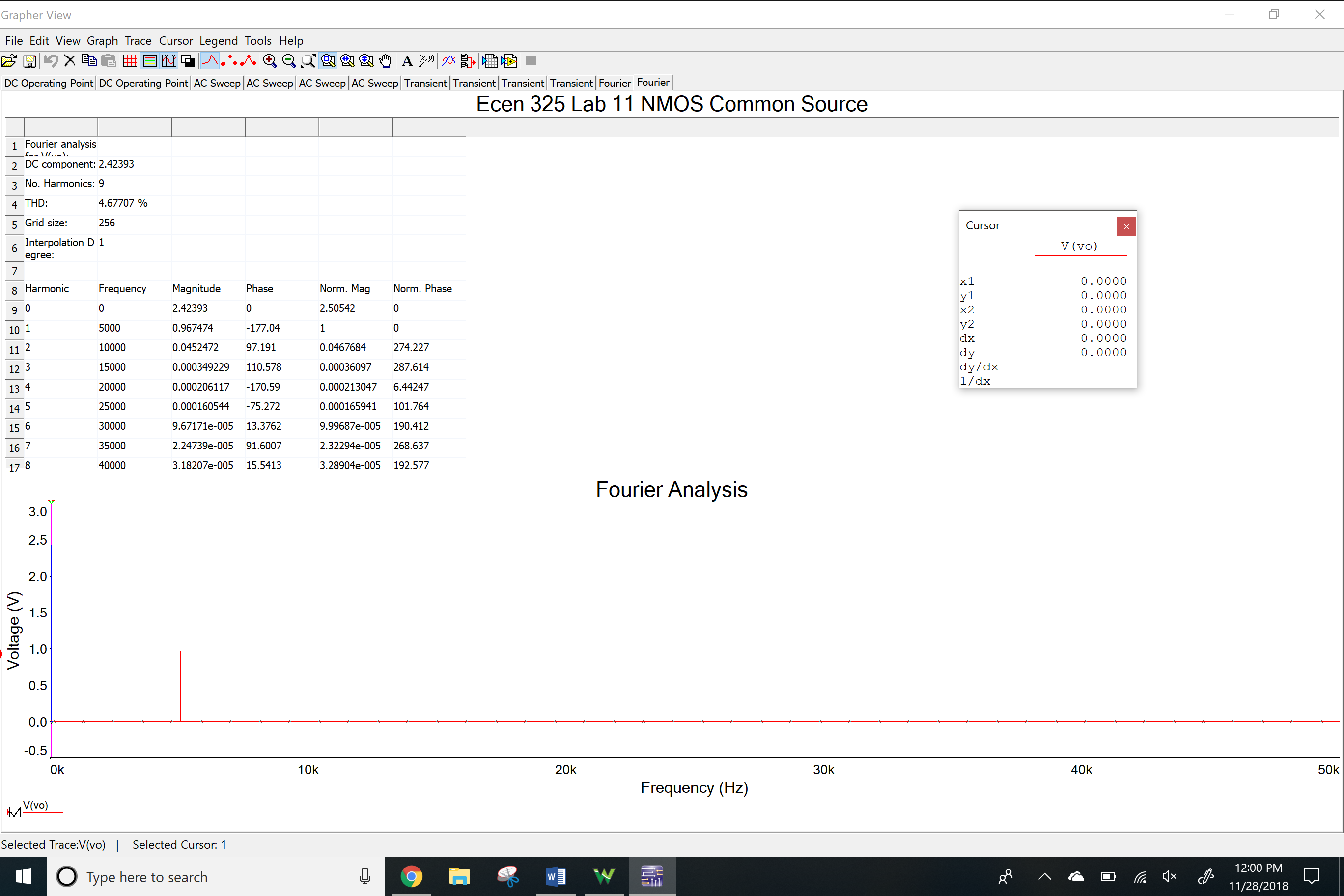
Ri



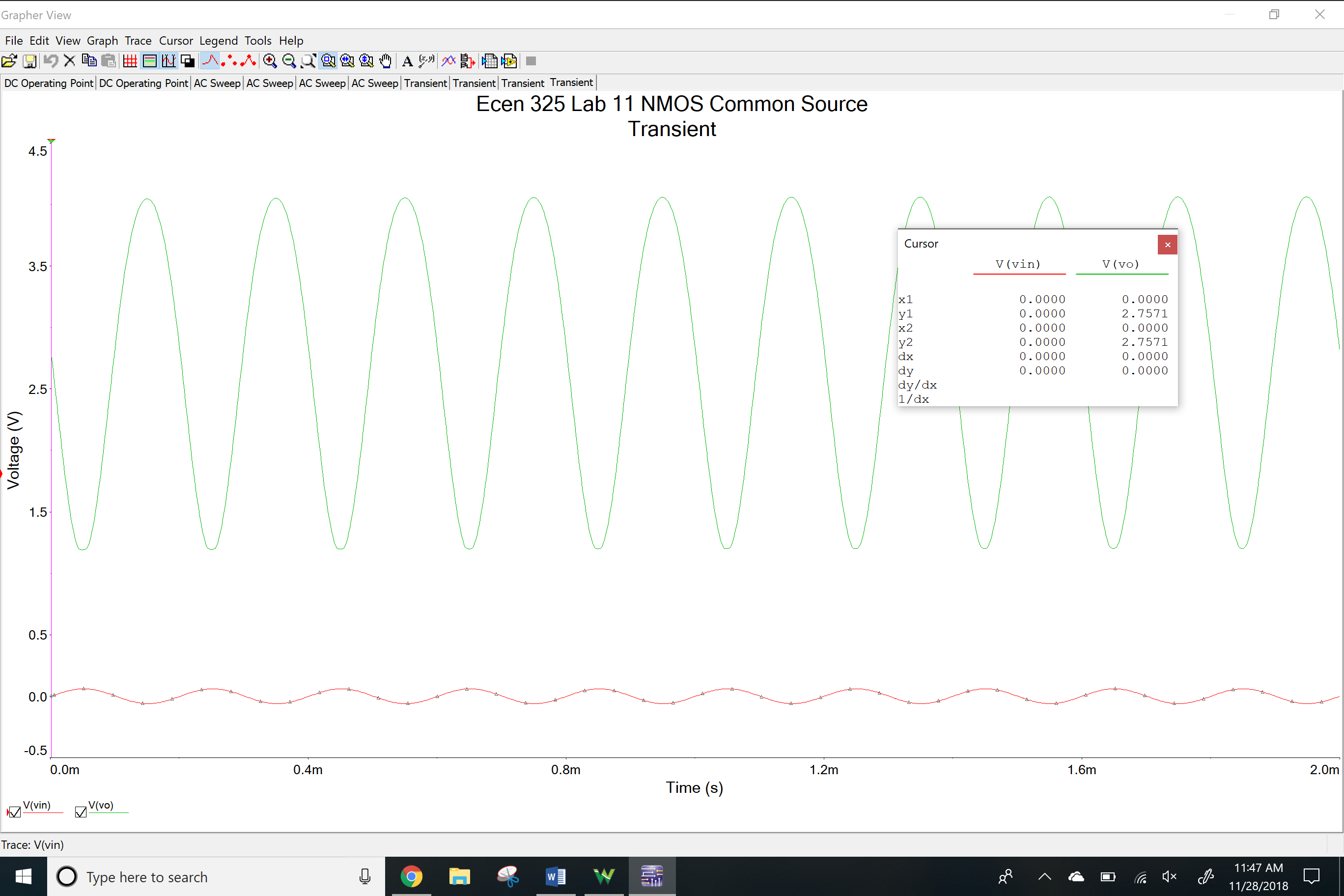
Time-domain waveform



THD



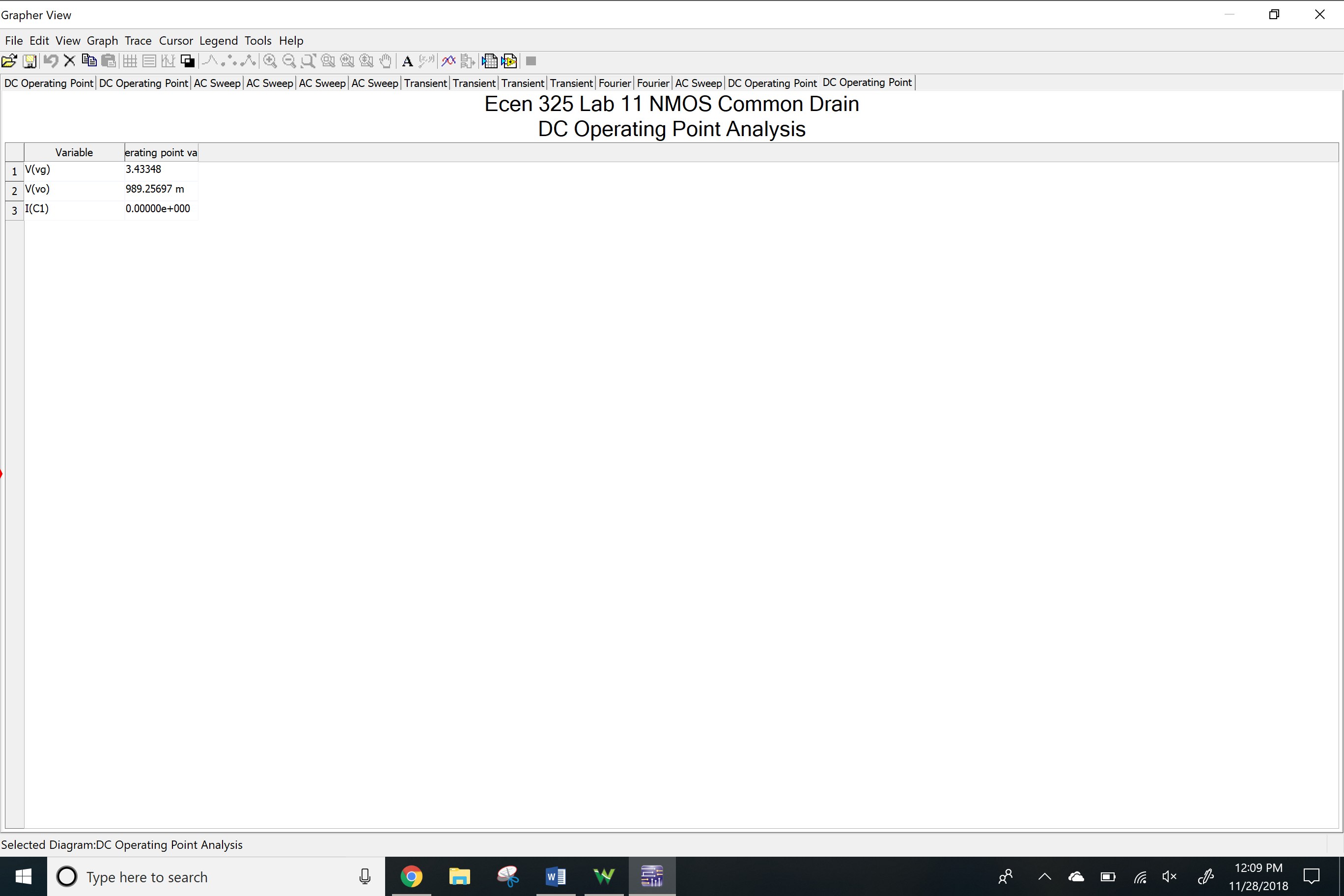
Clipping



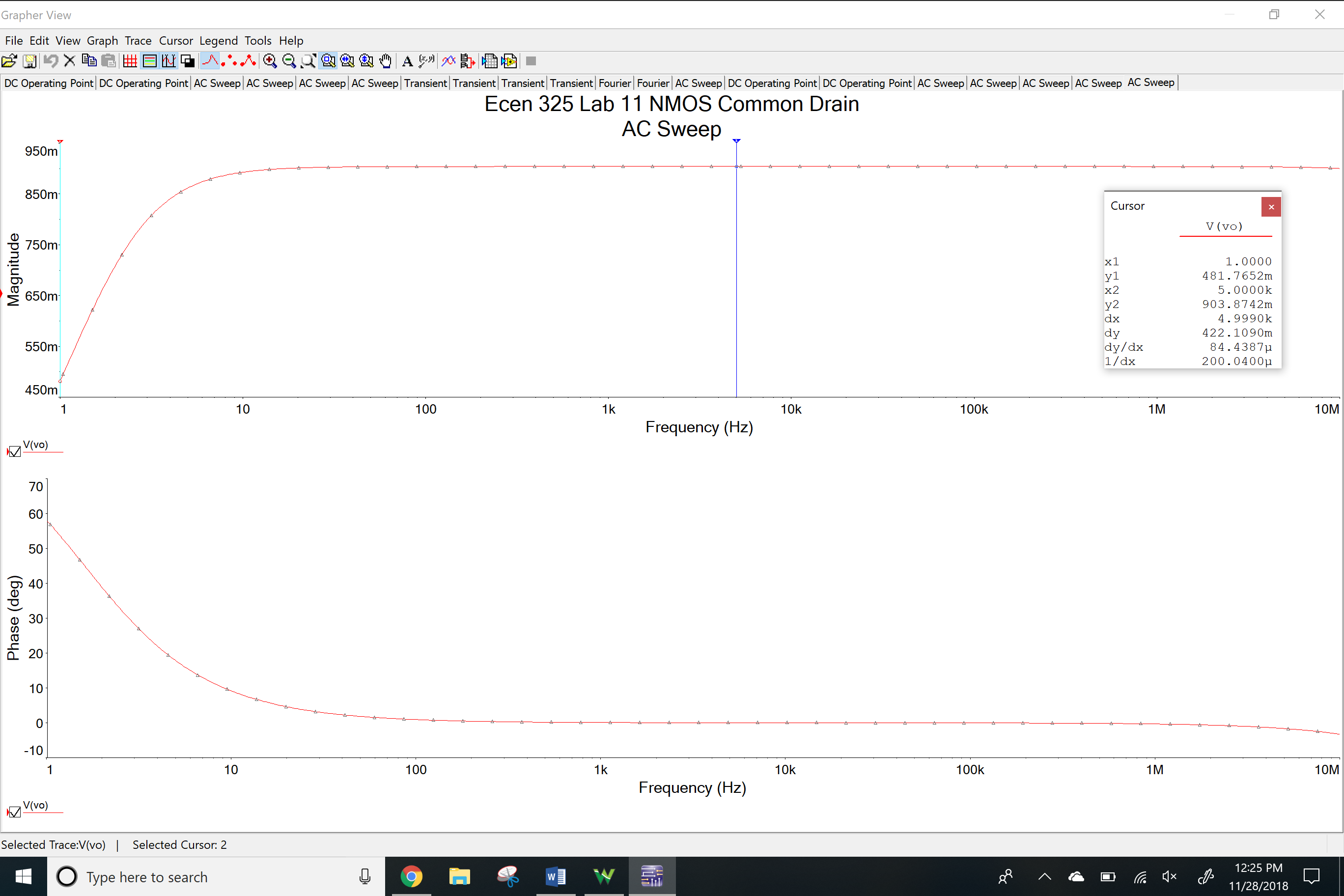
NMOS Common Drain



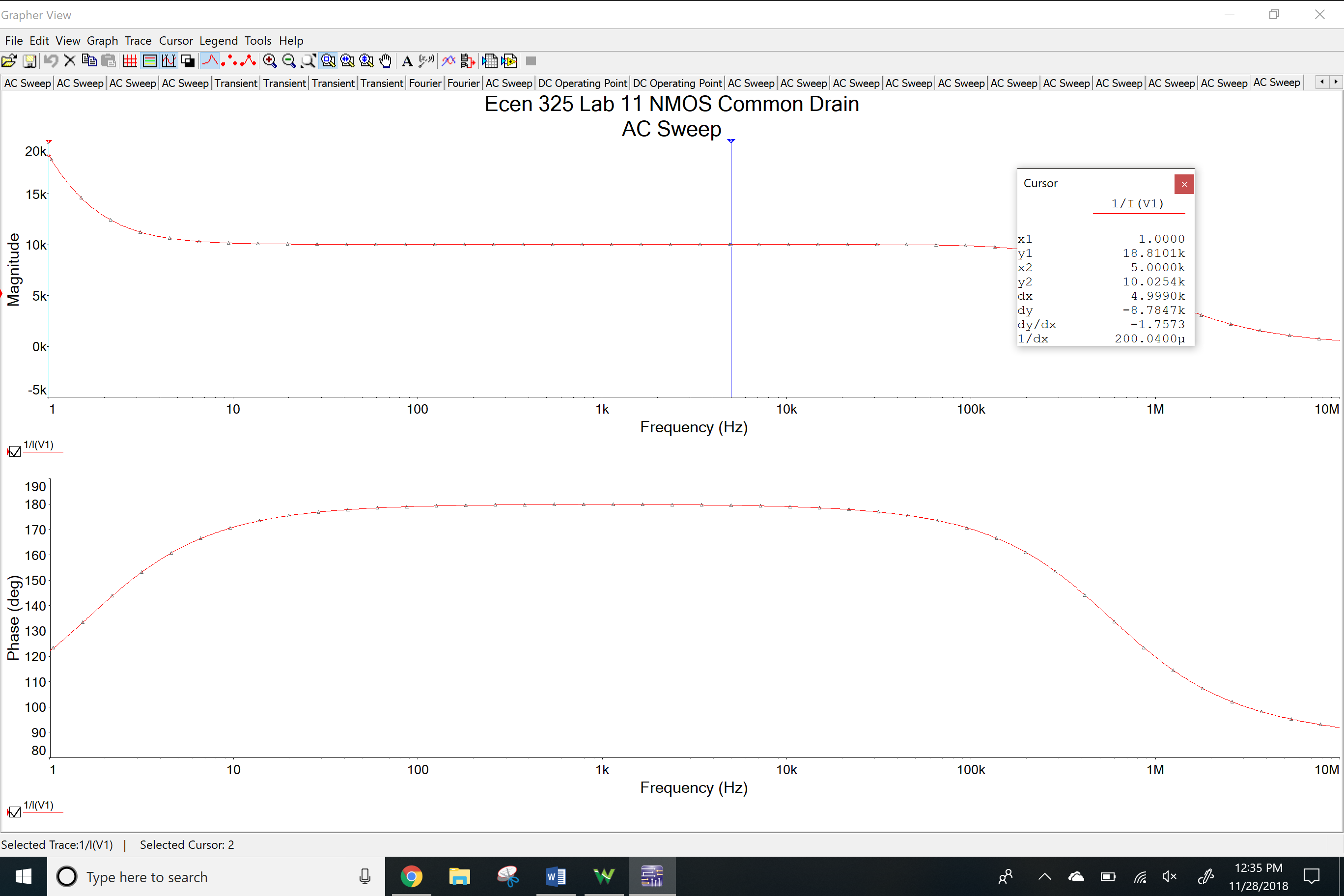
DC Operating Point

AC Simulation

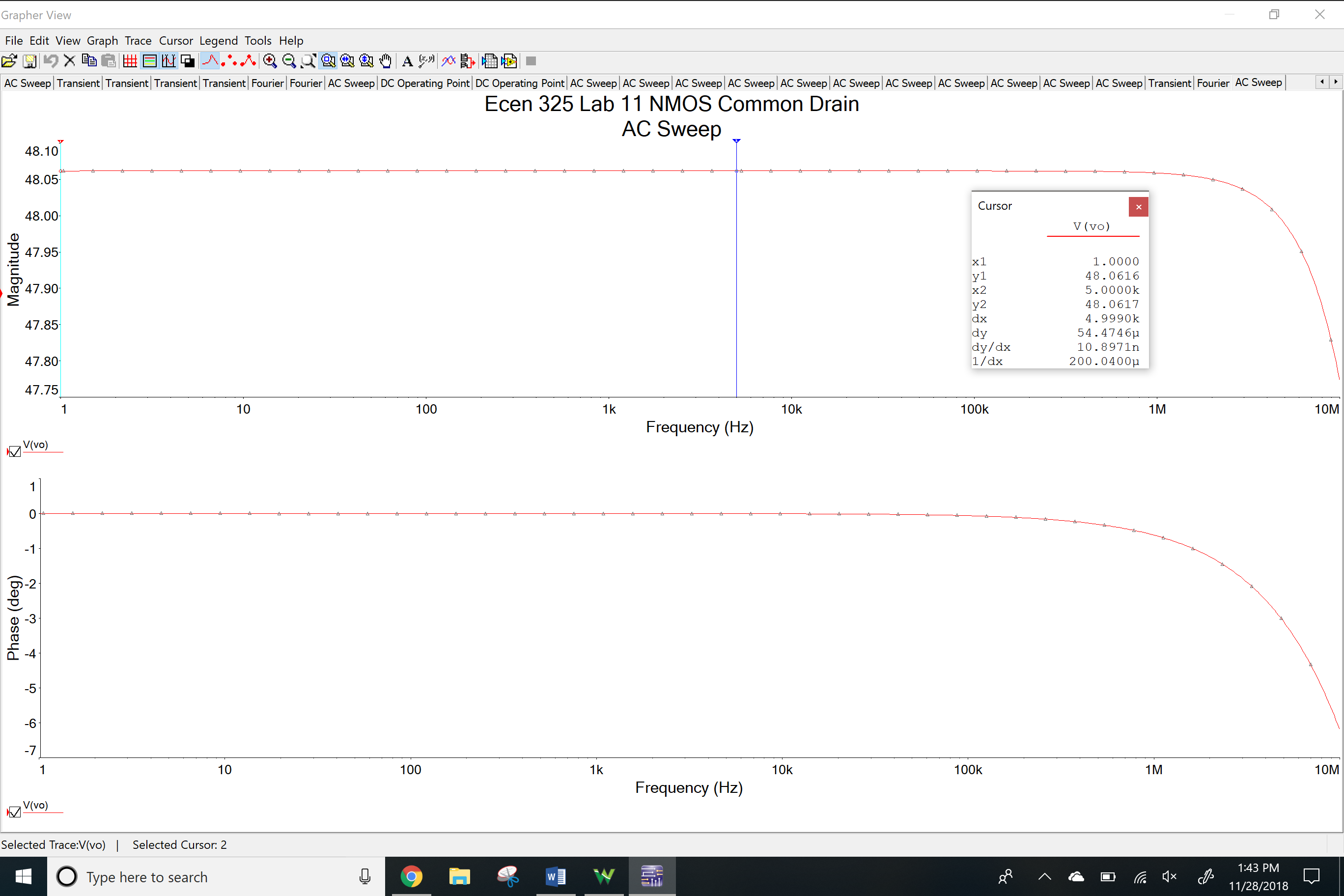
Av



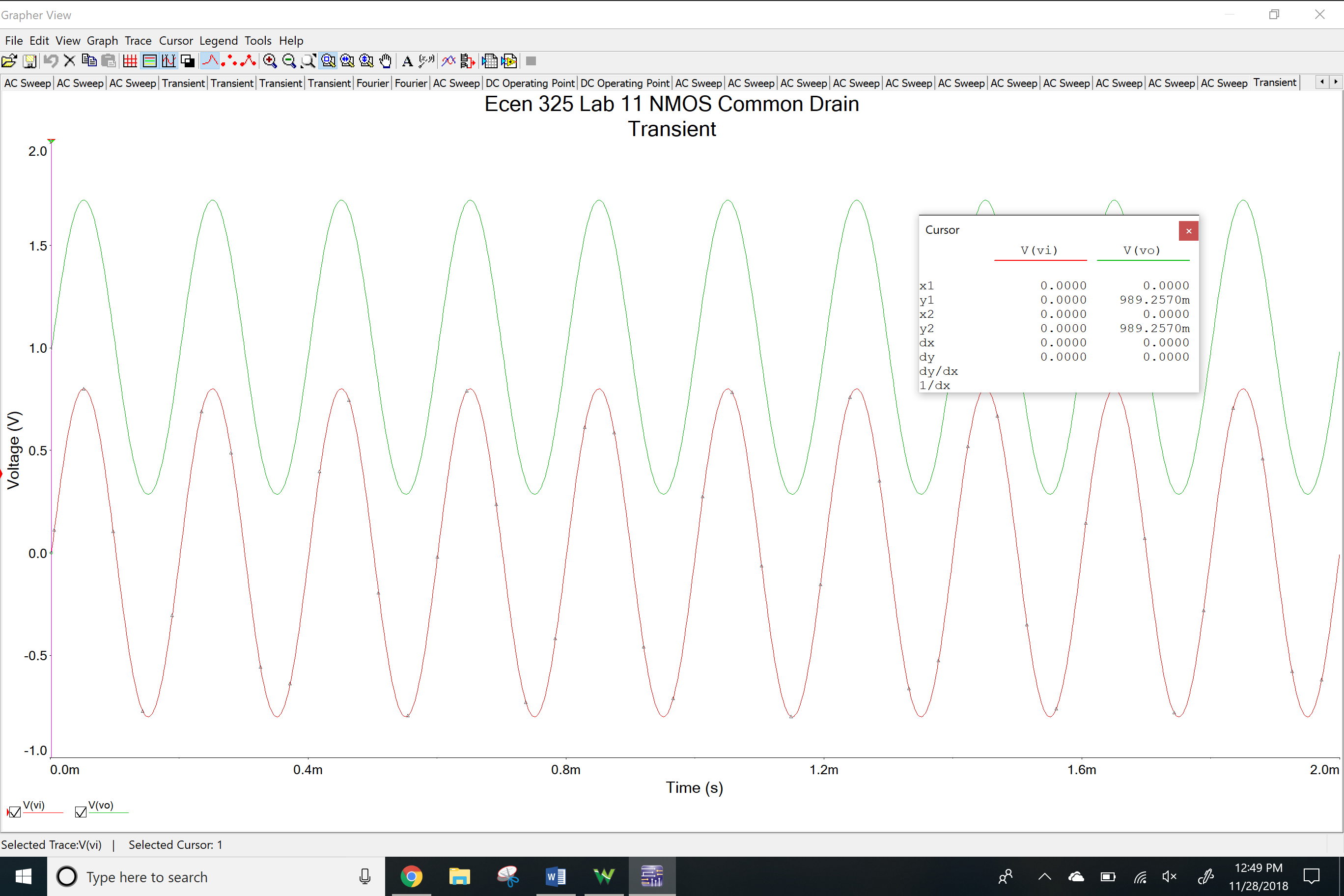
Rin



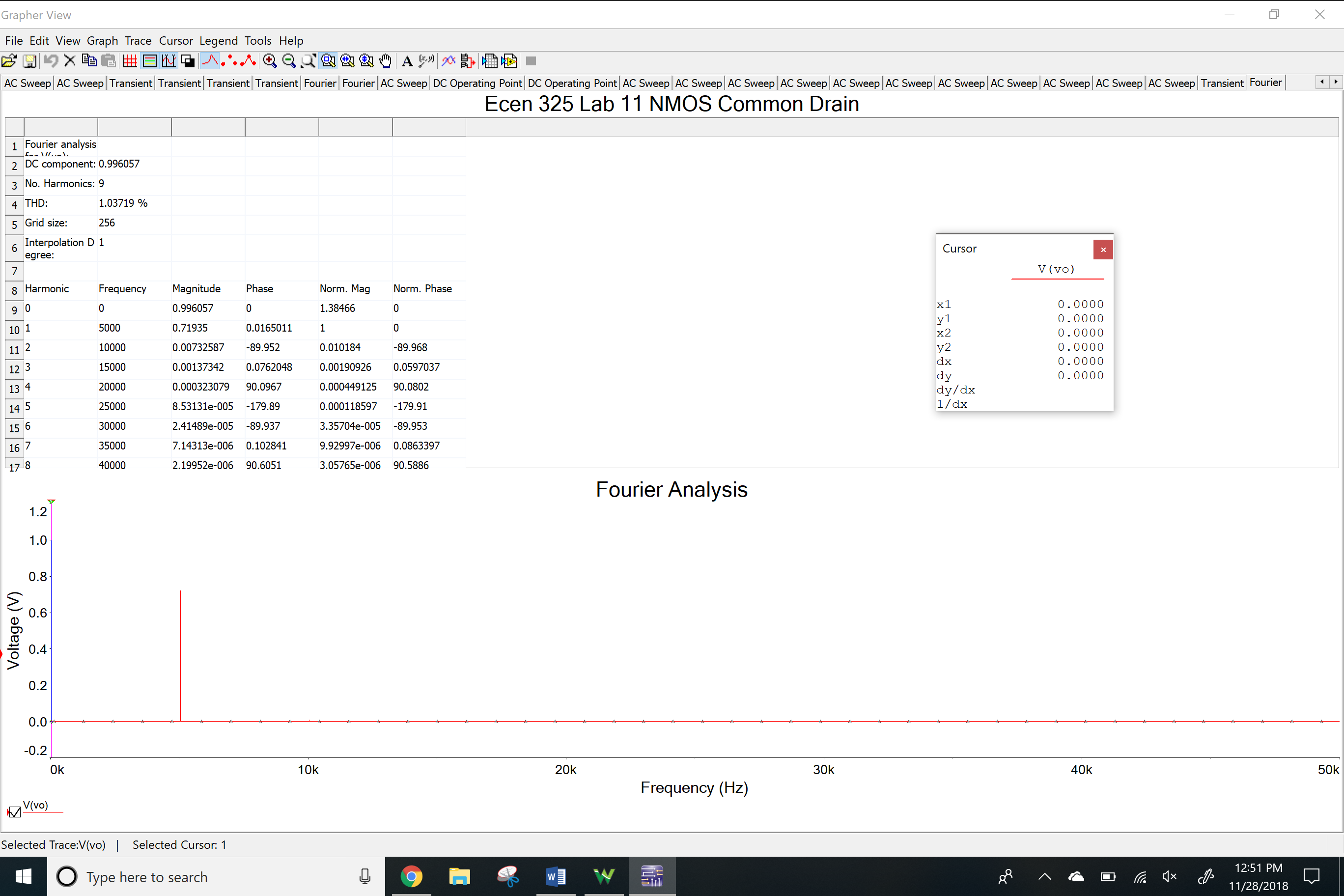
Rout



Time-domain waveform



THD

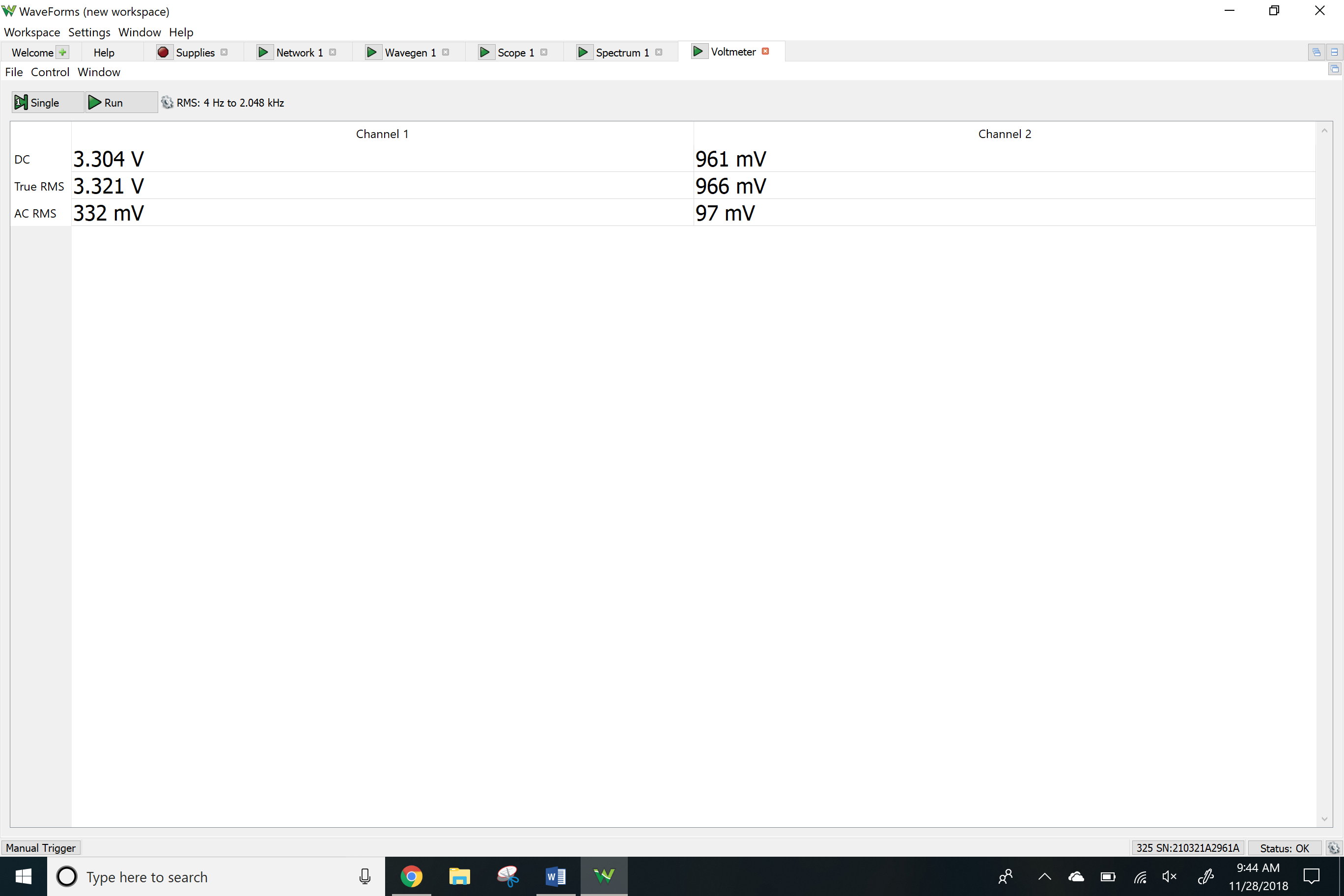


**Measurements**

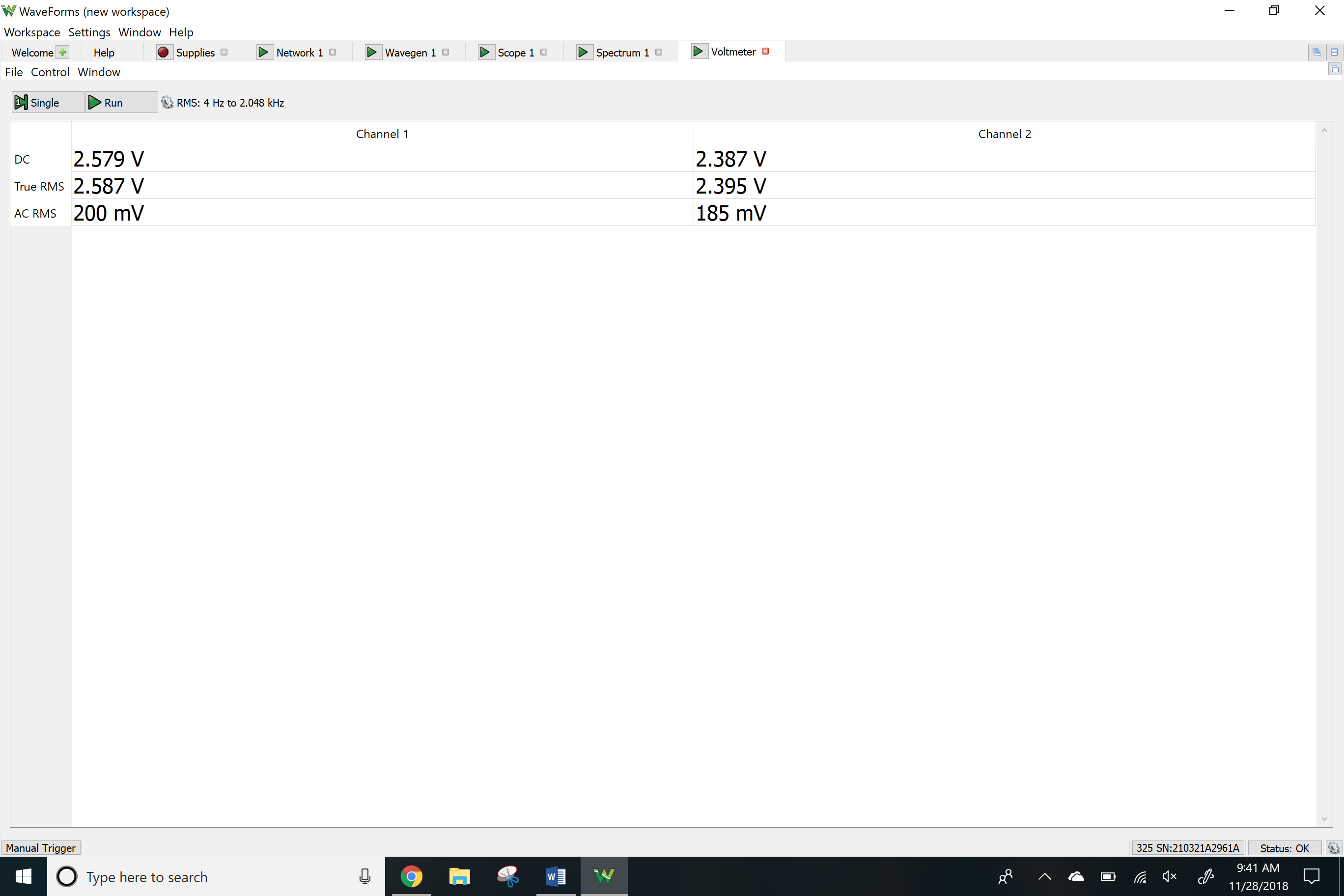
NMOS Common Source

DC Values

VRG2 and VRS



VRD and Vo



Network Analyzer

Av



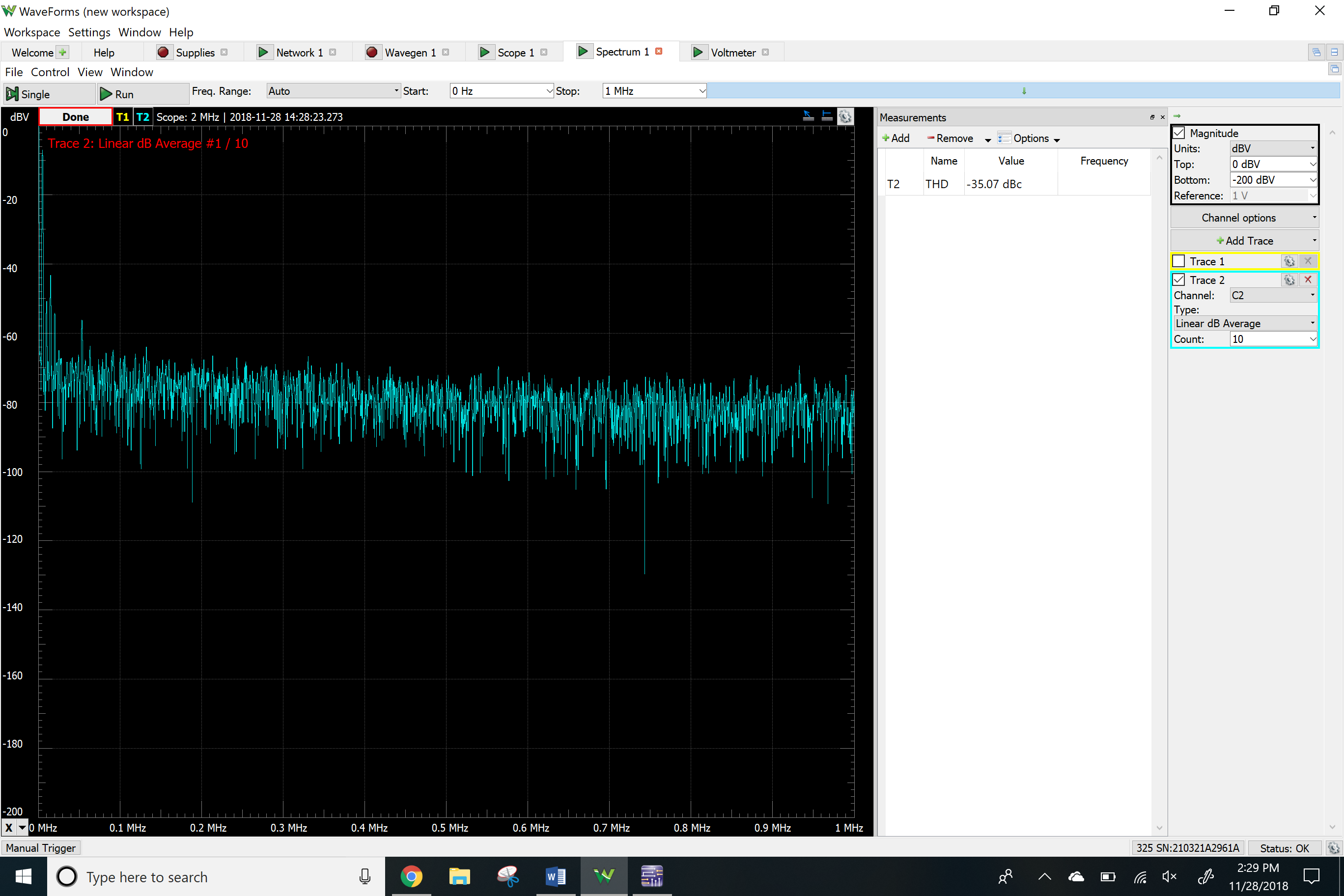
Ri



Time-domain waveform



THD



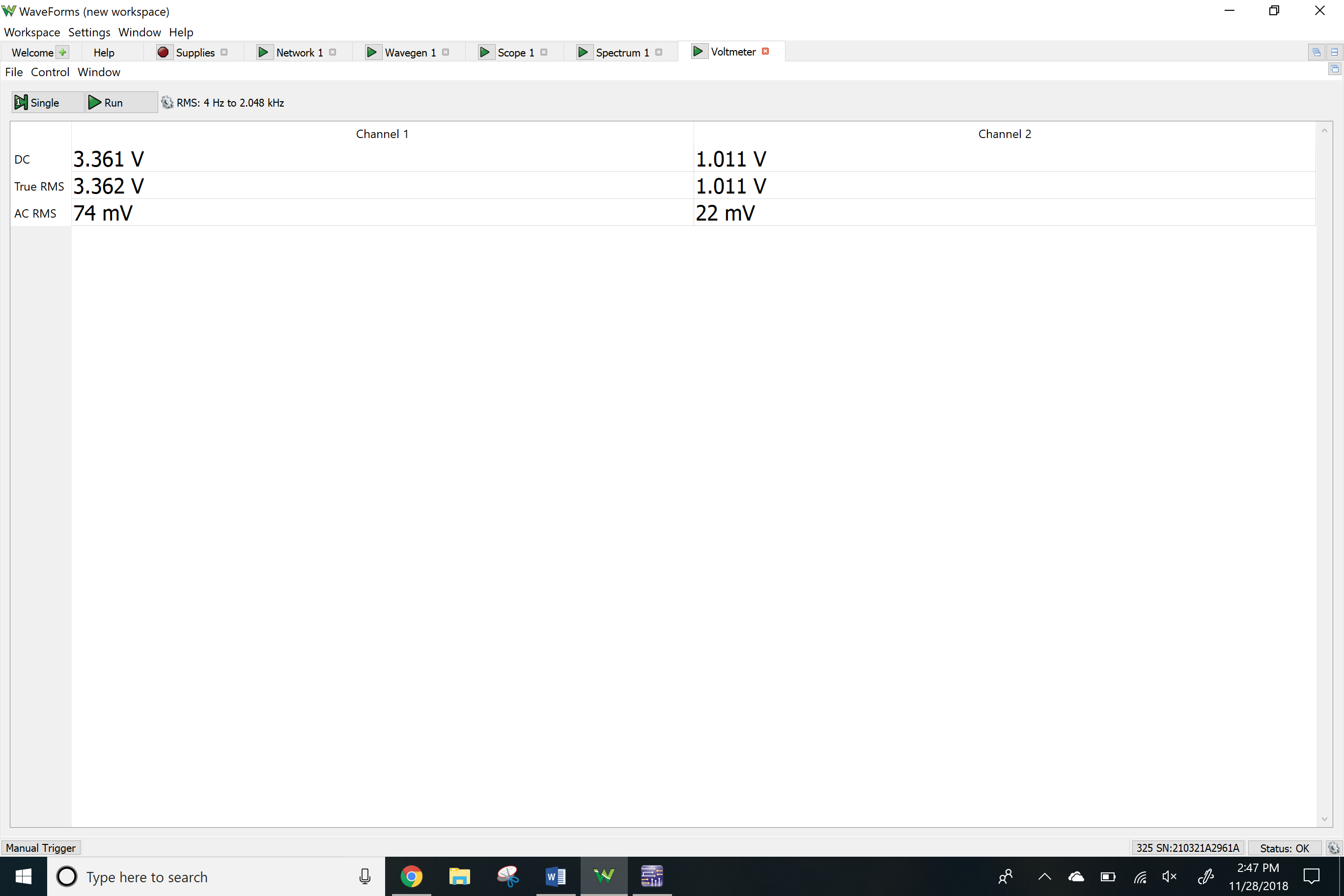
Clipping



NMOS Common Drain

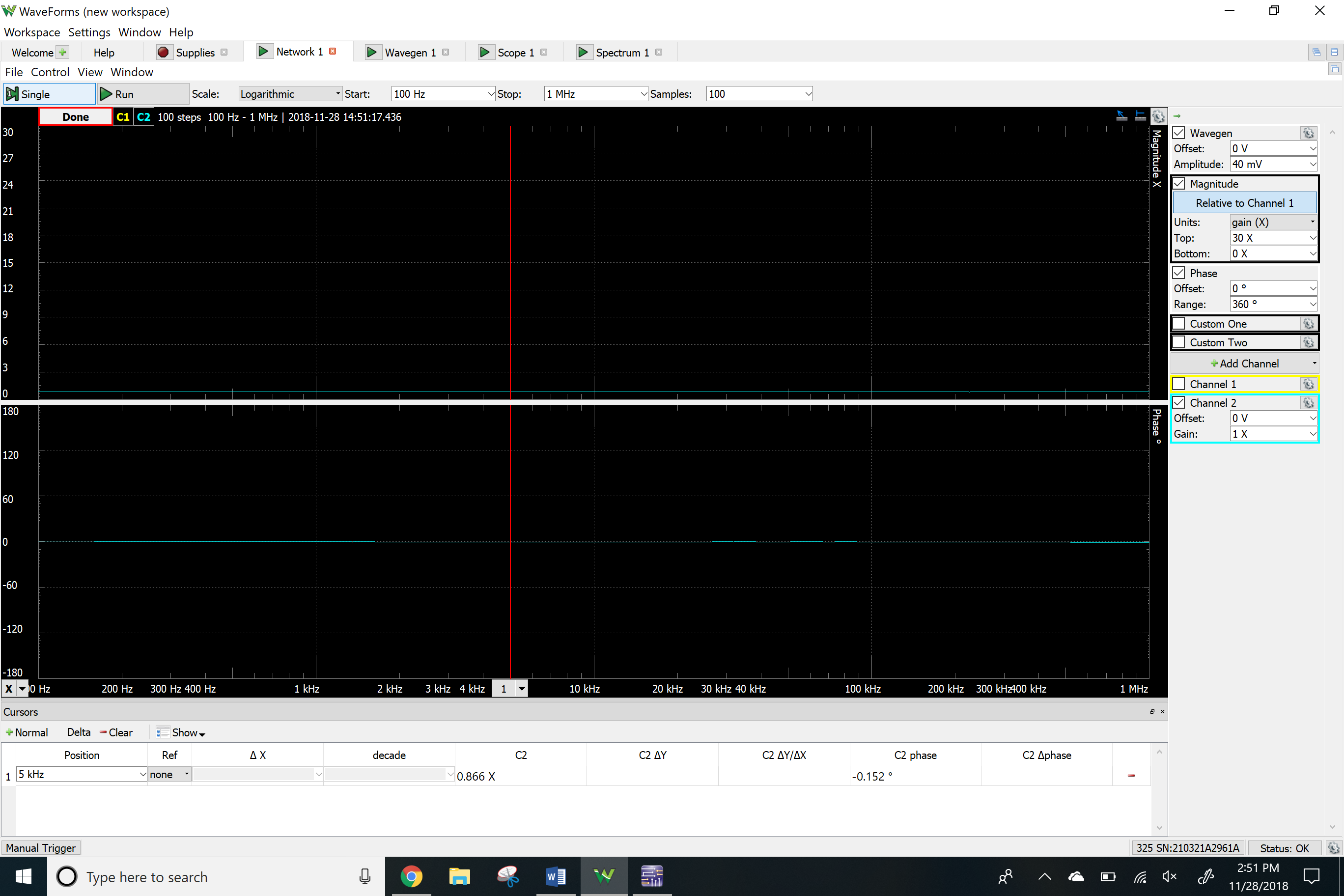
DC Values

VRG2 and VRS



Network Analyzer

Av



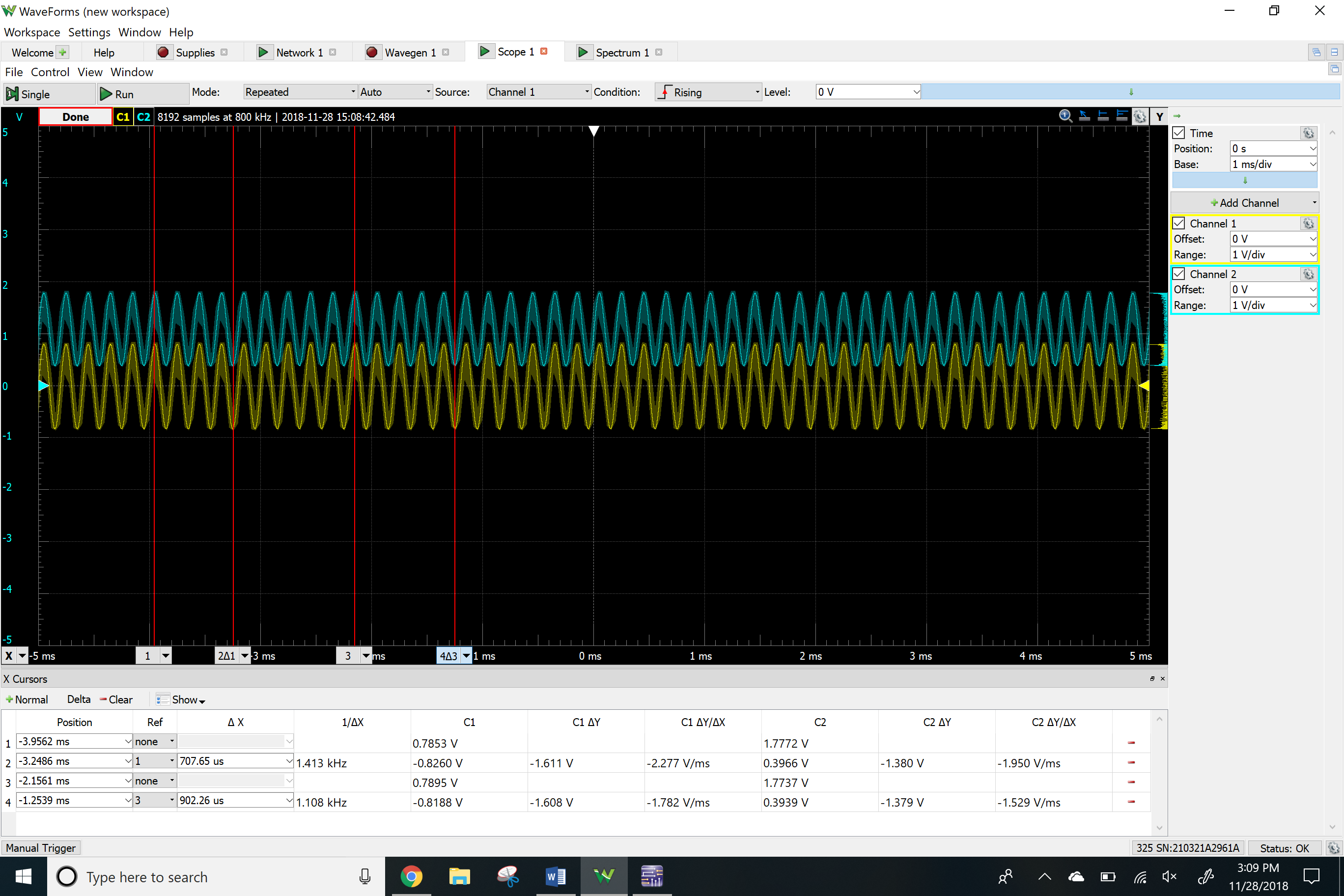
Ri



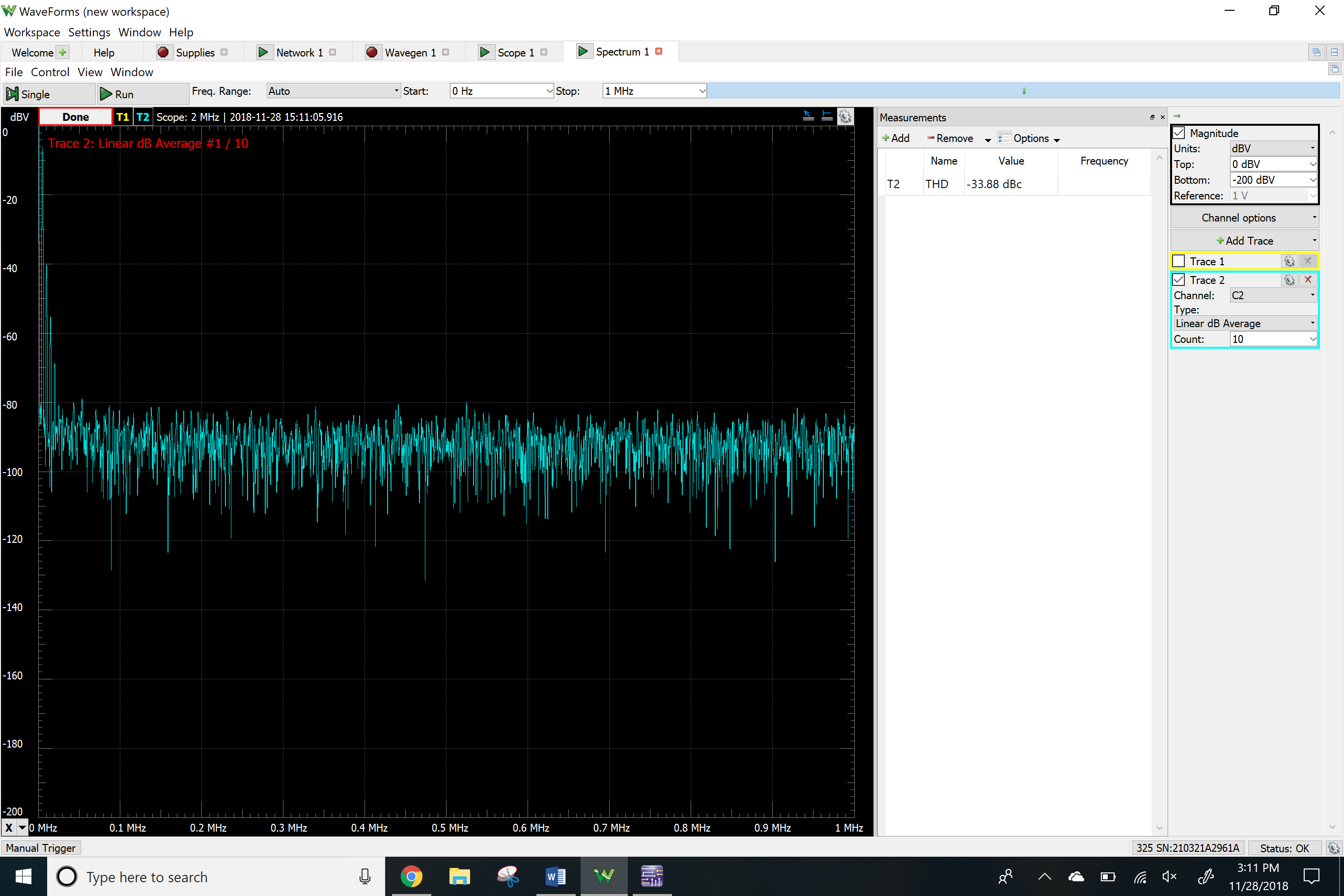
Ro



Time-domain waveform



THD



**Results**

Simulated

|  |  |  |
| --- | --- | --- |
|  | NMOS Common Source | NMOS Common Drain |
| VRG2 | 3.39 V | 3.43 V |
| VRS | 974 mV | 989 mV |
| VRD | 2.24 V | - |
| VO | 2.75 V | - |
| ID | 1.49 mA | 0 A |
| Av | 24.54 | 0.903 |
| Ri | 6352 Ω | 10025 Ω |
| Ro | - | 48 Ω |
| THD | 4.67 % | 1.03 % |
| Clipping | 60 mV | - |

Measured

|  |  |  |
| --- | --- | --- |
|  | NMOS Common Source | NMOS Common Drain |
| VRG2 | 3.30 V | 3.36 V |
| VRS | 961 mV | 1.01 V |
| VRD | 2.57 V | - |
| VO | 2.38 V | - |
| ID | 1.98 mA | 0 A |
| Av | 16.02 | 0.866 |
| Ri | 9989 Ω | 10111 Ω |
| Ro | - | 2144 Ω |
| THD | 1.76 % | 2.02 % |
| Clipping | 70 mV | - |

**Conclusion**

Overall the results that I simulated came out to be closed to the ones I measured and calculated. The only differences are for figure 3a the gain was measured to be 17, this could have been caused by using the Voltage threshold or the wrong k’ W/L ratio calculated in the previous lab. In this lab, I have learned the basic properties for the MOS amplifier configuration. The important concept learned during this lab were the DC operating point, Voltage gain and the input and output impedances of common source and common drain topologies. We were required to reach the gain of 25 but, the measurement of the implemented circuit was not able to fully reach the gain.