DX83E08

I2C Interface
ECC/SM2
AES/SM4
SHA1/SHA2/SM3
Signature and Authentication
Session Key Agreement
Encrypt/Decrypt
Single Chip Solution

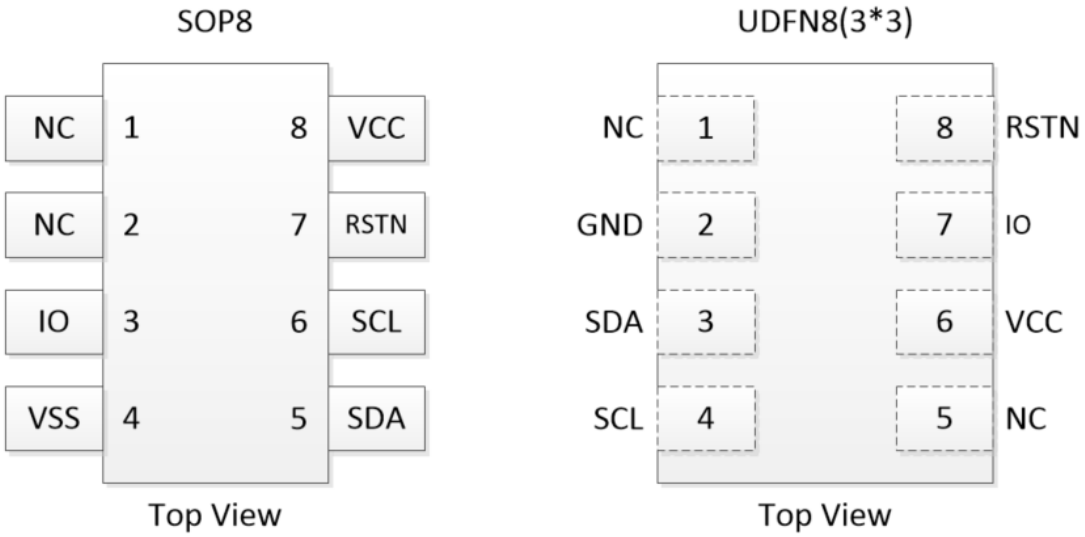
Revision 1.3
10/2020

Features

- Cryptographic Co-processor with Secure Hardware-based Key Storage
  --- Protected Storage for up to 8 Keys, Certificates or Data
- Hardware support for Asymmetric Sign, Verify, Key Agreement
  --- ECC-GF(p): 256-btis
  --- ECDSA: Elliptic Curve Digital Signature
  --- ECDH/ECDHE: Elliptic Curve Diffie-Hellman
  --- Support SM2 Signature and Key Agreement
- Hardware support for Symmetric Algorithms
  ---Cipher algorithms: AES (128, 192, 256-bits) and SM4
  ---Cipher mode: ECB, CBC, CTR, OFB, CFB, XTS, CCM, GCM
  ---Hash(MAC) algorithms: SHA-1, SHA-2 and SM3
  ---Hash mode: Raw, SSLMAC, HMAC
- Network Key Management Support
  --- Turnkey PRF/HMAC calculation for TLS 1.2
  --- Ephemeral key generation and key agreement in SRAM
  --- Small message encryption with keys entirely protected
- Secure Boot Support
  --- Full ECDSA code signature validation, optional stored digest/signature
  --- Optional communication key disablement prior to secure boot
  --- Encryption/Authentication for messages to prevent on-board attacks
- Internal High-quality True Random Number Generator(TRNG)
- Two high-endurance monotonic counters
- Guaranteed Unique 64-bit Serial Number
- 8*2K bytes User eFlash Memory for Keys, Certificates, and Data
- I2C Interface
  --- 1.0M Hz Compatibility for Fast Operation
  --- SOP8 Package has the Same Pinout as 2-wire (24 Series) Serial EEPROM's
- High reliability
  --- Endurance: 100K Cycles
  --- Data Retention: 10 years
  --- ESD Protection: 4KV
- Supply/IO Voltage: 1.8V—5.5V
- Temperature: -40^{0}C --- +85^{0}C
- < 1uA Sleep current
- Package: SOP8, UDFN8
- Applications
  --- IOT network and endpoint key management & exchange
  --- Encryption for small messages and data
  --- Secure Boot and Protected Download
  --- Ecosystem Control, Anti-cloning

Package and PINs

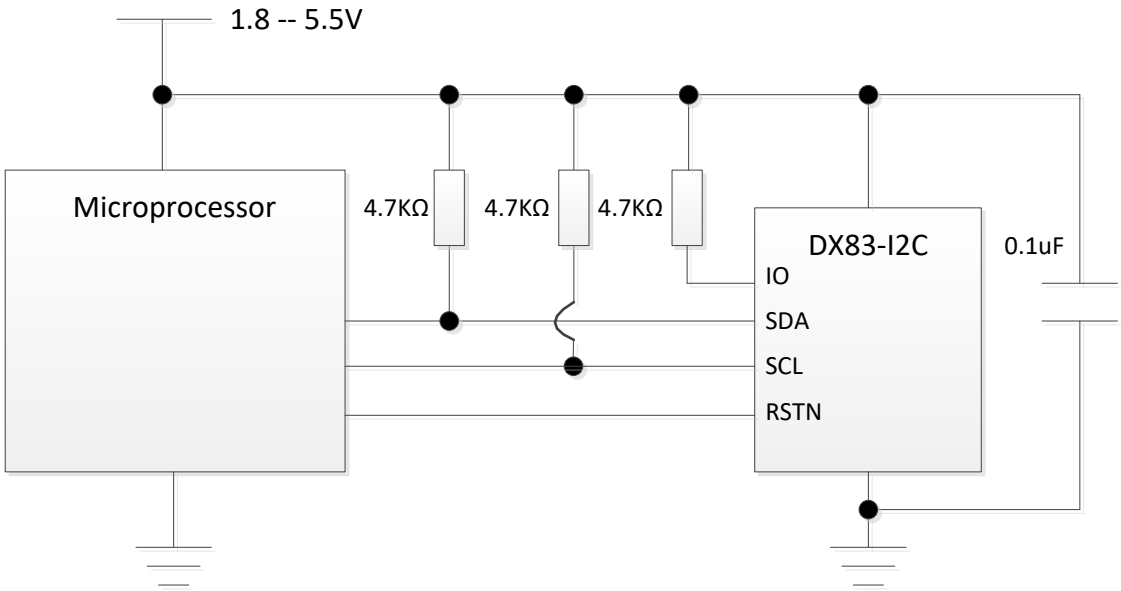
I2C Interface



Signal	IO	Description
VCC	I	Power supply 1.8V – 5.5V
VSS	G	Ground
RSTN	I	External Reset, Active Low
IO	I/O	RFU, Should be Tie High
SCL	I	I2C Interface Clock Line
SDA	I/O	I2C Interface Data Line

Typical Operation Circuit

I2C Interface



Order Information

Part	Interface	Package Type
DX83E08-C-SOP	I2C	SOP8
DX83E08-C-DFN		UDFN8

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	1.8	5.5	V
Operating Temperature	-45	+85	°C
DC Output Current	10		mA
Voltage on Any Pin	-0.5	V_{CC}+0.5	V

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Reliability

Parameter	Min	Typical	Max	Units
Write Endurance (each byte at 25^0C)	100K			Write Cycles
Data Retention (at 55^0C)	10			Years

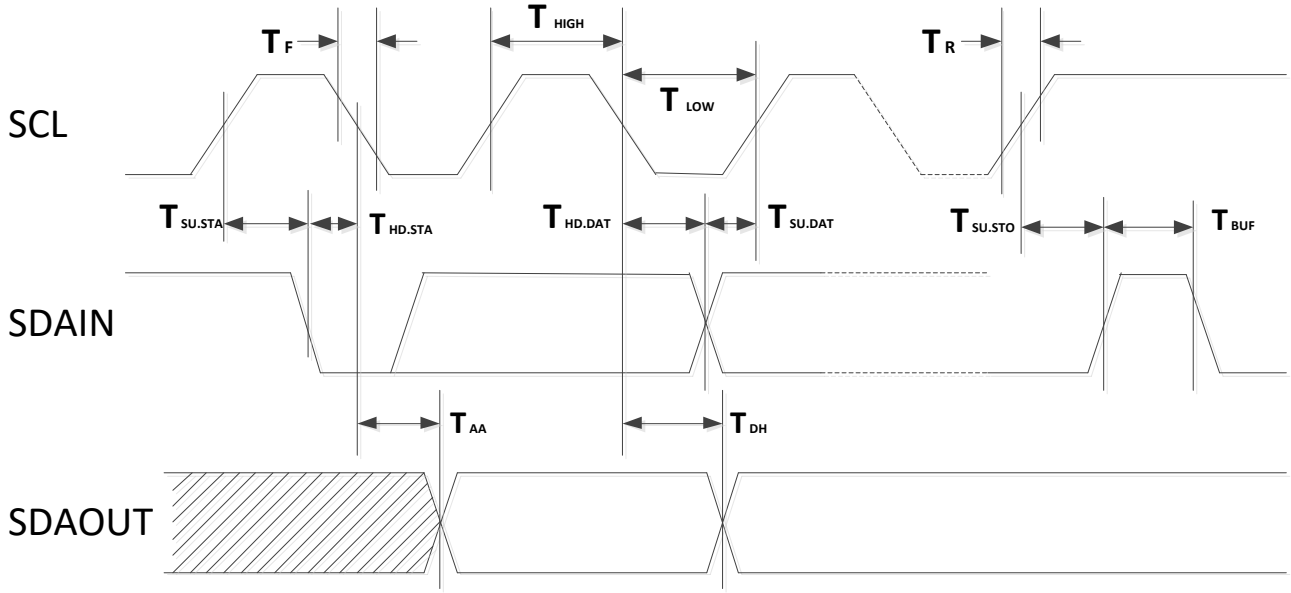
DC Electrical Characteristic

Symbol	Parameter[1]	Min.	Typ	Max.	Unit	Notes
T_O	Operating Temperature	-45		85	°C	
V_{CC}	Supply Voltage	1.8	3.3	5.5	V	
I_{CC}	Power Supply Current		7.0		mA	V_{CC} = 3.3V, T_A= 25°C
			8.0		mA	V_{CC} = 5.5V, T_A = 25°C
I_{SB}	Standby Current			1	uA	Device in Sleep mode **I2C Interface:** SCL and SDA to V_{CC}
V_{OL}	Output Low Voltage			0.4	V	V_{CC} =3.3V
V_{OH}	Output High Voltage	2.4		3.3	V	V_{CC} = 3.3V
V_{IH}	Input High Voltage	0.6 * V_{CC}			V	
V_{IL}	Input Low Voltage			0.3 * V_{CC}	V	

[1] The parameters are characterized but not 100% tested.

AC Electrical Characteristic

I2C Timing



Industrial: T_A = - 40°C to + 85°C, V_{CC} = 1.8 ~ 5.5V

Symbol	Parameter[1] [2]	Min.	Max.	Unit
F_{SCL}	SCL Clock Frequency		1	MHz
T_{LOW}	SCL Clock Low Period	400	--	ns
T_{HIGH}	SCL Clock High Period	400	--	ns
$T_{SU:STA}$	Start Condition Setup Time	250	--	ns
$T_{HD:STA}$	Start Condition Hold Time	250		ns
$T_{SU:STO}$	Stop Condition Setup Time	250	--	ns
$T_{SU:DAT}$	Data In Setup Time	100		ns
$T_{HD:DAT}$	Data In Hold Time	10		ns
T_R	Rise Time (SCL and SDA)	--	300	ns
T_F	Fall Time (SCL and SDA)	--	100	ns
T_{AA}	SCL Clock Low to SDA Data Out Valid Time	50	400	ns
T_{DH}	Data Out Hold Time	50		ns
T_{WR}	Write Cycle Time		4	ms
T_{BUF}	Bus Free Time Before New Transmission Start	500		ns

[1] The parameters are characterized but not 100% tested.

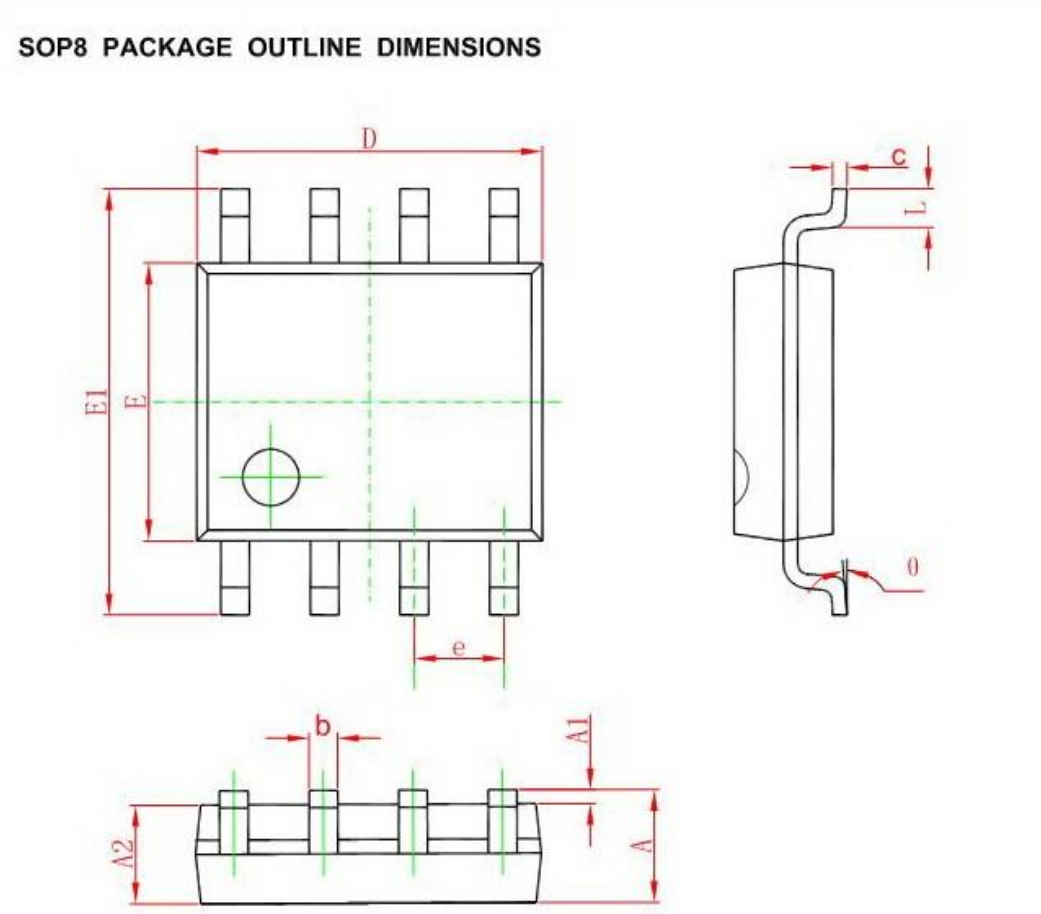
[2] AC measurement conditions:

RL (connects to VCC): 1.3kΩ (1.8V--5.0V); Input pulse voltages: 0.3*V_{CC} to 0.7*V_{CC};

Input rise and fall times: ≤ 50 ns; Timing reference voltages: half V_{CC} level;

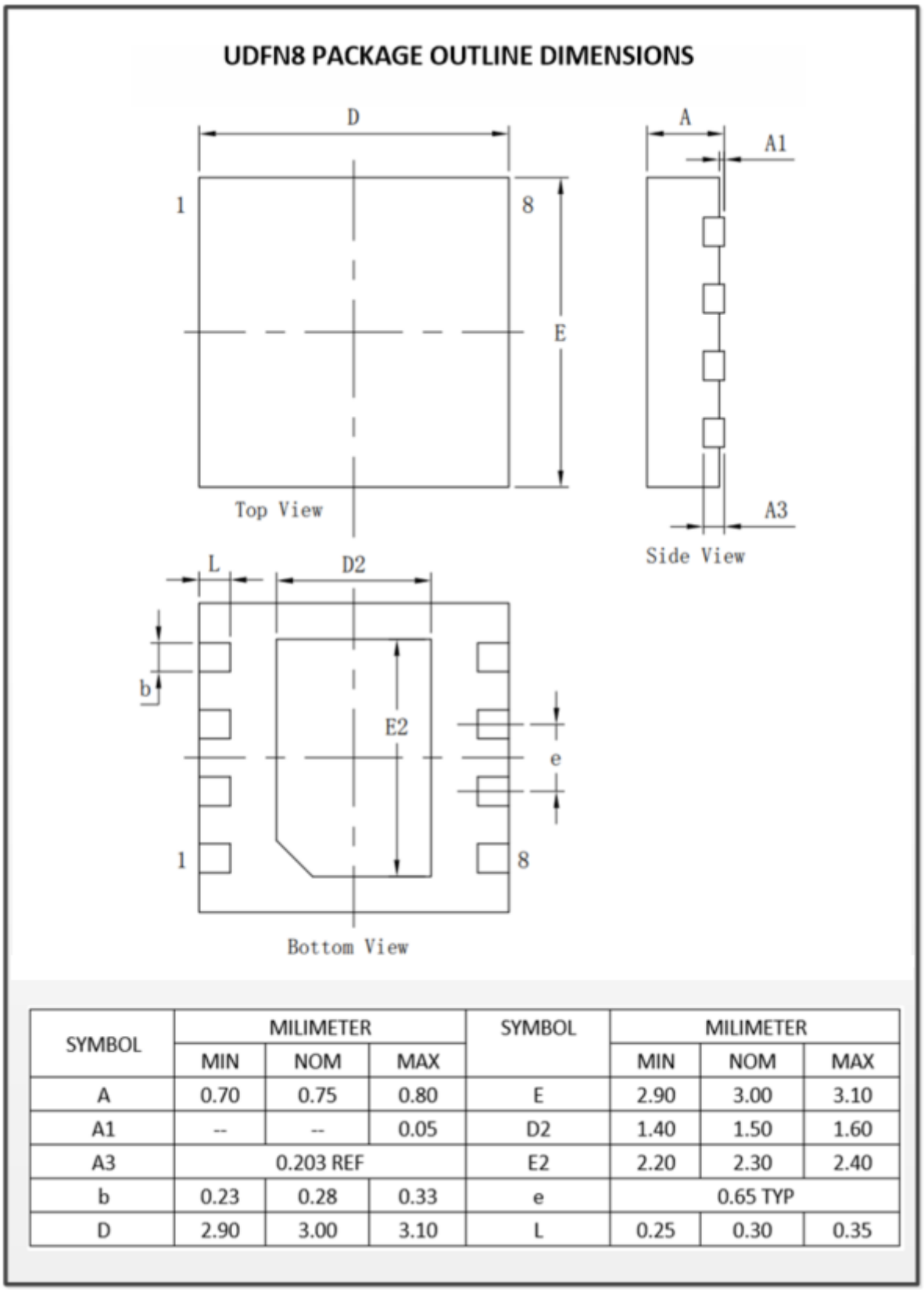
Package Drawing

SOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

UDFN8



SYMBOL	MILIMETER			SYMBOL	MILIMETER		
	MIN	NOM	MAX		MIN	NOM	MAX
A	0.70	0.75	0.80	E	2.90	3.00	3.10
A1	--	--	0.05	D2	1.40	1.50	1.60
A3	0.203 REF			E2	2.20	2.30	2.40
b	0.23	0.28	0.33	e	0.65 TYP		
D	2.90	3.00	3.10	L	0.25	0.30	0.35