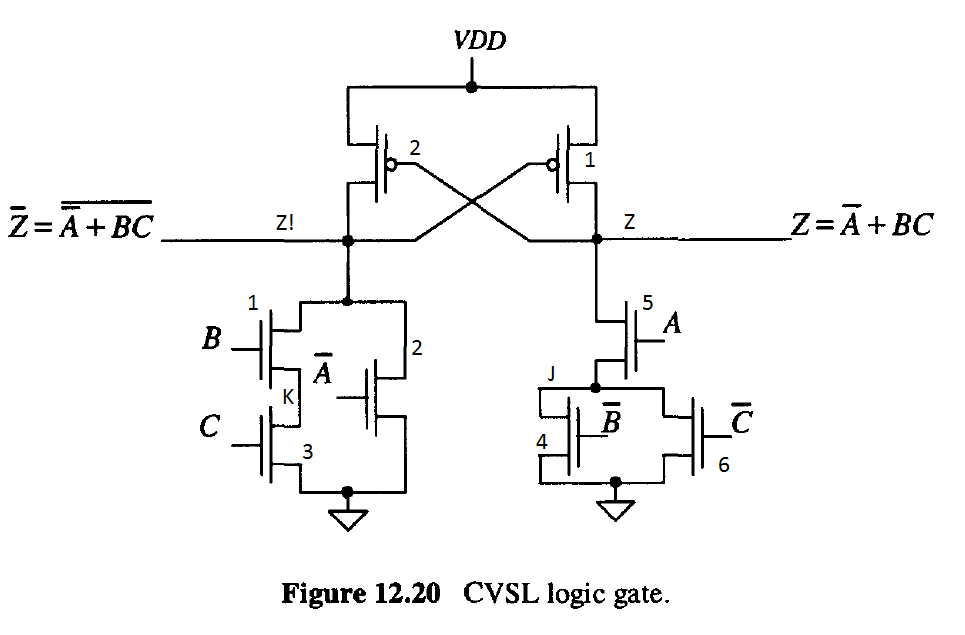
Gil Michael E. Regalado BS-ECE IV

**CVSL Activity**

**Cascode Voltage Switch Logic** or differential cascode voltage switch logic improves switching times of logic circuits by employing positive feedback.

In this exercise we consider the implementation of, . This will produce a differential opposite of . The following figure shows the circuit diagram. A SPICE script will be created and simulated using 0.18u architecture with 1.8V VDD and logic High.



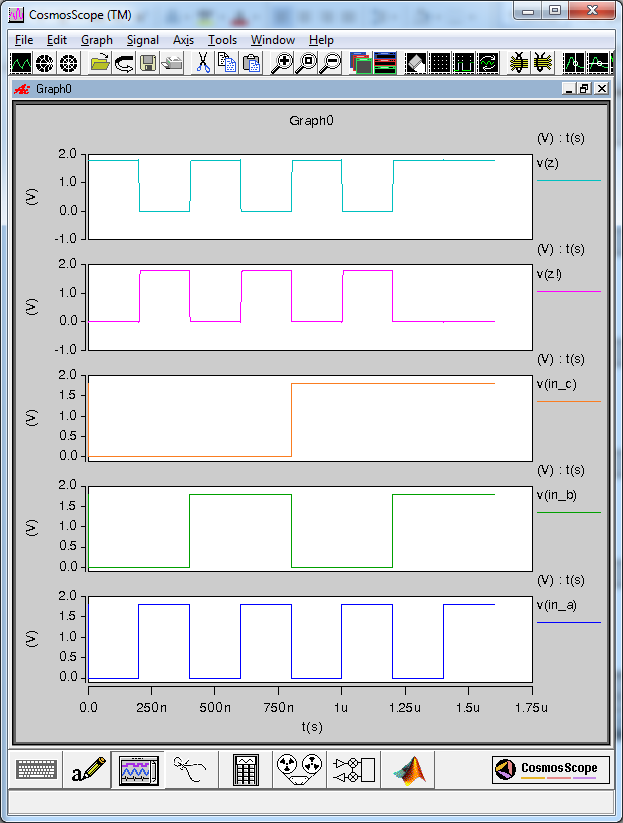
It has the following truth table.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | Z | Z! |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

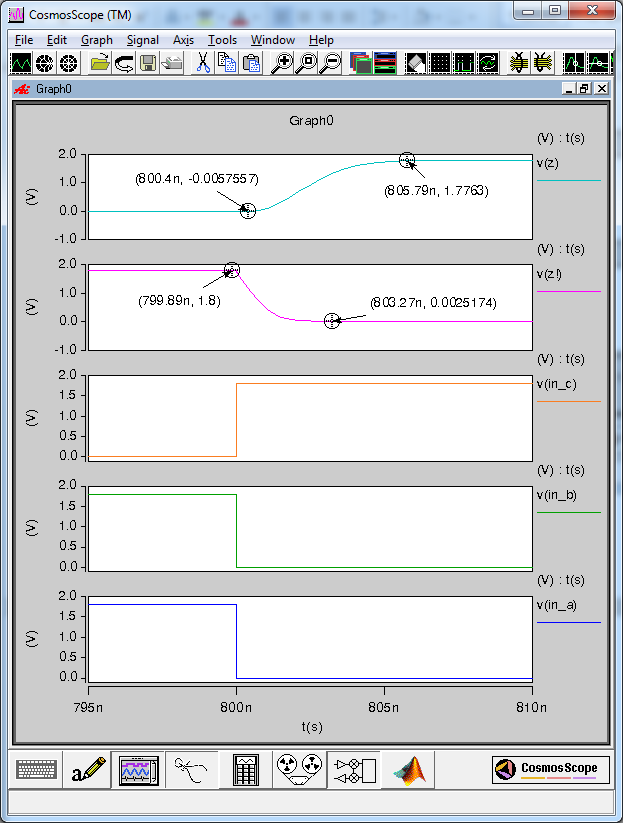
The following is the spice script:

|  |
| --- |
| CVSL  .PARAM LMIN=0.18u  .PARAM WFACTOR=1.5  .PARAM WMIN='LMIN\*WFACTOR'  .lib "C:\synopsys\rf018.l" TT  .global vdd  .option post  Cout\_z Z 0 100f  Cout\_!z Z! 0 100f  Vdd vdd 0 1.8  Vin\_a in\_a 0 pulse (1.8 0 1.0p 0 0 200n 400n)  Vin\_b in\_b 0 pulse (1.8 0 1.0p 0 0 400n 800n)  Vin\_c in\_c 0 pulse (1.8 0 1.0p 0 0 800n 1600n)  Vin\_!a in\_!a 0 pulse (0 1.8 1.0p 0 0 200n 400n)  Vin\_!b in\_!b 0 pulse (0 1.8 1.0p 0 0 400n 800n)  Vin\_!c in\_!c 0 pulse (0 1.8 1.0p 0 0 800n 1600n)  X\_cvsl in\_a in\_b in\_c in\_!a in\_!b in\_!c Z Z! cvsl  .subckt cvsl in\_a in\_b in\_c in\_!a in\_!b in\_!c Z Z!  MN1 Z! in\_b K 0 nch l=LMIN w='WMIN\*2'  MN2 Z! in\_!a 0 0 nch l=LMIN w=WMIN  MN3 K in\_c 0 0 nch l=LMIN w='WMIN\*2'    MN4 J in\_!b 0 0 nch l=LMIN w=WMIN  MN5 Z in\_a J 0 nch l=LMIN w='WMIN\*2'  MN6 J in\_!c 0 0 nch l=LMIN w=WMIN    MP1 Z Z! vdd vdd pch l=LMIN w='WMIN\*1'  MP2 Z! Z vdd vdd pch l=LMIN w='WMIN\*1'  .ends  .op  .tran 1p 1600n  .end |

Using Cosmoscope the simulation results are shown:



If we Zoon a little bit we can see the transition of the logic from 0 to 1.8V



We have determined that the response time for this logic circuit is around:

