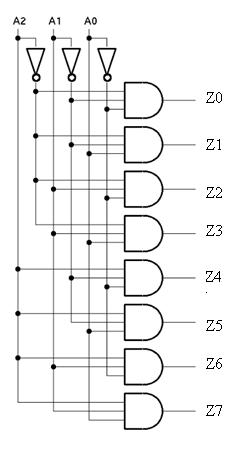
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

**3-8 DECODER**

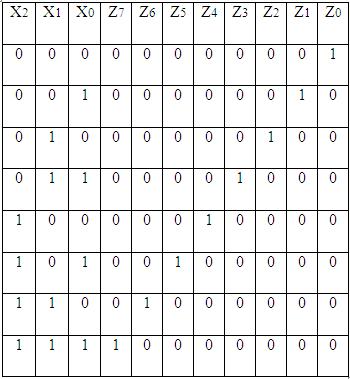


Table 2: Truth Table of 3:8 decoder

It uses all AND gates, and therefore, the outputs are active- high. For active- low outputs, NAND gates are used. It has 3 input lines and 8 output lines. It is also called as binary to octal decoder it takes a 3-bit binary input code and activates one of the 8(octal) outputs corresponding to that code.

**REQUIRED SUB CIRCUITS**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: INVERTER  .subckt not ndd nss in out  MN1 out in nss nss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in ndd ndd pch l='1\*LMIN' w='6\*LMIN'  .ends |

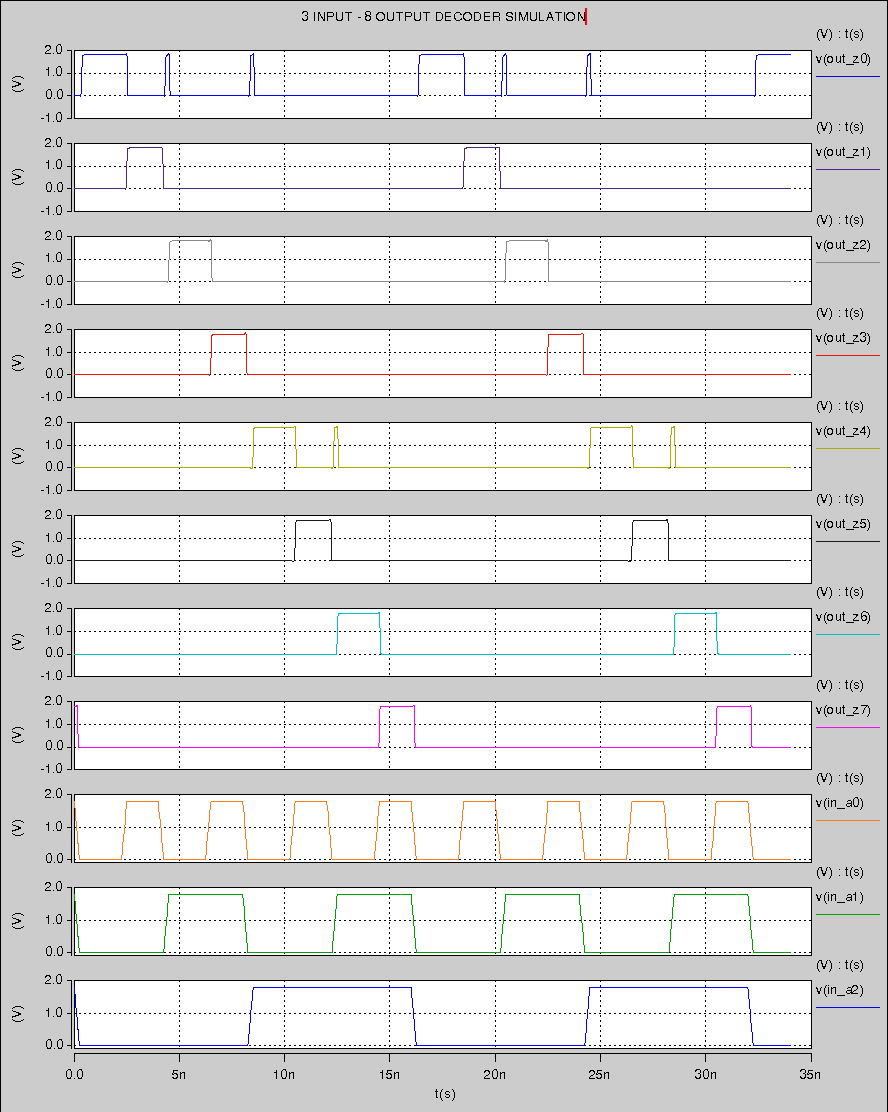
|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 3 INPUT NAND  .subckt nand3 dd ss a b c out  MN1 out a ab ss nch l='1\*LMIN' w='2\*LMIN'  MN2 ab b bc ss nch l='1\*LMIN' w='2\*LMIN'  MN3 bc c ss ss nch l='1\*LMIN' w='2\*LMIN'    MP1 out a dd dd pch l='1\*LMIN' w='6\*LMIN'  MP2 out b dd dd pch l='1\*LMIN' w='6\*LMIN'  MP3 out c dd dd pch l='1\*LMIN' w='6\*LMIN'  .ends |

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 3-8 DECODER  .include NAND3.SP  .include NOT.SP  .subckt decoder dd ss a0 a1 a2 z0 z1 z2 z3 z4 z5 z6 z7  Xnot0 dd ss a0 not\_a0 not  Xnot1 dd ss a1 not\_a1 not  Xnot2 dd ss a2 not\_a2 not  Xnot\_z0 dd ss not\_z0 z0 not  Xnot\_z1 dd ss not\_z1 z1 not  Xnot\_z2 dd ss not\_z2 z2 not  Xnot\_z3 dd ss not\_z3 z3 not  Xnot\_z4 dd ss not\_z4 z4 not  Xnot\_z5 dd ss not\_z5 z5 not  Xnot\_z6 dd ss not\_z6 z6 not  Xnot\_z7 dd ss not\_z7 z7 not  Xnand3\_0 dd ss not\_a0 not\_a1 not\_a2 not\_z0 nand3  Xnand3\_1 dd ss a0 not\_a1 not\_a2 not\_z1 nand3  Xnand3\_2 dd ss not\_a0 a1 not\_a2 not\_z2 nand3  Xnand3\_3 dd ss a0 a1 not\_a2 not\_z3 nand3  Xnand3\_4 dd ss not\_a0 not\_a1 a2 not\_z4 nand3  Xnand3\_5 dd ss a0 not\_a1 a2 not\_z5 nand3  Xnand3\_6 dd ss not\_a0 a1 a2 not\_z6 nand3  Xnand3\_7 dd ss a0 a1 a2 not\_z7 nand3  .ends |

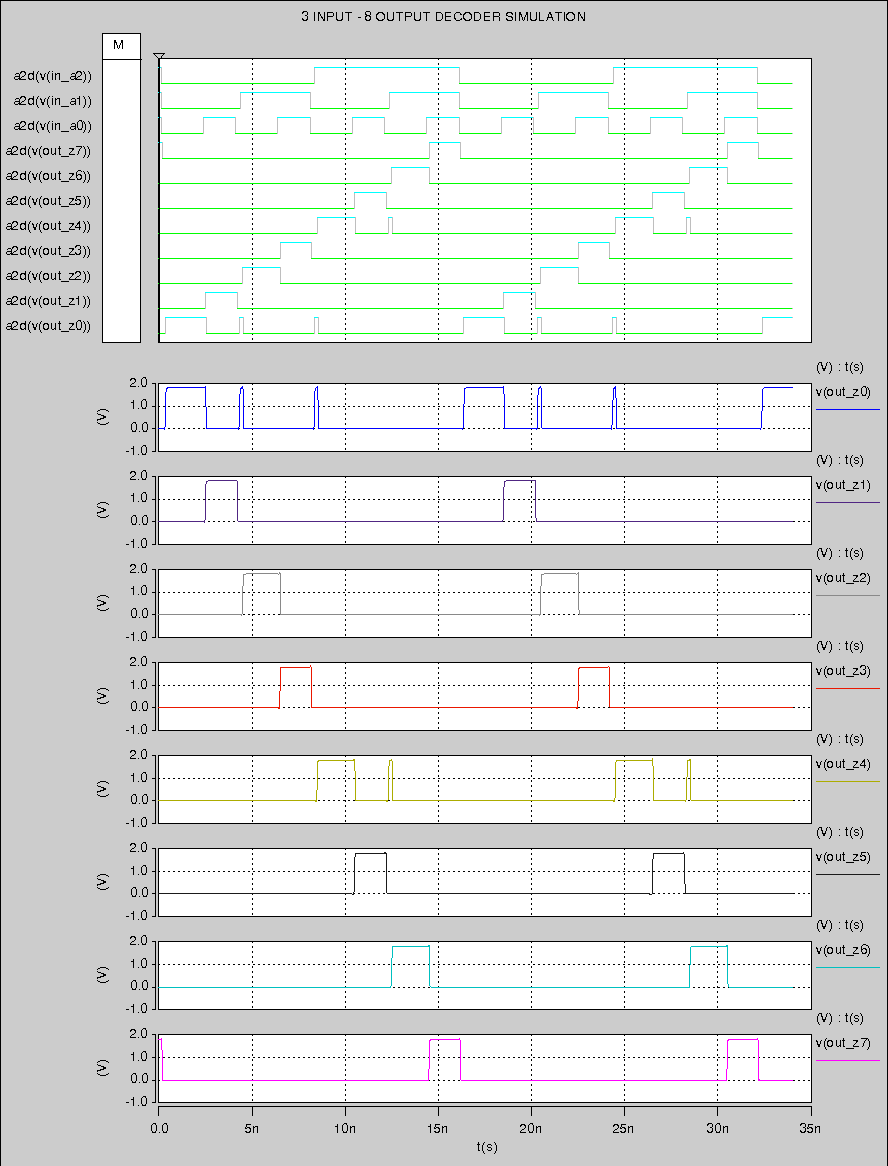
**TEST BENCH CODE**

|  |
| --- |
| 3-8 DECODER TEST BENCH  \*\*\*\*\*\* REFERENCE: http://coep.vlab.co.in/?sub=28&brch=81&sim=609&cnt=1  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 '32n + (8\*TRAN\_TIME)'  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va0 in\_a0 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Va1 in\_a1 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 4n 8n)  Va2 in\_a2 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 8n 16n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Cz0 out\_z0 ss 0.01f  Cz1 out\_z1 ss 0.01f  Cz2 out\_z2 ss 0.01f  Cz3 out\_z3 ss 0.01f  Cz4 out\_z4 ss 0.01f  Cz5 out\_z5 ss 0.01f  Cz6 out\_z6 ss 0.01f  Cz7 out\_z7 ss 0.01f  Xdecoder ndd 0 in\_a0 in\_a1 in\_a2 out\_z0 out\_z1 out\_z2 out\_z3 out\_z4 out\_z5 out\_z6 out\_z7 decoder  \*\*\*\*\*\* LOAD EXTERNAL FILES  .lib C:\synopsys\rf018.l TT  .include DECODER38.SP  .end |

**SIMULATION RESULTS**

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**USING COSMOSCOPE DIGITAL APPROXIMATION**

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