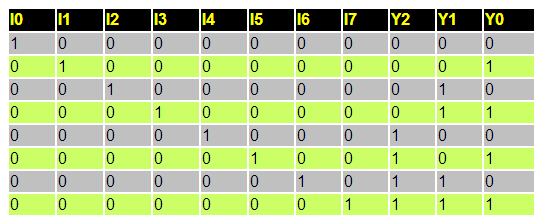
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

**8-3 ENCODER**

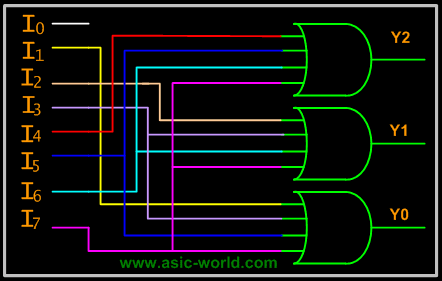
An encoder is a combinational circuit that performs the inverse operation of a decoder. If a device output code has fewer bits than the input code has, the device is usually called an encoder. e.g. 2n-to-n, priority encoders.

The simplest encoder is a 2n-to-n binary encoder, where it has only one of 2n inputs = 1 and the output is the n-bit binary number corresponding to the active input.

Octal-to-Binary take 8 inputs and provides 3 outputs, thus doing the opposite of what the 3-to-8 decoder does. At any one time, only one input line has a value of 1. The figure below shows the truth table of an Octal-to-binary encoder.



**Truth Table**



**Circuit Diagram**

**REQUIRED SUB CIRCUITS**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: INVERTER  .subckt not ndd nss in out  MN1 out in nss nss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in ndd ndd pch l='1\*LMIN' w='6\*LMIN'  .ends |

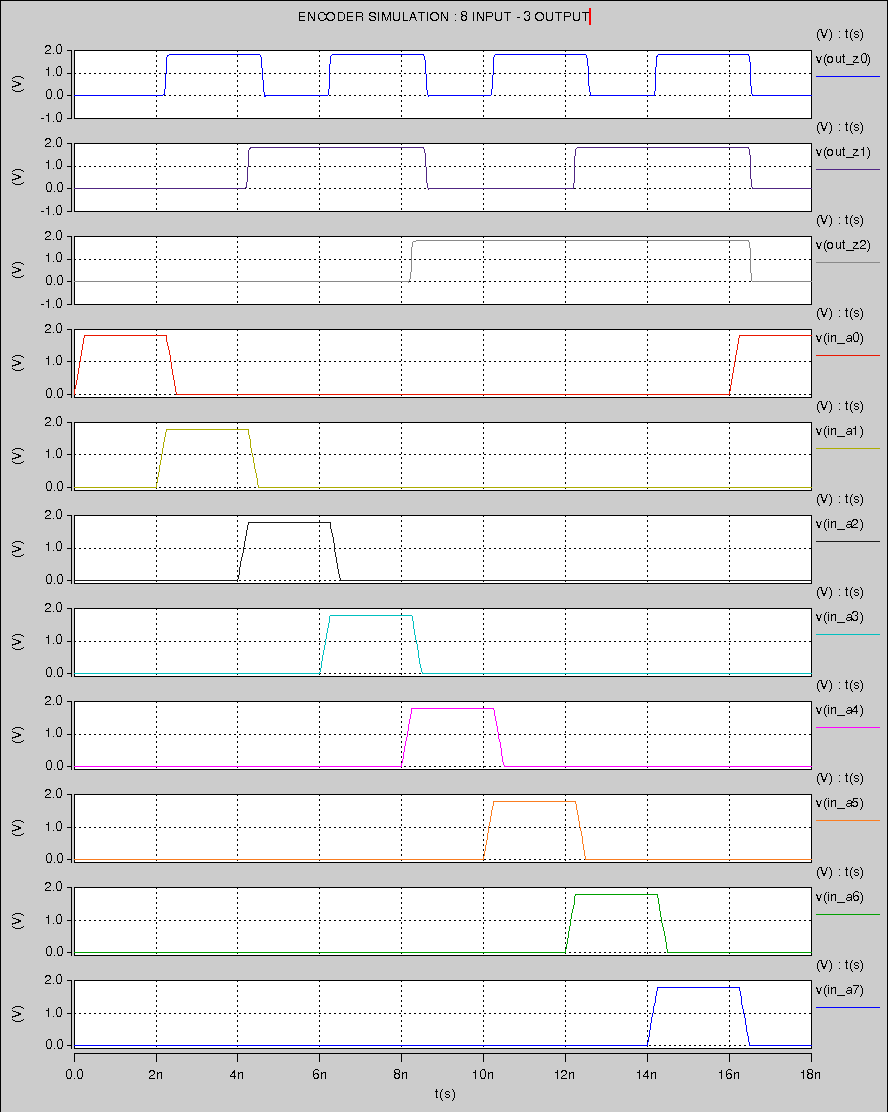
|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 4 INPUT NOR  .subckt nor4 dd ss a b c d out  MPA ab a dd dd pch l='1\*LMIN' w='6\*LMIN'  MPB bc b ab dd pch l='1\*LMIN' w='6\*LMIN'  MPC cd c bc dd pch l='1\*LMIN' w='6\*LMIN'  MPD out d cd dd pch l='1\*LMIN' w='6\*LMIN'    MNA out a ss ss nch l='1\*LMIN' w='2\*LMIN'  MNB out b ss ss nch l='1\*LMIN' w='2\*LMIN'  MNC out c ss ss nch l='1\*LMIN' w='2\*LMIN'  MND out d ss ss nch l='1\*LMIN' w='2\*LMIN'    .ends |

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 8-3 ENCODER  .include NOR4.SP  .include NOT.SP  .subckt encoder dd ss a0 a1 a2 a3 a4 a5 a6 a7 z0 z1 z2  Xnor4\_0 dd ss a1 a3 a5 a7 not\_z0 nor4  Xnor4\_1 dd ss a2 a3 a6 a7 not\_z1 nor4  Xnor4\_2 dd ss a4 a5 a6 a7 not\_z2 nor4  Xnot\_z0 dd ss not\_z0 z0 not  Xnot\_z1 dd ss not\_z1 z1 not  Xnot\_z2 dd ss not\_z2 z2 not  .ends |

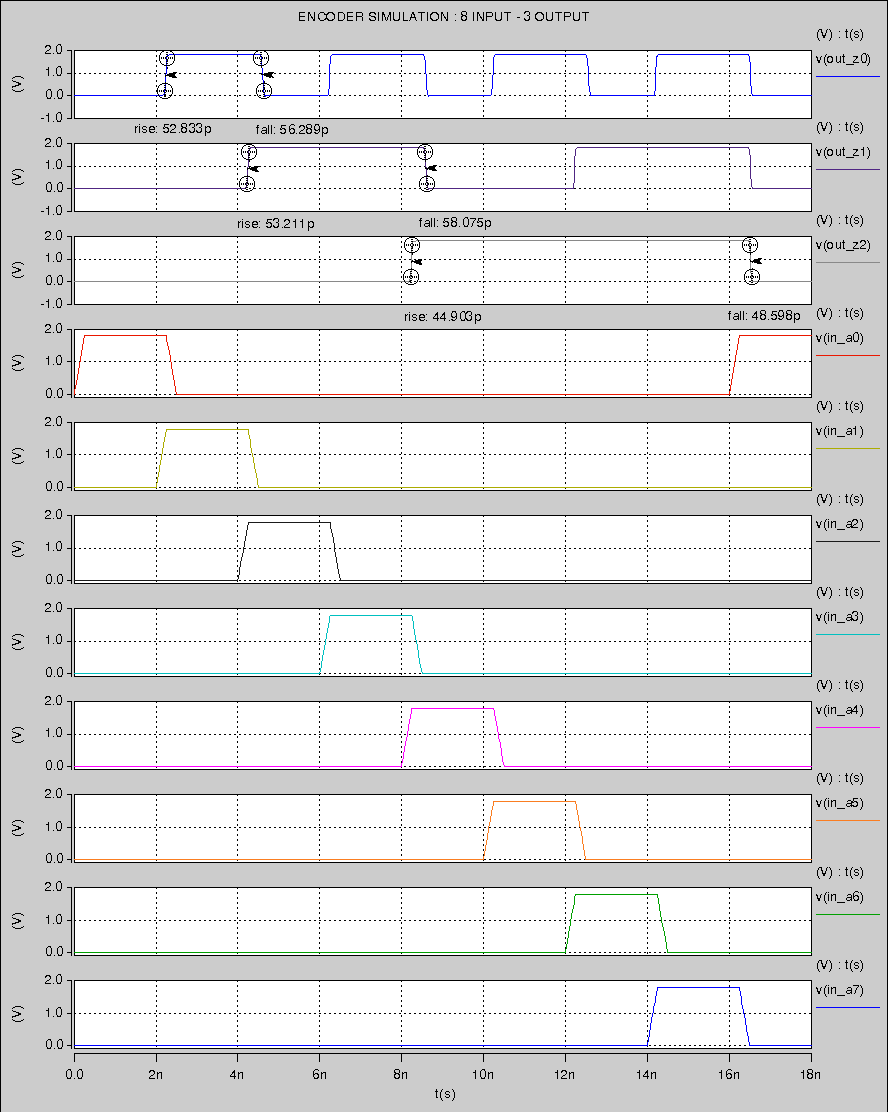
**TEST BENCH**

|  |
| --- |
| encoder 8-3  \*http://www.asic-world.com/digital/combo3.html  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  .PARAM MINTIME=2n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 'MINTIME\*9'  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va0 in\_a0 0 pulse ( 0 PVDD 0 TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va1 in\_a1 0 pulse ( 0 PVDD 'MINTIME\*1' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va2 in\_a2 0 pulse ( 0 PVDD 'MINTIME\*2' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va3 in\_a3 0 pulse ( 0 PVDD 'MINTIME\*3' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va4 in\_a4 0 pulse ( 0 PVDD 'MINTIME\*4' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va5 in\_a5 0 pulse ( 0 PVDD 'MINTIME\*5' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va6 in\_a6 0 pulse ( 0 PVDD 'MINTIME\*6' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  Va7 in\_a7 0 pulse ( 0 PVDD 'MINTIME\*7' TRAN\_TIME TRAN\_TIME MINTIME 'MINTIME\*8')  \*\*\*\*\*\* TEST BENCH CIRCUIT  Cz0 out\_z0 ss 0.01f  Cz1 out\_z1 ss 0.01f  Cz2 out\_z2 ss 0.01f  Xencoder ndd 0 in\_a0 in\_a1 in\_a2 in\_a3 in\_a4 in\_a5 in\_a6 in\_a7 out\_z0 out\_z1 out\_z2 encoder  \*\*\*\*\*\* LOAD EXTERNAL FILES  .lib C:\synopsys\rf018.l TT  .include ENCODER38.SP  .end |

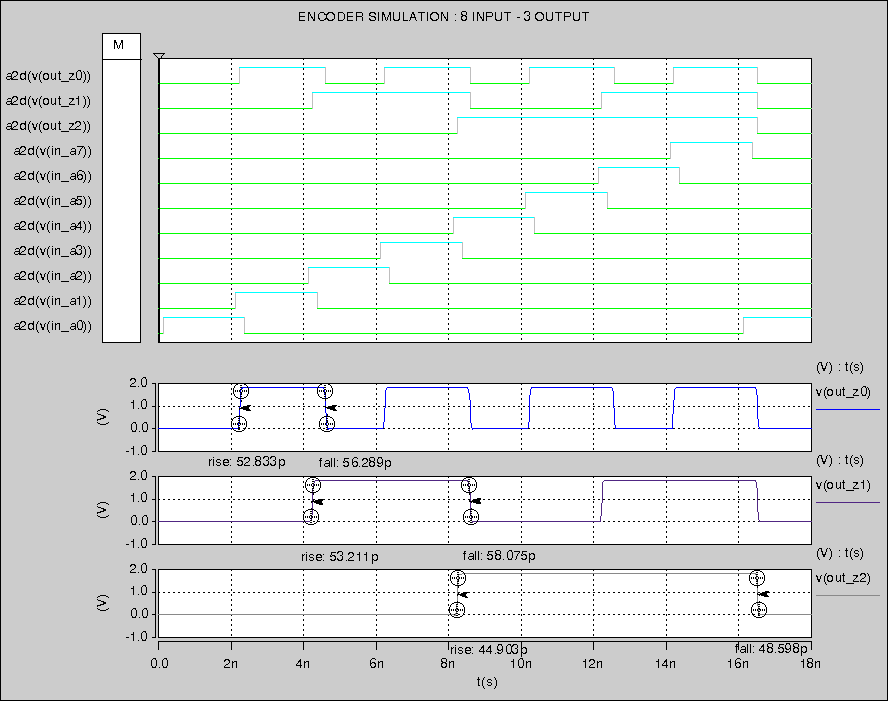
**SIMULATION RESULT**

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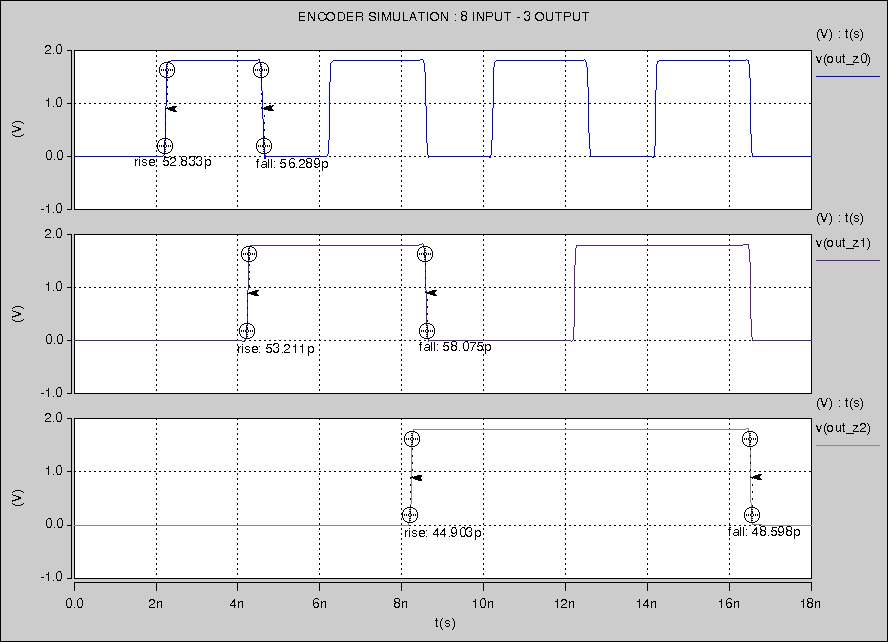
**SIMULATION RESULT WITH RISE TIME AND FALL TIME**

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**SIMULATION RESULT / APPROXIMATED DIGITAL VALUES USING COSMOSCOPE**

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**SIMULATION RESULT – CLOSE UP VIEW ON OUTPUT**

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