**GIL MICHAEL E. REGALADO BS ECE IV EE 272**

**TAKE HOME EXAM**

1. In this problem you are to compare the dc characteristics of PMOS and NMOS transistors when they are used as pull-up devices. Assume that the transistors are integrated in the NTPU Technology and that each has drawn channel length of 0.8 µm. The devices are to pull up a current source load of 2mA. Also, assume that VDD = +3.3V, that the PMOS transistor is driven with a gate voltage of 0V, and that the gate of the NMOS transistor is driven from a boosted supply voltage of +5V. You may neglect channel-length modulation, but do not ignore the body effect for the NMOS transistor.

For both the PMOS and NMOS devices, use hand calculations to determine the channel width, W, needed to pull the 2mA current source load up to 1.7V. Use Level 1 MOS models with KP modified to match the drain currents obtained with Level 3 models at |VGS| = |VDS| = 3V.

Solution

NMOS

Using level 1 enhancement MOSFET:

PMOS

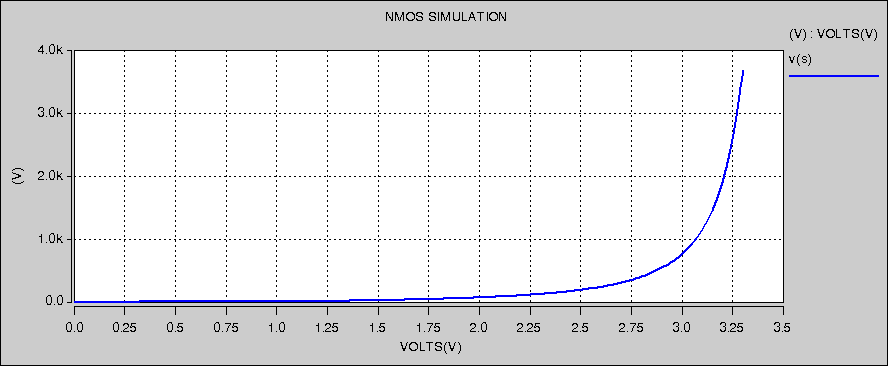
At saturation region:

Using level 1 enhancement MOSFET:

SIMULATION

|  |
| --- |
| NMOS Simulation  \* LEVEL 1 Enhancement NMOS  .model n1 nmos  + level=1  + vto=0.7  + kp=155u  + tox=100e-10  + gamma=0.624  + phi=0.83  + lambda=0.03  + ld=0.03u  + xj=0.2u  + uo=450  + tpg=1  + rsh=2  + js=3.22e-8  + nsub=1.4e17  + cj=1.1e-3  + cjsw=3e-10  + mj=0.5  + mjsw=0.25  + pb=0.976  + cgso=2e-10  + cgdo=2e-10  + cgbo=1.18e-10  m1 d g s 0 n1 w=1.9u l=0.8u  vdd d 0 3.3  vin g 0 5  cl s 0 10p  il 0 s 2m  .option post probe  .op  .dc vdd 0 3.3 0.01  .probe v(s)  .probe i1(m1)  .end |

**NMOS SIMULATION VOLTAGE VIEW USING COSMOSCOPE**



2. A CMOS inverter is integrated in the NTPU CMOS Technology with the drawn dimensions WP/LP = 4.8µm/0.6µm and WN/LN = 1.8µm/0.6µm. Assume that VDD = +3.3V and neglect channel length modulation.

a. Calculate the unity gain margins, UGML and UGMH, for the inverter. Use Level 1 MOS models modified to match the drain currents of the Level 3 models at |VGS| = |VDS| = 3V.

Solution:

The voltage at which the input and output voltages are equal is given by:

Unity Gain Noise Margins: