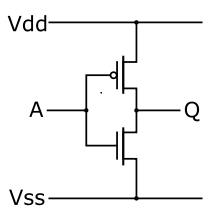
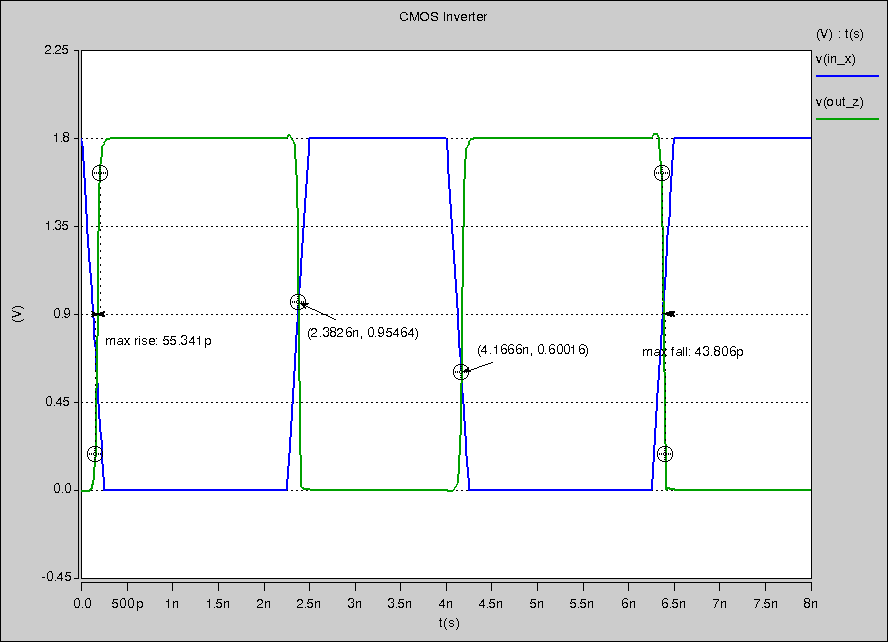
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

CMOS INVERTER GATE SIMULATION



|  |
| --- |
| \*\*\*\*\*\* FILENAME: inverter.cir  \*\*\*\*\*\* SUBCIRCUIT DEFINITION: INVERTER  .subckt inverter dd ss in out  MN1 out in ss ss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in dd dd pch l='1\*LMIN' w='3\*LMIN'  .ends |

|  |
| --- |
| \*\*\*\*\*\* FILENAME: inverter\_tb.sp  \*\*\*\*\*\* INVERTER TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 8n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Vin in\_x 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 2n 4n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  X\_inverter ndd 0 in\_x out\_z inverter  Cout out\_z 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib "C:\synopsys\rf018.l" TT  .include "inverter.cir"  .unprot  .end |



Rise Time: 55.341 ps

Fall Time: 43.806 ps

Input Rise Time Cross Over: 0.95464 Volts

Input Fall Time Cross Over: 0.6 Volts