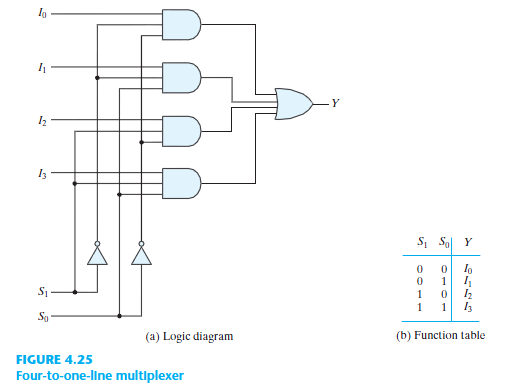
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

**4-1 MULTIPLEXER**

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**REQUIRED SUB CIRCUITS**

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| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 3 INPUT NAND  .subckt nand3 dd ss a b c out  MN1 out a ab ss nch l='1\*LMIN' w='2\*LMIN'  MN2 ab b bc ss nch l='1\*LMIN' w='2\*LMIN'  MN3 bc c ss ss nch l='1\*LMIN' w='2\*LMIN'  MP1 out a dd dd pch l='1\*LMIN' w='6\*LMIN'  MP2 out b dd dd pch l='1\*LMIN' w='6\*LMIN'  MP3 out c dd dd pch l='1\*LMIN' w='6\*LMIN'  .ends |

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| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 4 INPUT NOR  .subckt nor4 dd ss a b c d out  MPA ab a dd dd pch l='1\*LMIN' w='6\*LMIN'  MPB bc b ab dd pch l='1\*LMIN' w='6\*LMIN'  MPC cd c bc dd pch l='1\*LMIN' w='6\*LMIN'  MPD out d cd dd pch l='1\*LMIN' w='6\*LMIN'  MNA out a ss ss nch l='1\*LMIN' w='2\*LMIN'  MNB out b ss ss nch l='1\*LMIN' w='2\*LMIN'  MNC out c ss ss nch l='1\*LMIN' w='2\*LMIN'  MND out d ss ss nch l='1\*LMIN' w='2\*LMIN'    .ends |

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| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: INVERTER  .subckt not ndd nss in out  MN1 out in nss nss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in ndd ndd pch l='1\*LMIN' w='6\*LMIN'  .ends |

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| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 4-1 MULTIPLEXER  .include NOT.SP  .include NOR4.SP  .include NAND3.SP  .subckt mux dd ss a0 a1 a2 a3 s0 s1 z  Xnand3\_a0 dd ss a0 not\_s1 not\_s0 n0 nand3  Xnand3\_a1 dd ss a1 not\_s1 s0 n1 nand3  Xnand3\_a2 dd ss a2 s1 not\_s0 n2 nand3  Xnand3\_a3 dd ss a3 s1 s0 n3 nand3  xnot\_n0 dd ss n0 not\_n0 not  xnot\_n1 dd ss n1 not\_n1 not  xnot\_n2 dd ss n2 not\_n2 not  xnot\_n3 dd ss n3 not\_n3 not  xnot\_s0 dd ss s0 not\_s0 not  xnot\_s1 dd ss s1 not\_s1 not  xnor4 dd ss not\_n0 not\_n1 not\_n2 not\_n3 not\_z nor4    xnot\_z0 dd ss not\_z z not  .ends |

**TEST BENCH CIRCUIT**

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| 4 TO 1 MULTIPLEXER  \*\*\*\*\*\* REFERENCE:  \*\*\*\*\*\* http://www.asic-world.com/digital/combo3.html  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  .PARAM MINTIME=2n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 128n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va0 in\_a0 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Va1 in\_a1 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 4n 8n)  Va2 in\_a2 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 8n 16n)  Va3 in\_a3 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 16n 32n)  Vs0 in\_s0 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 32n 64n)  Vs1 in\_s1 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 64n 128n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Cz0 out\_z ss 0.01f  Xmux ndd 0 in\_a0 in\_a1 in\_a2 in\_a3 in\_s0 in\_s1 out\_z mux  \*\*\*\*\*\* LOAD EXTERNAL FILES  .lib C:\synopsys\rf018.l TT  .include MUX.SP  .end |

**SIMULATION RESULT**

