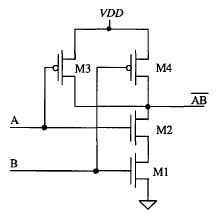
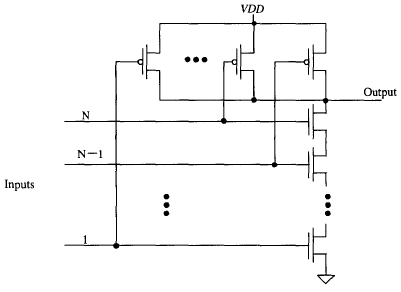
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

**CMOS NAND GATE SIMULATION**



2 INPUT CMOS NAND GATE



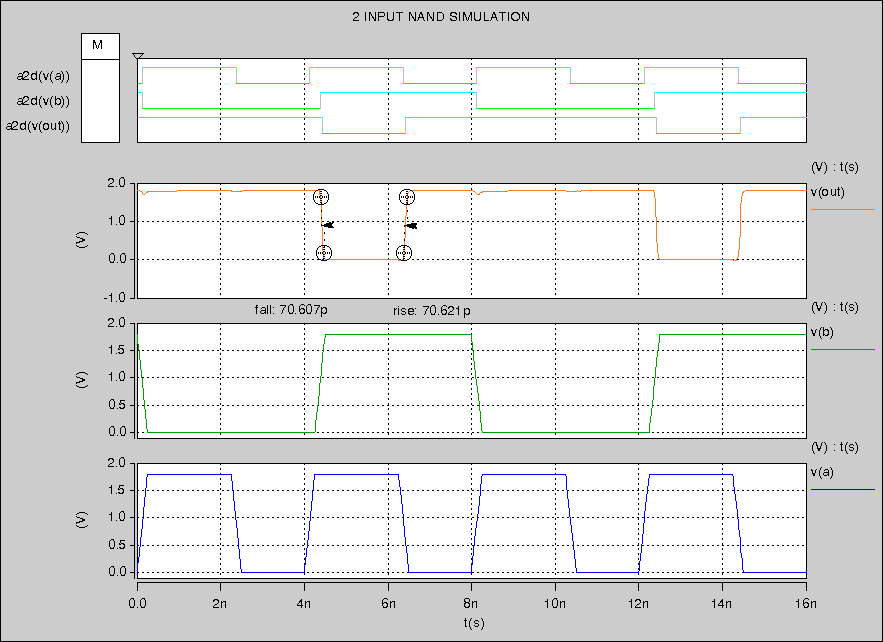
N-INPUT CMOS NAND GATE

**2 INPUT NAND SIMULATION**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 2 INPUT NAND  .subckt nand dd ss a b out  MN1 ab b ss ss nch l='1\*LMIN' w='2\*LMIN'  MN2 out a ab ss nch l='1\*LMIN' w='2\*LMIN'    MP3 out a dd dd pch l='1\*LMIN' w='6\*LMIN'  MP4 out b dd dd pch l='1\*LMIN' w='6\*LMIN'  .ends |

|  |
| --- |
| 2 INPUT NAND TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 16n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (0 PVDD 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Vb b 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 4n 8n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnand ndd 0 a b out nand  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib C:\synopsys\rf018.l TT  .include nand2.sp  .unprot  .end |

**SIMULATION RESULT**

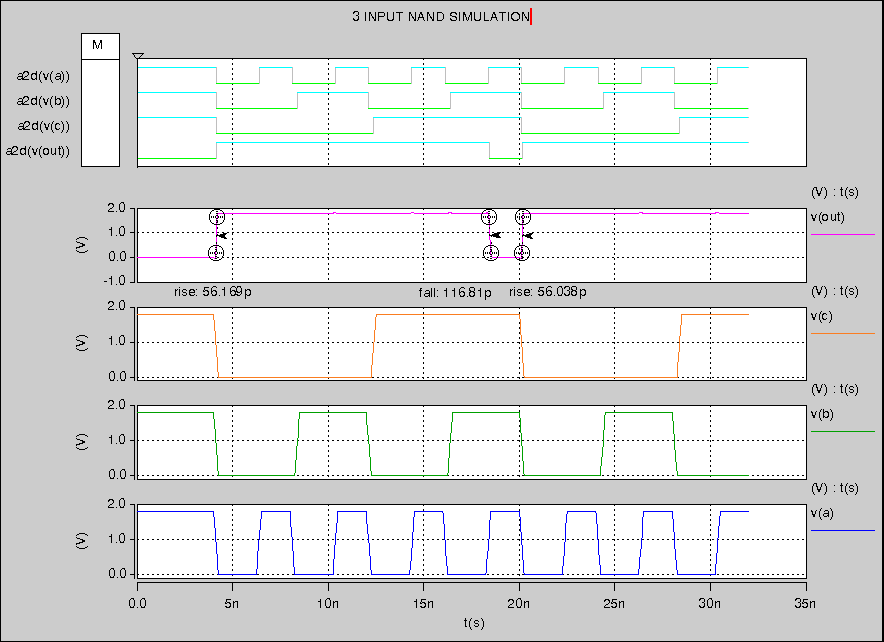


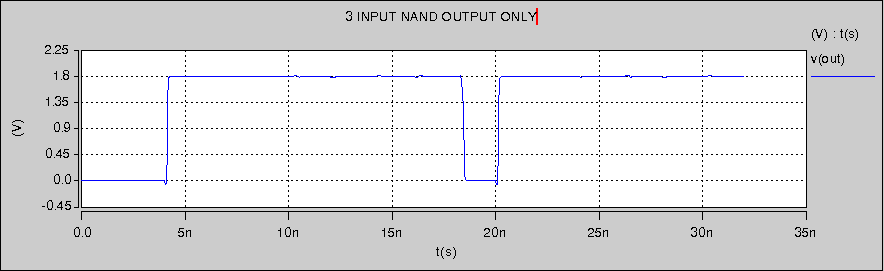
**3 INPUT NAND SIMULATION**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 3 INPUT NAND  .subckt nand3 dd ss a b c out  MN1 out a ab ss nch l='1\*LMIN' w='2\*LMIN'  MN2 ab b bc ss nch l='1\*LMIN' w='2\*LMIN'  MN3 bc c ss ss nch l='1\*LMIN' w='2\*LMIN'    MP1 out a dd dd pch l='1\*LMIN' w='6\*LMIN'  MP2 out b dd dd pch l='1\*LMIN' w='6\*LMIN'  MP3 out c dd dd pch l='1\*LMIN' w='6\*LMIN'  .ends |

|  |
| --- |
| 3 INPUT NAND TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 32n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (PVDD 0 4n TRAN\_TIME TRAN\_TIME 2n 4n )  Vb b 0 pulse (PVDD 0 4n TRAN\_TIME TRAN\_TIME 4n 8n )  Vc c 0 pulse (PVDD 0 4n TRAN\_TIME TRAN\_TIME 8n 16n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnand3 ndd 0 a b c out nand3  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib "C:\synopsys\rf018.l" TT  .include "nand3.sp"  .unprot  .end |

**SIMULATION RESULT**





**4 INPUT NAND SIMULATION**

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| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 4 INPUT NAND  .subckt nand4 dd ss a b c d out  MN1 out a ab ss nch l='1\*LMIN' w='2\*LMIN'  MN2 ab b bc ss nch l='1\*LMIN' w='2\*LMIN'  MN3 bc c cd ss nch l='1\*LMIN' w='2\*LMIN'  MN4 cd d ss ss nch l='1\*LMIN' w='2\*LMIN'    MP1 out a dd dd pch l='1\*LMIN' w='6\*LMIN'  MP2 out b dd dd pch l='1\*LMIN' w='6\*LMIN'  MP3 out c dd dd pch l='1\*LMIN' w='6\*LMIN'  MP4 out d dd dd pch l='1\*LMIN' w='6\*LMIN'  .ends |

|  |
| --- |
| 4 INPUT NAND TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 64n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 2n 4n )  Vb b 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 4n 8n )  Vc c 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 8n 16n)  Vd d 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 16n 32n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnand4 ndd 0 a b c d out nand4  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib "C:\synopsys\rf018.l" TT  .include "nand4.sp"  .unprot  .end |

**SIMULATION RESULT**

