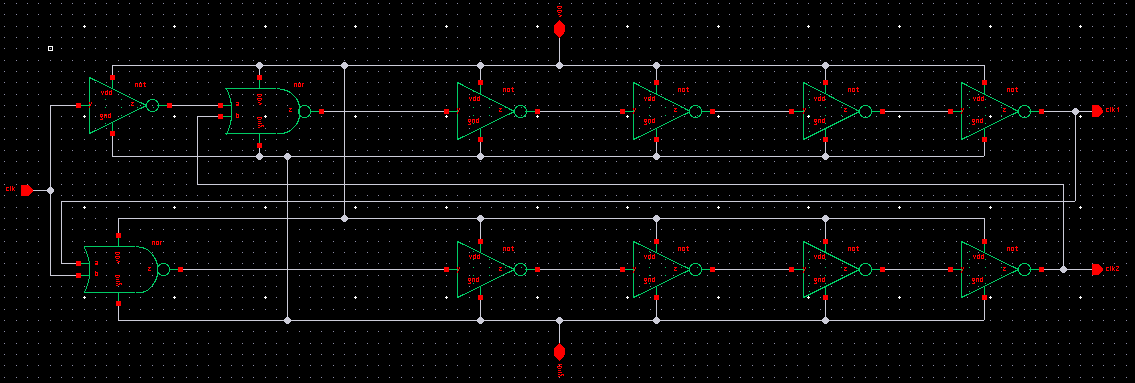
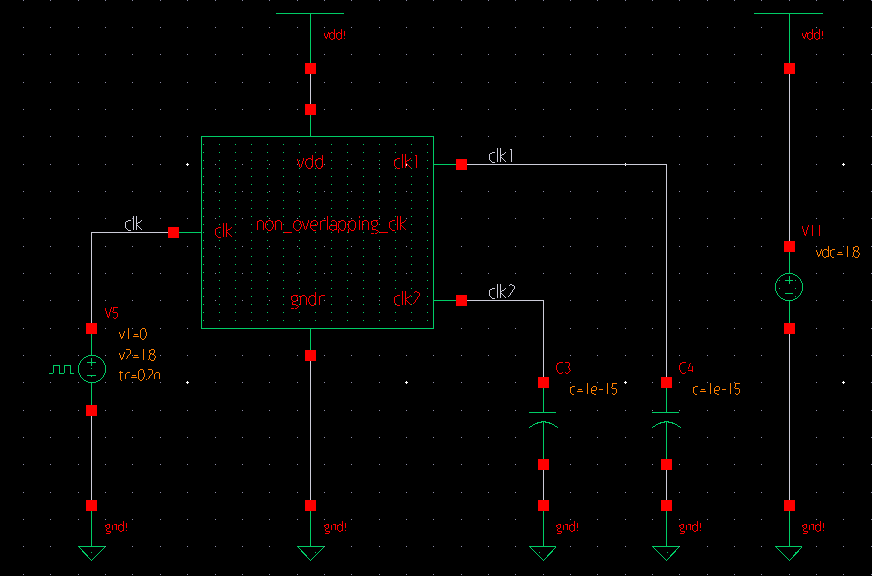
**GIL MICHAEL E. REGALADO BS ECE IV EE 272**

**LABORATORY #7 NONOVERLAPPING CLOCK**

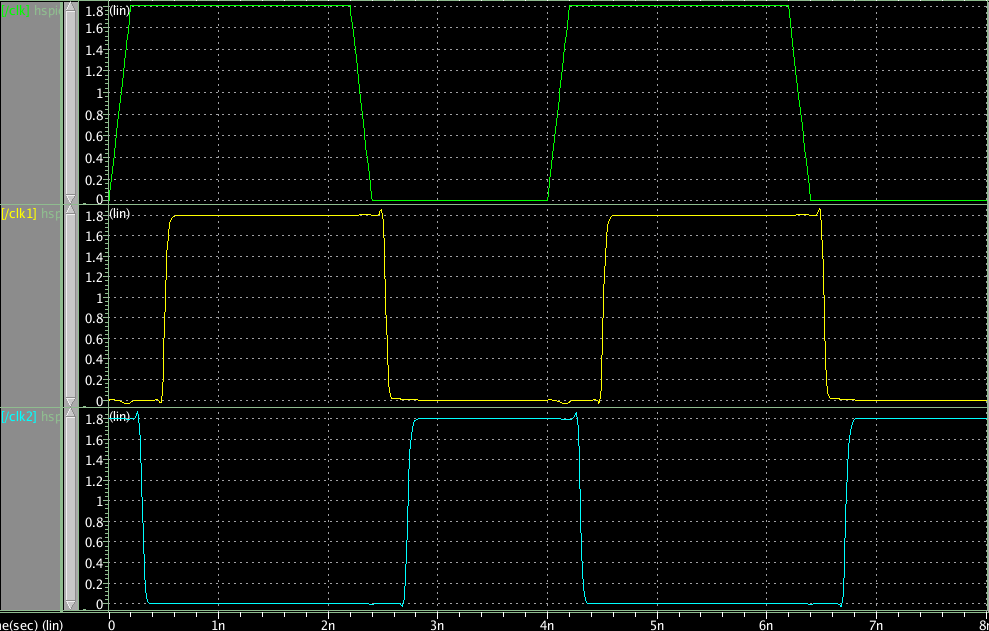
SCHEMATIC

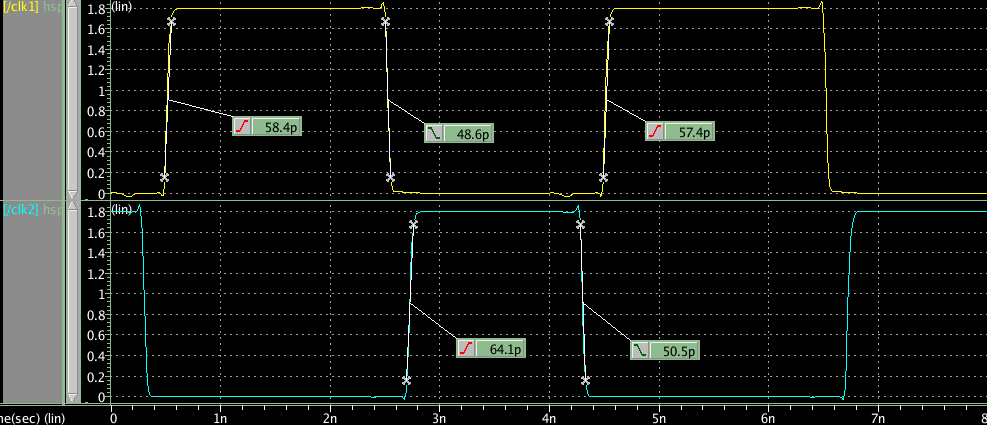


TEST BENCH



SIMULATION





This NOR-flipflop based circuit implements a non-overlapping two-phase clock signal generator and can be used to derive a two-phase clock signal from a single and possibly non-symmetrical clock signal.