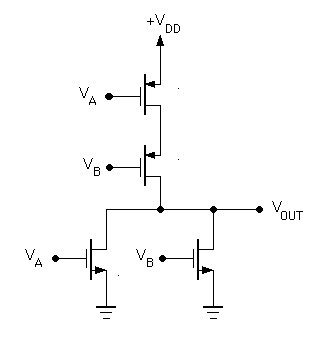
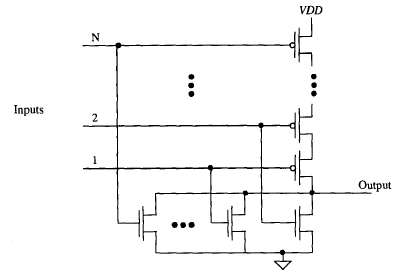
**GIL MICHAEL E. REGALADO BS ECE IV - EE 272**

**CMOS NOR GATE SIMULATION**



2 INPUT NOR



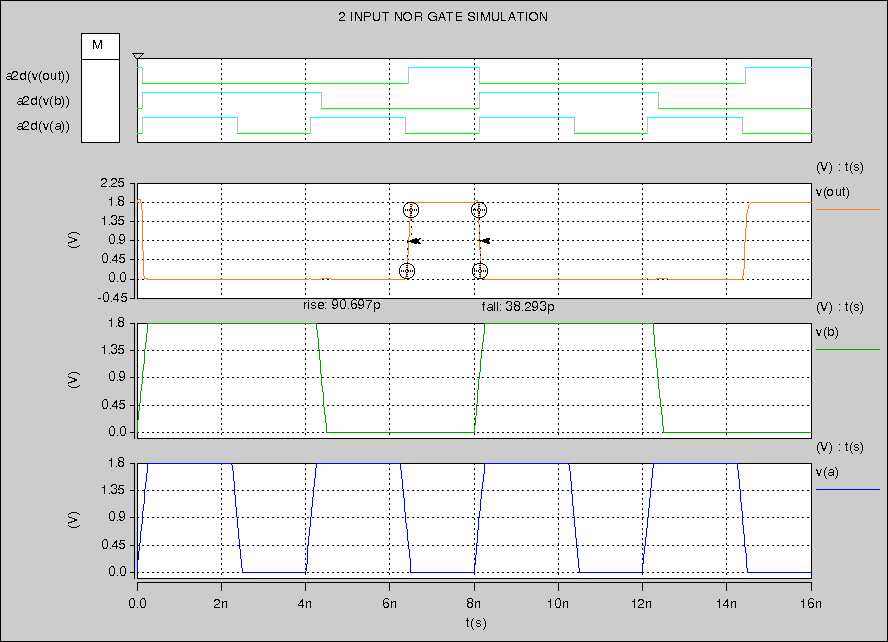
N-INPUT NOR

**2 INPUT NOR SIMULATION**

|  |
| --- |
| \*\*\*\*\*\* nor2.sp  \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 2 INPUT NOR  .subckt nor2 dd ss a b out  MPA ab a dd dd pch l='1\*LMIN' w='6\*LMIN'  MPB out b ab dd pch l='1\*LMIN' w='6\*LMIN'  MNA out a ss ss nch l='1\*LMIN' w='2\*LMIN'  MNB out b ss ss nch l='1\*LMIN' w='2\*LMIN'  .ends |

|  |
| --- |
| 2 INPUT NOR TEST BENCH  \*\*\*\*\*\* nor2\_tb.sp  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 16n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (0 PVDD 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Vb b 0 pulse (0 PVDD 0 TRAN\_TIME TRAN\_TIME 4n 8n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnor2 ndd 0 a b out nor2  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib C:\synopsys\rf018.l TT  .include nor2.sp  .unprot  .end |

**SIMULATION RESULT**

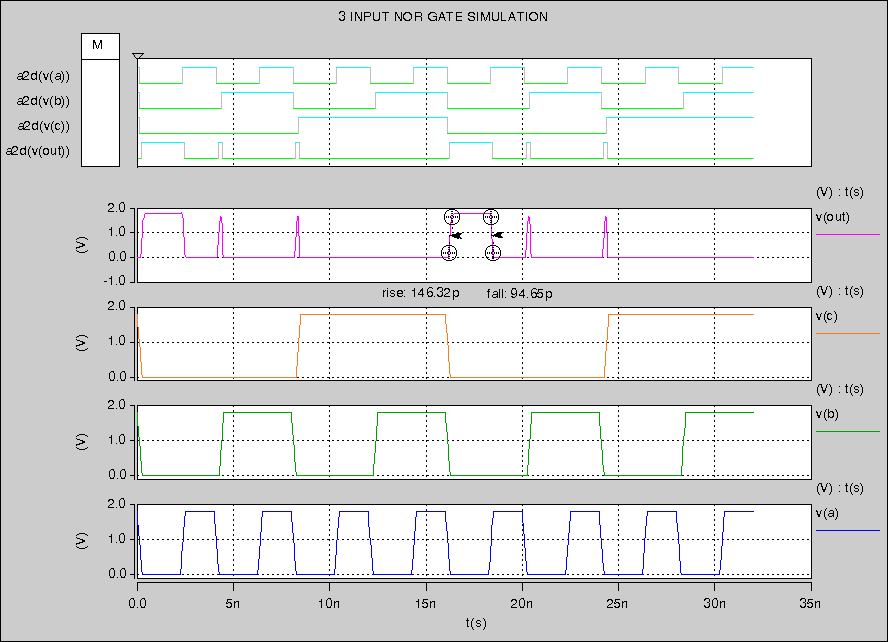


**3 INPUT NOR SIMULATION**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 2 INPUT NOR  .subckt nor2 dd ss a b out  MPA ab a dd dd pch l='1\*LMIN' w='6\*LMIN'  MPB out b ab dd pch l='1\*LMIN' w='6\*LMIN'  MNA out a ss ss nch l='1\*LMIN' w='2\*LMIN'  MNB out b ss ss nch l='1\*LMIN' w='2\*LMIN'  .ends |

|  |
| --- |
| 2 INPUT NOR TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 16n  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (0 PVDD 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Vb b 0 pulse (0 PVDD 0 TRAN\_TIME TRAN\_TIME 4n 8n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnor2 ndd 0 a b out nor2  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib C:\synopsys\rf018.l TT  .include nor2.sp  .unprot  .end |

**SIMULATION RESULT**



**4 INPUT NOR SIMULATION**

|  |
| --- |
| \*\*\*\*\*\* SUBCIRCUIT DEFINITION: 4 INPUT NOR  .subckt nor4 dd ss a b c d out  MPA ab a dd dd pch l='1\*LMIN' w='6\*LMIN'  MPB bc b ab dd pch l='1\*LMIN' w='6\*LMIN'  MPC cd c bc dd pch l='1\*LMIN' w='6\*LMIN'  MPD out d cd dd pch l='1\*LMIN' w='6\*LMIN'    MNA out a ss ss nch l='1\*LMIN' w='2\*LMIN'  MNB out b ss ss nch l='1\*LMIN' w='2\*LMIN'  MNC out c ss ss nch l='1\*LMIN' w='2\*LMIN'  MND out d ss ss nch l='1\*LMIN' w='2\*LMIN'    .ends |

|  |
| --- |
| 4 INPUT NOR TEST BENCH  \*\*\*\*\*\* SIMULATION PARAMETERS  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  \* Input transition time.  .PARAM TRAN\_TIME=0.25n  \*\*\*\*\*\* ANALYSIS OPTIONS  .option post  .op  .tran 1e-15 '32n + (8\*TRAN\_TIME)'  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Va a 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 2n 4n)  Vb b 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 4n 8n)  Vc c 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 8n 16n)  Vd d 0 pulse (PVDD 0 0 TRAN\_TIME TRAN\_TIME 16n 32n)  \*\*\*\*\*\* TEST BENCH CIRCUIT  Xnor4 ndd 0 a b c d out nor4  Cout out 0 0.01f  \*\*\*\*\*\* LOAD EXTERNAL FILES  .prot  .lib C:\synopsys\rf018.l TT  .include nor4.sp  .unprot  .end |

**SIMULATION RESULT**

