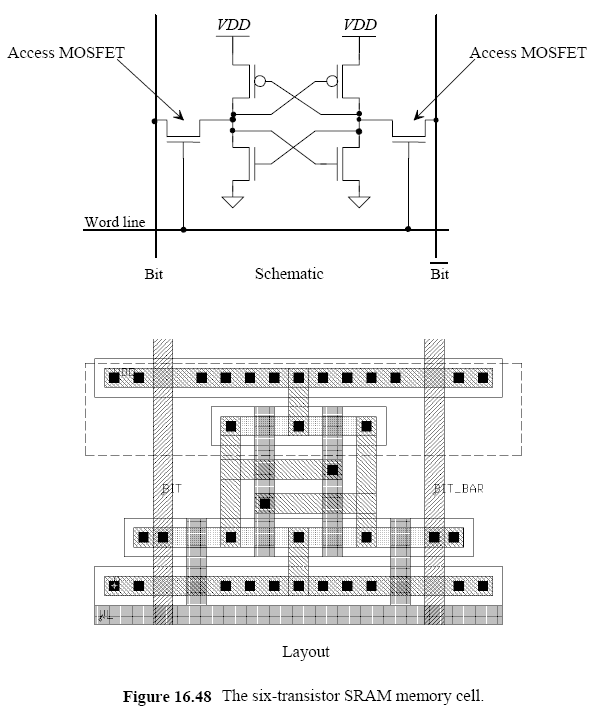
**GIL MICHAEL E. REGALADO BS-ECE IV**

**SRAM**



IN\_BB

IN\_BN

OUT\_BN

OUT\_BB

MP1

MN1

MN2

MN4

MN3

MP2

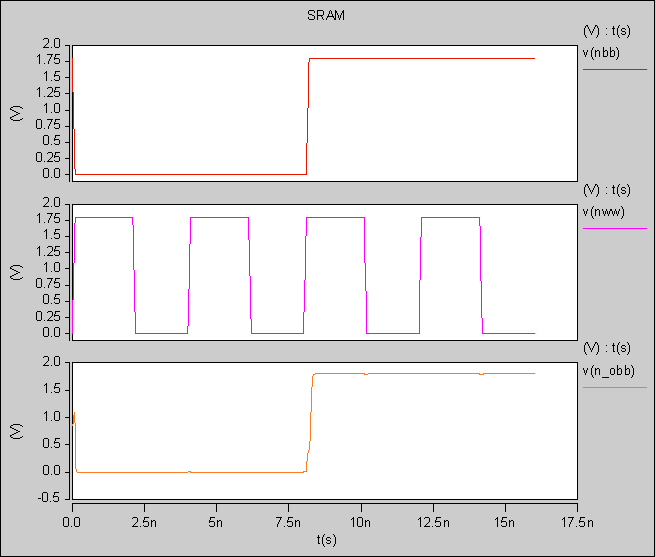
1. Simulate the operation of the SRAM cell seen in figure above. Use the 0.18 um process.
2. Simulate a 1x2-bit memory composed of 2 cells (refer to the figure above). The block diagram is shown below.



SINGLE SRAM CELL

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| --- |
| SRAM SINGLE CELL SIMULATION  \*\*\*\*\*\* PARAMETER DEFINITION  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  .PARAM RFTIME=0.1n  \*\*\*\*\*\* ANALYSIS PARAMTERS  .option post  .op  .tran 1e-12 '16n'  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  Vin\_bb nbb 0 pulse (PVDD 0 0 RFTIME RFTIME 8n 16n)  Vin\_ww nww 0 pulse (0 PVDD 0 RFTIME RFTIME 2n 04n)  Co\_bb n\_obb 0 1f  Co\_bn n\_obn 0 1f  \*\*\*\*\*\* MAIN CIRCUIT : SINGLE SRAM CELL SIMULATION  X\_sram\_cell ndd 0 nww nbb n\_obb n\_obn sram\_cell  \*\*\*\*\*\* SRAM CELL  .subckt sram\_cell dd ss ww bb obb obn  x\_inverter dd ss bb bn inverter  MP1 obb obn dd dd pch l=LMIN w='6\*LMIN'  MP2 obn obb dd dd pch l=LMIN w='6\*LMIN'  MN1 obb obn ss ss nch l=LMIN w='2\*LMIN'  MN2 obn obb ss ss nch l=LMIN w='2\*LMIN'  MN4 bb ww obb ss nch l=LMIN w='3\*LMIN'  MN3 bn ww obn ss nch l=LMIN w='3\*LMIN'  .ends  \*\*\*\*\*\* INVERTER CELL  .subckt inverter ndd nss in out  MN1 out in nss nss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in ndd ndd pch l='1\*LMIN' w='6\*LMIN'  .ends  \*\*\*\*\*\* LIBRARY  .prot  .lib "C:\synopsys\rf018.l" TT  .unprot  .end |

SRAM SINGLE CELL SIMULATION RESULT

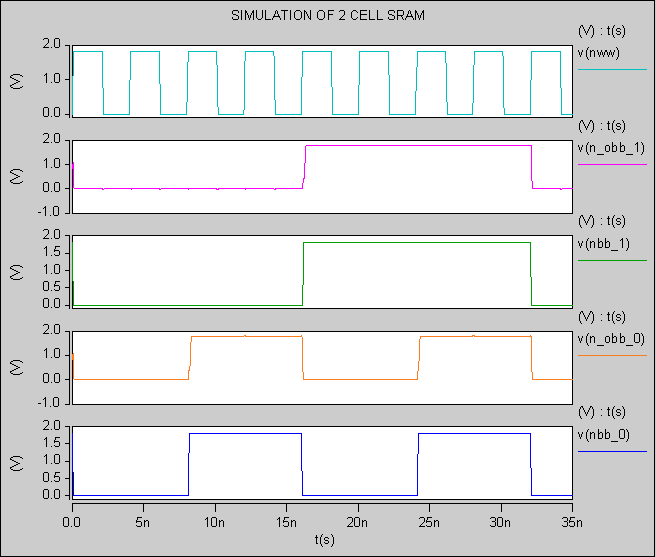


Synchronised with the World Line clock, the output follows the input for the respective pins.

SRAM WITH 2 CELLS SIMULATION

|  |
| --- |
| SRAM 2 CELL SIMULATION  \*\*\*\*\*\* PARAMETER DEFINITION  .PARAM LMIN=0.18u  .PARAM PVDD=1.8  .PARAM RFTIME=0.1n  \*\*\*\*\*\* ANALYSIS PARAMTERS  .option post  .op  .tran 1e-12 '35n'  \*\*\*\*\*\* STIMULI  Vdd ndd 0 PVDD  \*\* INPUTS FOR SRAM\_CELL\_0  Vin\_bb\_0 nbb\_0 0 pulse (PVDD 0 0 RFTIME RFTIME 08n 16n)  \*\* INPUTS FOR SRAM\_CELL\_1  Vin\_bb\_1 nbb\_1 0 pulse (PVDD 0 0 RFTIME RFTIME 16n 32n)  Vin\_ww nww 0 pulse (0 PVDD 0 RFTIME RFTIME 02n 04n)  \*\* CAPS FOR SRAM\_CELL\_0 OUTPUT  Co\_bb\_0 n\_obb\_0 0 1f  Co\_bn\_0 n\_obn\_0 0 1f  \*\* CAPS FOR SRAM\_CELL\_1 OUTPUT  Co\_bb\_1 n\_obb\_1 0 1f  Co\_bn\_1 n\_obn\_1 0 1f  \*\*\*\*\*\* MAIN CIRCUIT : SINGLE SRAM CELL SIMULATION  X\_sram\_cell\_0 ndd 0 nww nbb\_0 n\_obb\_0 n\_obn\_0 sram\_cell  X\_sram\_cell\_1 ndd 0 nww nbb\_1 n\_obb\_1 n\_obn\_1 sram\_cell  \*\*\*\*\*\* SRAM CELL  .subckt sram\_cell dd ss ww bb obb obn  x\_inverter dd ss bb bn inverter  MP1 obb obn dd dd pch l=LMIN w='6\*LMIN'  MP2 obn obb dd dd pch l=LMIN w='6\*LMIN'  MN1 obb obn ss ss nch l=LMIN w='2\*LMIN'  MN2 obn obb ss ss nch l=LMIN w='2\*LMIN'  MN4 bb ww obb ss nch l=LMIN w='3\*LMIN'  MN3 bn ww obn ss nch l=LMIN w='3\*LMIN'  .ends  \*\*\*\*\*\* INVERTER CELL  .subckt inverter ndd nss in out  MN1 out in nss nss nch l='1\*LMIN' w='2\*LMIN'  MP2 out in ndd ndd pch l='1\*LMIN' w='6\*LMIN'  .ends  \*\*\*\*\*\* LIBRARY  .prot  .lib "C:\synopsys\rf018.l" TT  .unprot  .end |

SIMULATION RESULTS



For the SRAM\_CELL\_0

Input: nbb\_0

Output: n\_obb\_0

For the SRAM\_CELL\_1

Input: nbb\_1

Output: n\_obb\_1

SUMMARY

The output of the SRAM cell follows the input synchronized by the Word Line posedge. If the World Line is low the value in the input bit is kept in memory on the main SRAM cell.