**GIL MICHAEL E. REGALADO BS ECE IV EE 272**

**COMPILATION OF LAB ACTIVITIES IN EE 272**

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| **RS FLIP FLOP** |  |
| **D-LATCH** |  |
| **NAND GATE 2, 3 AND 4 INPUT (REDESIGNED)** |  |
| **NOR GATE 2, 3, AND 4 INPUT (REDESIGNED)** |  |
| **CMOS TRANSMISSION GATE** |  |
| **LEVEL SHIFTER (UP AND DOWN)** |  |
| **NON OVERLAPPING CLOCK** |  |
| **SRAM** | **A+** |
| **NP LOGIC** | **A+** |
| **DOMINO LOGIC AND 2 INPUTS** | **A+** |
| **3-8 DECODER** | **B-** |
| **8-3 ENCODER** | **A-** |
| **4-1 MULTIPLEXER** | **A-** |
| **CMOS INVERTER** | **A-** |