Homework 3
COM S 352
Fall 2021

1. (10 points) For each of the following memory allocation schemes explain why it experiences external fragmentation or internal fragmentation.

a. Base and bounds
b. Segmentation
c. Paging

2. (10 points) For each of the following virtual addresses, compute the page number and offset when using 4KB pages.

a. 22,000
b. 77,056
c. 197,012

3. (10 points) A cache hit rate is the number of hits divided by total accesses. Assume a computer keeps its page tables in main memory. The average overhead required for reading an entry from the page table is 51ns. To reduce this overhead, the computer has a TLB, which holds 32 page table entries, and can do a look up in 1ns. What hit rate is needed to reduce the mean overhead to 2ns?

4. (15 points) Consider the following function.

```
/**
 * Find the sum of all elements of an array.
 *
 * Parameters:
 * array – an array of integers
 * size – the size of the array
 **/
int sum(int *array, int size) {
     int total = 0;
     for (int i=0; i<size; i++) {
          total += arr[i];
     }
     return total;
}
```

Assume the program instructions for executing the function fit on one page and the stack fits on one page. Assume an int takes 4 bytes of memory, the page size is 4KB, the TLB has 32 entries, and the TLB uses a LRU replacement policy. Suppose the function is called with an array (which is not stored on the stack) of size 4,096, compute the number of TLB misses assuming the TLB is initially empty.

5. (15 points) On some systems, virtual and physical addresses are different sizes. Consider a small embedded system with a virtual address space of 4,096 pages and a 2KB page size. The physical memory has a maximum capacity of 1,024 frames.

a. How many bits are required for addresses in the virtual address space?
b. How many bits are required for addresses in physical memory?

6. (15 points) The following is a TBL cache and page table for a system with 2KB pages. The TLB Cache is the type that only hold entries for a single process.

TLB Cache

VPN	PFN	Valid	Dirty
5	7	1	1
6	11	1	1
1	4	1	0
4	0	0	0

Page Table

VPN	PFN	Valid	Present	Dirty
0	1	1	1	1
1	4	1	1	0
2	0	1	0	0
3	0	0	0	0
4	0	0	0	0
5	7	1	1	1
6	11	1	1	1

For each of the following virtual memory operations performed by a program, indicate all of the following that occur: TLB Cache miss, page fault, segmentation fault or dirty bit changed

a. Read from address 1,000
b. Write to address 2,950
c. Read from address 7,800
d. Write to address 5,025

7. (15 points) Consider the following page reference string:
2, 7, 1, 2, 1, 5, 2, 1, 7, 1, 5

Assuming paging with three frames, how many page faults would occur for the following replacement policies? You must show your work (i.e., create a table similar to either the book or lecture notes that shows the contents of memory after every reference).

a. Optimal replacement
b. FIFO replacement
c. LRU replacement

8. (10 points) What is the cause of thrashing? How does the system detect thrashing? Once it detects thrashing, what can the system do to eliminate this problem?