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1.

a. Base and bound is only one continuous segment. So it cannot cause external fragmentation or internal fragmentation.

b. When processes are loaded and removed, the free memory space is broken into segments of many different sizes, causing External fragmentation.

c. Paging divides physical memory into frames with fixed size. So it cannot be external fragmentation. But there is some empty space in the last page. It causes internal fragmentation.

2.

$4KB = 2^2.2^{10}B = 4096B = 2^{12}B$

a.

22,000

Page number=$\frac{22000}{4\,KB/Page}$= $\frac{22000}{4*2^{10B}/Page}$ = 5

Offset = 22000-5*4096=1520

b.

77056

Page number=$\frac{77056}{4\,KB/Page}$= $\frac{77056}{4*2^{10B}/Page}$ = 18

Offset = 77056-18*4096=3328

c.

197012

Page number=$\frac{197012}{4\,KB/Page}$= $\frac{197012}{4*2^{10B}/Page}$ = 48

Offset = 197012-48*4096=404

3.

Let call TLB hit ratio h then

2 = h x 1 + (1-h)(1+51)

h = 0.98

Need 0.98 hit rate to reduce the mean overhead to 2ns.

4.

Need 2 TLB entries for executing the function(1 page) and the stack(1 page).

Each element is 4 bytes, so 1024 elements is 1 page.

Arr[0] .. Arr[1023] -> page 0

Arr[1024] .. Arr[2047] -> page 1

Arr[2048] .. Arr[3071] -> page 2

Arr[3072] .. Arr[4095] -> page 3

→ 4 TLB misses

The total number of TLB misses is 6.

5.

Virtual address space of 4096 bytes need 12 bits

Page size is 2KB. It take 11 bites.

1024 frames requires 10 bits

a. (12+11) = 23 bits required for addresses in the virtual address space
b. (10+11) = 21 bits required for address in physical memory

6.

2KB pages use 11 bits. Because VPN maximum is 6, so we need 3 bits for VPN and 11 bits for offset.

a. Read from address 1000

1000 = 0b00001111101000→VPN 0→PFN 1, offset is 1000, TLB cache miss (6-1-4-0), it's present and valid to read.

b. Write to address 2950

2950=0b00101110000110→VPN 1→PFN 4, offset is 902, page already is in TLB cache, it's present and valid to write, Dirty bit changes to 1.

c. Read from address 7800

7800=0b01111001111000→VPN 3→PFN 0, offset is 1656, It's not valid, segmentation fault.

d. Write to address 5025

5025=0b01001110100001 → VPN 2 → PFN 0, offset is 929, It's valid but not present, page fault.

7. page string: 2, 7, 1, 2, 1, 5, 2, 1, 7, 1, 5

a. OTP

Access	Hit/Miss?	Evict	Resulting Cache State
2	Miss		2
7	Miss		2,7
1	Miss		2,7,1
2	Hit		2,7,1
1	Hit		2,7,1
5	Miss	7	2,5,1
2	Hit		2,5,1
1	Hit		2,5,1
7	Miss	2	7,5,1
1	Hit		7,5,1
5	Hit		7,5,1

b. FIFO

Access	Hit/Miss?	Evict	Resulting Cache State
2	Miss		First in-> 2
7	Miss		First in-> 2,7
1	Miss		First in-> 2,7,1
2	Hit		First in-> 2,7,1
1	Hit		First in-> 2,7,1
5	Miss	2	First in-> 7,1,5
2	Miss	7	First in-> 1,5,2
1	Hit		First in-> 1,5,2
7	Miss	1	First in-> 5,2,7
1	Miss	5	First in-> 2,7,1
5	Miss	2	First in->

			7,1,5

c. LRU

Access	Hit/Miss?	Evict	Resulting Cache State
2	Miss		LRU-> 2
7	Miss		LRU-> 2,7
1	Miss		LRU-> 2,7,1
2	Hit		LRU-> 7,1,2
1	Hit		LRU-> 7,2,1
5	Miss	7	LRU-> 2,1,5
2	Hit		LRU-> 1,5,2
1	Hit		LRU-> 5,2,1
7	Miss	5	LRU-> 2,1,7
1	Hit		LRU-> 2,7,1
5	Miss	2	LRU-> 7,1,5

8.

The problem is caused by the process allocating the minimum number of pages required by a process, forcing page fault. Thrashing can be detected by evaluating CPU usage versus multi-programming. It can be eliminated by reducing the degree of multi-programming.