

C3: Nivelul de achizitie si control: Achizitia datelor si controlul parametrilor. Notiunea de timp real. Cracteristicile sistemelor de timp real. Sisteme hardware si software de timp real. Structura aplicatiilor software de achizitie si reglare.

Cuprins:

- Introducere – Functii
- Achizitia datelor
- Notiunea de timp real
- Structura software a aplicatiilor de timp real
- Arhitecturi hardware si software de timp real
- Algoritmi de control
- Alte exemple



C3: Nivelul de achizitie si control

1. Introducere – Functii

Achizitie (Level 1):

- Conexiune traductoare/elemente de executie
- Filtrare
- Conversie AD/DA
- Multiplexare
- Formatare/prelucrare date
- Transfer de date
- Stocare partiala date
- (Auto)diagnoza

Control (Level 2):

- Timp real
- Algoritmi de reglare
- Configurare
- (Auto)acordare
- Rulare programe
- Comunicatie
- (Auto)Diagnoza

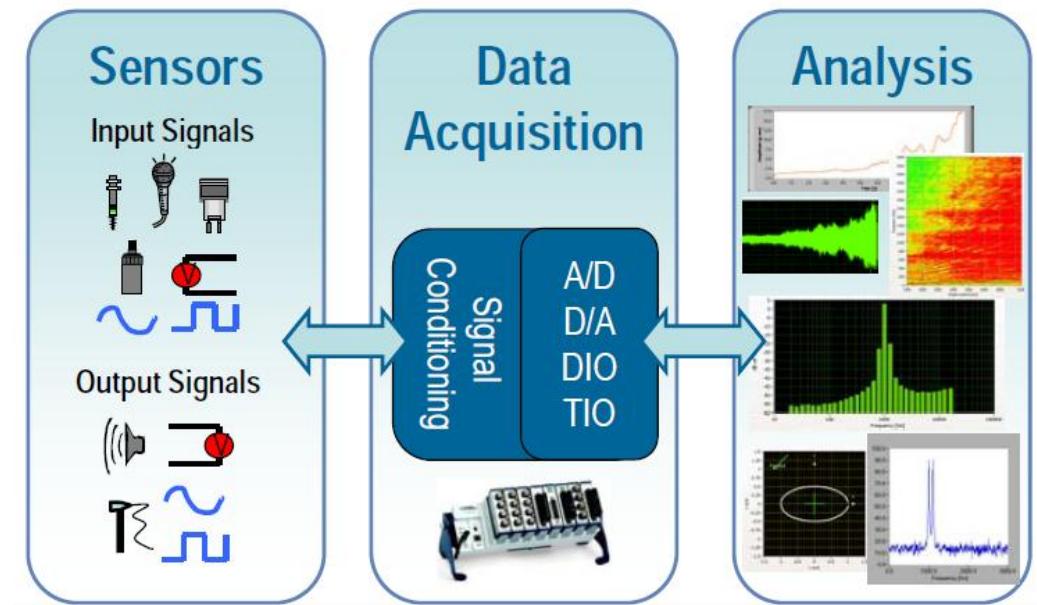
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2. Achizitia datelor

Parametri:

- a) AI
- b) AO
- c) DI
- d) DO
- e) Counter
- f) Deformare
- g) Acceleratie
- h) Video

Etc.



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2. Achizitia datelor

Tip semnale:

Digitale:

- 0 – 5 V (TTL)
- 0 – 24 V (industrial)
- 0 – 110 V (0 – 220 V)

Etc.

Analogice:

- -10 – 10 V (0 – 10 V, -5 – 5 V)
- 4 – 20 mA (0 – 20 mA)(industrial)
- 2 – 10 mA

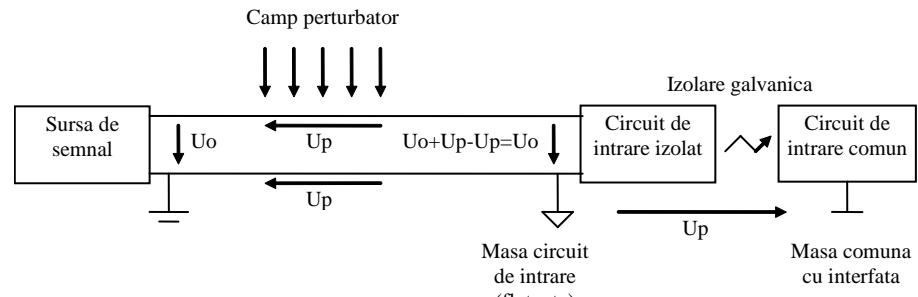
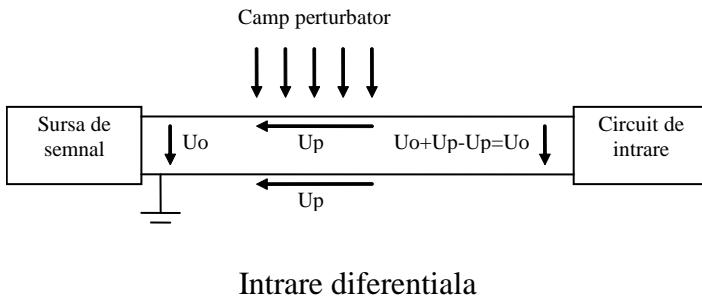
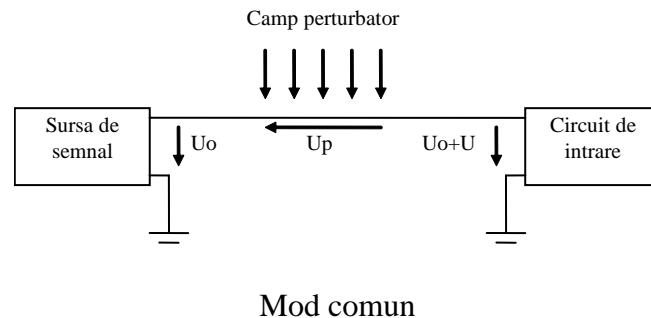
Etc.

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2. Achizitia datelor

Tip conexiune (AI):

- Mod comun
- Intrare diferentiala
- Izolare galvanica



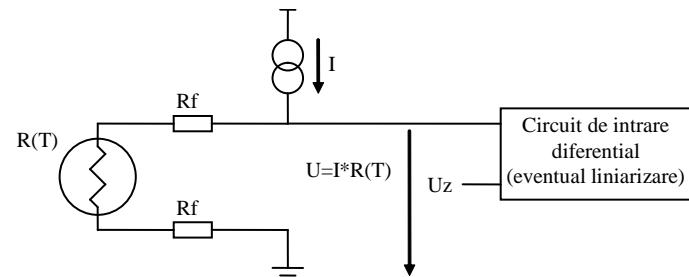
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2. Achizitia datelor

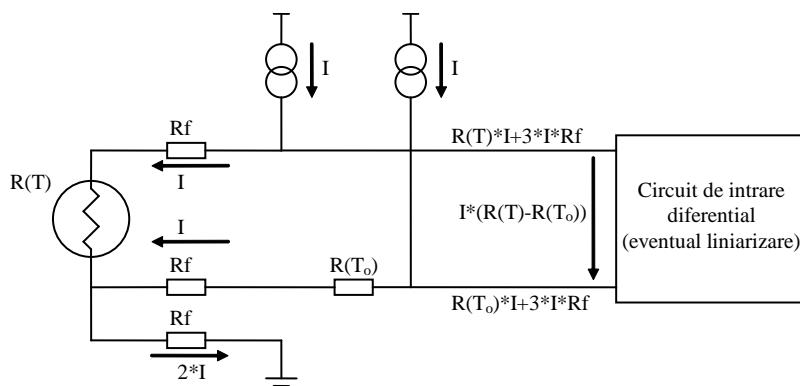
Tip conexiune (AI - temperatura):

- Doua fire
- Trei fire

$$R(T) = R_0 \left(1 + \alpha \cdot T + \beta \cdot T^2 \right)$$



Conecțarea (termorezistențelor) pe 2 fire



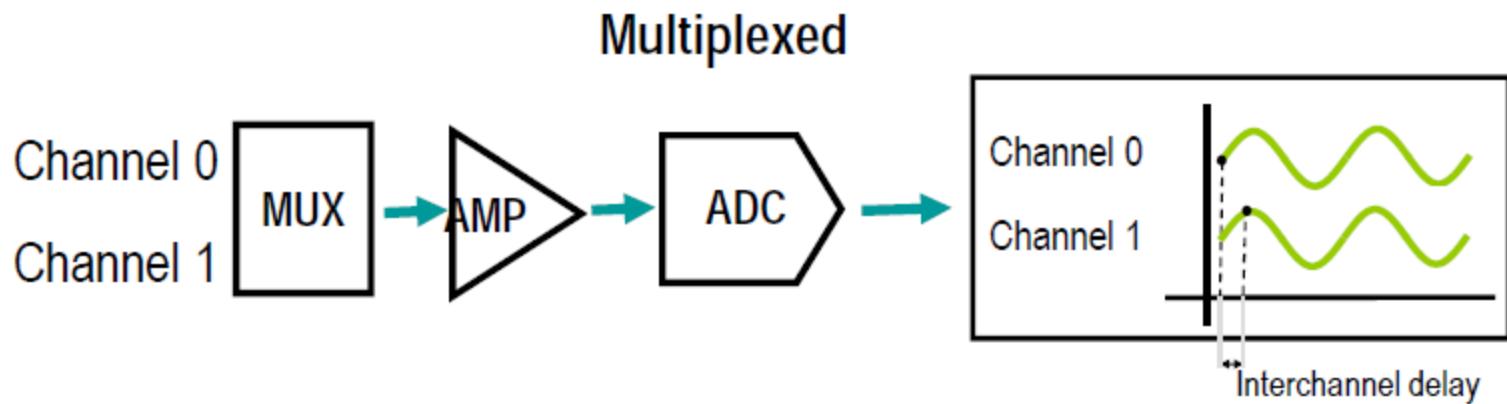
Conecțarea (termorezistențelor) pe 3 fire

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2. Achizitia datelor

Arhitecturi(AI):

- Multiplexata

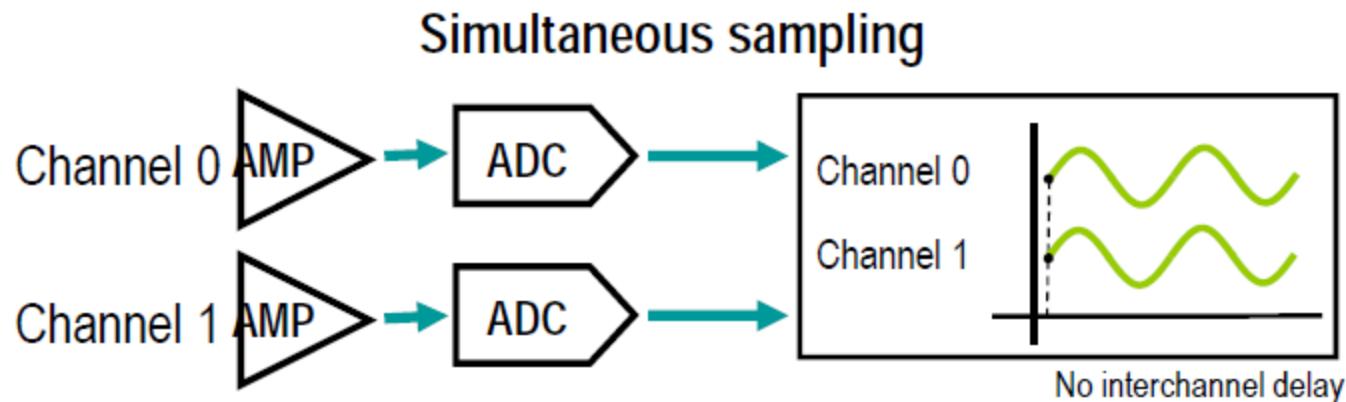


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Arhitecturi(AI):

- Simultana (neMultiplexata)

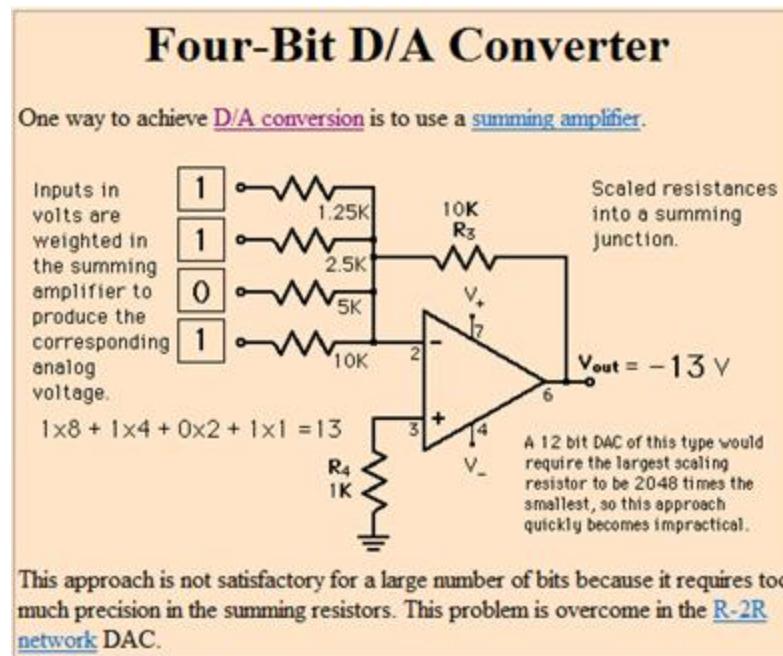


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Conversie D/A:

- Convertor D/A (4 biti)

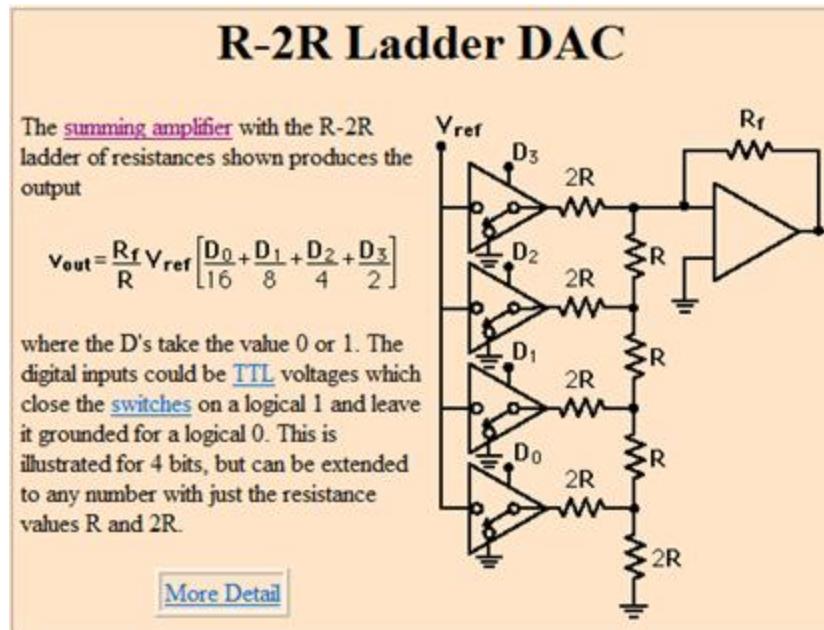


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Conversie D/A:

- Convertor D/A (4 biti)

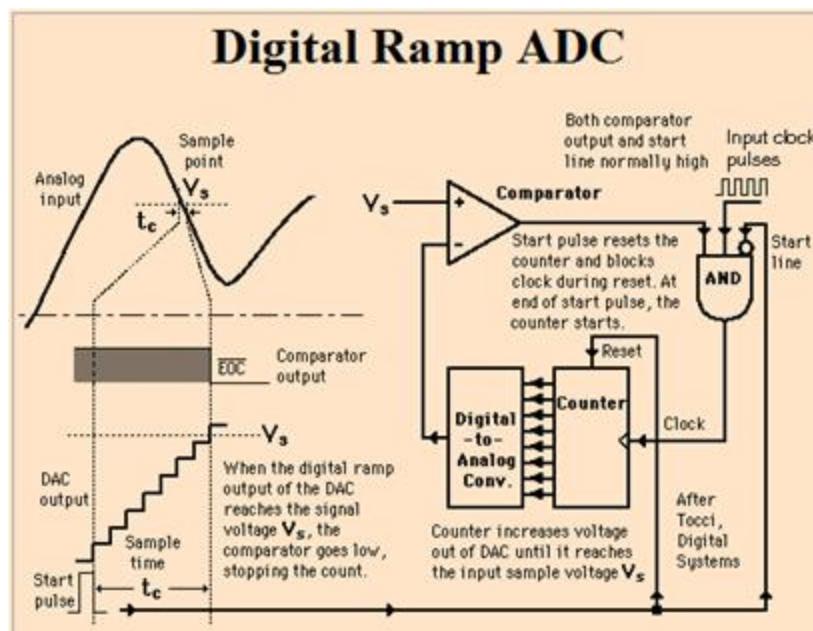


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2. Achizitia datelor

Conversie A/D:

- Convertor servo-operatii

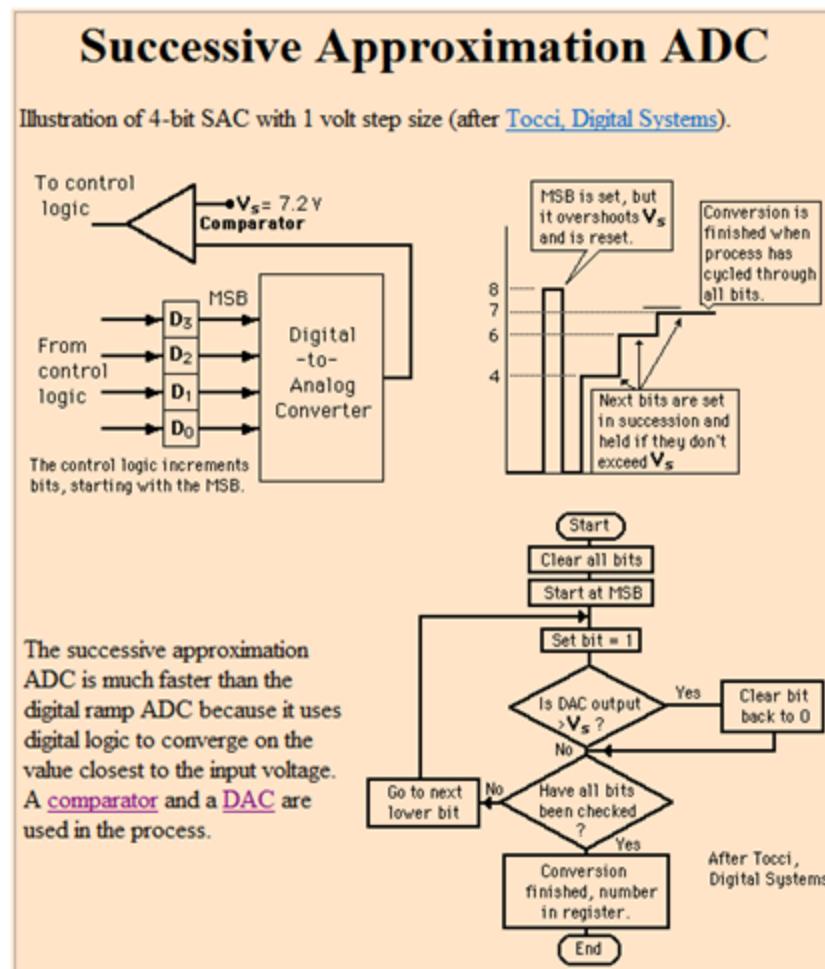


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Conversie A/D:

Convertor aproximatii succesive

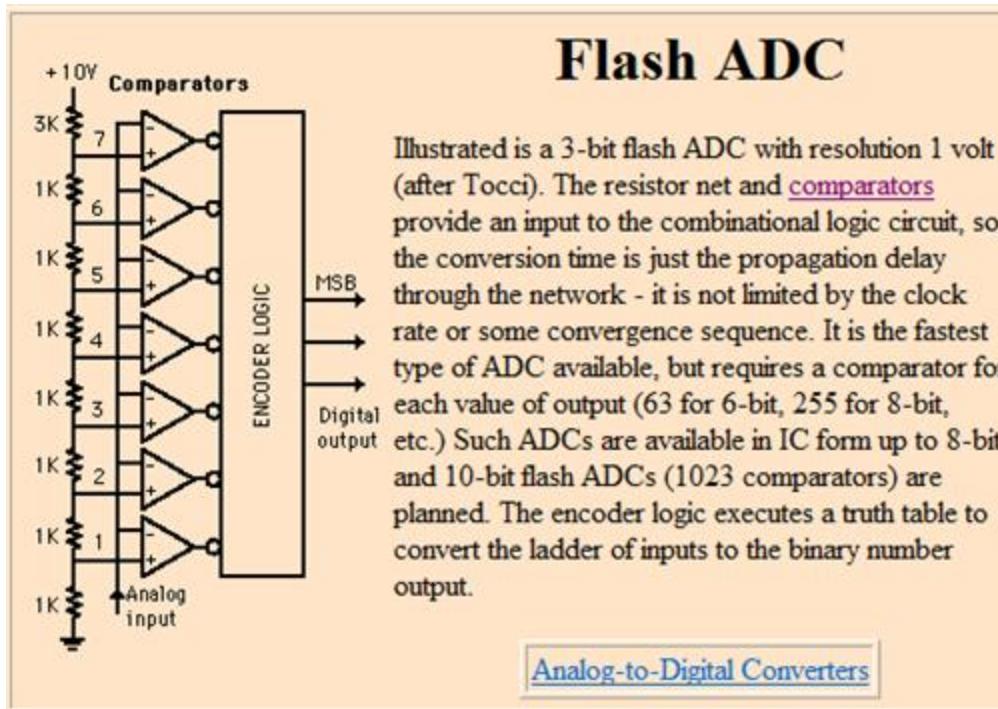


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2. Achizitia datelor

Conversie A/D:

- Convertor instant (flash)

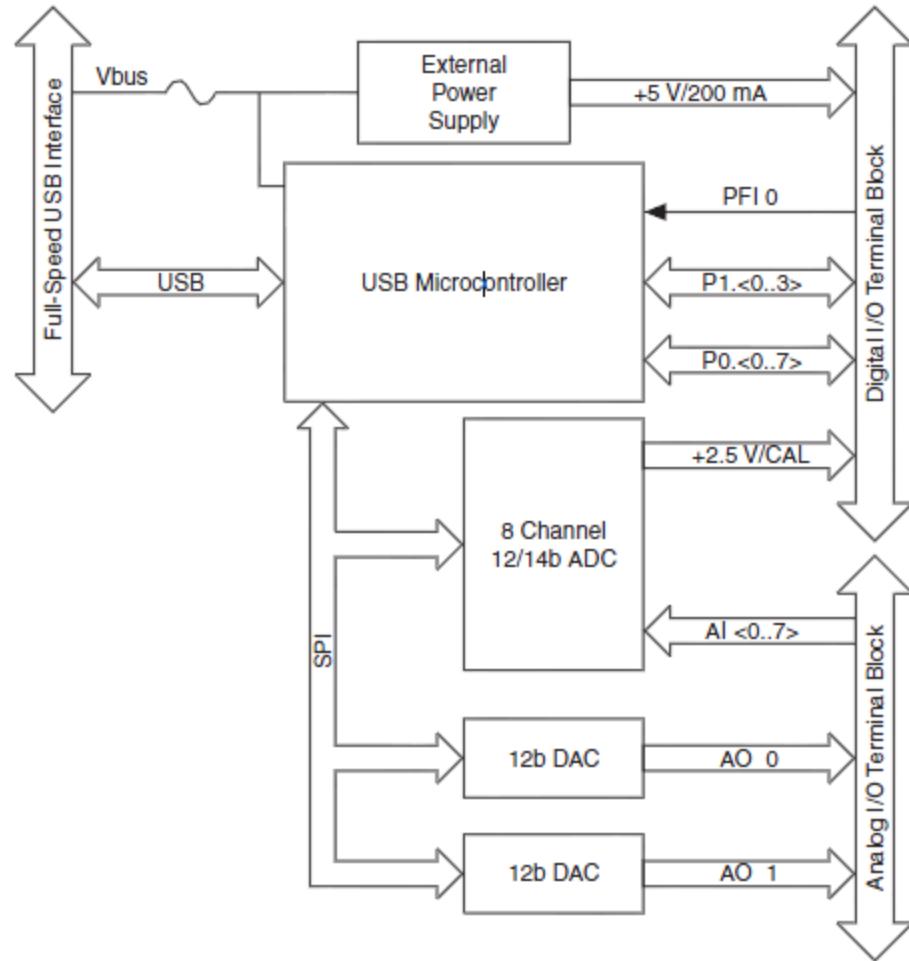


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Ex. Arhitecturi:

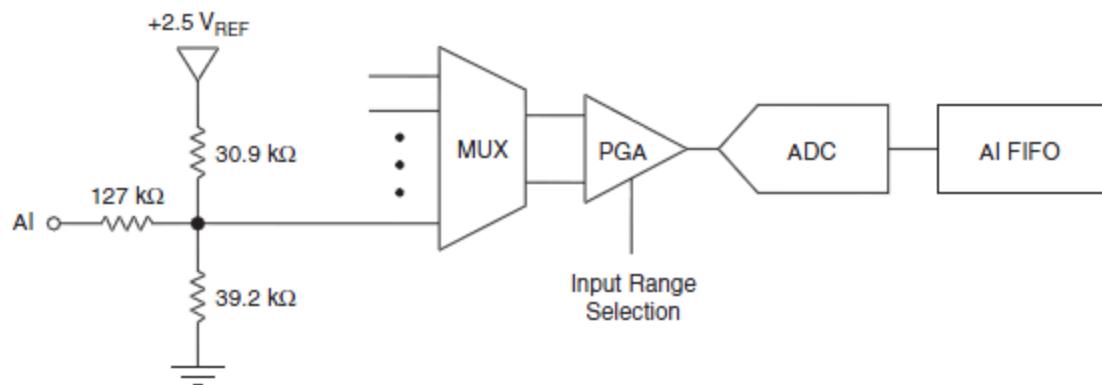
- **NI USB 6008/6009**



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2. Achizitia datelor

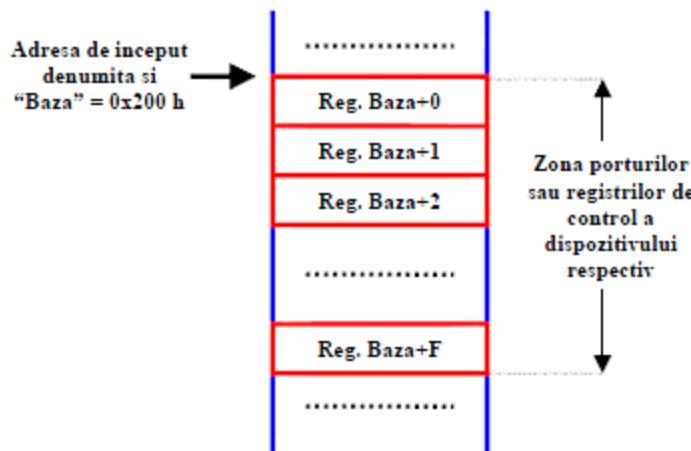
Arhitectura canal achizitie AI:



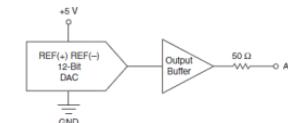
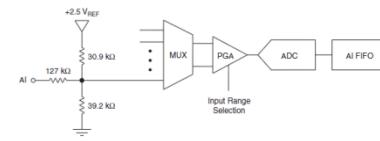
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Arhitectura memorie (porturi):



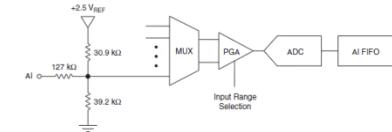
Adresa	Functie la citire	Functie la scriere
Baza + 0	Contor 0 8253	Contor 0
Baza + 1	Contor 1	Contor 1
Baza + 2	Contor 2	Contor 2
Baza + 3	neutilizat	Registru de control 8253
Baza + 4	A/D octet low	D/A 1 octet low
Baza + 5	A/D octet high	D/A 1 octet high
Baza + 6	DI octet low	D/A 2 octet low
Baza + 7	DI octet high	D/A 2 octet high
Baza + 8	neutilizat	interupere placa
Baza + 9	neutilizat	neutilizat
Baza + A	neutilizat	Selectie canal multiplexor
Baza + B	neutilizat	Cuvant de control placa
Baza + C	neutilizat	Decl. soft a conv. A/D
Baza + D	neutilizat	DO octet low
Baza + E	neutilizat	DO octet high
Baza + F	neutilizat	neutilizat



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Asamblare rezultat conversie AI:



Registrul Baza + 5



Partea ce mai
semnificativa a
conversiei

Registrul Baza + 4



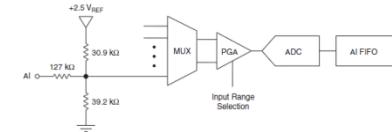
Partea ce mai putin
semnificativa a
conversiei

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2. Achizitia datelor

Arhitectura driver achizitie AI:

- selectie mod de functionare al dispozitivului respectiv: intreruperi, interogare, DMA;
- setarea amplificarii canalului de achizitie;
- alegerea canalului achizitionat;
- declansarea operatiei de conversie;
- asteptare a incheierii operatiei de conversie analog numerice;
- citirea rezultatelor din registrii corespunzatori;
- normarea datelor din gama CAN 0 – 2ⁿ⁻¹ (n nr. de biti pe care se face conversia) in unitati ingineresti.



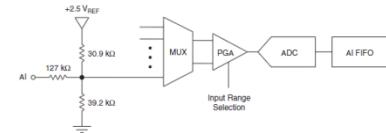
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2. Achizitia datelor

Arhitectura driver achizitie AI:

```
int ai(int canal)
{
    unsigned char h,l;
    // setare a modului de lucru al placii
    outp(MOD,0x01);
    // setarea amplificarii
    outp(AMP,0x02);
    // selectarea canalului citit
    outp(MPX,canal);
    // pauza pentru stabilizarea oscilatiilor
    delay(1);
    // declansarea operatiei de achizitie
    outp(TRG,0x00);
    // testare a sfarsitului de conversie
    /* do{
        h=inp(ADH);
        }while((h&0x10)==0x10); */
    delay(1);
    // preluarea rezultatului conversiei partea H x 256 + L
    h=inp(ADH)&0x0F;
    l=inp(ADL);
    return(256*h+l);
}
```

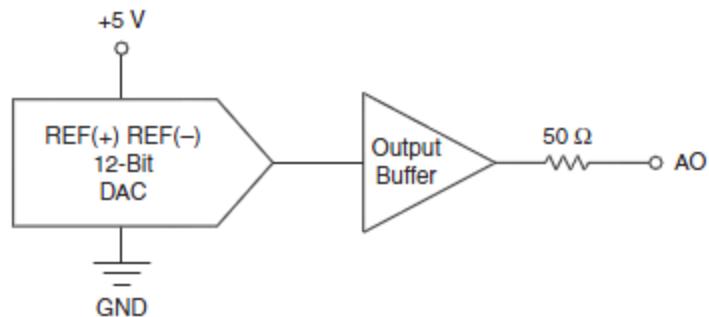
// definirea unor constante ce corespund adreselor
// registrilor utilizati
#define ADL 0x224
#define ADH 0x225
#define AMP 0x229
#define MPX 0x22A
#define MOD 0x22B
#define TRG 0x22C



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2. Achizitia datelor

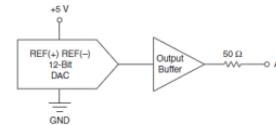
Arhitectura canal AO:



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2. Achizitia datelor

Arhitectura driver AO:



- denormarea datelor din gama unitatilor ingineresti in gama CNA $0 - 2^n - 1$ (n nr. de biti din care se face conversia);
- separarea partilor High si Low ale datelor de convertit;
- scrierea registrilor corespunzatori cu valorile dorite;
- setarea amplificarii canalului de achizitie;
- alegerea canalului achizitionat;

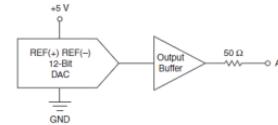
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2. Achizitia datelor

Arhitectura driver AO:

```
void ao0(int val)
{
    unsigned char h,l;
    // separarea partii High de partea Low
    h=(unsigned char)(val/256);
    l=(unsigned char)(val%256);
    // scrierea registrilor corespunzatori partilor Low si High
    outp(DAL,l);
    outp(DAH,h);
}
```

// definirea unor constante ce corespund adreselor
// registrilor utilizati
#define DAL0x224
#define DAH0x225

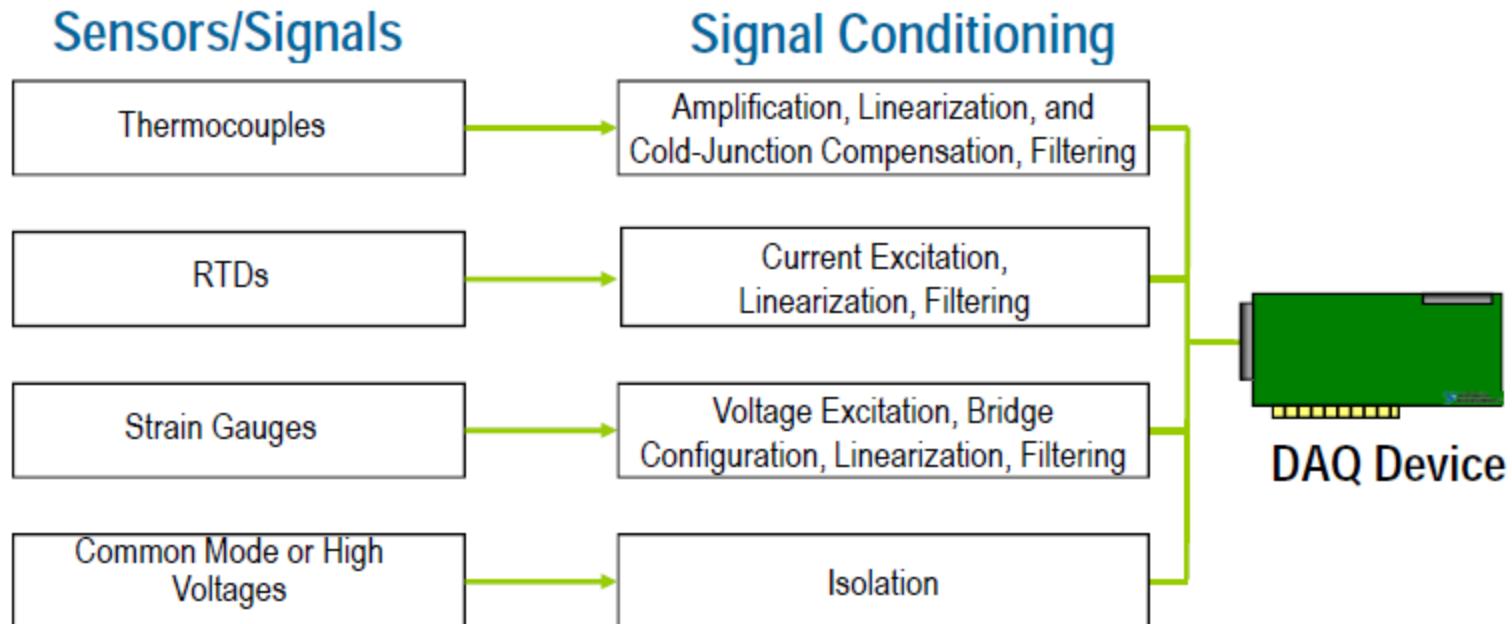


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2. Achizitia datelor

Arhitecturi(AI):

- Conditionare semnal

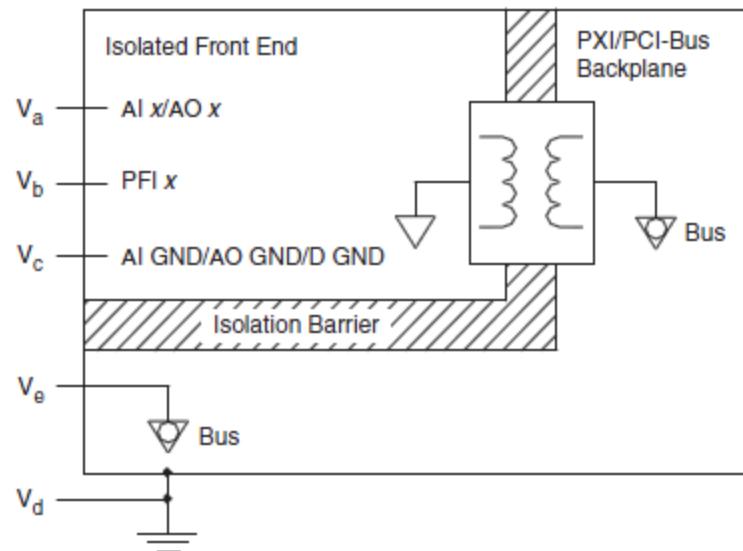
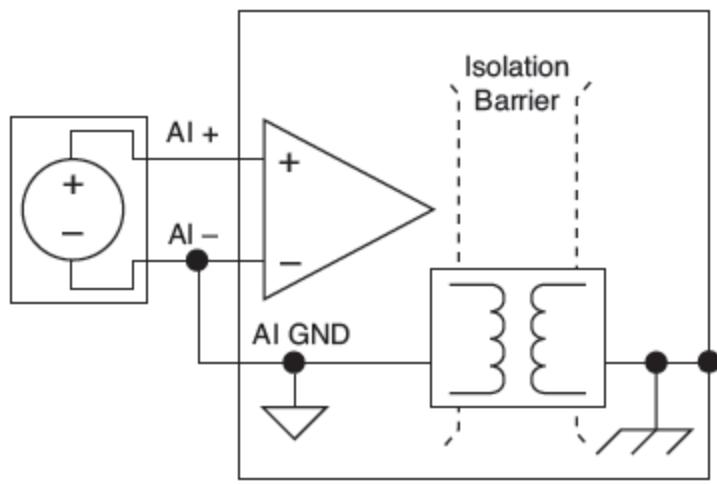


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2. Achizitia datelor

Arhitecturi(AI):

- Izolare speciala interna

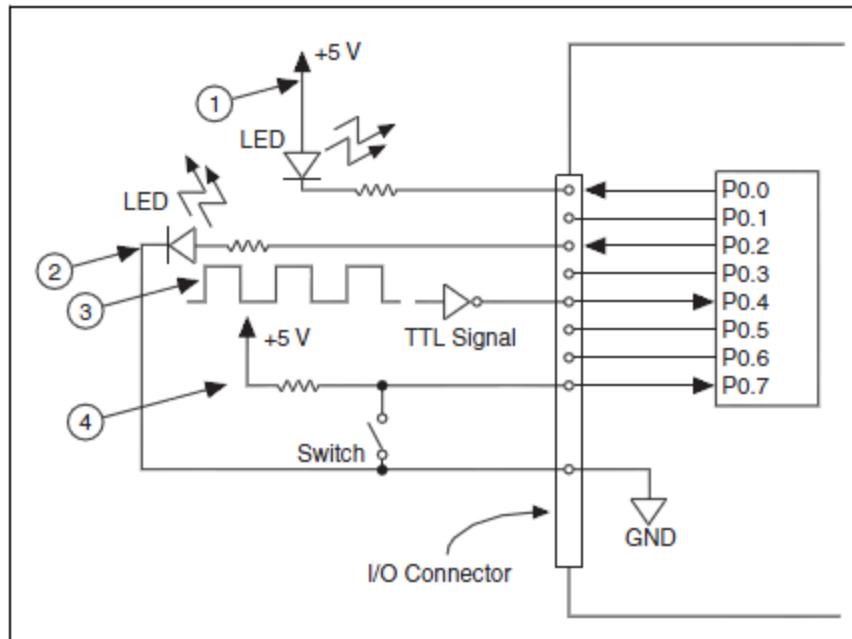


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2. Achizitia datelor

DI/DO:

- Citire porturi
- Setare porturi



- 1 P0.0 configured as an open collector digital output driving an LED
- 2 P0.2 configured as an active drive digital output driving an LED
- 3 P0.4 configured as a digital input receiving a TTL signal from a gated inverter
- 4 P0.7 configured as a digital input receiving a 0 V or 5 V signal from a switch

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2. Achizitia datelor

Conexiune module achizitie:

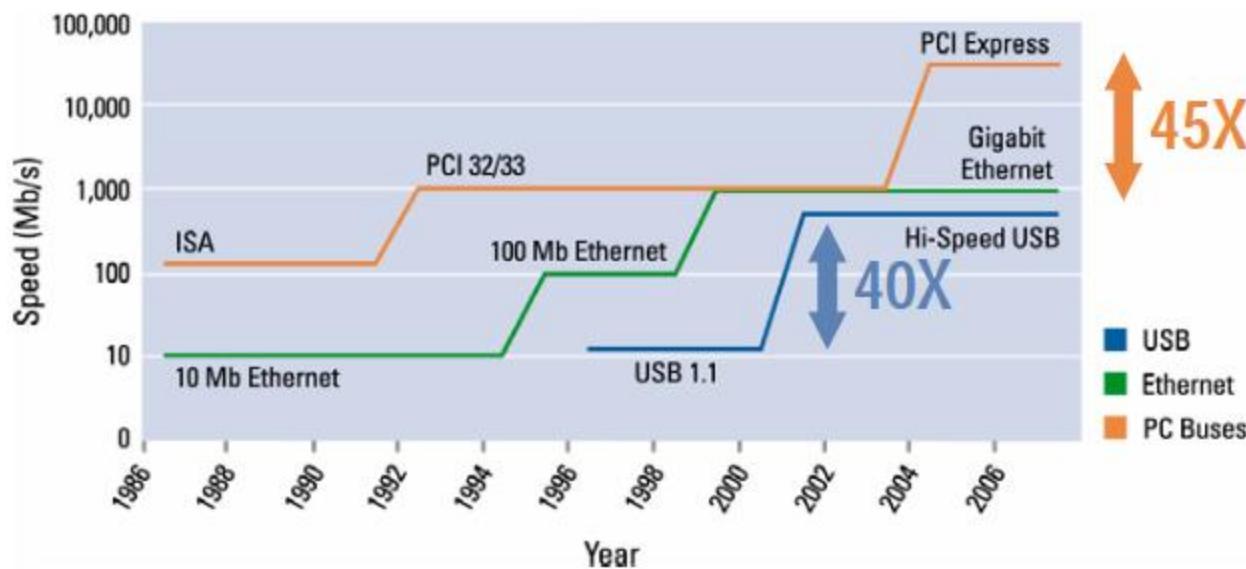
- PCI (ISA)
- USB
- Ethernet
- Arhitecturi proprii (PXI etc.)
- Radio
- Wireless



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2. Achizitia datelor

Conexiune module achizitie:



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Conexiune module achizitie:

- USB

USB Data Acquisition



Low-Cost

Starting at \$145
8 AI, 2 AO, 12 DIO, 1 CTR

Integrated Signal Conditioning



16-bit simultaneous sampling AI
24-bit thermocouple input
Rugged features

High Performance



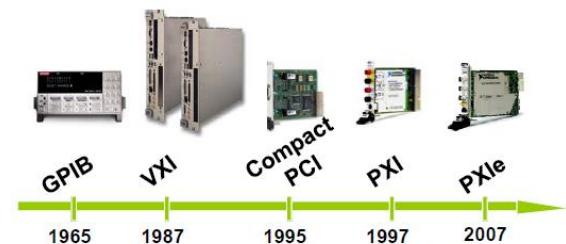
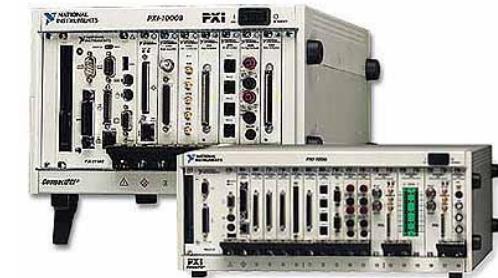
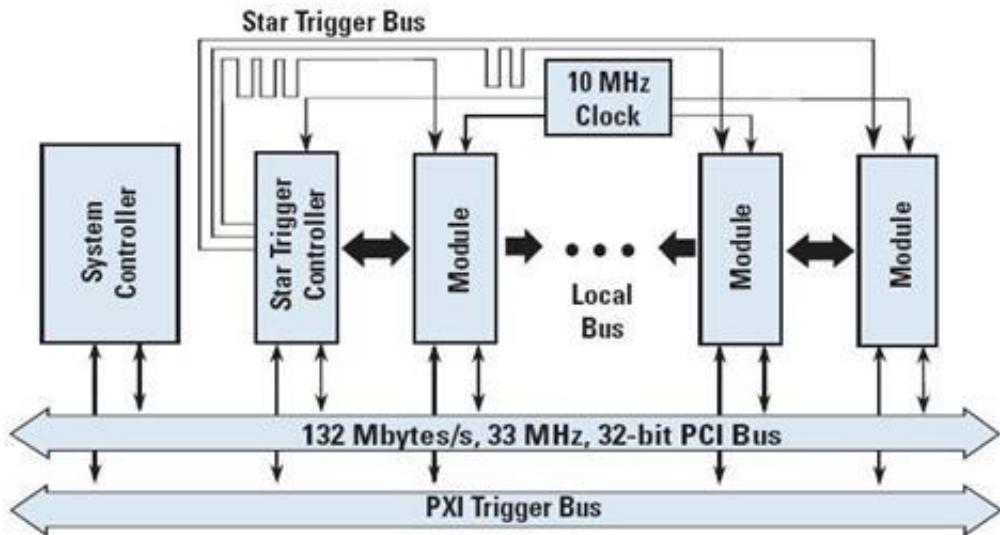
16 bits, 200 kS/s
16 AI, 2 AO, 32 DIO, 2 CTR

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2. Achizitia datelor

Conexiune module achizitie:

- **PXI**



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2. Achizitia datelor

Arhitecturi achizitie:

- NI cDAQ



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Arhitecturi achizitie:

- NI cRIO

