

# **FILTER DESIGN FOR MULTILEVEL INVERTERS**

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Visvesvaraya National Institute of Technology, Nagpur  
in partial fulfillment of the requirements for the award of  
the degree*

## **Bachelor of Technology In Electrical and Electronics Engineering**

*by*

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**Certificate**

This is to certify that the project titled “FILTER DESIGN FOR MULTILEVEL INVERTERS”, submitted by **Juthuga Sahithi Vineela, Neha Sute, Vaidehi Korde and Banoth Vishnu Vardhan** in partial fulfillment of the requirements for the award of the degree of **Bachelor of Technology in “Electrical and Electronics Engineering”**, VNIT Nagpur. The work is comprehensive, complete and fit for final evaluation.

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We, Juthuga Sahithi Vineela, Neha Sute and Vaidehi Korde, Banoth Vishnu Vardhan hereby declare that this project work titled “FILTER DESIGN FOR MULTILEVEL INVERTERS” is carried out by us in the Department of Electrical and Electronics Engineering of Visvesvaraya National Institute of Technology, Nagpur. The work is original and has not been submitted earlier whole or in part for the award of any degree at this or any other Institution.

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## **ABSTRACT**

Power electronics is the art of converting electrical energy from one form to another in an efficient, clean, compact and robust manner for convenient utilization. The power electronic device which converts DC power to AC power at required output voltage and frequency level is known as an Inverter. The Voltage Source Inverters which produces an output voltage or output current with levels either 0 or positive or negative DC voltage ( $V_{dc}$ ) are known as Two-Level Inverters. A Multilevel Inverter is a more advanced inverter which generates a near sinusoidal desired output voltage from several levels of DC voltages. From various conventional topologies, Cascaded H-Bridge topology is chosen owing to its various advantages compared to the other topologies. Using CHB Topology, various Level (3, 5 and 7) Inverters are compared with each other. Different types of Sine PWM Control Techniques of Multilevel Inverters are examined and out of them, Phase Opposition Disposition (POD) technique was put in use till the end of this work. With decrease in the Modulation Index, there is reduction in fundamental voltage and in the output voltage levels. Also, there is decrease in %THD with increase in Switching Frequency of the carrier signals. The output of Multilevel Inverter is a stepped waveform and is not purely sinusoidal. This implies the presence of harmonics in the output of inverter. To reduce these harmonics and hence to improve %THD, various filters (L, LC and LCL) are used which are classified under Passive Filters. These filters are designed accordingly and optimal values of inductance and capacitance are obtained. Further, this analysis is extended to various levels of Multilevel Inverter. To validate all the theoretical analysis of the Multilevel Inverters and their Filter Design, simulations have been used throughout this work. These Simulations are done in MATLAB SIMULINK environment for feasibility.

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# **1.INTRODUCTION**

## **1.1 Inverters**

Inverters are the power electronic circuit, which converts the DC voltage into AC voltage. The DC source is normally a battery or output of the controlled rectifier. The output voltage waveform of the inverter can be square wave, quasi-square wave or low distorted sine wave. The output voltage can be controlled with the help of drives of the switches. The pulse width modulation techniques are most commonly used to control the output voltage of inverters. Such inverters are called as PWM inverters. The output voltage of the inverter contains harmonics whenever it is not sinusoidal. These harmonics can be reduced by using proper control schemes.

Inverters can be broadly classified into two types. They are-

1. Voltage Source Inverter (VSI)
2. Current Source Inverter (CSI)

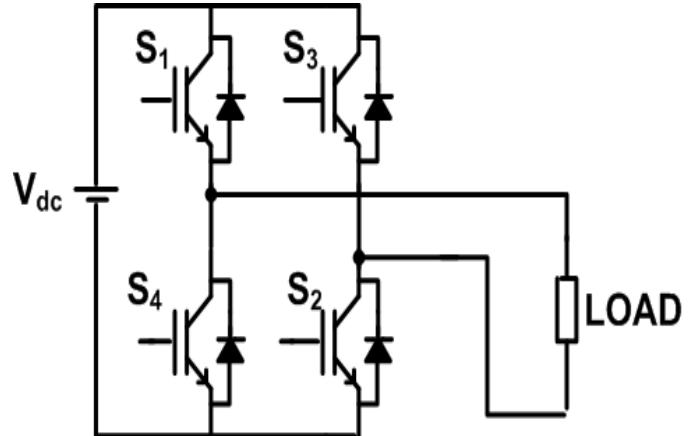
When the DC voltage remains constant, then it is called voltage inverter (VSI) or voltage fed inverter (VFI). When input current is maintained constant, then it is called current source inverter (CSI) or current fed inverter (CFI). Sometimes, the DC input voltage to the inverter is controlled to adjust the output. Such inverters are called variable DC link inverters. The inverters can have single phase or three-phase output.

The following points gives us the comparative study between VSI and CSI

- A voltage source inverter is fed by a stiff dc voltage, whereas a current source inverter is fed by a stiff current source.
- A voltage source can be converted to a current source by connecting a series inductance and then varying the voltage to obtain the desired current.
- A VSI can also be operated in current-controlled mode, and similarly a CSI can also be operated in the voltage control mode.
- The inverters are used in variable frequency ac motor drives, uninterrupted power supplies, induction heating, static VAR compensators, etc. The following sections gives us the comparative study between VSI and CSI.

### 1.1.1 Voltage Source Inverters (VSI)

- VSI is fed from a DC voltage source having small or negligible impedance.
- Input voltage is maintained constant.
- Output voltage does not depend on the load.
- The waveform of the load current as well as its magnitude depends upon the nature of load impedance.
- VSI requires feedback diodes.

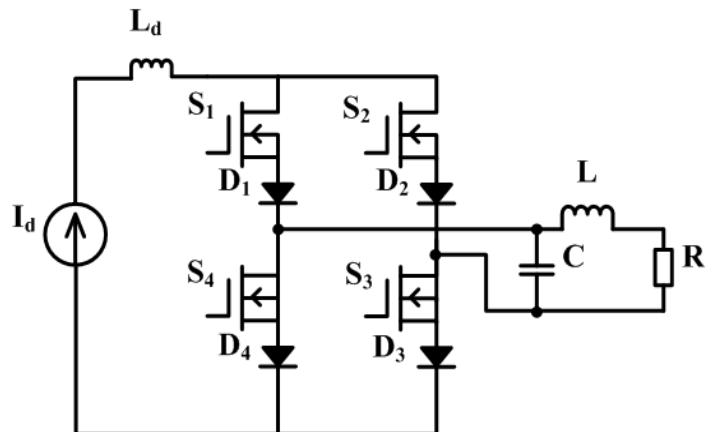


**Figure 1-1: Voltage-source inverter**

- Power BJT, Power MOSFET, IGBT and GTO with self-commutation can be used in the circuit.
- Commutation circuit is complex.

### 1.1.2 Current Source Inverters (CSI)

- CSI is fed with adjustable current from a DC voltage source of high impedance.
- The input current is constant but adjustable.
- The amplitude of output current is independent of the load.
- The magnitude of output voltage and its waveform depends upon the nature of the load impedance.
- The CSI does not require any feedback diodes.
- Commutation circuit is simple.



**Figure 1-2: Current-source inverter**

## 1.2 Classification of VSI

VSI can be categorized into two types. They are-

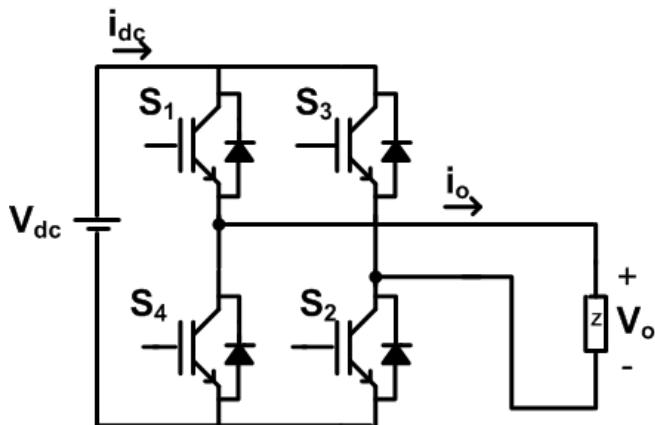
1. Conventional inverters
2. Multilevel inverters

### 1.2.1 Conventional Inverters

As previously mentioned, the purpose of an inverter is to convert DC power to AC power. Inverters are an integral part of many technologies including uninterruptable power supplies, induction heating, high-voltage direct current power transmission, variable frequency drives, electric vehicle drives, and multiple renewable energy applications. All of these technologies use inverters to achieve different goals, but all produce AC power from a DC input. There are many varieties of inverter designs. The most common topology used is shown in the figure and is referred to as the H-bridge topology.

The term H Bridge is derived from the typical graphical representation of such a circuit. An H bridge is built with four switches (solid-state or mechanical). When the switches S1 and S2 are closed a positive voltage will be applied across the motor. By opening S1 and S2 switches and closing S3 and S4 switches, this voltage is reversed, allowing reverse operation.

#### 1.2.1(a) Single-phase Conventional Inverter



**Figure 1-3: Conventional Single-phase inverter**

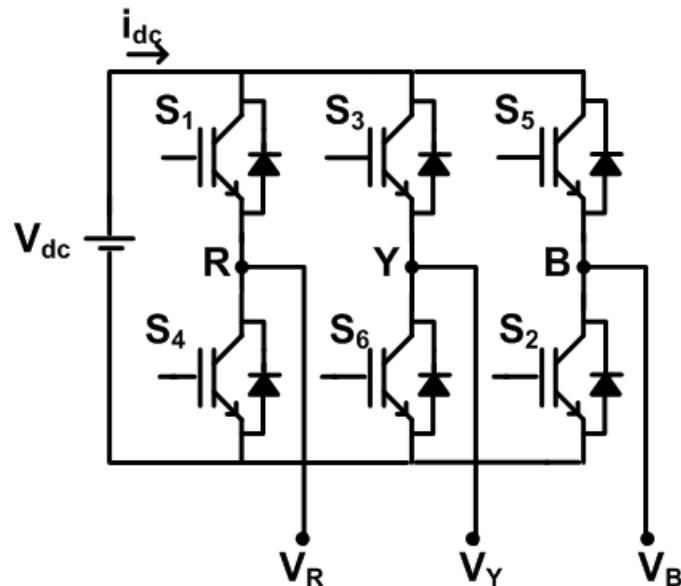
Using the nomenclature above, the switches  $S_1$  and  $S_3$  should never be closed at the same time, as this would cause a short circuit on the input voltage source. The same applies to the switches  $S_2$  and  $S_4$ . This condition is known as shoot-through. Its basic configuration is shown in figure. This topology is used in conjunction with either the square wave, or pulse width modulation (PWM) switching schemes. The square-wave switching scheme is a method for controlling the switches (labelled  $S_1$  through  $S_2$ ) in order to achieve a square wave AC output signal. The AC output is achieved by using a control signal with a 50%

duty cycle wired to S1 and S2. An inverted copy of the same signal is also wired to S3 and S4. This switching scheme ensures that S1 and S2 are always on when S3 and S4 are off. It should be easily seen how such a switching scheme creates the square wave output shown in figure. The advantage of using an H-bridge inverter is that only a single, simple control signal is required to control four transistors.

The disadvantage, however, is that the square wave output is a low-quality AC signal that injects many harmonics into any loads to which it is powering. We thus aim to reduce the harmonics in the output AC voltage by use of various modulation techniques.

### 1.2.1(b) Three-phase Conventional Inverter

A basic three phase inverter consist of three legs, each attached to the phase output line. The upper and lower switching transistor are S1 & S4 for R phase, S3 & S6 for Y phase and S5 & S2 for B phase respectively.



**Figure 1-4: Basic three-phase inverter**

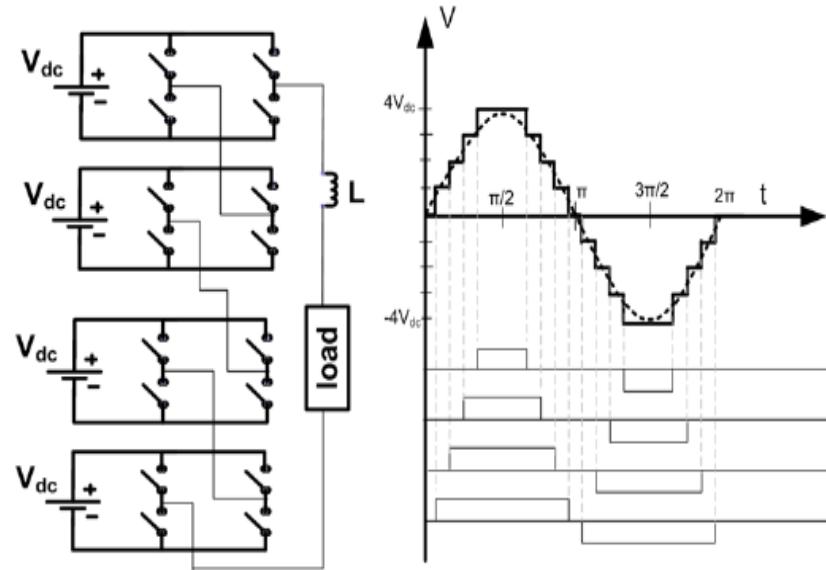
This circuit may be identified as three single-phase half-bridge inverter circuits put across the same dc bus. The individual pole voltages of the 3-phase bridge circuit are identical to the square pole voltages output by single-phase half bridge or full bridge circuits. The three pole voltages of the 3-phase square wave inverter are shifted in time by one third of the output time period.

### 1.2.2 Multilevel Inverters

A multilevel inverter is a power electronic device which is capable of providing desired alternating voltage level at the output using multiple lower level DC voltages as an input. Mostly a two-level inverter is used in order to generate the AC voltage from DC voltage. Although this method of creating AC is effective but it has few drawbacks as it

creates harmonic distortions in the output voltage and also has a high dv/dt as compared to that of a multilevel inverter. Normally this method works but, in few applications, it creates problems particularly those where low distortion in the output voltage is required.

The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two-level voltage instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together and the output waveform obtained in this case has lower dv/dt and also lower harmonic distortions. Smoothness of the waveform is proportional to the voltage levels, as we increase the voltage level the waveform becomes smoother but the complexity of controller circuit and components also increases along with the increased levels.



**Figure 1-5: Basic Cascaded H-bridge Topology**

The topological structure of multilevel inverter must cope with the following points-

- It should have less switching devices as far as possible.
- It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.
- Each switching device should have lower switching frequency owing to multilevel approach.

### 1.3 Comparison of Multilevel Inverters

**Table 1-1: Comparison between Conventional and Multilevel Inverters**

Sr.no	Conventional Inverter	Multilevel Inverter
1	Higher THD in output voltage	Low THD in output voltage
2	More switching stresses on devices	Reduced switching stresses on devices
3	Higher voltage levels are not produced	Higher voltage levels are produced
4	Since $dV/dt$ is high, the EMI from the system is high	Since $dV/dt$ is low, the EMI from the system is low
5	Higher switching frequency is used hence switching losses is high	Lower switching frequency can be used and hence reduction in switching losses
6	Power bus structure, control schemes are simple	Control scheme is complex as the number of levels increases
7	Not applicable for high voltage applications	Applicable for high voltage applications

Thus, it can be concluded that Multilevel inverters are advantageous than conventional inverters.

### 1.4 Inverter Applications

- **DC power source utilization**

An inverter converts the DC electricity from sources such as batteries or fuel cells to AC electricity.

- **Uninterrupted powers source utilization**

An uninterruptible power supply (UPS) uses batteries and an inverter to supply AC power when main power is not available. When main power is restored, a rectifier supplies DC power to recharge the batteries.

- **Electric motor speed control**

Inverter circuits designed to produce a variable output voltage range are often used within motor speed controllers. The DC power for the inverter section can be derived from a normal AC wall outlet or some other source. Control and feedback

circuitry are used to adjust the final output of the inverter section which will ultimately determine the speed of the motor operating under its mechanical load.

- **Power grid**

Grid-tied inverters are designed to feed into the electric power distribution system. They transfer synchronously with the line and have as little harmonic content as possible. They also need a means of detecting the presence of utility power for safety reasons, so as not to continue to dangerously feed power to the grid during a power outage.

- **Solar**

A solar inverter is a balance of system (BOS) component of a photovoltaic system and can be used for both, grid-connected and off-grid systems. Solar inverters have special functions adapted for use with photovoltaic arrays, including maximum power point tracking and anti-islanding protection.

- **HVDC**

With HVDC power transmission, AC power is rectified and high voltage DC power is transmitted to another location. At the receiving location, an inverter in a static inverter plant converts the power back to AC. The inverter must be synchronized with grid frequency and phase and minimize harmonic generation.

## **2.MULTILEVEL INVERTERS**

### **2.1 Necessity of Multilevel inverters**

Now a day's many industrial applications have begun to require high power. Some appliances in the industries however require medium or low power for their operation. Using a high-power source for all industrial loads may prove beneficial to some motors requiring high power, while it may damage the other loads. Some medium voltage motor drives and utility applications require medium voltage.

The multilevel inverter has been introduced since 1975 as alternative in high power and medium voltage situations. The Multi-level inverter is like an inverter and it is used for industrial applications as alternative in high power and medium voltage situations.

Multilevel inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level.

A multilevel inverter generates a staircase output which resembles close to a sinusoidal waveform. The closeness of this output waveform to sine wave is indicated by %THD parameter. It generates a desired output voltage from several DC voltage levels at its input.

The term "Multilevel" begins with a "Three-Level Converter".

#### **2.1.1 Advantages of Multilevel Inverter**

The multilevel converter has a several advantages such as-

- Common Mode Voltage:**

The multilevel inverters produce common mode voltage, reducing the stress of the motor and don't damage the motor.

- Input Current:**

Multilevel inverters can draw input current with low distortion.

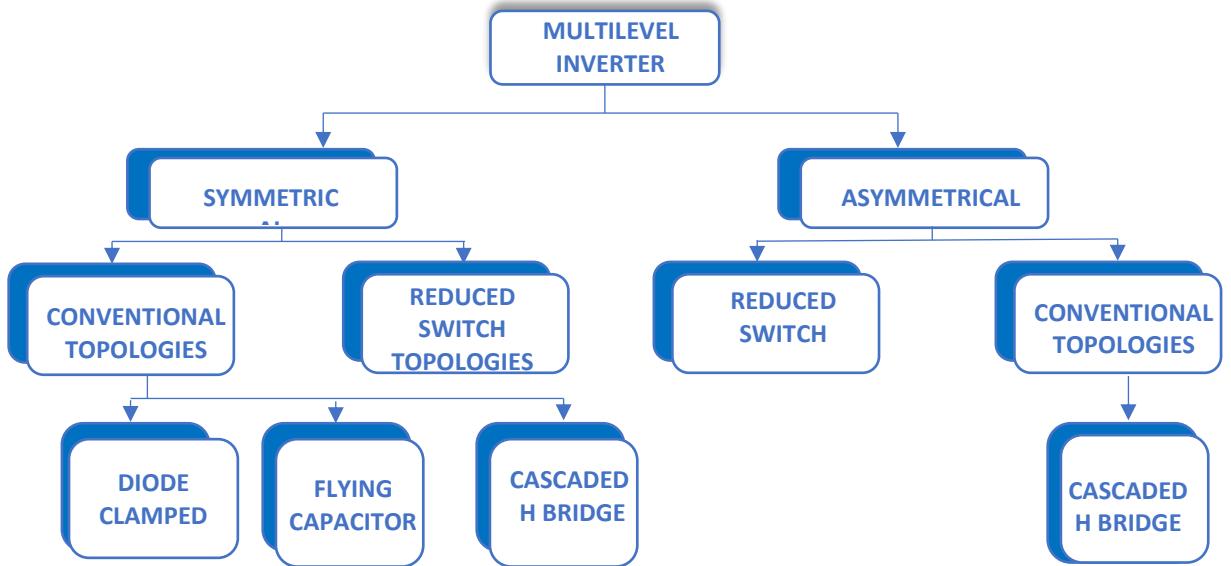
- Switching Frequency:**

The multilevel inverter can operate at both fundamental switching frequencies that are higher switching frequency and lower switching frequency. It should be noted that the lower switching frequency means lower switching loss and higher efficiency is achieved.

- Reduced harmonic distortion:**

Selective harmonic elimination technique along with the multilevel topology results the total harmonic distortion becomes low in the output waveform without filter.

## 2.2 Classification of Multilevel Inverters



**Fig 2-1: Classification of multilevel inverters**

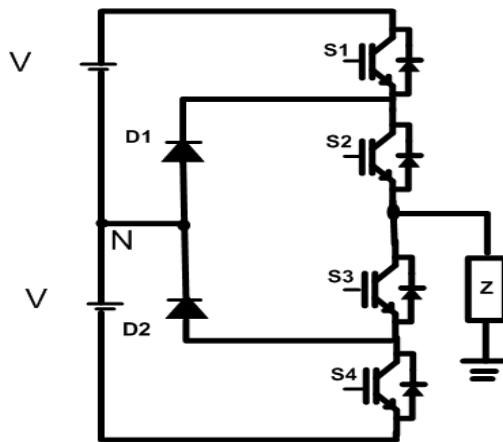
Multilevel inverters are classified on the basis of the circuit structure and are of three types as follows:

## 2.3 Diode-clamped Multilevel Inverter/ Neutral Point-Clamped (NPC)

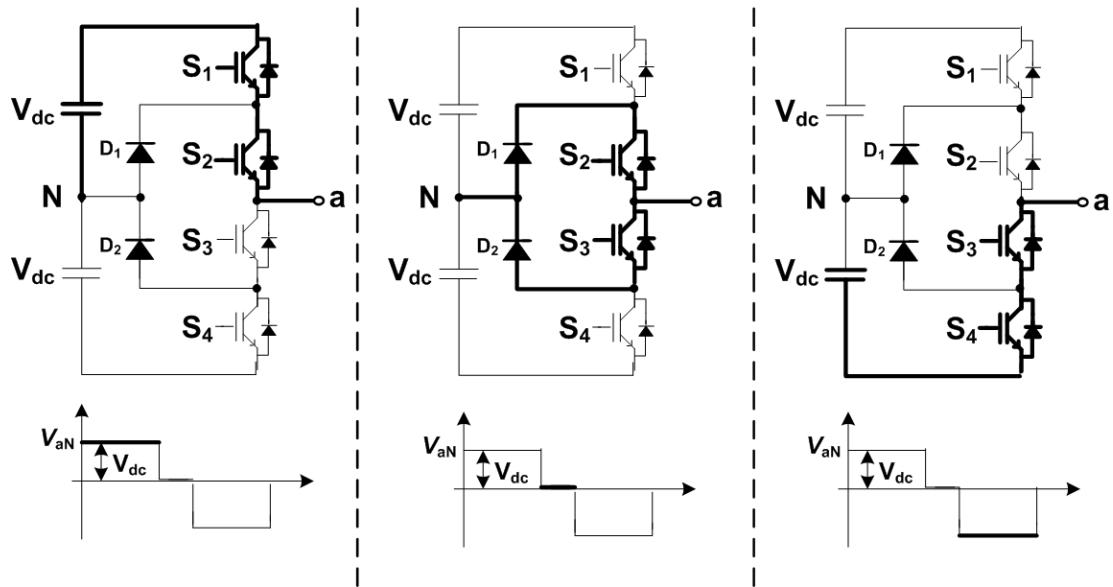
The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A diode transfers a limited amount of voltage, thereby reducing the stress on other electrical devices. The maximum output voltage is half of the input DC voltage. It is the main drawback of the diode clamped multilevel inverter. This problem can be solved by increasing the switches, diodes, capacitors.

Due to the capacitor balancing issues, these are limited to the three levels. This type of inverters provides the high efficiency because the fundamental frequency used for all switching devices and it is a simple method of the back to back power transfer systems.

For generalized structure of DCMLI,  $N$  levels on phase voltage and  $(2N-1)$  levels on line voltage are produced using  $2(N-1)$  switching devices/leg and  $(N-1) * (N-2)$  clamping diodes.



**Fig 2-2: Diode Clamped Multilevel Inverter**



**Fig 2-3: Three-level Diode clamped Multilevel inverter**

**Table 2-1: Switching sequence of 3 level diode clamped Multilevel inverter**

Switching combination		Output Voltage $V_{an}$
Switches ON	Switches OFF	
S <sub>1</sub> , S <sub>2</sub>	S <sub>3</sub> , S <sub>4</sub>	V <sub>dc</sub>
S <sub>2</sub> , S <sub>3</sub>	S <sub>1</sub> , S <sub>4</sub>	0
S <sub>3</sub> , S <sub>4</sub>	S <sub>1</sub> , S <sub>2</sub>	-V <sub>dc</sub>

### **2.3.1 Applications of Diode Clamped Multilevel Inverter:**

- Static VAR compensation
- Variable speed motor drives
- High voltage system interconnections
- High voltage DC and AC transmission lines

### **2.3.2 Advantages**

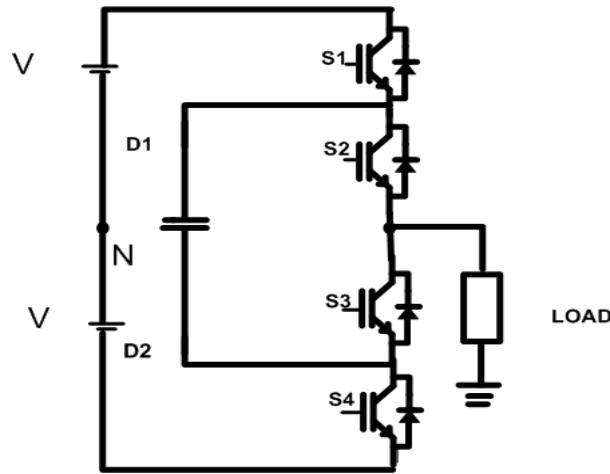
- When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters.
- Efficiency is high due to all devices which are being switched at the fundamental frequency.
- We are able to control the reactive power flow.
- The control method is easy for a back to back intertie system.

### **2.3.3 Disadvantages**

- Excessive clamping diodes are being required when the number of levels get high.
- It is hard to do a real power flow control for individual converter.

## **2.4 Flying Capacitor Multilevel Inverter**

The main concept of this inverter is to use capacitors. It is of series connection of capacitor clamped switching cells. The capacitors transfer the limited amount of voltage to electrical devices. In this inverter switching states are like in the diode clamped inverter. Clamping diodes are not required in this type of multilevel inverters. The output is half of the input DC voltage. It is drawback of the flying capacitors multilevel inverter. It also has the switching redundancy within phase to balance the flying capacitors. It can control both the active and reactive power flow. But due to the high frequency switching, switching losses will takes place.



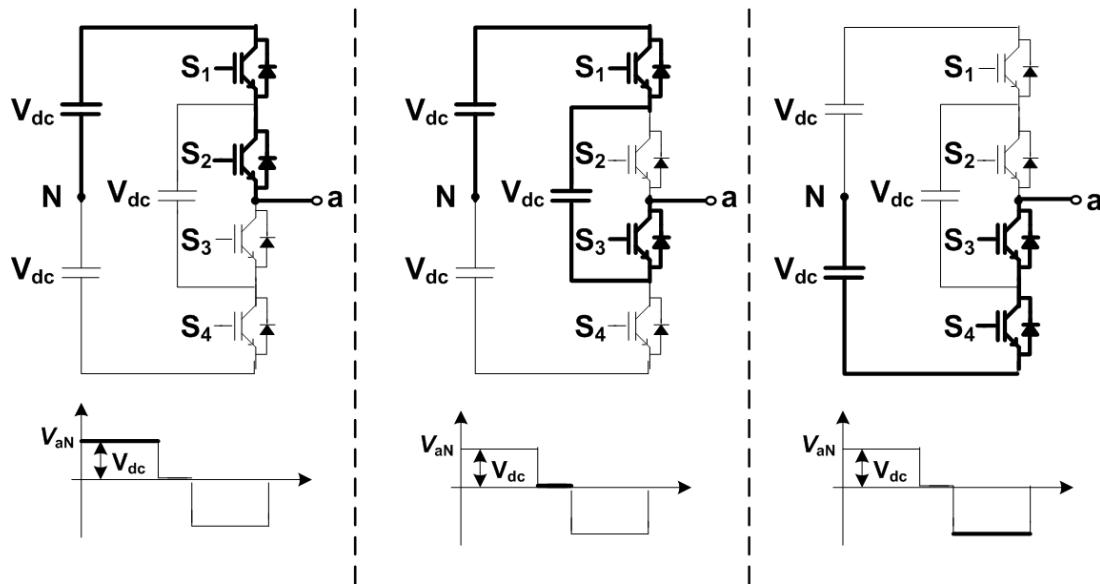
**Figure 2-4: Flying capacitor Multilevel inverter topology**

For  $N$  level inverter leg requires,  $(N-1)$  capacitors are used on dc bus,  $2(N-1)$  switching devices,  $(N-1) * (N-2)/2$  auxiliary capacitors, Total capacitors ( $Nc$ ) required are

$$Nc = \sum_{j=1}^N (N-j) = [(N-1)*(N-2)/2 + (N-1)]$$

**Table 2-2: Switching sequence of 3 level flying capacitor Multilevel inverter**

Switching combination		Output Voltage $V_{an}$
Switches ON	Switches OFF	
S <sub>1</sub> , S <sub>2</sub>	S <sub>3</sub> , S <sub>4</sub>	$V_{dc}$
S <sub>1</sub> , S <sub>3</sub>	S <sub>2</sub> , S <sub>4</sub>	0
S <sub>3</sub> , S <sub>4</sub>	S <sub>1</sub> , S <sub>2</sub>	- $V_{dc}$



**Figure 2-5: Three-level Flying capacitor Multilevel inverter**

#### **2.4.1 Applications of Flying Capacitors Multilevel Inverter**

- Induction motor control using DTC (Direct Torque Control) circuit.
- Static VAR generation.
- Both AC-DC and DC-AC conversion applications.
- Converters with Harmonic distortion capability.
- Sinusoidal current rectifiers.

#### **2.4.2 Advantages:**

- Huge amount of storage capacitors will provide additional ride through capabilities during power rage.
- Switch combination redundancy are provided for balancing different voltage levels.
- When the number of levels is high enough, the harmonic content will be low enough not to use the filter.
- We are able to control both the real and reactive power flow, and making a possible voltage source converter candidate for high voltage dc transmission.

#### **2.4.3 Disadvantages:**

- When the number of converter levels get high, a huge amount of storage capacitor is required. Those high-level systems are more difficult to package and those bulky capacitors are expensive.
- The switching frequency and switching losses will soar high for real power transmission and the converter control will get very complicated.

### **2.5 Cascaded H-Bridge Multilevel Inverter**

A cascaded H-bridge multilevel inverter (CHB) is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Such inverters have been the subject of research in the last several years, where the DC levels were considered to be identical in that all of them were either batteries, solar cells, etc.

The number of units to be connected in series to obtain an  $N$  level (odd) of the output voltage is given as

$$M = \frac{N-1}{2}$$

where  $N$  is the number of output levels and

$M$  is the number of H-bridge unit

Currently, each phase of a cascade H-bridge multilevel inverter requires ' $N$ ' DC sources for ' $2N+1$ ' levels in applications that involve real power transfer.

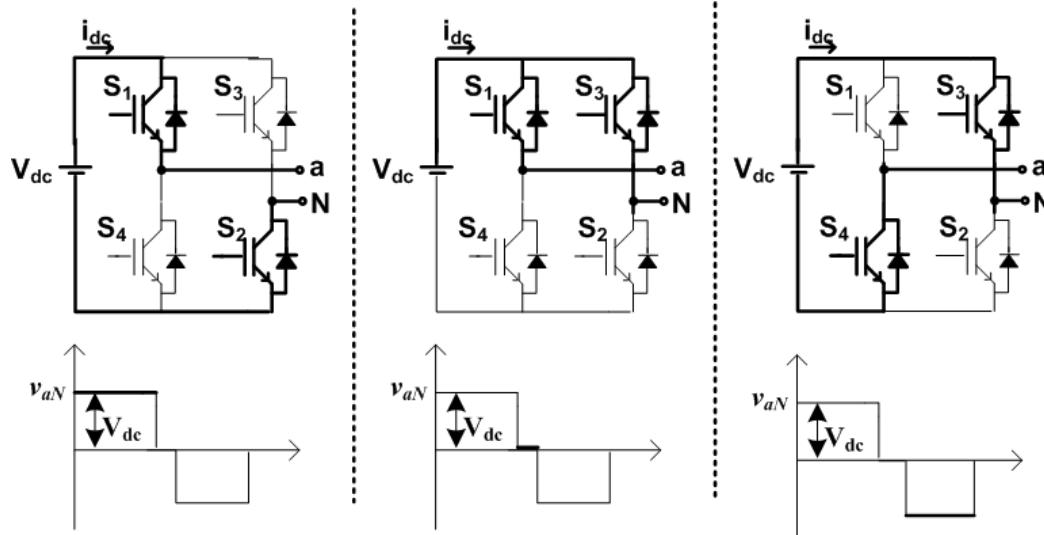


Figure 2-6: Three-level Cascaded H-bridge Multilevel inverter

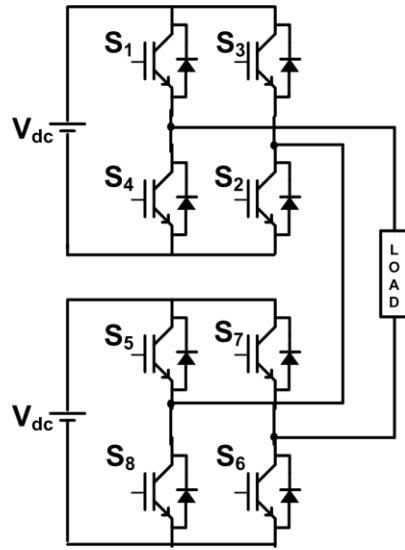
Table 2-3: Switching sequence of Three-level Cascaded H-bridge Multilevel inverter

Switching combination		Output Voltage V <sub>an</sub>
Switches ON	Switches OFF	
S <sub>1</sub> , S <sub>2</sub>	S <sub>3</sub> , S <sub>4</sub>	V <sub>dc</sub>
S <sub>1</sub> , S <sub>3</sub>	S <sub>2</sub> , S <sub>4</sub>	
S <sub>2</sub> , S <sub>4</sub>	S <sub>1</sub> , S <sub>3</sub>	0
S <sub>3</sub> , S <sub>4</sub>	S <sub>1</sub> , S <sub>2</sub>	-V <sub>dc</sub>

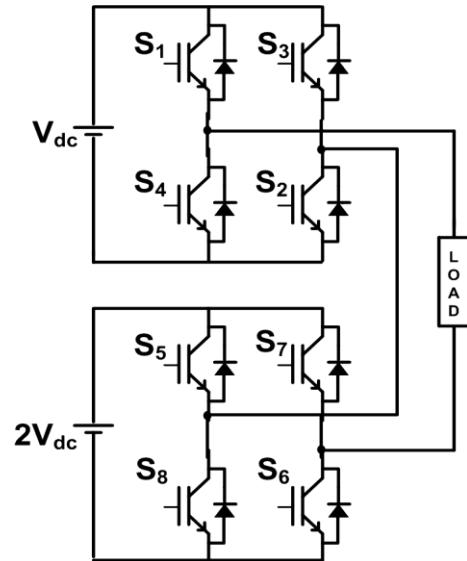
Based on the values of DC voltage sources, CHB is classified as

- **Symmetric CHB:** It is the inverter in which equal DC voltages are used in H-bridge cells.
- **Asymmetric CHB:** It is the inverter in which unequal DC voltages are used in H-bridge cells. With unequal DC voltages, the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells.

Following **figure 2-6** and **2-7** represent symmetric Five-level and asymmetric Seven-level CHB



**Fig 2-7: Five-level Symmetric CHB**



**Fig 2-8: Seven-level Asymmetric CHB**

**Table 2-4: Switching sequence of Symmetric 5- Level CHB**

Switching Combination		Output Voltage $V_{an}$
Switches ON	Switches OFF	
S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	2V <sub>dc</sub>
S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>1</sub> , S <sub>2</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	
S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>7</sub> , S <sub>8</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	
S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>2</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>1</sub> , S <sub>2</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	0
S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>7</sub> , S <sub>8</sub>	
S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>2</sub> , S <sub>7</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	-V <sub>dc</sub>
S <sub>2</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>6</sub>	
S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	-2V <sub>dc</sub>

**Table 2-5: Switching sequence of Asymmetric 7- Level CHB**

Switching Combination		Output Voltage $V_{an}$
Switches ON	Switches OFF	
S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	3V <sub>dc</sub>
S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	2V <sub>dc</sub>
S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>7</sub> , S <sub>8</sub>	
S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	V <sub>dc</sub>
S <sub>1</sub> , S <sub>2</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	0
S <sub>1</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>6</sub> , S <sub>8</sub>	
S <sub>2</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>7</sub>	
S <sub>3</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>7</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>6</sub> , S <sub>8</sub>	-V <sub>dc</sub>
S <sub>3</sub> , S <sub>4</sub> , S <sub>6</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	
S <sub>1</sub> , S <sub>3</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>2</sub> , S <sub>4</sub> , S <sub>5</sub> , S <sub>6</sub>	-2V <sub>dc</sub>
S <sub>2</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>3</sub> , S <sub>5</sub> , S <sub>6</sub>	
S <sub>3</sub> , S <sub>4</sub> , S <sub>7</sub> , S <sub>8</sub>	S <sub>1</sub> , S <sub>2</sub> , S <sub>5</sub> , S <sub>6</sub>	-3V <sub>dc</sub>

### 2.5.1 Applications of Cascaded Multilevel Inverter:

- Motor drives
- Active filters
- Electric vehicle drives.
- DC power source utilization
- Power factor compensators
- Back to back frequency link systems
- Interfacing with renewable energy resources.

### 2.5.2 Advantages:

- The modularized structure allows easy packaging and storage.
- The quantity of possible voltage levels is more than DC and FC type.

### 2.5.3 Disadvantages:

- Separated DC sources or capacitor are required for each module.
- A more complex controller is required due to the number of capacitors, which need to be balanced.

**Table 2-6: Comparison of different topologies of Multi-level Inverters**

	DIODE CLAMPED	FLYING CAPACITOR	CASCADED H-BRIDGE
<b>Output voltage (phase) levels for star connected load</b>	N	N	N
<b>Power semiconductor switches (Three phase)</b>	$6(N-1)$	$6(N-1)$	$6(N-1)$
<b>Clamping diodes (Independent)</b>	$3(N-1)(N-2)$	0	0
<b>DC bus capacitors</b>	$N-1$	$(N-1)$	$\frac{(3N - 3)}{2}$
<b>Balancing capacitors</b>	0	$\frac{3(N - 1)(N - 2)}{2}$	0
<b>Voltage unbalancing problem</b>	Average	High	Very small
<b>Modularity</b>	Less	Less	High
<b>Asymmetrical input voltage configuration</b>	Not possible	Not possible	Possible
<b>Output voltage (line-to-line) levels</b>	$(2N-1)$	$(2N-1)$	$(2N-1)$
<b>Switching states of the converter (in the SVD including multiple states)</b>	$N^3$	$N^3$	$N^3$
<b>Applications</b>	Motor drive system, STATCOM	Motor drive system, STATCOM	Motor drive system, PV, fuel cells, battery sys

## 2.6 Preference of CHB over Diode Clamped and Flying Capacitor Topologies

- The number of possible output voltage levels is more than twice the number of dc sources.
- In case of any fault in H-bridge, it can be checked and replaced without disturbing the operation, unlike in diode clamped and flying capacitor.
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.
- The output voltage obtained is twice the input voltage to CHB (symmetrical source) when compared to flying capacitor and diode clamped, hence it is used in high power applications.
- CHB does not require any clamping diode and capacitors & the THD values of all the configurations are comparable (decrease with increase in levels).

### **3.CONTROL TECHNIQUES OF MULTILEVEL INVERTERS**

#### **3.1 Control Techniques for Inverter output**

Modulation is the process of switching the power electronic device in a power converter from one state to another. All modulations are aimed at generating a stepped waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency and phase fundamental component that is usually sinusoidal in steady state.

The requirements of multilevel modulation algorithm are as follows:

1. Voltage quality should be good
2. Modular design
3. Simultaneous switching of multiple voltage levels is not allowed
4. Switching frequency of power devices should be minimized
5. Power modules should share the load equally
6. Control algorithm should be simple
7. Implementation cost should be low

In many industrial applications, the output voltage of inverters should be controlled to overcome the changes in input voltage and to meet the need of v/f control. The most efficient method of controlling the output voltage is to incorporate **Pulse Width Modulation (PWM)** control within the inverters. In addition to PWM method, there are methods involving external control of AC output voltage and DC input voltage. To distinguish these methods from the PWM method, PWM method is referred to as the internal control method since the output voltage control is realized by means of modifications in the conduction patterns of the inverter switches.

The various methods for the control of output voltage of inverters can be enumerated as follows:

1. External control of the AC output voltage
2. External control of the DC input voltage
3. Internal control of the inverter output voltage

In the first two methods, extra circuits for the control of either DC input or AC output become necessary. The third method, however, does not require such circuits. The first two methods require the use of peripheral components whereas the third method requires no external components. Mostly the internal control of the inverters is dealt, and so the third method of control is discussed in great detail in the following section.

#### **3.2 Internal Pulse Control of Multilevel Inverter Output**

Pulse width modulation is the most commonly used technique to control the output voltage of inverter. Pulse width modulation is a technique in which a fixed input dc voltage

is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components.

The various techniques under this scheme are:

1. Sine PWM
2. Space Vector PWM
3. Third Harmonic Injection

The advantages possessed by PWM technique are:

1. The output voltage control with this method can be obtained without any additional components.
2. With this method, lower order harmonics can be eliminated or minimized along with its output voltage control. As higher order harmonics can be filtered easily, the filtering requirements are minimized.

The main disadvantage of this method is that the SCRs are expensive as they must possess low turn on and turn off times.

The gating signals are generated by comparing a reference signal of amplitude  $A_r$  with a triangular carrier wave of amplitude  $A_c$ . The frequency of the reference signal determines the fundamental frequency of the output voltage.

The ratio of  $A_r$  to  $A_c$  is the control variable and defined as the **Amplitude Modulation Index** or **Modulation Index ( $M_a$ )** and is given by

$$M_a = \frac{A_r}{A_c}$$

### 3.3 Sine PWM:

The reference signal is taken as sinusoidal waveform whereas the carrier signal is taken as triangular waveform in this method. The width of pulse in the Sine PWM is not equal due to reference signal is taken as sinusoidal waveform. The amplitude of sinusoidal waveform is also not constant. The width of gate pulse is determined by intersect point of the sinusoidal waveform and triangular waveform. The frequency of inverter output voltage depends upon frequency of reference signal  $f_R$  and amplitude of reference signal  $V_R$  controls the modulation index ( $M_a$ ). It is to be noted that by controlling the modulation index one can control the amplitude of applied output voltage.

The modulation index is  $V_R/V_C$

Where  $V_R$  is amplitude of reference signal voltage  
 $V_C$  is amplitude of carrier signal voltage

Sine PWM is further classified as

1. Level shifted
  - a) In Phase Disposition (IPD)
  - b) Alternate Phase Opposite Disposition (APOD)
  - c) Phase Opposite Disposition (POD)
2. Phase Shifted

These are also called Carrier Based PWM schemes. Both the schemes are applied for CHB inverters.

### 3.4 Level-shifted Sine PWM scheme

In Level shifted SPWM technique, we use carrier waves which are shifted by certain amplitude. The gating signal can be generated by comparing a sinusoidal reference signal with a triangular carrier wave and the width of each pulse varied proportionally to the amplitude of a sine wave. Maximum gate pulse width is obtained at the sinusoidal peak.

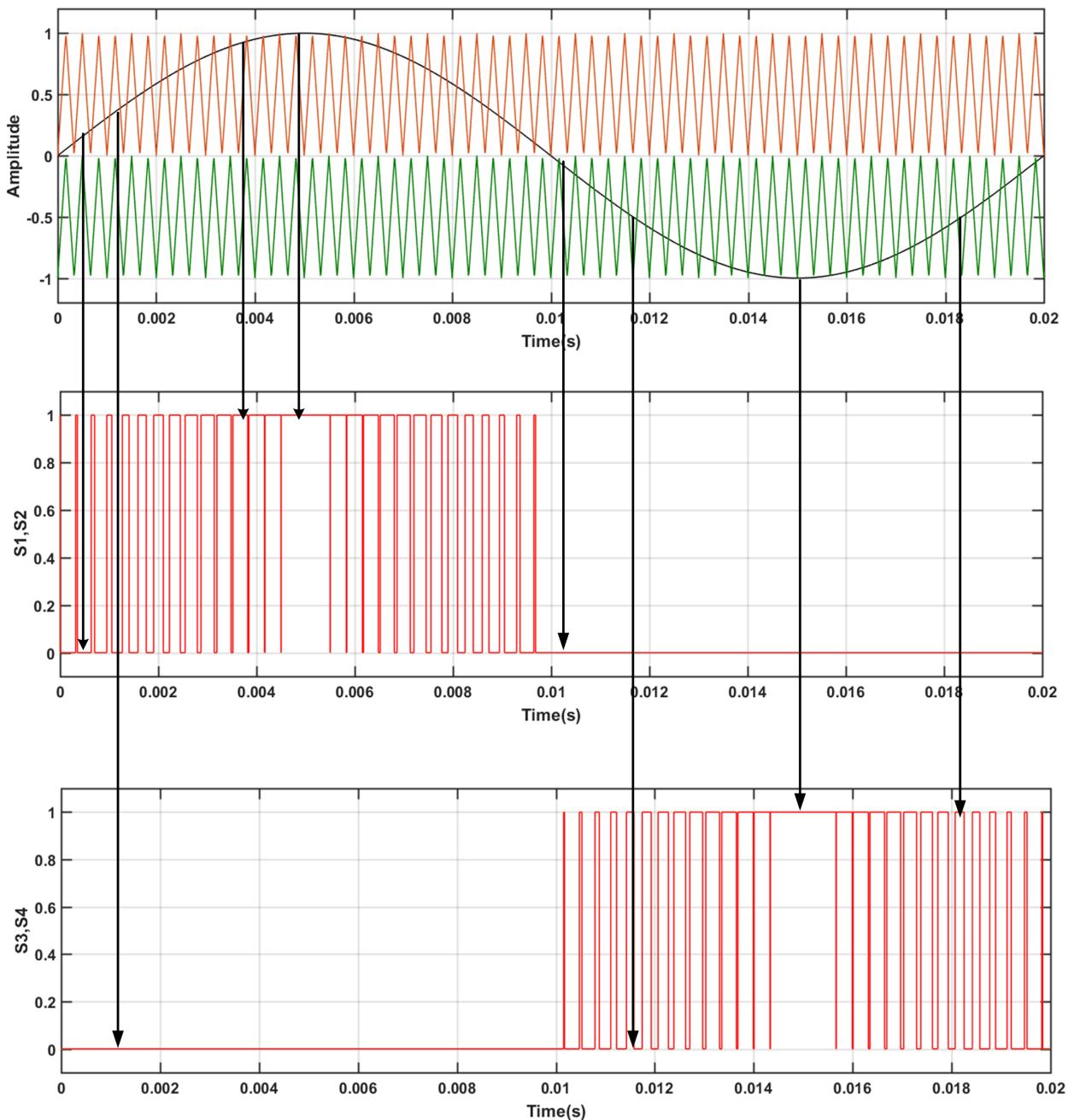
For carrier signals, the time values of each carrier waves are set to [0 1/6000 1/3000] while the outputs values are set according to the disposition of carrier waves.

After comparing, the output signals of comparator are transmitted to the switches (IGBT). It requires (**N-1**) triangular carriers, all having the same frequency and amplitude, where ‘N’ is number of levels in output of phase voltage. The frequency modulation index ( $m_f$ ) is given by  $m_f = f_{cr}/f_m$ . The switching frequency of the inverter using the level-shifted modulation is equal to the carrier frequency, that is, (device switching frequency)  $f_C = f_{cr}$ , where  $f_C$  is switching frequency of inverter. Average device switching frequency is  $f_C = f_{cr}/(N - 1)$ . The conduction time of the devices is not evenly distributed either.

Level shifted SPWM is further classified into three types based on the pattern of shift of carrier waves.

#### 3.4.1 In-Phase Disposition (IPD)

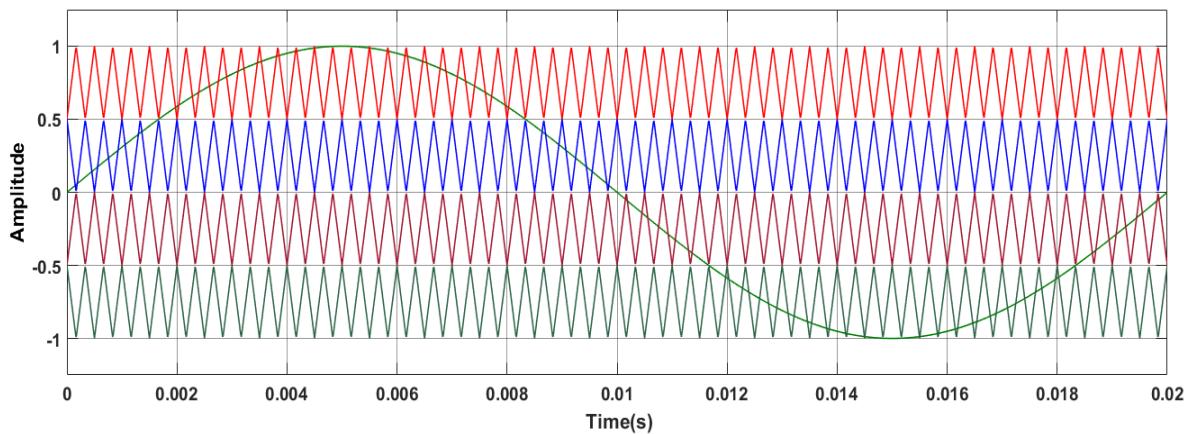
In this method for N-level inverter (N-1) carrier signals are required. These carrier waves have same amplitude and frequency where there is no phase shift between them. But these carriers are at different offset values. This method is suitable in CHB inverters. The comparison between the modulating and carrier wave for IPD SPWM is shown in figure 3-1. The gate pulses for upper and lower switches are shown in figure 3-1. Above modulation are carried at unity modulation index.



**Figure 3-1: Switching pattern produced using the IPD carrier-based PWM scheme**  
**(a) Modulation and carrier waveforms (b) S1, S2 (c) S3, S4**

### 3.4.2 Alternative Phase opposite Disposition (APOS)

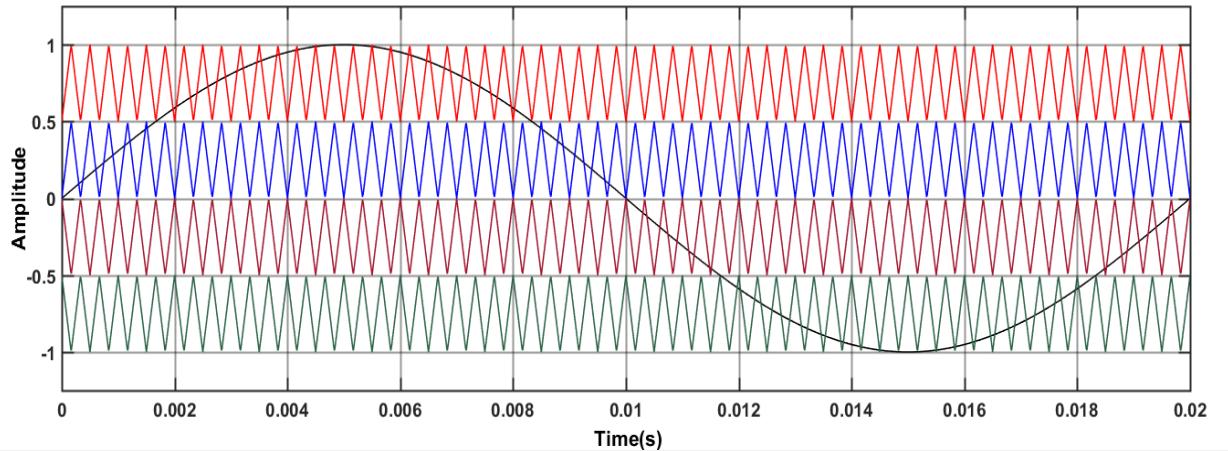
Alternative Phase Opposite Disposition (APOS), for N level inverter, (N-1) carrier waves are used. In this technique all the (N-1) carrier waves are alternatively in phase opposition with each other.



**Figure 3-2: Simulation of carrier-based PWM scheme using APOD for a five-level inverter. (a) Modulation signal and carrier waveforms**

### 3.4.3 Phase Opposite Disposition (POD)

In Phase Opposite Disposition (POD), for  $N$  level inverter,  $(N-1)$  carrier waves are used. In which the carrier wave above the zero reference are in same phase and the carrier wave below the zero reference are in same phase. The simulation using POD can be seen in figure 3-3.



**Figure 3-3: Simulation of carrier-based PWM scheme using POD. (a) Modulation signal and phase carrier waveforms**

The modulating signal of each phase is displaced from each other by  $120^\circ$ . All the carrier signals have same frequency  $f_C$  and amplitude  $A_C$  while the modulating signal has a frequency of  $f_r$  and amplitude of  $A_r$ . The switching pattern in carrier-based schemes is produced by comparing the carrier waves with the modulating wave. The carrier waves above zero reference are compared with modulating wave to generate positive half output voltage, whereas carrier waves below zero reference are responsible for negative half output voltage. In positive half cycle, whenever amplitude of modulating wave is greater than

carrier, switches will be on whereas in negative half cycle, when amplitude of modulating wave is lesser than carrier then switches will be turned on. The switching patterns produced for 3-level IPD technique can be observed in figure 3-1.

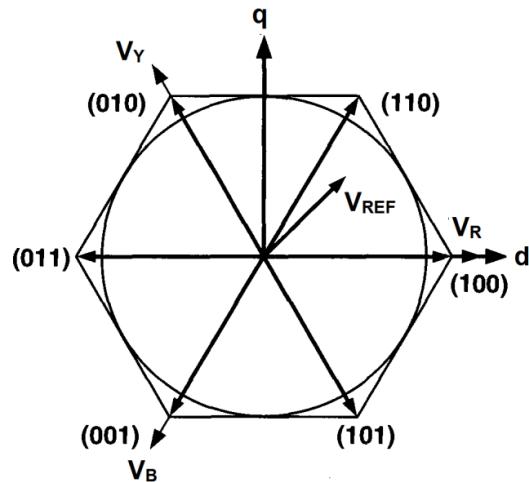
### 3.5 Phase Shifted Sine PWM scheme

In Phase Shifted Sine PWM all the triangular carriers have the same frequency and same peak-peak amplitude. But there is a phase shift between any two adjacent carrier waves. For  $m$  Voltage levels ( $N-1$ ) carrier signals are required and they are phase shifted with an angle of  $\theta = (360^\circ/N-1)$ . The gate signals are generated with proper comparison of carrier wave and modulating signal.

In general, a multilevel inverter with  $m$  voltage levels requires  $(N - 1)$  triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by  $\text{Ph}_{\text{CR}} = 360^\circ / (N - 1)$ .

### 3.6 Space Vector PWM

Space Vector modulation technique is another method available for obtaining output voltage above that of the standard Sine PWM technique. This is achieved by rotating a reference vector around the state diagram, which is composed of six basic non zero vectors forming a hexagon. The complete full circular rotation of the reference vector in the state diagram constitutes unit pulse time cycle i.e. 20ms for a frequency of 50Hz.



**Figure 3-4: Space Vector representation**

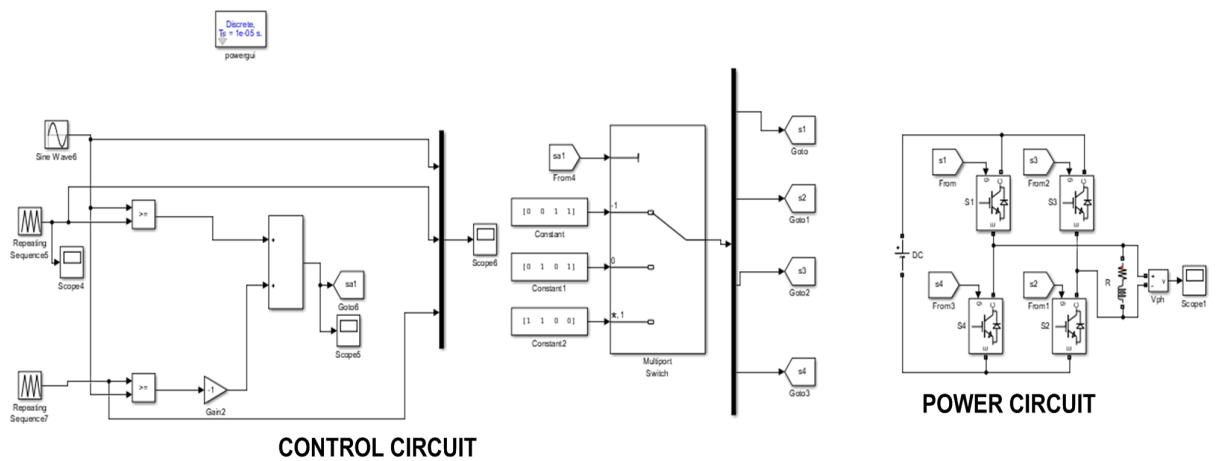
### 3.7 Why SPWM is advantageous?

- The advantage of this technique is that all the dominant harmonics are concentrated at the carrier frequency.
- By properly designing a filter, those dominant harmonics can be eliminated.
- The higher order harmonics are of low magnitude anyways and also by SPWM they are bypassed as it tries to concentrate all the harmonics at the carrier frequency.
- The filter requirements are reduced. Hence size of the system is reduced.

### 3.8 Simulations & Results

In this project, MATLAB SIMULINK is used for simulations. Simulink, developed by Math Works, is a graphical programming environment for modelling, simulating and analyzing multi domain dynamical systems. Its primary interface is a graphical block diagramming tool and a customizable set of block libraries. It offers tight integration with the rest of the MATLAB environment and can either drive MATLAB or be scripted from it. Simulink is widely used in automatic control and digital signal processing for multi domain simulation and Model-Based Design.

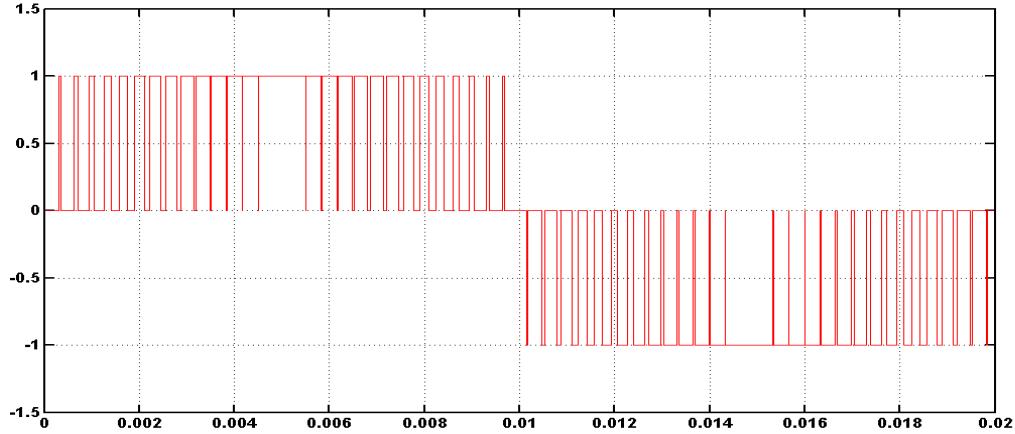
#### 3.8.1 Simulations of Three level CHB



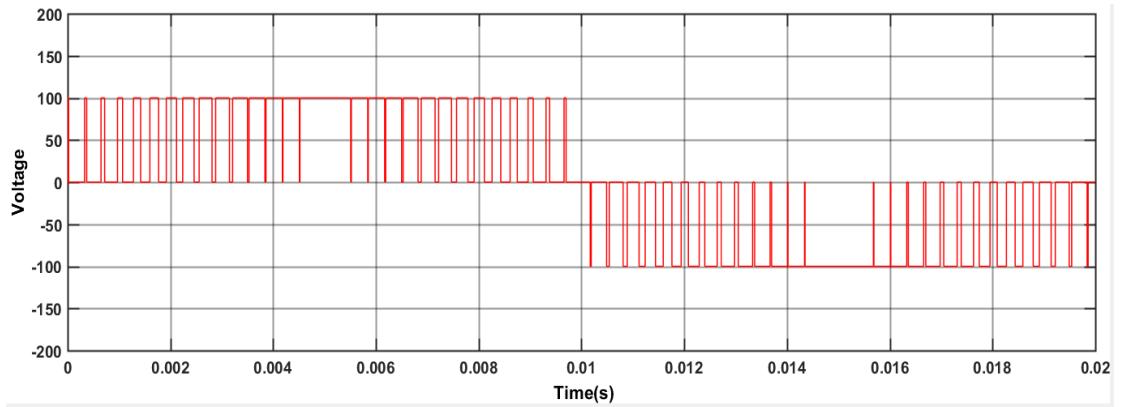
**Figure 3-5: Simulation circuit of Single phase three level CHB**

The power circuit and the control circuit for single phase three level CHB can be seen in figure 3-5. All the simulations of single-phase CHB circuits are carried out for  $V_{dc}=100V$  &  $M_a=1$ . In three level CHB, two carrier waves are there. Corresponding switching pulses are generated according to the switching logic of carrier based PWM schemes and these can be seen in figure 3-1. The switching pulses generated by comparison of modulating wave and carrier wave below zero reference are inverted and added through an adder block to obtain a combined switching pulse for a complete cycle which can be seen in

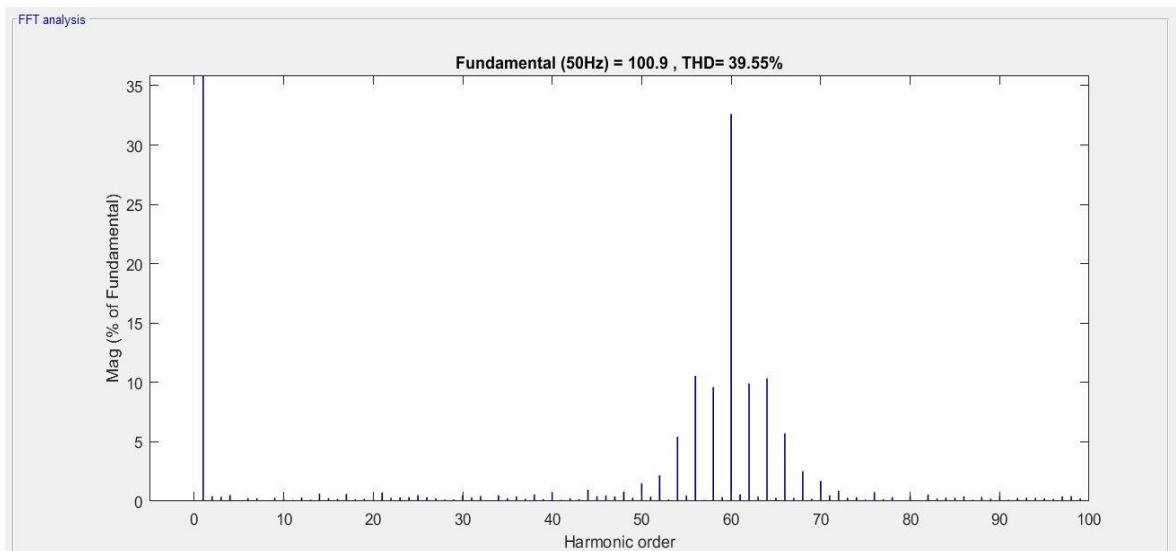
figure 3-6. According to the switching sequence of three level CHB, which is fed using multi-port switch, these switching pulses will be available to corresponding switches in CHB and hence a three-level voltage can be observed as output which is shown in figure 3-7. FFT analysis for % THD is shown in FFT window along with the fundamental peak voltage value in figure 3-8.



**Figure 3-6: Pulses output to multi-port switch**

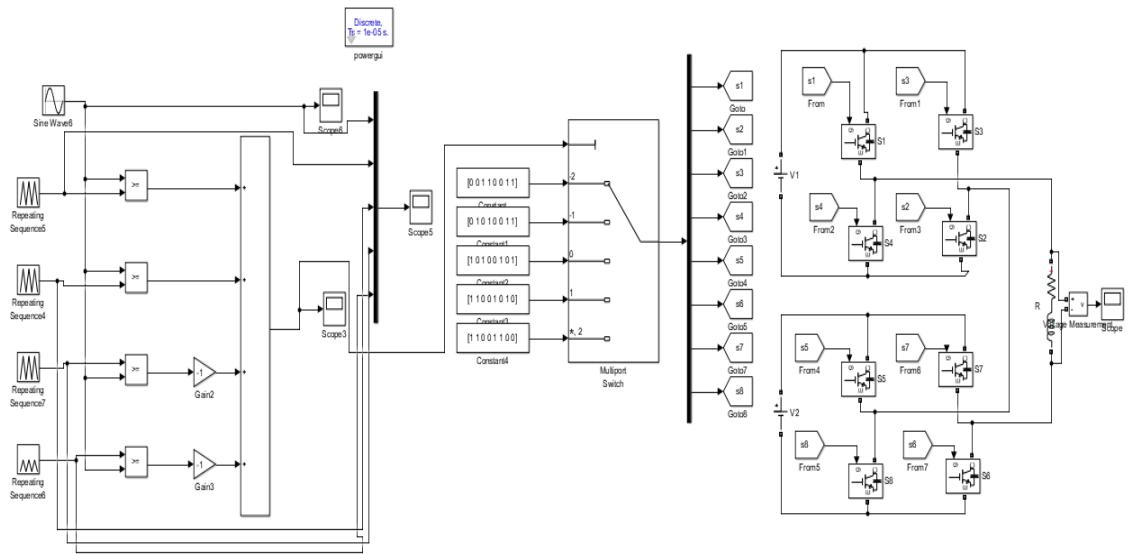


**Figure 3-7: Three level output phase voltage**

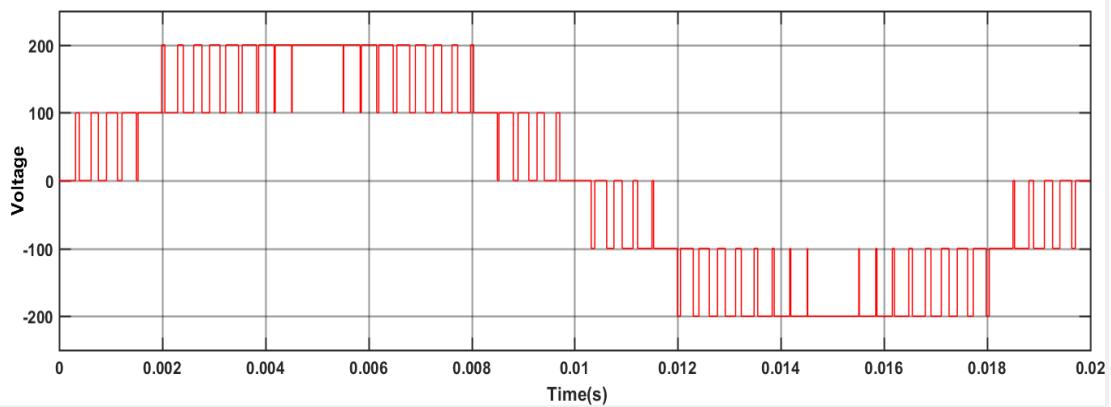


**Figure 3-8: FFT window of Single phase Three-level CHB**

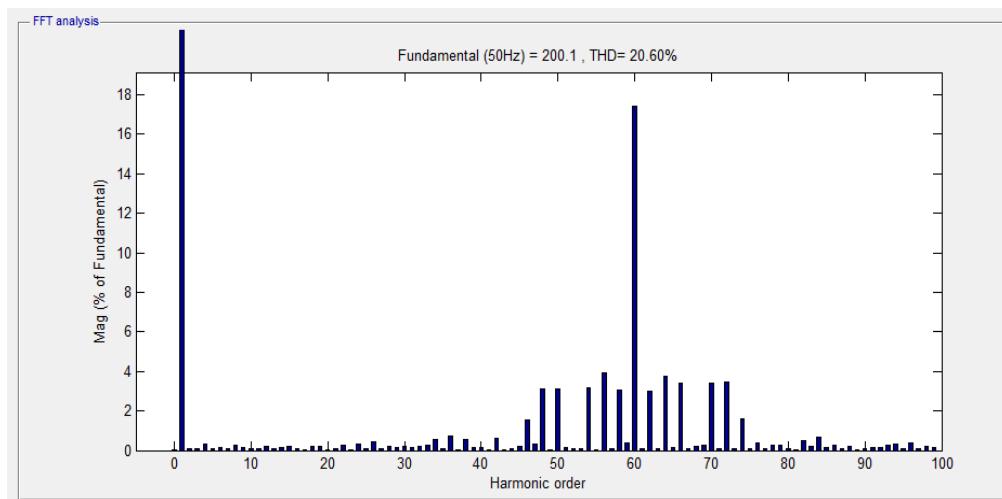
### 3.8.2 Simulations of Five-level CHB



**Figure 3-9: Simulation circuit of Single phase Five-level CHB**

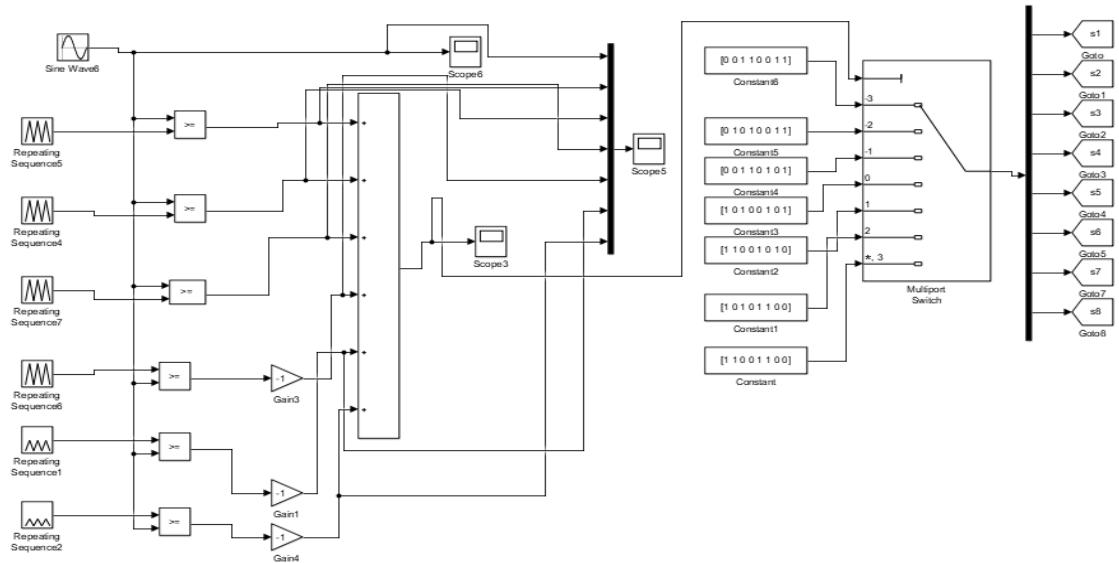


**Figure 3-10: Five-level output phase voltage**

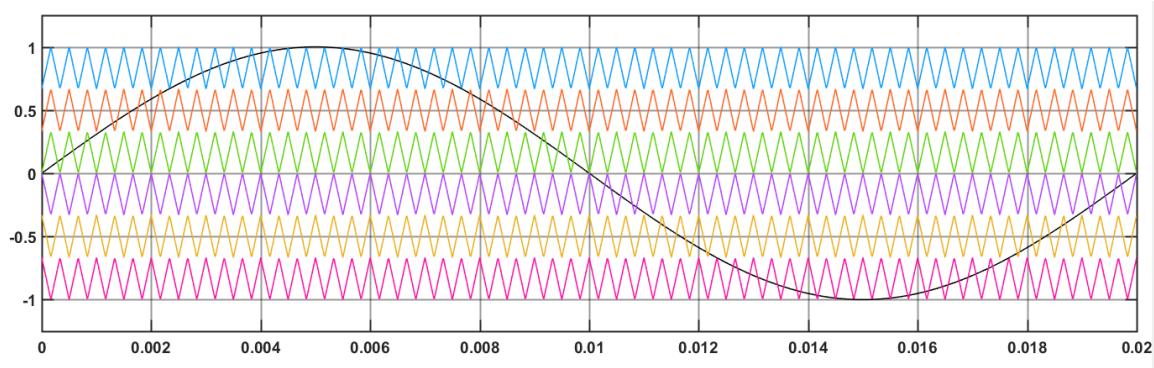


**Figure 3-11: FFT window for Five-level CHB**

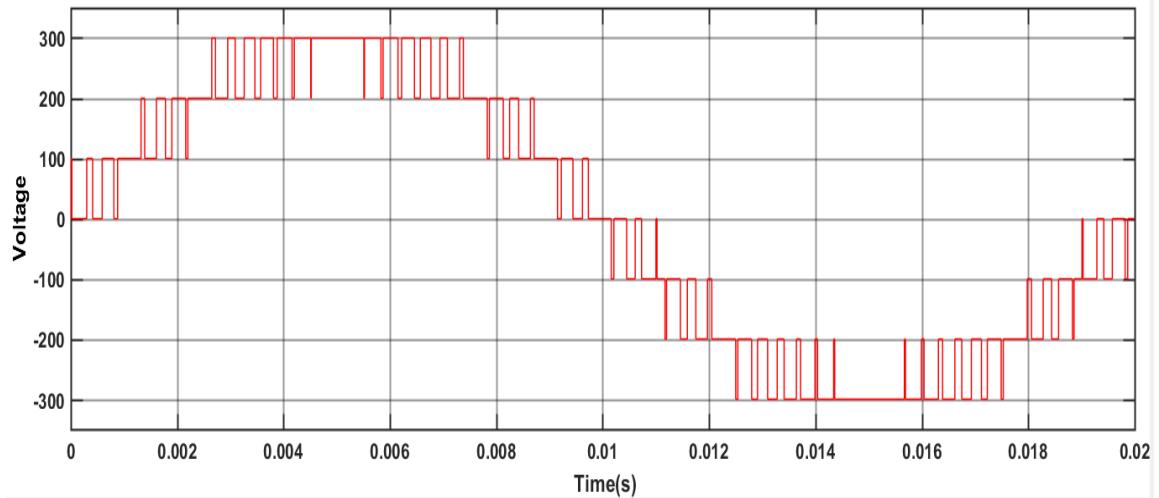
### 3.8.3 Simulations of Asymmetrical Seven-level CHB



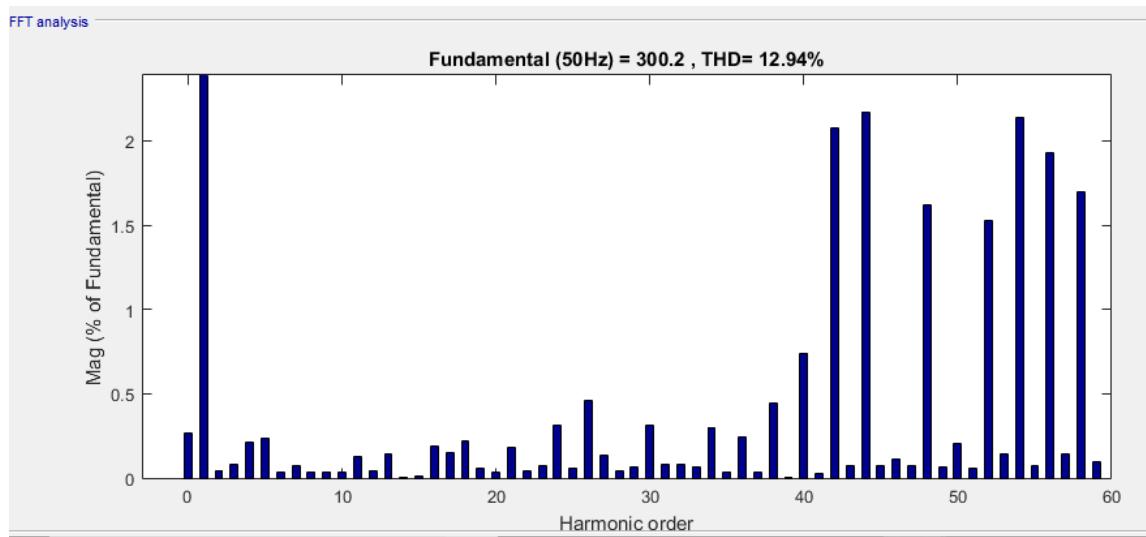
**Figure 3-12: Simulation of Control circuit of asymmetrical seven-level CHB**



**Figure 3-13: Modulation and carrier waves of asymmetrical seven-level CHB**

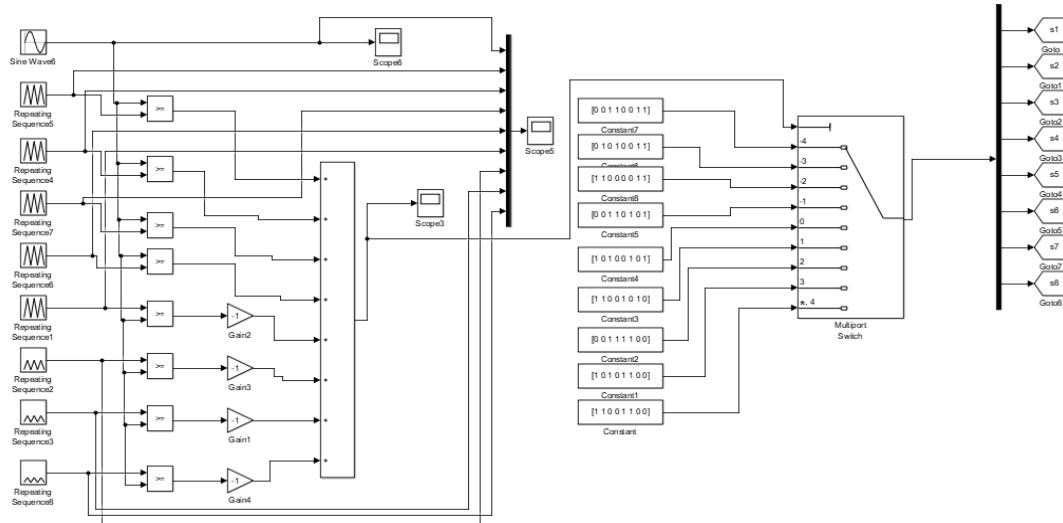


**Figure 3-14: Asymmetric seven-level output phase voltage**

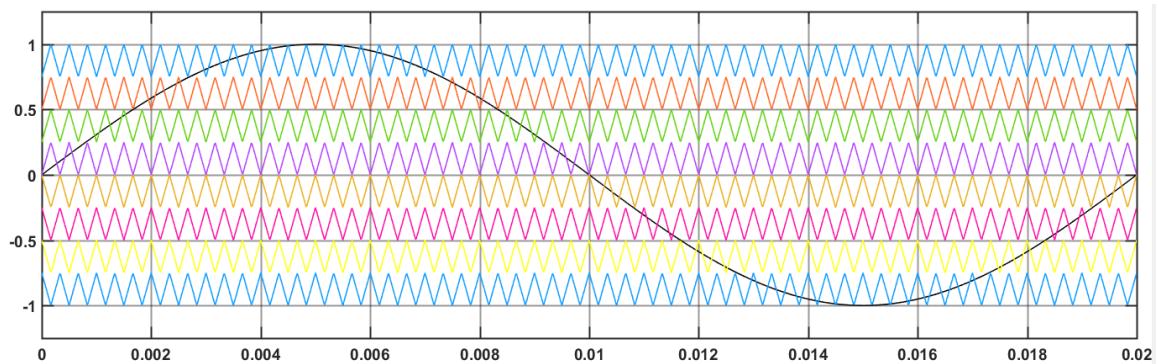


**Figure 3-15: FFT window of Asymmetric seven-level output phase voltage**

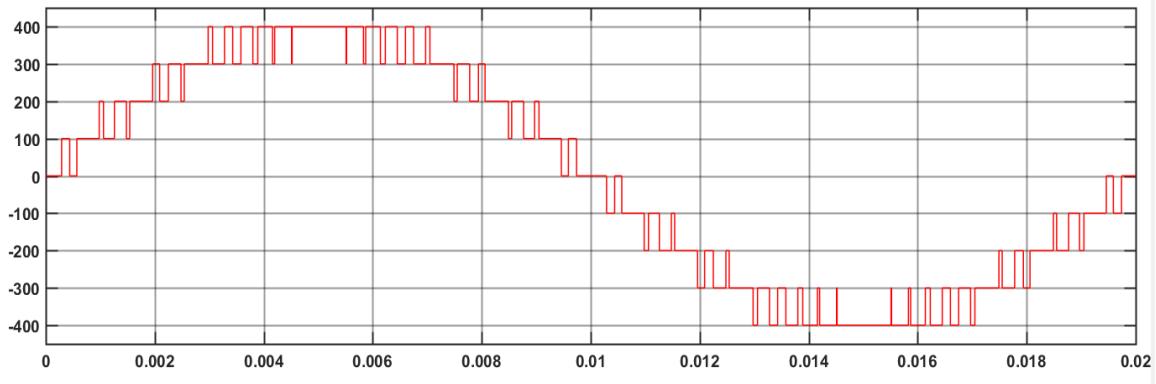
### 3.8.4 Simulations of Asymmetrical Nine-level CHB



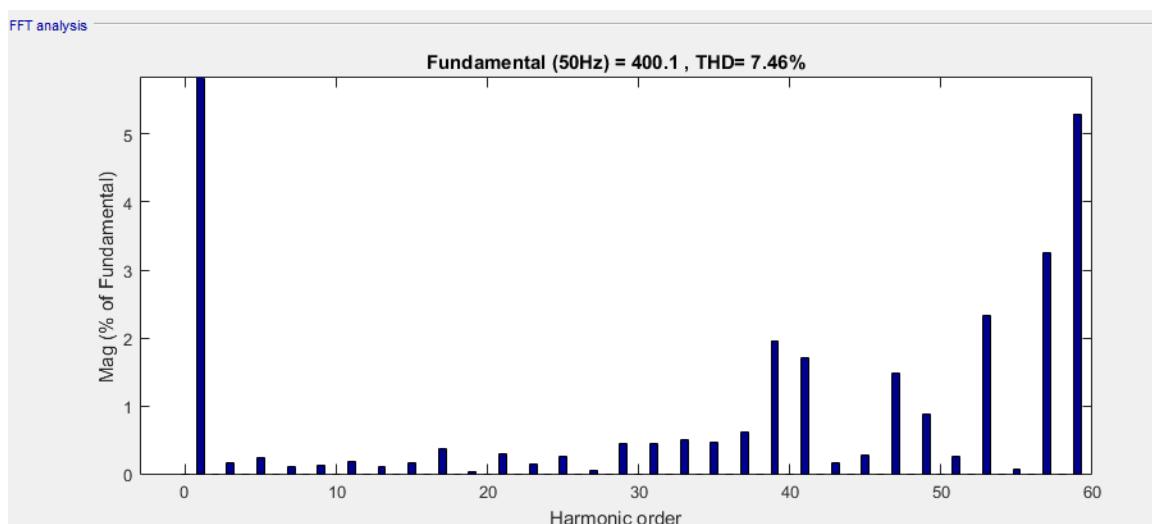
**Figure 3-16: Simulation of Control circuit of asymmetrical nine-level CHB**



**Figure 3-17: Modulation and carrier waves of asymmetrical nine-level CHB**



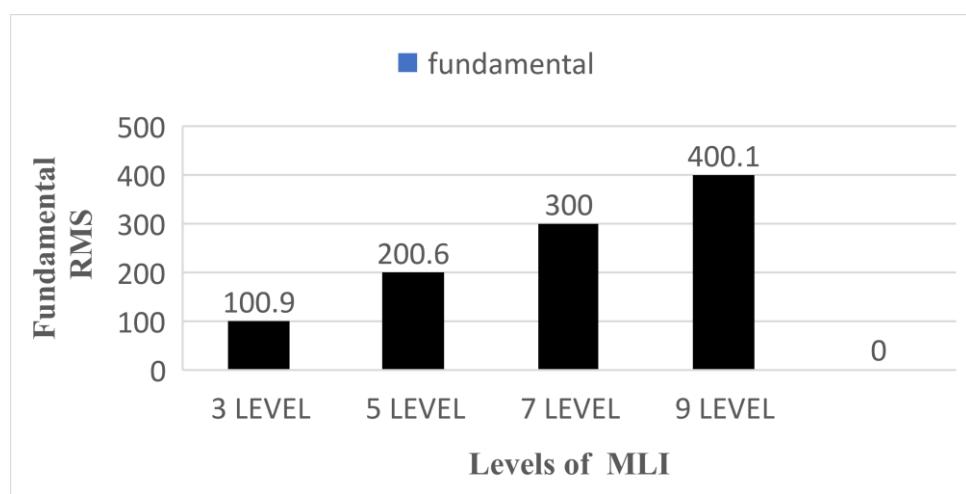
**Figure 3-18: Asymmetric nine-level output phase voltage**



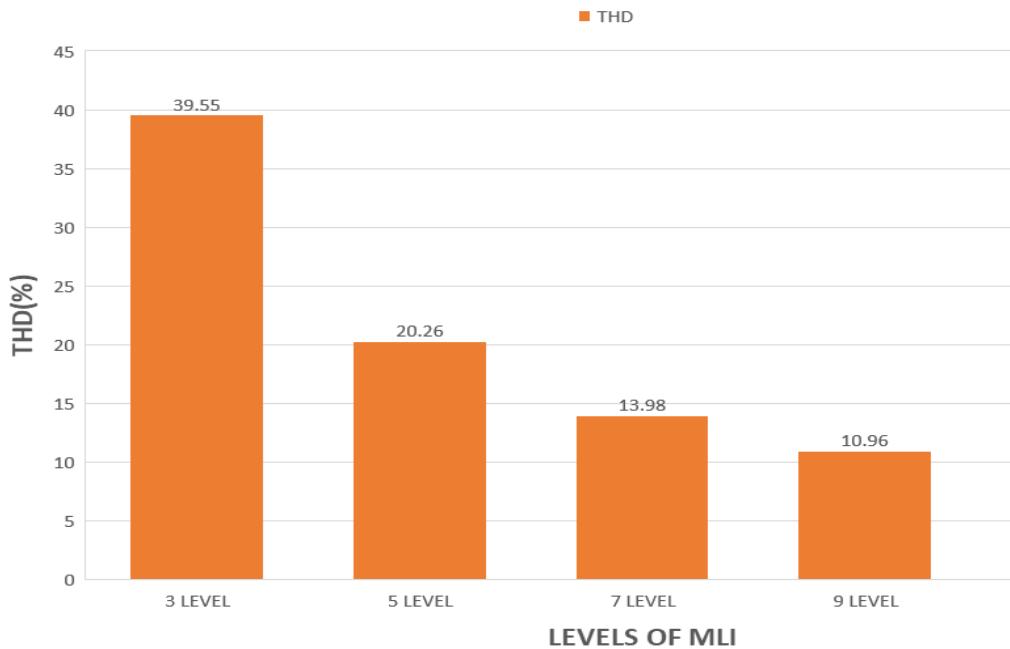
**Figure 3-19: FFT window of Asymmetric nine-level output phase voltage**

### 3.8.5 Effect of increase in levels

As levels in multi-level inverter goes on increasing the % THD will be reduced and steps in phase voltage will be increased and waveform will be closer to sinusoidal.



**Figure 3-20: Levels Vs Fundamental voltage**

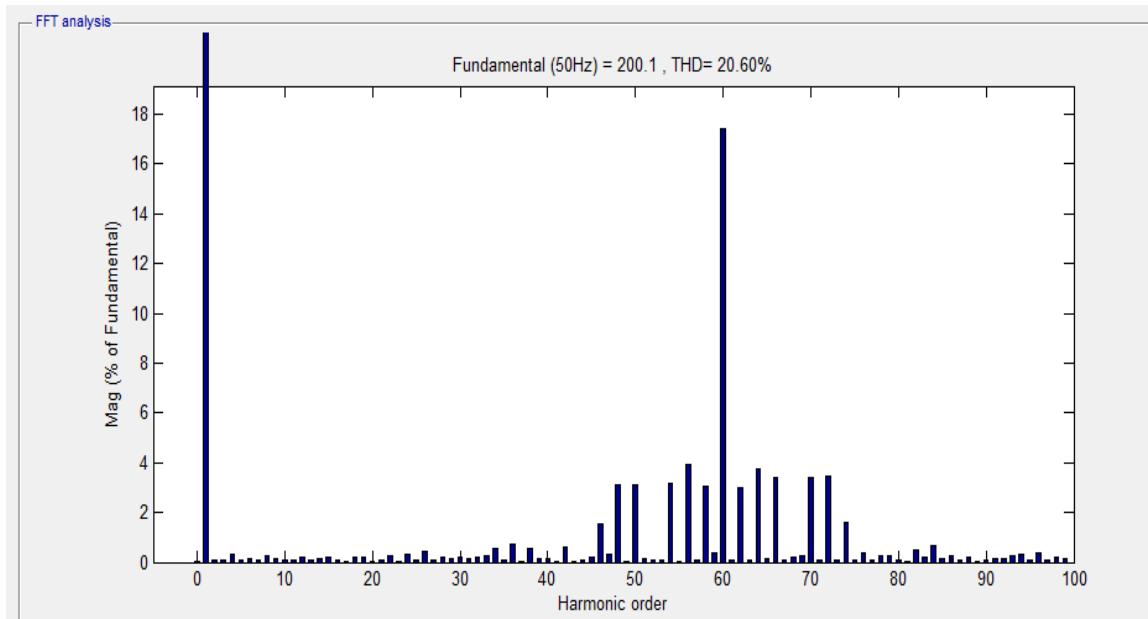


**Figure 3-21: Levels Vs %THD**

### 3.9 Comparative analysis of Carrier based PWM schemes

The comparative analysis of all the three-carrier based PWM schemes (IPD, APOD, POD) is carried out on symmetrical five-level CHB.

#### (a) In Phase Disposition (IPD)



**Figure 3-22: FFT window for Five-level CHB IPD technique**

### (b) Alternate Phase Opposite Disposition (APOD)

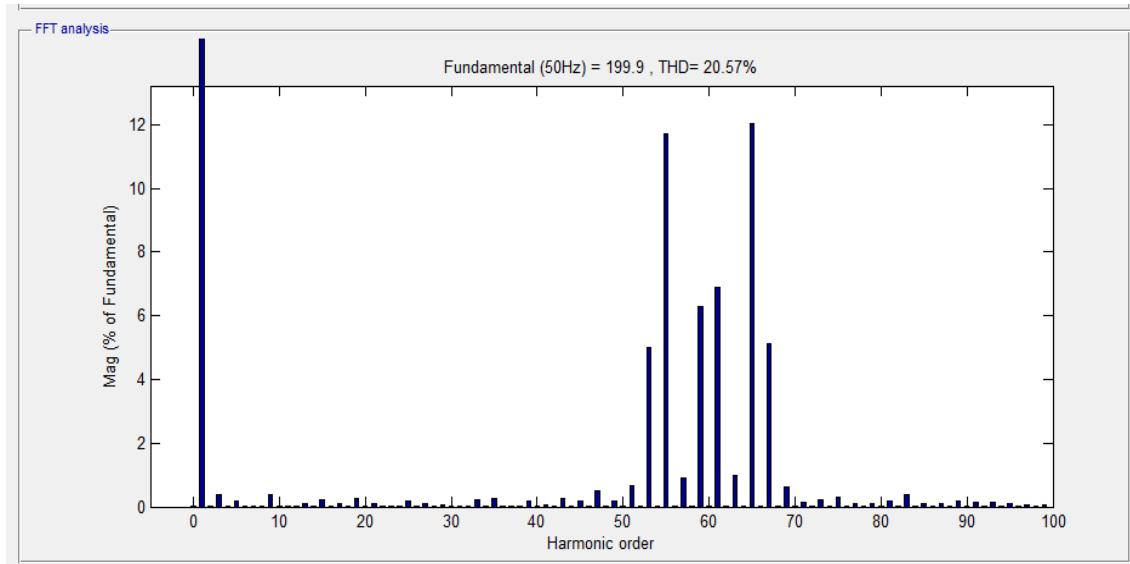


Figure 3-23: FFT window for Five-level CHB APOD technique

### (c) Phase Opposite Disposition (POD)

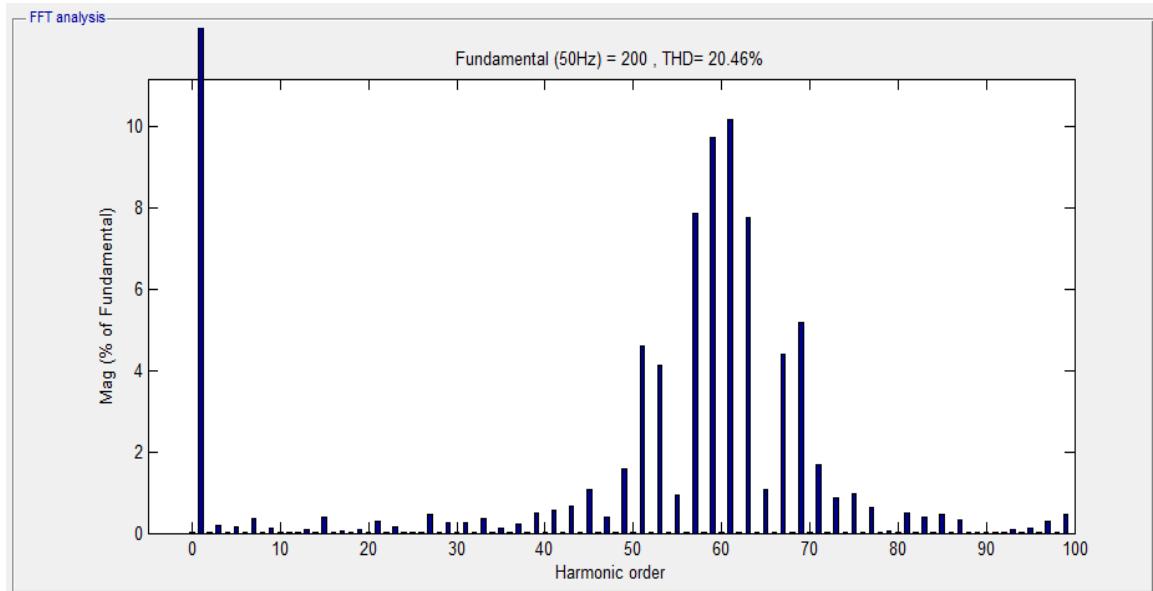
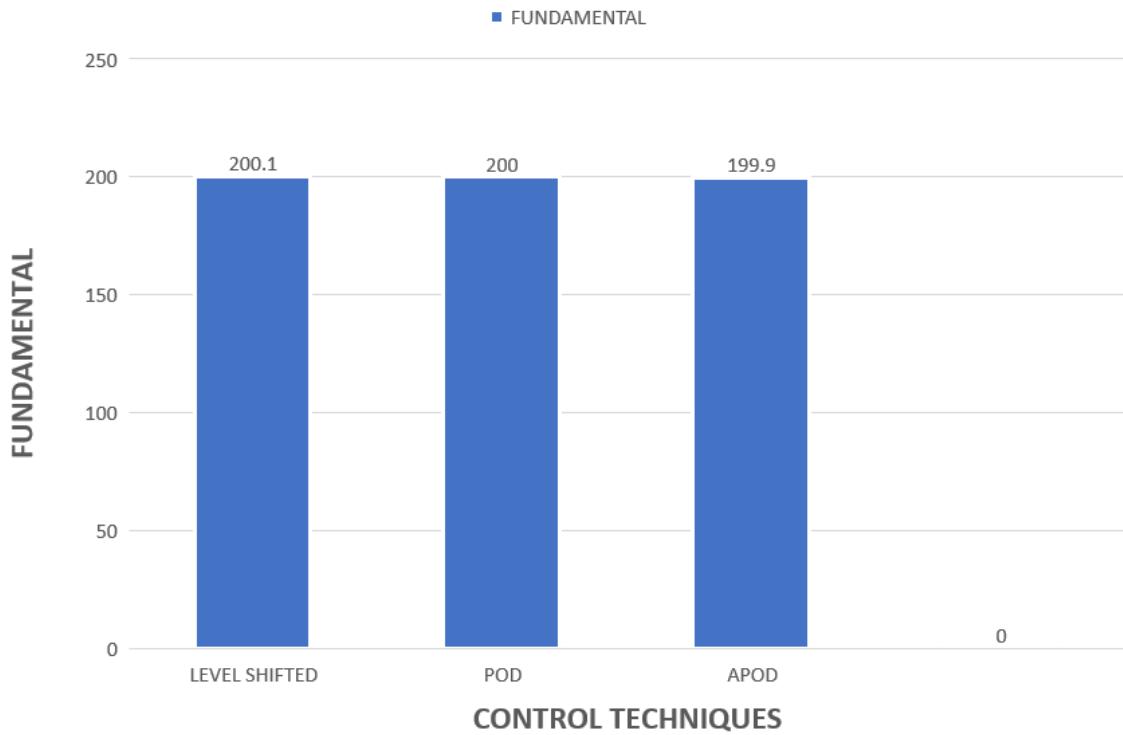
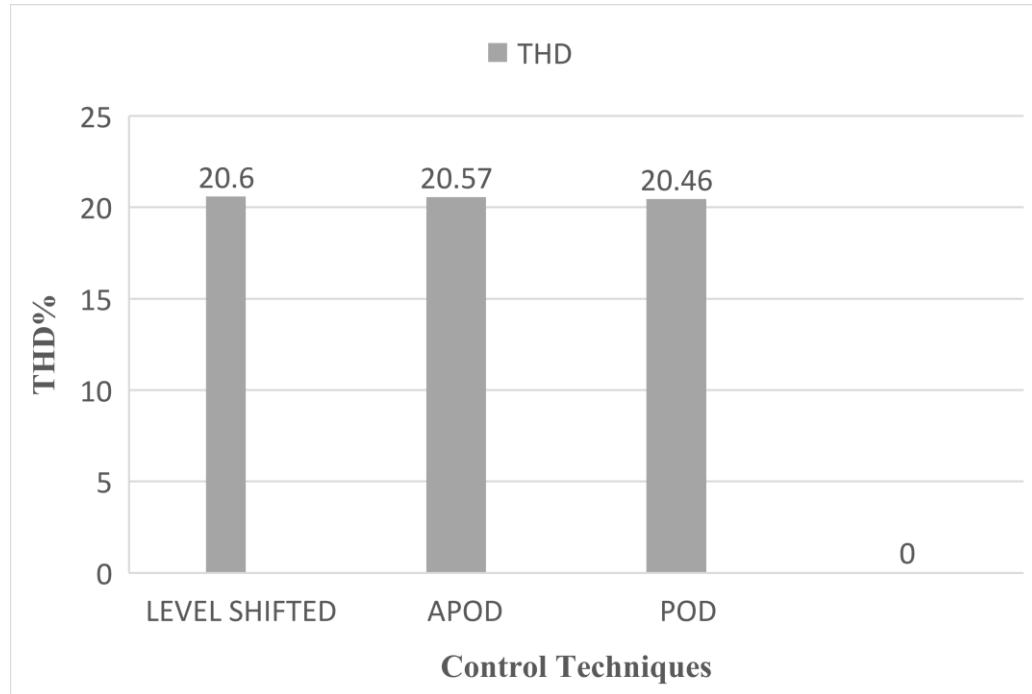


Figure 3-24: FFT window for Five-level CHB POD technique

On comparing all the three- carrier based PWM schemes, we can see that there is no much variation in fundamental voltage of output but the % THD is varying by driving the system towards closer to sinusoid i.e., improvement in system performance.



**Figure 3-25: Variation in fundamental voltage with PWM technique**



**Figure 3-26: Variation in %THD with PWM technique**

By observing the results, it can clearly conclude that **POD** technique is giving the better %THD performance. Hence, the further analysis is carried out based on **POD carrier based PWM scheme**.

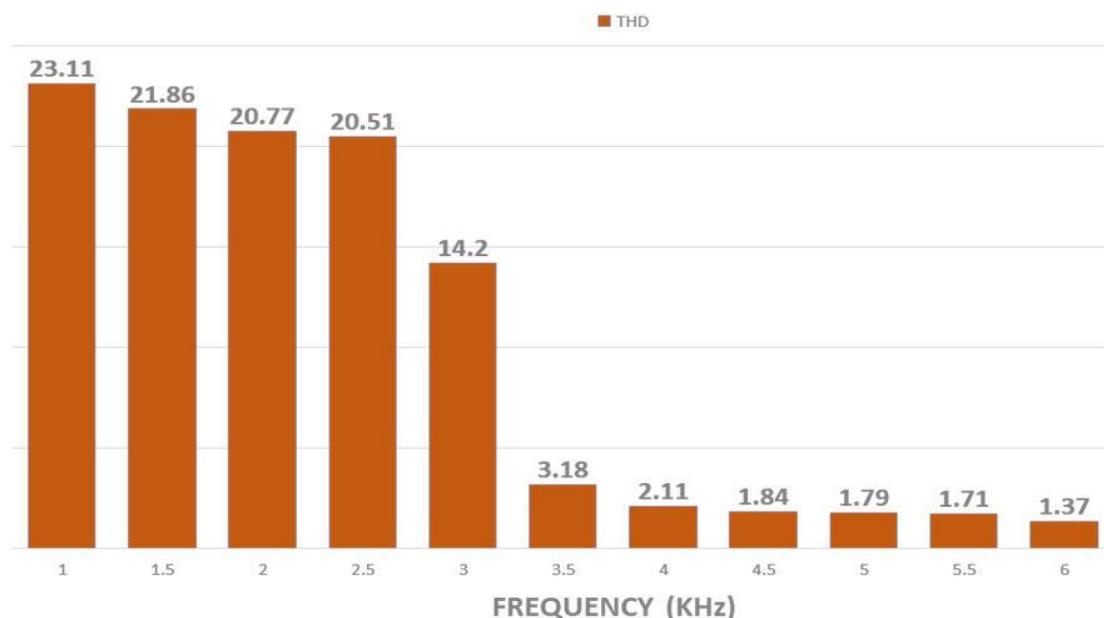
### 3.10 Effect of change in Carrier frequency

It is observed on symmetrical five-level Cascaded H-bridge.

- It is observed from previous simulations that the POD technique has less %THD in comparison to other multi-carrier SPWM techniques.
- The effect of increase in the switching frequency of carrier signals is observed in the simulation and %THD decreases with increase in frequency.
- This is because the dominant harmonics get concentrated at switching frequency in case of multicarrier SPWM techniques.
- There is not much variation in fundamental voltage.

**Table 3-1: %THD and fundamental voltage variation with  $F_c$**

<u><math>F_c</math> (KHz)</u>	<u>THD%</u>	<u>FUNDAMENTAL (V)</u>
1	23.11	200.5
1.5	21.86	201
2	20.77	199.8
2.5	20.51	199.8
3	14.20	200
3.5	3.18	199.7
4	2.11	200.7
4.5	1.84	200.2
5	1.79	198.6
5.5	1.37	200.2
6	1.11	200



**Figure 3-27: Variation in %THD with Carrier frequency ( $F_c$ )**

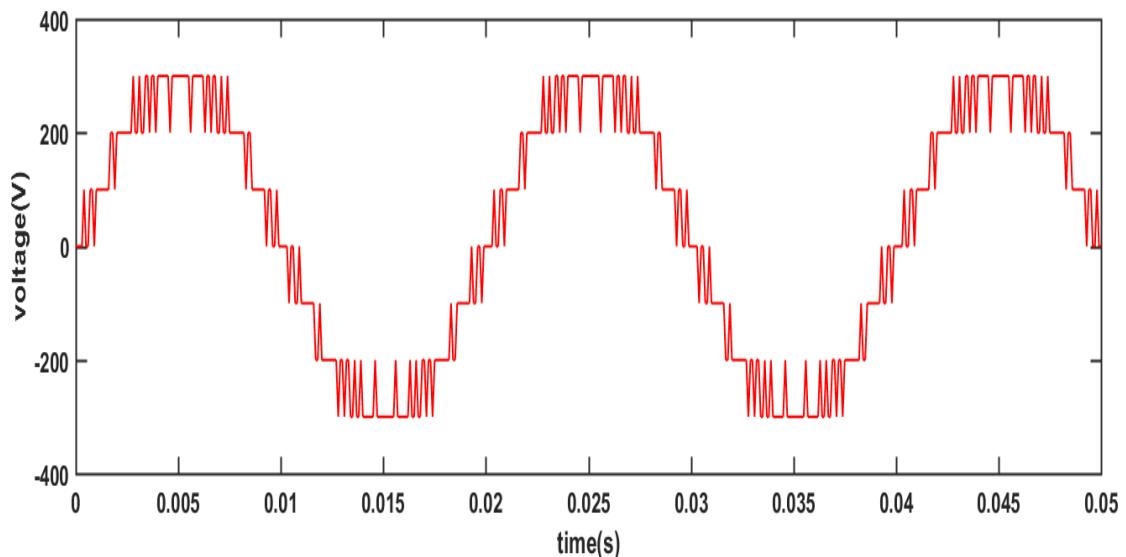
### 3.11 Effect of change in Modulation Index ( $M_a$ )

It is observed on symmetric seven-level cascaded H-bridge.

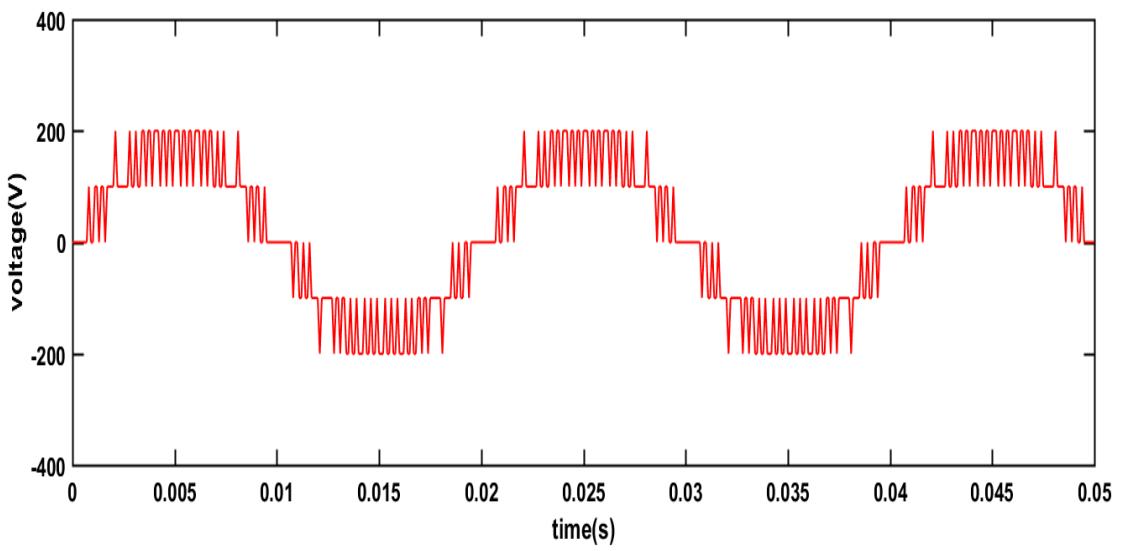
- As Modulation Index ( $M_a$ ) reduces from unity there is reduction in levels of output voltage.
- In 7 level voltage, three steps are available in positive half cycle. If  $M_a$  reduces by one-third the 7 level voltage will be reduced to 5. Similarly, if it reduces by two-third 5 level is reduced to 3.
- As we decrease the  $M_a$ , the fundamental decreases and THD increases. The increase in THD is due to the decrease in the number of levels.

**Table 3-2: Effect of change in  $M_a$  on %THD and fundamental voltage  
for  $f_c = 3\text{KHz}$ ,  $V_{dc} = 100\text{V}$**

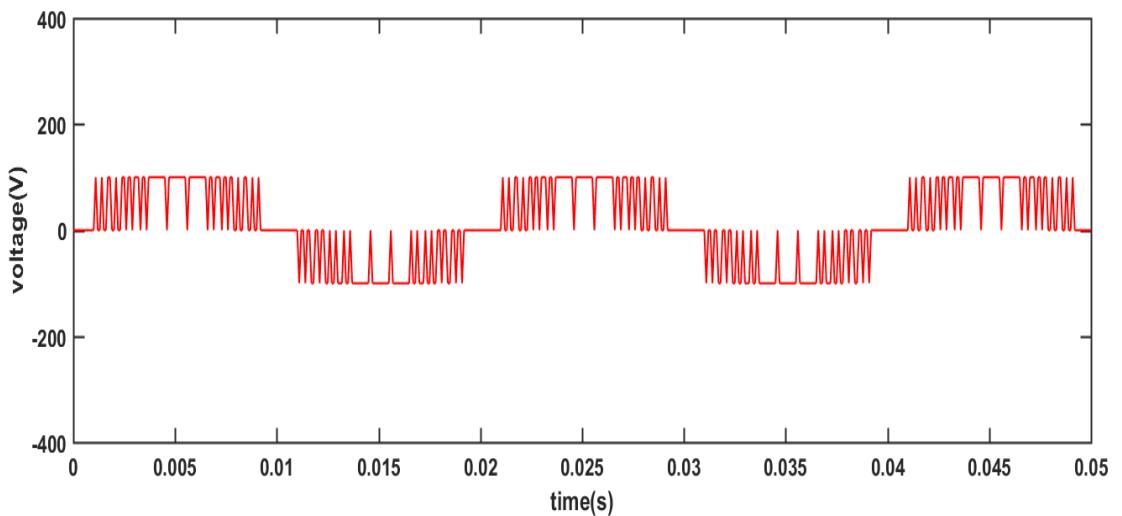
<u><math>M_a</math></u>	<u>THD%</u>	<u>FUNDAMENTAL (V)</u>
1	14.1	296.7
0.9	17.22	265.2
0.8	16.45	240.6
0.7	16.84	207.6
0.6	19.72	175.6
0.5	24.77	149.9
0.4	27.79	162
0.3	35.46	90.46



**Figure 3-28: Symmetrical seven-level output phase voltage  
when  $M_a = 1$**



**Figure 3-29: Symmetrical seven-level output phase voltage  
when  $M_a = 0.6$**



**Figure 3-30: Symmetrical seven-level output phase voltage  
when  $M_a = 0.3$**

## 4. FILTER DESIGN

### 4.1 Need of Filters

Recently, the development of renewable energy technologies has been accelerating, making the simultaneous development of power conversion devices for applications, such as wind and solar power systems extremely important, the development of these technologies is actively underway. The harmonics caused by the switching of the power conversion devices are the main factor-causing problems to sensitive equipment or the connected loads, especially for applications above several kilowatts, where the price of filters and total harmonics distortion (THD) is also an important consideration in the systems design phase.

Since maintaining a good power quality is important for the reliable operation of the system and loads, these filters will be applied to a three-phase PV system. Then, the inverter output will be filtered in order to obtain low voltage and current distortions which are occurring due to the harmonics caused by semiconductor switching.

The filter has to be designed such that the output voltage and current harmonics stay within the limits even for the worst condition.

Harmonic (voltage or current distortion) in distribution system increases with the increase of high rating nonlinear load. The filter design is becoming more and more essential for industrial distribution systems. So to correct the undesirable voltage profile as well as to decrease the harmonic content we use filters and they are classified as Active filters and Passive filters.

### 4.2 Classification of Filters:

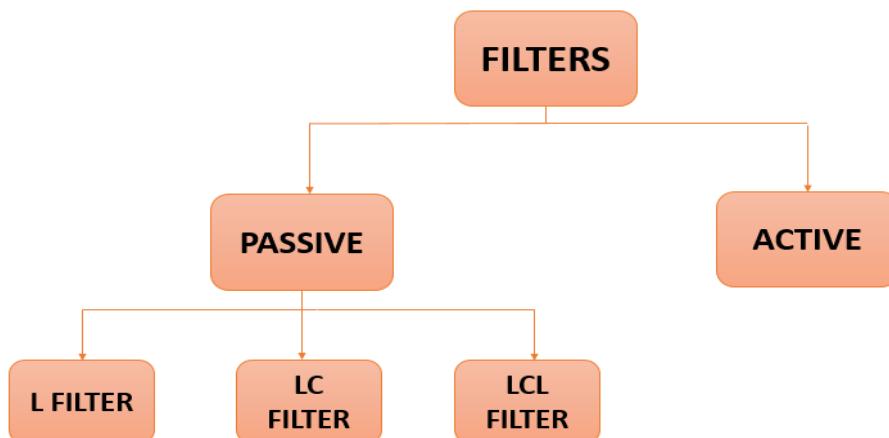


Figure 4-1: Classification of filters

#### 4.2.1 Passive Filters

A passive filter is an arrangement of inductances, capacitances as well as resistances orderly in such a manner that it acts as a frequency discriminator, i.e., it provides low impedance path for harmonics component or we can say that it allows passing of several frequencies and discards others. It is possible to connect more than one passive filter in either shunt and/or series configuration.

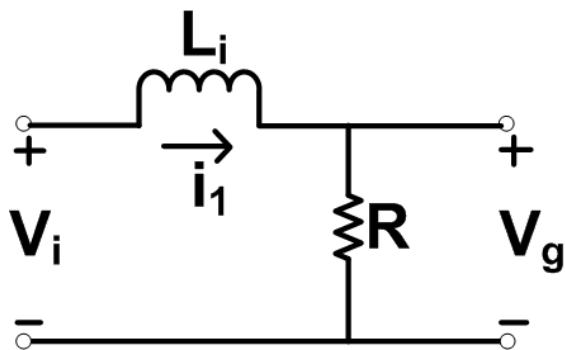
#### 4.2.2 Active Filters

The design complexity and high cost of losses of the conventional passive filters, as well as their restricted capability to eliminate inter-harmonics and non-characteristic harmonics, has encouraged the development of harmonic compensation by means of power electronic devices, and commonly referred to as active filters. Shunt active filter is used instead of passive filter because it absorbs the current harmonics dynamically by injecting equal and opposite harmonic current into the system.

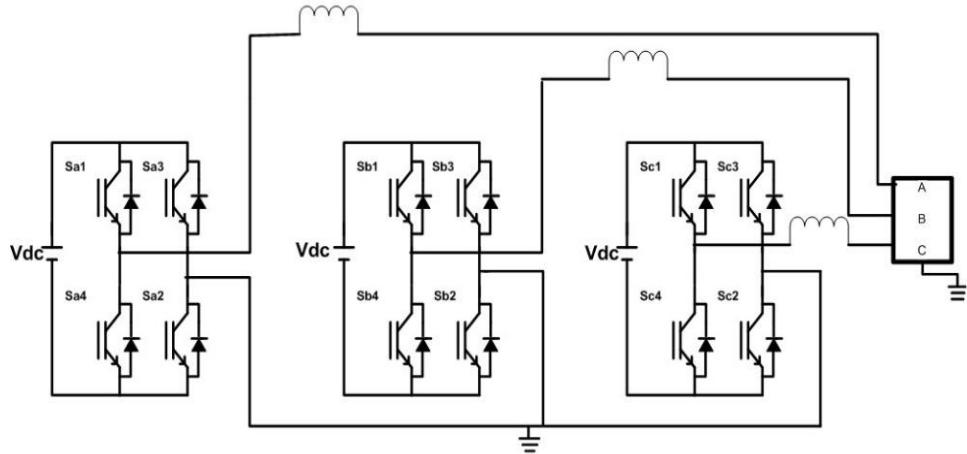
### 4.3 Analysis of L, LC and LCL filters

#### 4.3.1 L-Filter

The L-filter is the first order filter with attenuation 20 dB/decade over the whole frequency range. Therefore, the application of this filter type is suitable for converters with high switching frequency. The main disadvantage of this type of filters is their big size which increases the losses and also makes the system bulky hence its study has been limited in high power applications. Fig 4-2(b) shows three phase three level CHB grid connected inverter with 'L' filter. [1]



4-2(a)



4.2(b)

**Fig 4-2(a), 4-2(b): Basic ‘L’ filter topology and Three Phase Three Level CHB inverter with ‘L’ Filter respectively.**

The transfer function of inductor filter is given as

$$H(s) = \frac{R}{R + L_i s}$$

**Equation 4-1: Transfer function of ‘L’ filter**

#### 4.3.1(a) Design of ‘L’ Filter:

The value of inductance should be selected such that it should be less than 20% to limit the voltage drop during the normal operation.[2]

The calculation of ripple current is given by: [3]

$$I_{\text{ripple}} = \frac{0.2 * \sqrt{2} * P}{3 * (V_L / \sqrt{3})}$$

**Equation 4-1(a): Ripple current in designing of ‘L’ filter**

Where,  $V_L$  = Rms value of line voltage

$P$  = Load Power

The filter inductance can be given as follows:

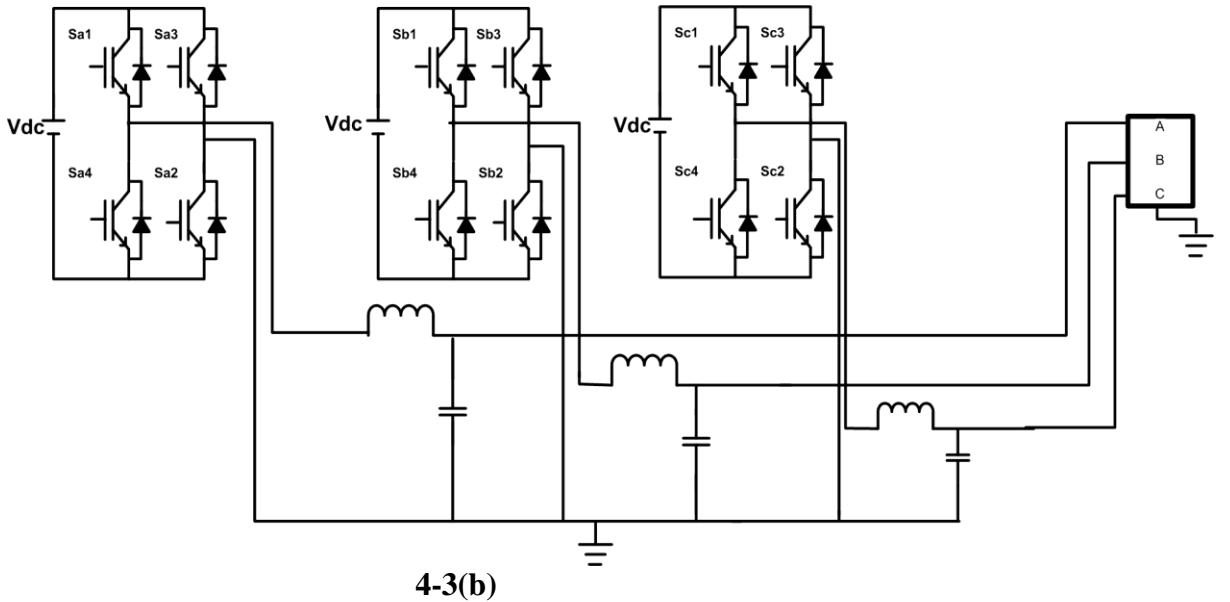
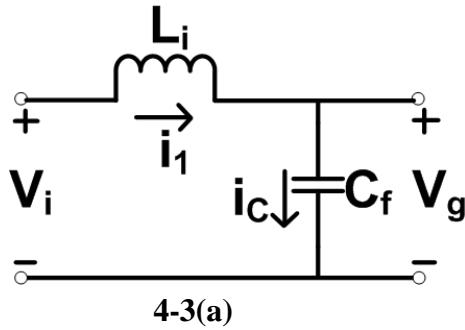
$$L_i = \frac{(V_{dc} - V_{dc}/2) * 0.5}{2 * I_{\text{ripple}} * f_{sw}}$$

**Equation 4-1(b): Inductance calculation in designing of ‘L’ filter**

Where,  $V_{DC}$  = DC input voltage

#### 4.3.2 LC Filter:

The LC-filter is depicted in Fig 4-3. It is second order filter and it has better damping behaviour than L-filter.



**Fig 4-3(a), 4-3(b): Basic ‘LC’ filter topology and Three Phase Three Level CHB inverter with ‘LC’ Filter**

The second order filter provides 12 dB per octave of attenuation after the cut-off frequency and it has no gain before the cut-off frequency, but it presents a peaking at the resonant frequency, which is given as,

$$f_r = \frac{1}{2\pi\sqrt{L_i C_f}}$$

**Equation 4-2: Resonant frequency of ‘LC’ filter**

The filter consists of an inductance in series with the inverter and a capacitance in parallel with the grid (Fig 4-3). By using this parallel capacitance, the inductance can be reduced, thus reducing costs and losses as compared with L filter.

With use of large capacitance, other problems such as high inrush currents and high capacitance current at the fundamental frequency or dependence of the filter on the grid impedance for overall harmonic attenuation will appear. [1]

The LC filter transfer function of grid side voltage and inverter input voltage in grid-connected mode of operation is given by Equation 4-3: [1]

$$G(s) = \frac{V_g}{V_{inv}} = \frac{1}{s^2 L_i C_f + sL + 1}$$

**Equation 4-3: Transfer function of ‘LC’ filter**

The high capacitor has positive effects on the voltage quality. On the other hand, higher inductance value is required to achieve demanded cut-off frequency of the filter.

While connecting system with this kind of filter to the supply grid, the resonant frequency of the filter becomes dependent on the grid impedance and therefore this filter is not suitable, too.

#### 4.3.2(a) Design of ‘LC’ Filter:

Inverter side inductance is as calculated previously in ‘L’ Filter.[3]

Base impedance:  $Z_b = \frac{V_L^2}{P}$  ..... (a)

Capacitance:  $C_b = \frac{1}{Z_b * w}$  ..... (b)

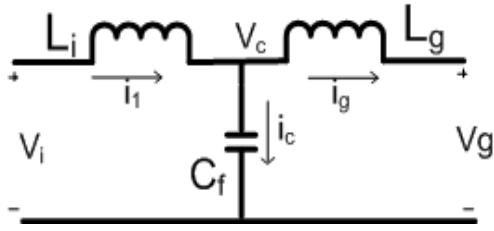
Filter capacitance:  $C_f = x * C_b$  ..... (c)

**Equation 4-4(a), 4-4(b), 4-4(c): Calculation of capacitance in ‘LC’ filter**

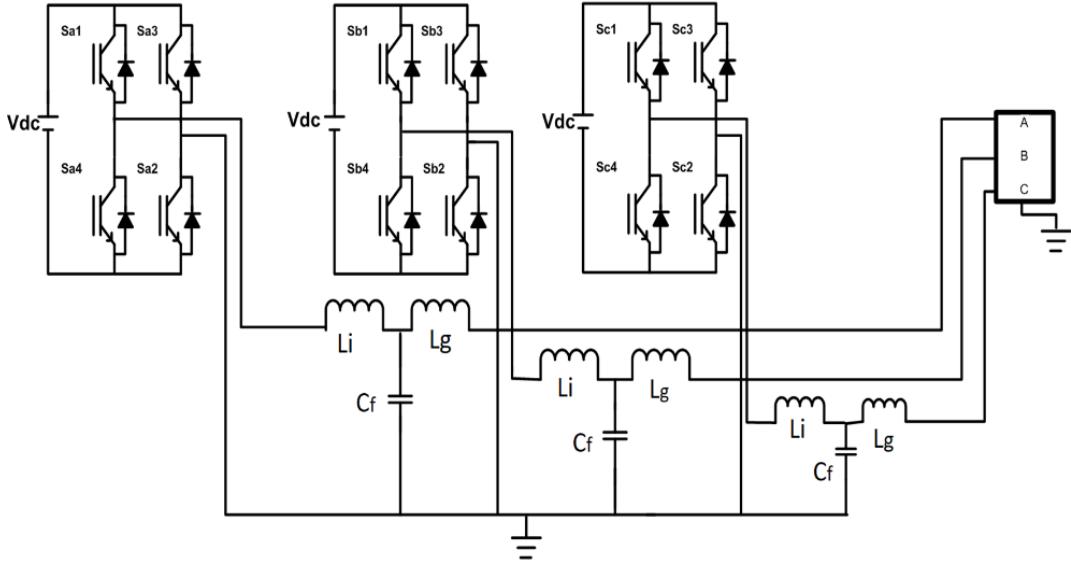
For the design of the filter capacitance, it is considered that the maximum power factor variation seen by the grid is 5%, indicating that the base impedance of the system is adjusted as  $x= 0.05$ . A design factor higher than 5% can be used, when it is necessary to compensate the inductive reactance of the filter. [3]

#### 4.3.3 LCL Filter:

The attenuation of the LCL-filter is 60 dB/decade for frequencies above resonant frequency, therefore lower switching frequency for the converter can be used. It also provides better decoupling between the filter and the grid impedance and lower current ripple across the grid inductor. Therefore LCL-filter fits to our application. [1]



4-4(a)



4-4(b)

**Fig 4-4(a): ‘LCL’ filter topology, Fig 4-4(b) Three phase three-level CHB with LCL filter**

The LCL filter has good current ripple attenuation even with small inductance values. However, it can bring also resonances and unstable states into the system. Therefore, the filter must be designed precisely according to the parameters of the specific converter. Important parameter of the filter is its cut-off frequency.

The cut-off frequency of the filter must be minimally one half of the switching frequency of the converter, because the filter must have enough attenuation in the range of the converter's switching frequency. [1] The cut-off frequency must have a sufficient distance from the grid frequency, too. The cut-off frequency of the LCL filter can be calculated as,

$$F_{res} = \frac{1}{2\pi} \sqrt{\frac{Li + Lg}{Li \cdot Lg \cdot Cf}}$$

**Equation 4-5: Resonant frequency of ‘LCL’ filter**

#### 4.3.3(a) Advantages of LCL Filters:

- LCL filter provides better decoupling between the filter and the grid impedance and lower current ripple across the grid inductor. It provides higher harmonic attenuation

compared to simple L filter with same per unit circuit inductance and hence they are more suitable for converters operating at low switching frequencies whereas the inductor size tends to become very large in case of simple L filter.

- The decrease in the total inductance in case of LCL filters also results in decrease in voltage drop across filter and consequently reduction in required DC link voltage. The smaller DC voltage also means decrease in ratings of semiconductor switches and further reduction of cost of whole system.
- Compared with a first-order and second-order filters, a third-order LCL filter has lower cost and smaller size in applications above several kilowatts. Therefore, LCL-filter fits to our application.

Nevertheless, the design of current control scheme becomes more complex with LCL filter owing to its resonance. However, it can bring also resonances and unstable states into the system leading to complex design scheme.

Therefore, the filter must be designed precisely according to the parameters of the specific converter.

The LCL filter will be vulnerable to oscillations too and it will magnify frequencies around its cut-off frequency. The simplest way is to add damping resistor in series or in parallel with capacitor.

#### **4.3.3 (b) Design of ‘LCL’ Filter:**

In order to design an LCL filter the following constraints are to be followed: [3]

- The value of the capacitor is to be selected such that the decrease of the power factor at rated power should be tolerable, which is usually below 5%.
- The value of inductance should be selected such that it should be less than 10% to limit the voltage drop during the normal operation.
- In order to avoid the resonance problems in the higher and the lower harmonic spectrum the resonant frequency is to be selected in the range of ten times the line frequency and one half of the switching frequency.
- It should be seen that losses would be low which maintains a better efficiency.
- In order to avoid the oscillations, the passive damping should not be too low.

**L<sub>i</sub> and C<sub>f</sub> are calculate using the equations used in ‘L’ and ‘LC’ filter**

For calculation of grid side inductor, we use the following equation:

$$L_g = r * L_i$$

**Equation 4-6: Grid side inductor designing of ‘LCL’ filter**

In order to find the value of the grid side inverter a constant ‘r’ called as ripple attenuation constant is defined. The constant r can be defined as the relation between the grid side inductance and the inverter side inductance. By keeping this factor as 30%, the voltage drop across grid side inductor is found to be min. [4]

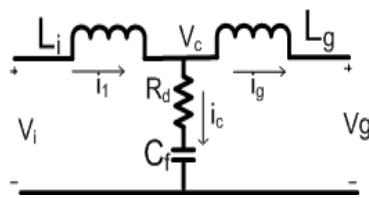
#### 4.3.3(c) LCL Filter with Damping Resistor:

The LCL filter will be vulnerable to oscillations too and it will magnify frequencies around its cut-off frequency. Therefore, the filter is added with damping. The simplest way is to add damping resistor. In general, there are four possible places where the resistor can be placed series/parallel to the inverter side inductor or series/parallel to filter capacitor. The variant with resistor connected in series with the filter capacitor has been chosen. The value of the damping resistor can be calculated as

$$R_d = \frac{1}{3 * 2\pi * F_{res} * C_f} \quad \dots \dots \dots (a)$$

Where,  $F_{res} = \frac{1}{2\pi} \sqrt{\frac{L_i + L_g}{L_i * L_g * C_f}}$  ..... (b)

**Equation 4-7(a), 4.7(b): Damping resistor in designing of ‘LCL’ filter**



**Fig 4-5: Basic topology of LCL Filter with damping resistor**

A damping resistance is added in series with the filter capacitor in order to limit the resonance effects of the filter. This resistance can also be connected in parallel with the capacitor.

The peak near resonant frequency has nearly vanished. Its value is taken such that it should be equal to one-third of the filter capacitor impedance at the resonant frequency. This is simple and reliable solution, but it increases the heat losses in the system and it greatly decreases the efficiency of the filter. [1]

The LCL filter transfer function of grid side voltage and inverter input voltage in grid-connected mode of operation is given by Equation 4-8:

$$G_d(s) = \frac{I_g}{V_i} = \frac{C_f R_d s + 1}{L_i C_f L_g s^3 + C_f (L_i + L_g) R_d s^2 + (L_i + L_g) s}$$

**Equation 4-8: Transfer function of ‘LCL’ filter with Damping resistor**

Where,  $I_g$  = Grid side current

$V_i$  = Inverter output voltage

$R_d$  = Damping resistor

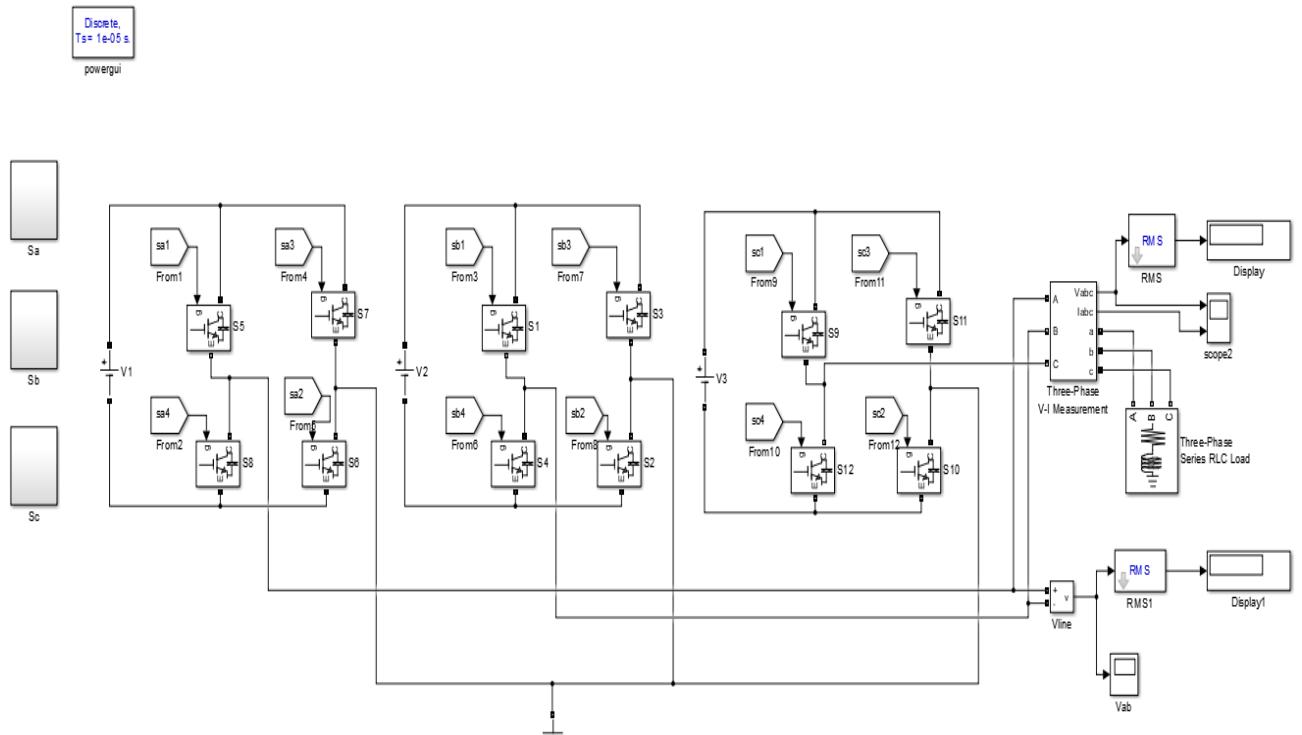
## 5. ANALYSIS OF FILTER DESIGN BY SIMULATIONS

Simulations are done through MATLAB-Simulink. From simulations we tried to observe the output waveform, calculate the Total harmonic Distortion THD, perform FFT analysis and observe the dominant harmonics created and derive conclusions accordingly. According to our previous analysis we found that Phase Opposite Disposition (POD) gives better performance compared to other SPWM techniques.

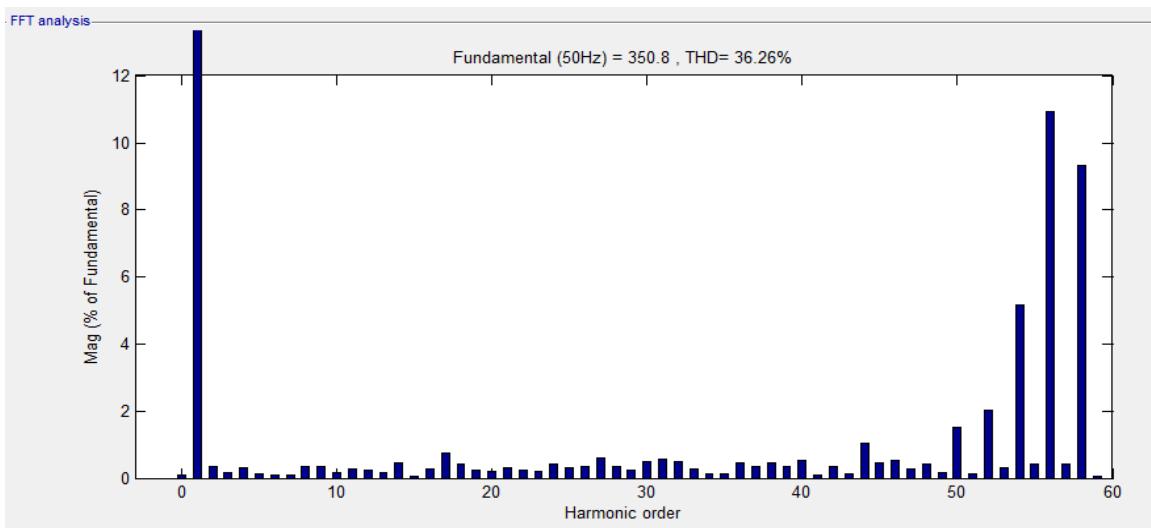
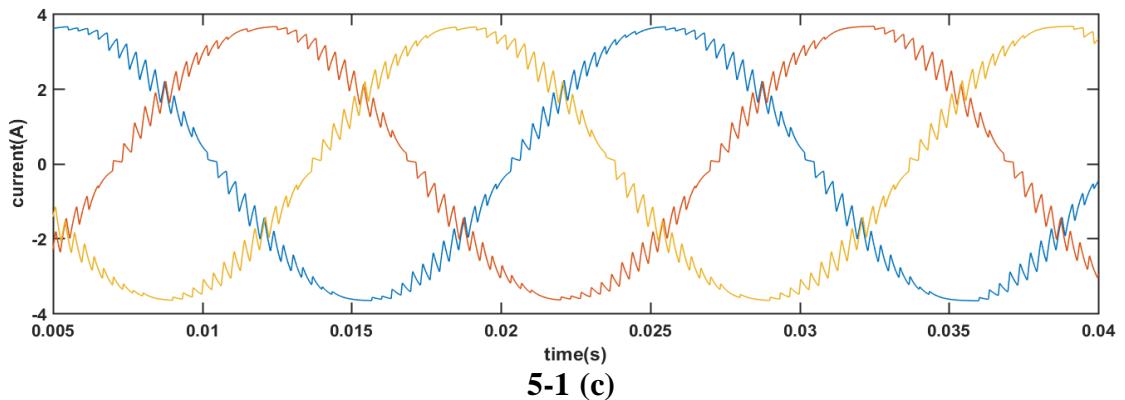
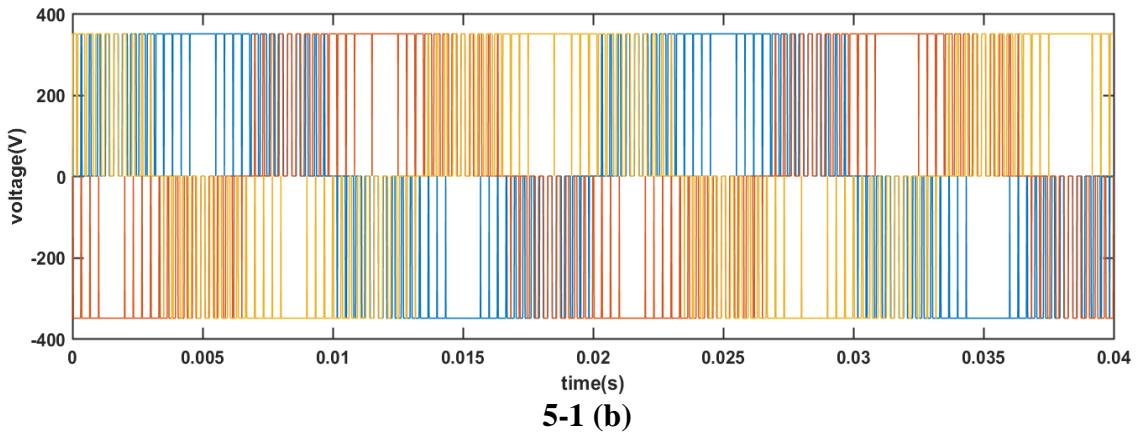
### 5.1. Analysis of Three Phase Three-Level CHB

With switching frequency as 3KHz and system frequency as 50Hz and giving input DC input voltage to the CHB as 350V following analysis of phase voltage and phase current is studied. The load power is consuming 2KW. The FFT window showing dominant harmonics as well as THD is observed.

#### 5.1.1 Without Filter:



5-1 (a)



**Fig 5-1(a), 5-1(b), 5-1(c), 5-1(d) represent three phase three level CHB inverter without filter simulation circuit, phase voltage waveform and phase current waveforms and FFT window respectively.**

From the figures we can see that the stepped phase voltage is obtained without filter while the current waveform is having ripples. Hence, the THD of phase voltage is found to be

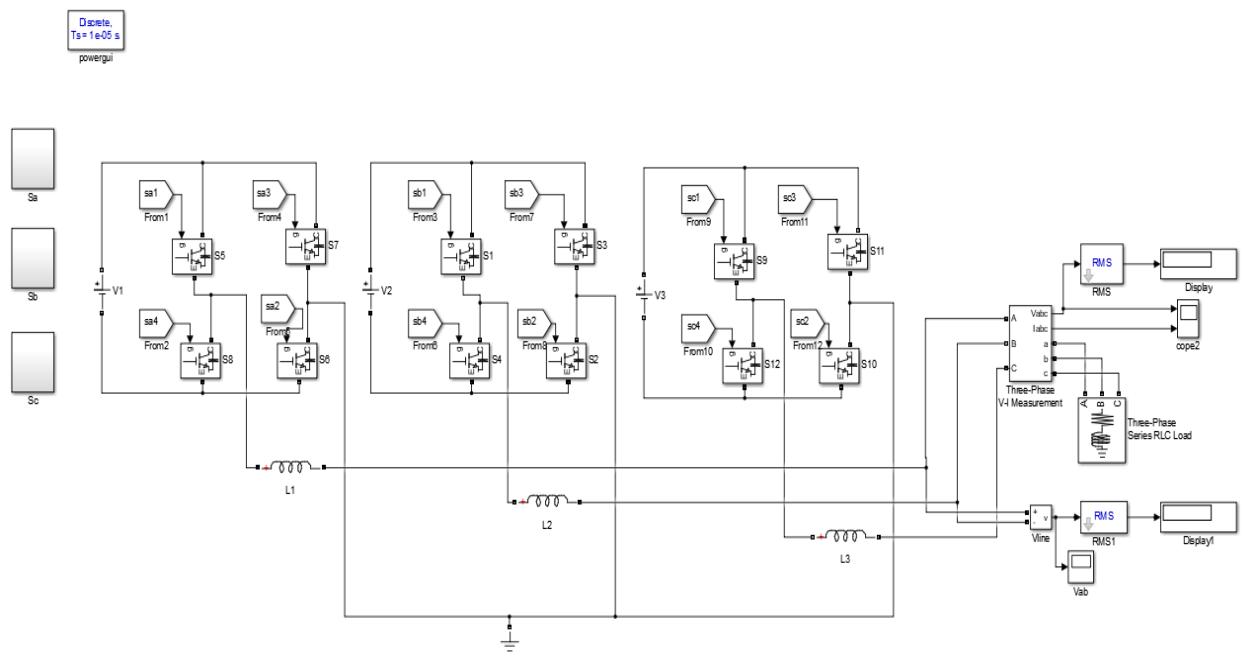
36.26%. The dominant harmonics are situated at 56<sup>th</sup> harmonic. The fundamental peak value of fundamental is found out as 350.8V while total phase voltage rms as 279.7 V To get pure sinusoidal we need to use filters.

### 5.1.2 With 'L' Filter:

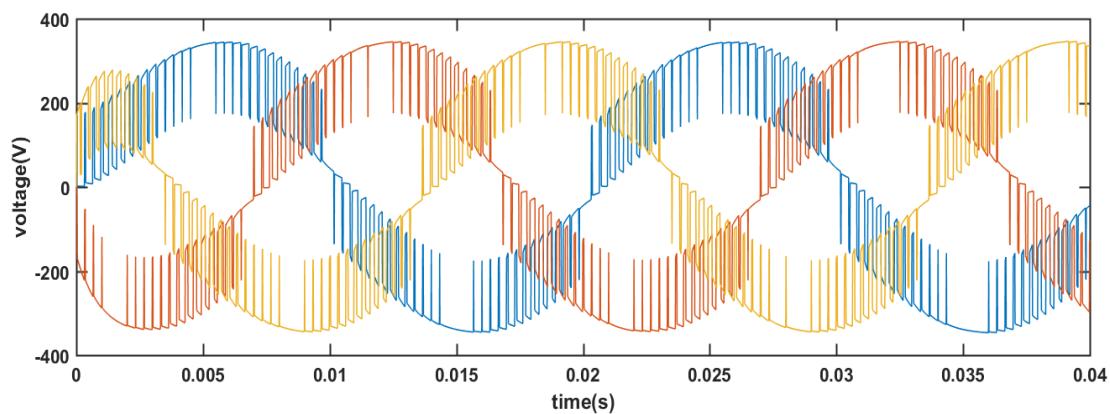
From the calculations of 'L' filter design from the equations 4-1(a), 4-1(b) we get

$$I_{\text{ripple}} = \frac{0.2 * \sqrt{2} * 2 * 1000}{3 * \frac{436.9}{\sqrt{3}}} = 0.74$$

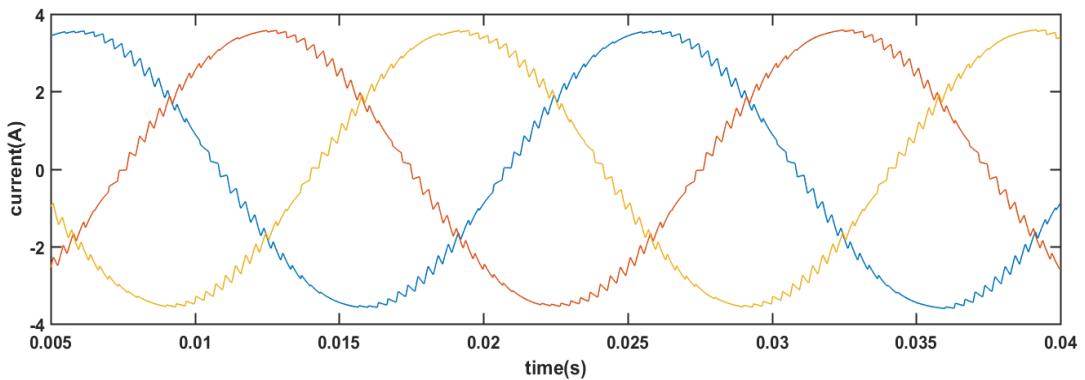
$$L_i = \frac{\left(350 - \frac{350}{2}\right) * 0.5}{2 * 0.74 * 3 * 1000} = 19.45 \text{ mH}$$



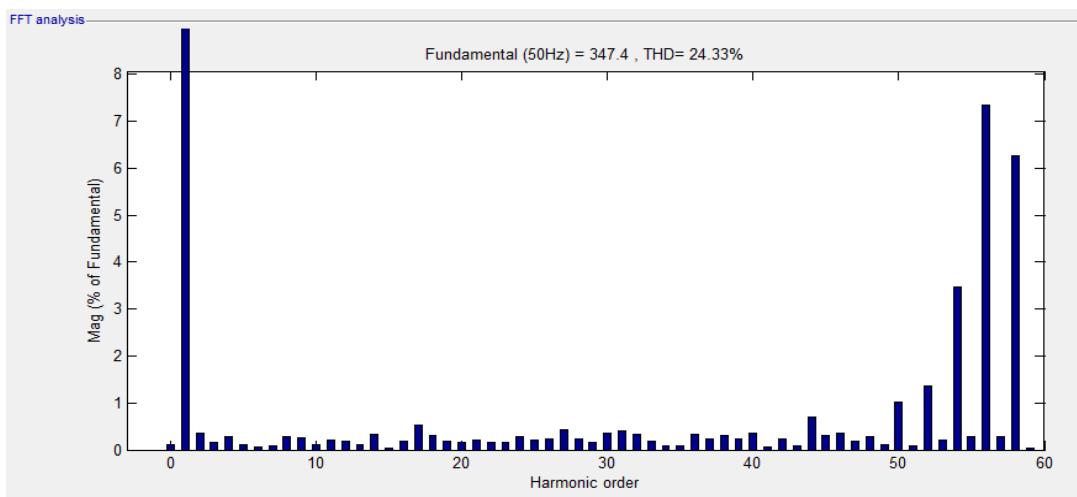
5-2 (a)



5-2 (b)



**5-2 (c)**



**5-2(d)**

**Fig 5-2(a), 5-2(b), 5-2(c), 5-2(d) represent three phase three level CHB inverter with ‘L’ filter simulation circuit, phase voltage waveform and phase current waveforms and FFT window respectively.**

From the figures we can see that there is no change in phase voltage while inductor reduced the current ripples. Hence, the THD of phase voltage is found to be 24.33% which is decreased. The dominant harmonics are situated at near 3KHz. The fundamental peak value is found out as 347.4 V it has reduced because of drop across the inductor. With such high value if inductor the circuit has become bulky so we move to LC filter.

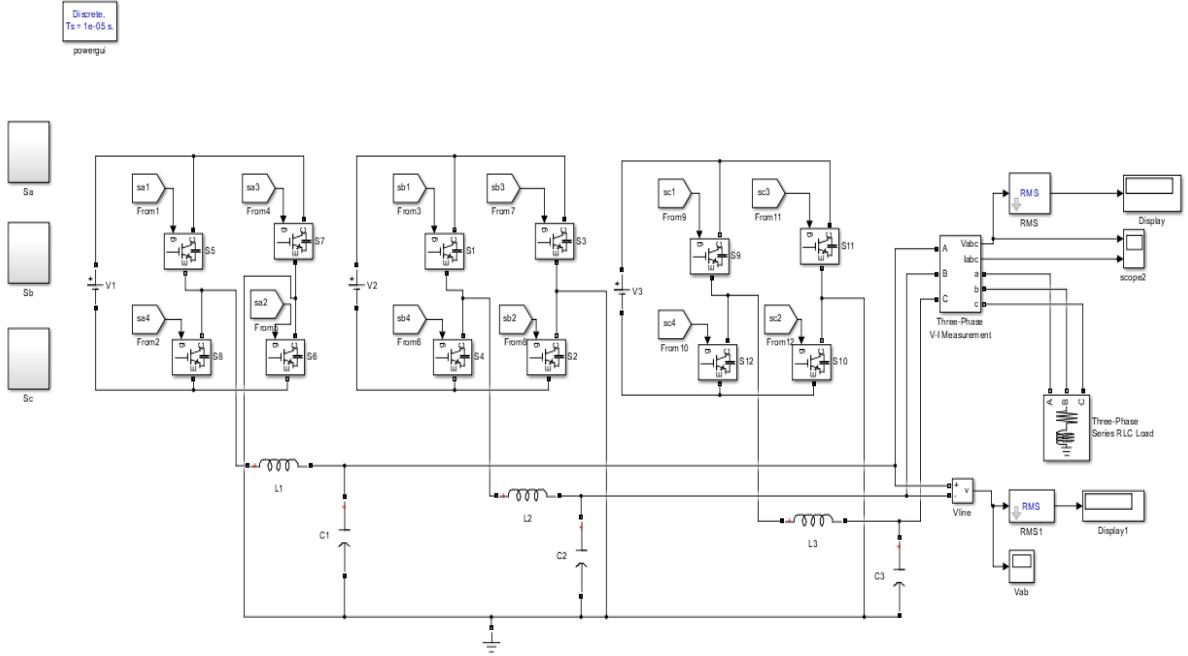
### 5.1.3 With ‘LC’ Filter:

From equations 4-1(a), (b) and 4-4(a),(b),(c),  $L = 19.45\text{mH}$  and

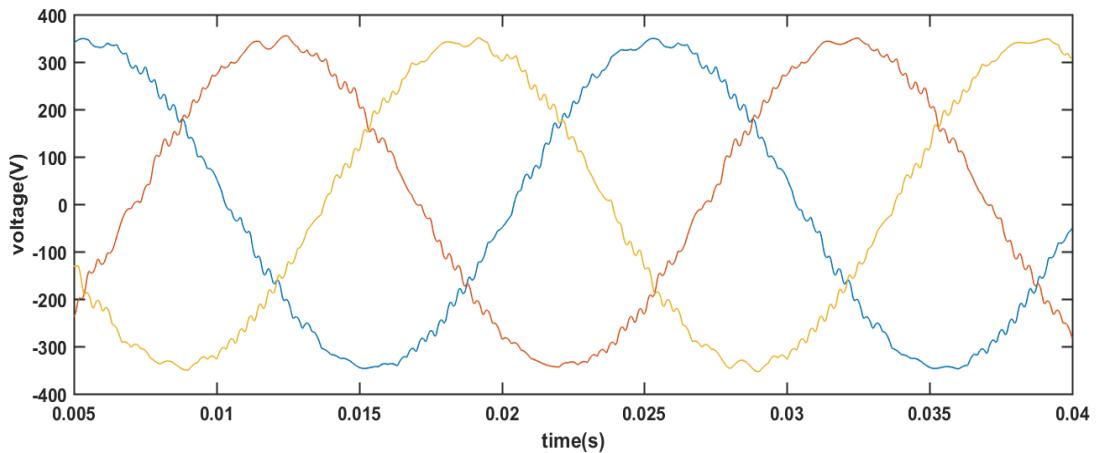
$$Z_b = \frac{436.9^2}{2*1000} = 95.44 \Omega$$

$$C_b = \frac{1}{95.44*2\pi*50} = 3.3 * 10^{-5} \text{ F}$$

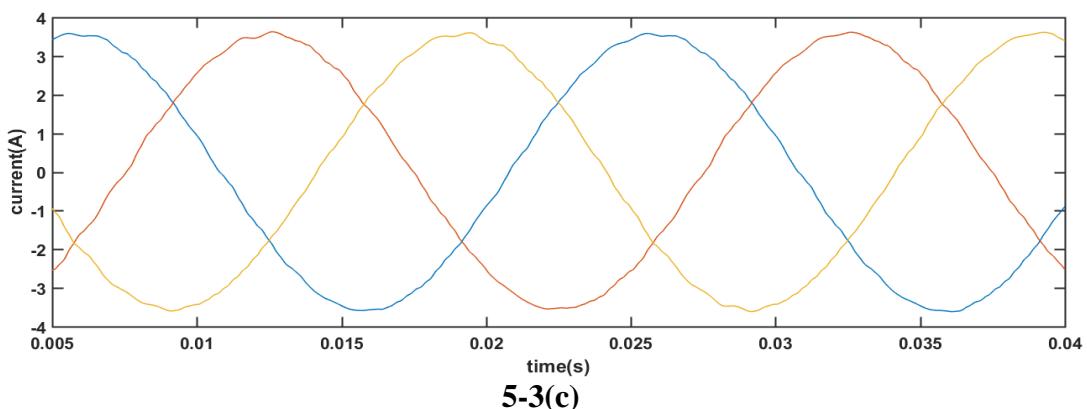
$$C_f = 0.05 * 3.3 * 10^{-5} = 1.66 \text{ uF}$$

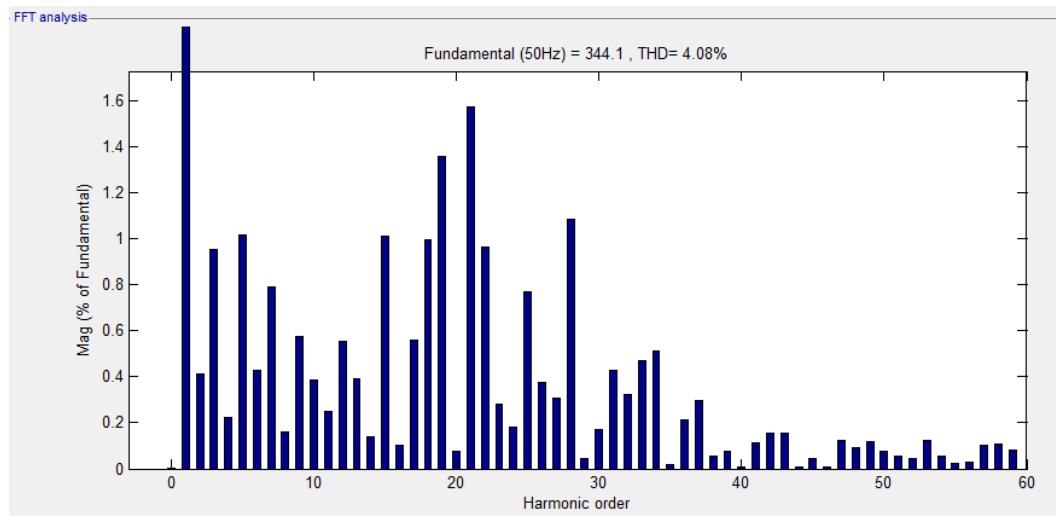


**5-3(a)**



**5-3(b)**





**5-3(d)**

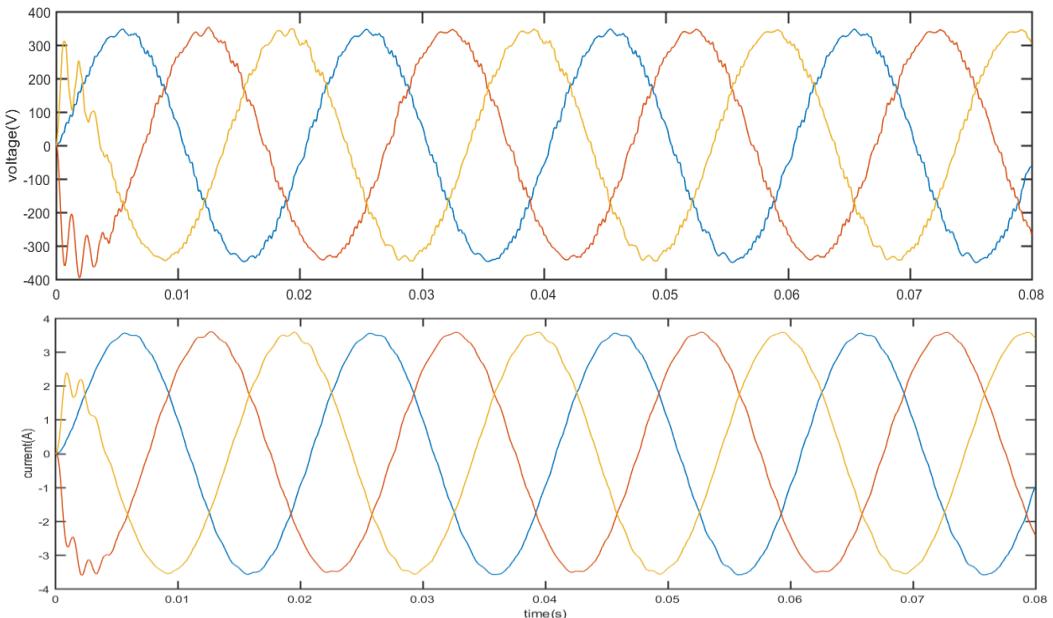
**Fig 5-3(a), 5-3(b), 5-3(c), 5-3(d) represent three phase three level CHB inverter with ‘LC’ filter simulation circuit, phase voltage waveform and phase current waveforms and FFT window respectively**

It is observed that the voltage ripples are also decreased in ‘LC’ Filter because of capacitor and hence the waveform has become smooth.

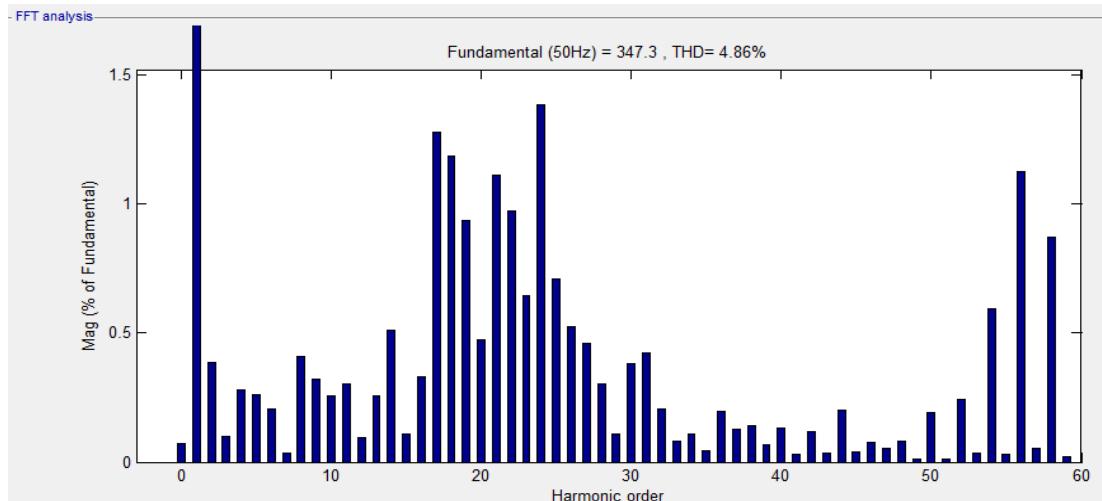
#### 5.1.4 With ‘LCL’ Filter:

From equations 4-1(a), (b) and 4-4(a), (b), (c), and 4-6  $L_i = 19.4\text{mH}$  and  $C_f = 1.66\mu\text{F}$ , and  $L_g$  will be 30% of  $L_i$  which is  $5.86\text{mH}$ .

Like previous simulations the filter circuit will be same.



**5-4 (a) & 5-4(b)**



**5-4(c)**

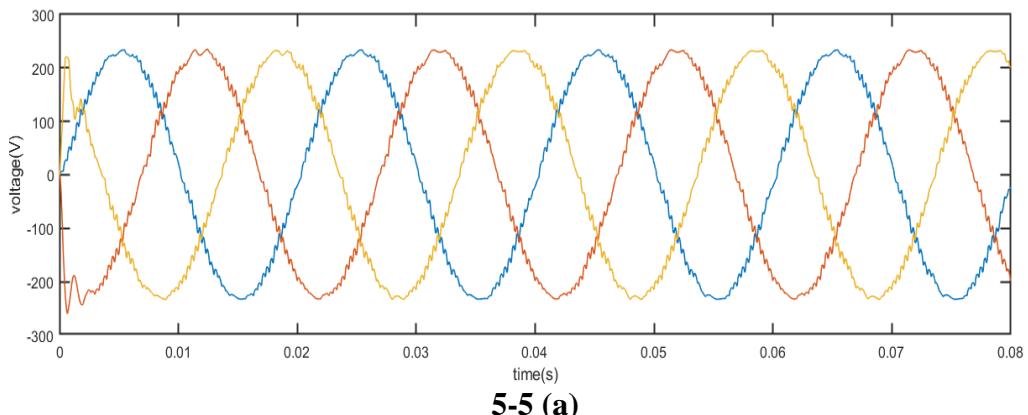
**Fig 5-4(a), 5-4(b), 5-4(c) represent three phase three level CHB inverter with ‘LCL’ filter phase voltage waveform and phase current waveforms and FFT window respectively.**

### 5.1.5 ‘LCL’ Filter with Damping resistor:

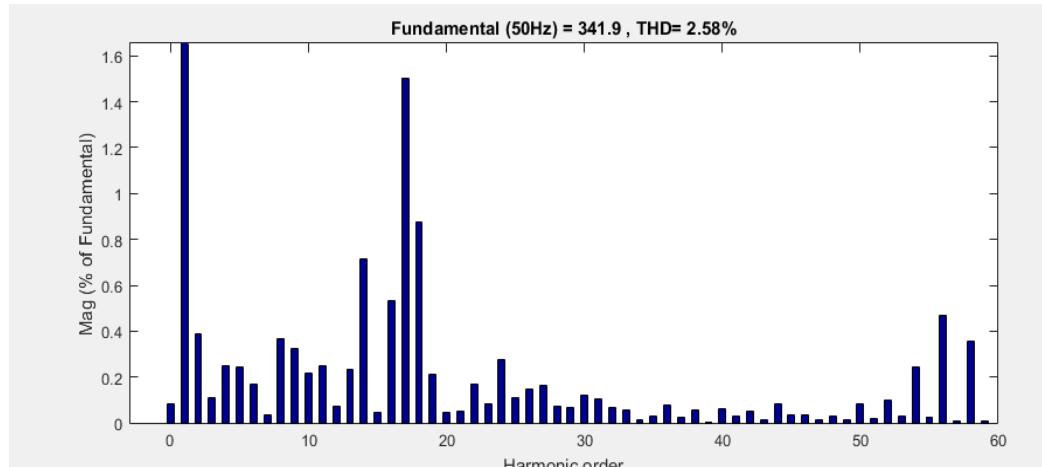
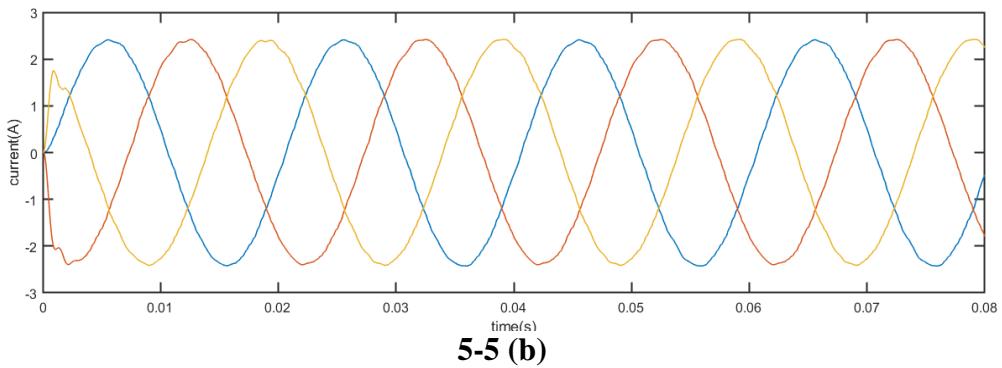
As previously calculated,  $L_i = 19.4\text{mH}$  and  $C_f = 1.66\mu\text{F}$ ,  $L_g = 5.86\text{mH}$  the values in designing of damping resistor case will be same. From the equations 4-7(a) and (b), we get

$$F_{res} = \frac{1}{2\pi} \sqrt{\frac{19.4 \text{ m} + 5.86 \text{ m}}{19.4 \text{ m} * 5.86 \text{ m} * 1.66 \mu}} \\ = 1841.336 \text{ Hz}$$

$$R_d = \frac{1}{3 * 2\pi * 1841.336 * 1.66\mu} \\ = 17.37\Omega$$



**5-5 (a)**



5-5(c)

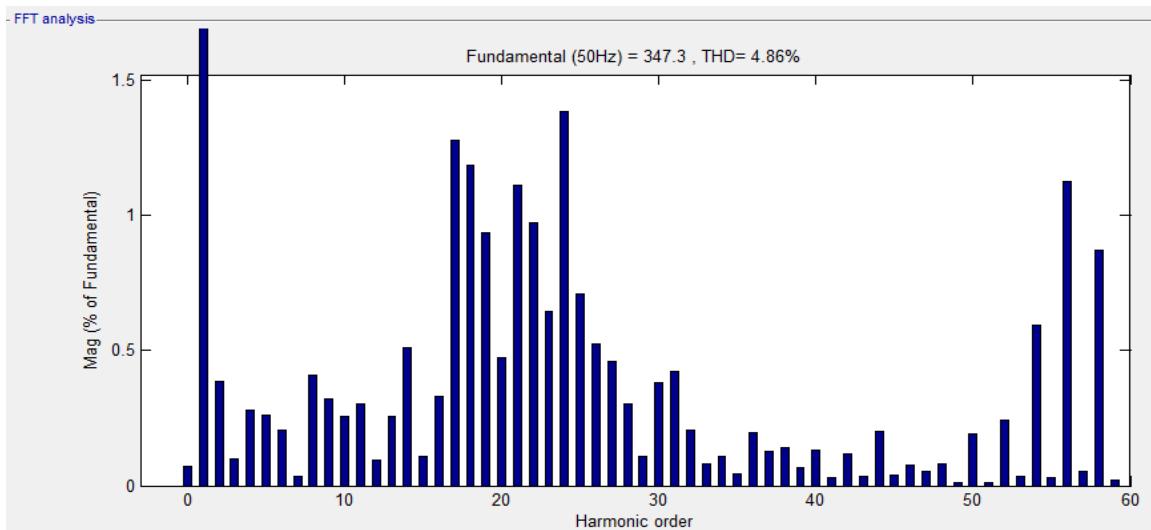
**Fig 5-5(a), 5-5(b) represent the phase voltage and phase current of three phase three level CHB inverter with ‘LCL’ filter and damping resistor**

From the waveforms it can be seen that the oscillations at the start have decreased when compared with figures 5-4 (a) and (b).

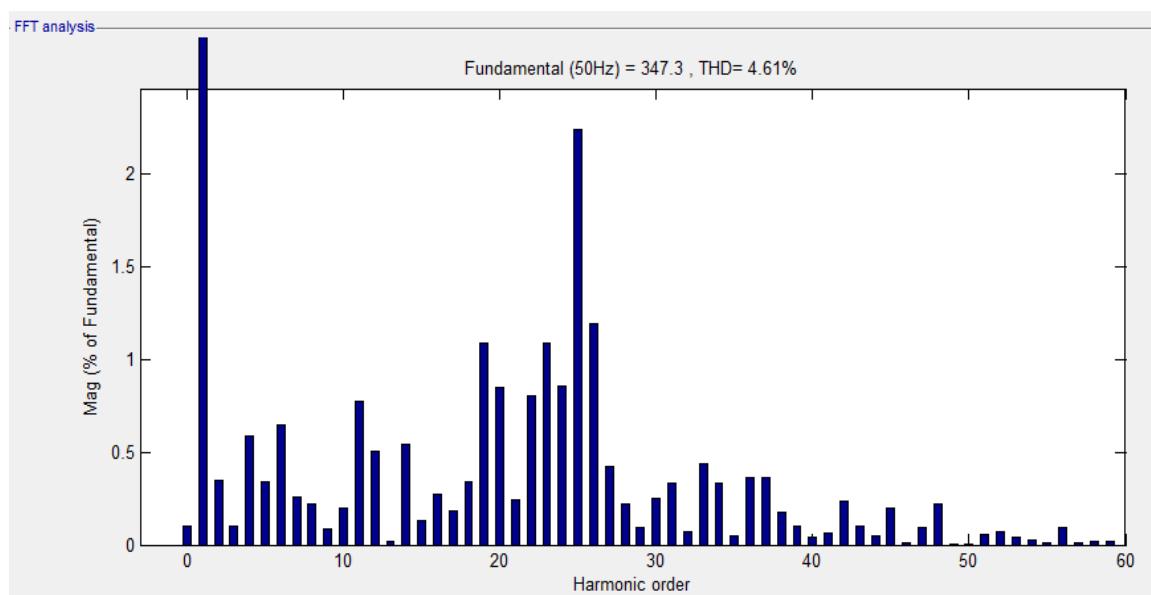
## 5.2. LCL Design parameters of Three Phase Three Level for various $f_c$

**Table 5-1: LCL filter design parameters at various  $f_c$**

SWITCHING FREQUENCY $f_c$ (KHz)	INVERTER SIDE INDUCTOR $L_i$ (mH)	FILTER CAPACITOR $C_f$ (uF)	GRID SIDE INDUCTOR $L_g$ (mH)	DAMPING RESISTOR $R_d$ (OHM)
3KHz	19.54	1.66	5.86	17.37
4KHz	14.65	1.66	4.395	15.04
5Khz	11.7	1.66	3.51	13.44



**Fig 5-6(a): FFT analysis of three phase three level CHB with  $f_c$  as 3 KHz**



**Fig 5-6(b): FFT analysis of three phase three level CHB with  $f_c$  as 4 KHz**

By conventional filter design formulas, LCL filter parameters have been calculated at various carrier frequencies. FFT analysis of three phase three level CHB has been carried out with these design parameters of LCL filter.

### 5.3. Effect on %THD by variation of levels and $f_c$ of three-phase CHB

By conventional filter design formulas, the filter design is carried out at different levels and at various switching frequencies. The effect on %THD of filter parameters designed at various  $f_c$  and of different levels can be seen in figure 5-7.



**Fig 5-7: THD analysis of different levels of three phase CHB for various  $f_c$**

By using calculated LCL filter design parameters, it can be observed that with increase in levels %THD is decreasing.

#### 5.4. Comparison of filter sizes according to IEEE standards

For grid-tied mode, converters require L or LCL filters for output current filtering and reducing the number of harmonics injected to the grid below limits stipulated by the IEEE Std. 512-1992 and IEEE Std. P1547-2003.[5]

IEEE Std. 519-1992: Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems.

According to the standards the tolerable ripple (THD) should be within 5%.

**Table 5-2: Arbitrarily chosen LCL filter parameters to maintain IEEE standards**

LEVELS	SWITCHING FREQUENCY $f_c$								
	3KHz			4KHz			5KHz		
	$L_i$ (mH)	$C_f$ (uF)	$L_g$ (mH)	$L_i$ (mH)	$C_f$ (uF)	$L_g$ (mH)	$L_i$ (mH)	$C_f$ (uF)	$L_g$ (mH)
<b>3 level</b>	19.54	1.66	5.86	14.65	1.66	4.395	11.7	1.66	3.51
<b>5 level</b>	12	1.66	3.6	10.5	1.66	3.15	9.25	1.66	2.775
<b>7 level</b>	10.85	1.66	3.325	9.18	1.66	2.75	4.8	1.66	1.44

According to the analysis carried out based on the calculated filter design parameters by using conventional design formulas the %THD values have decreased much less than 5%. But according to IEEE Std. 519-1992, the tolerable ripple (%THD) is up to 5%. So the filter sizes can be reduced by considering this reason and hence filter parameters have been chosen arbitrarily to maintain %THD according to IEEE std. i.e., near to 5%.

The LCL filter design parameters are shown in Table 5-2 for different levels and at various  $f_c$ .

## 5.5 Stability of designed LCL filter

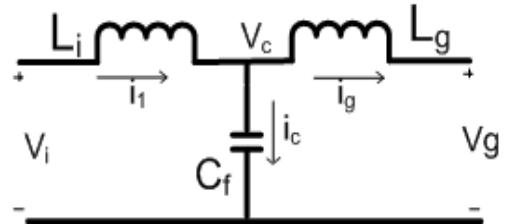
### 5.5(a) Stability analysis of LCL filter without damping resistance

Open loop transfer function of LCL filter is given as:

$$G_d(s) = \frac{I_g}{V_i} = \frac{1}{L_i C_f L_g s^3 + (L_i + L_g)s}$$

Where  $I_g$  = Grid side current

$V_i$  = inverter output



The derivation of transfer function can be seen in Appendix. From the transfer function, it can be inferred that the LCL filter has three poles, one at the origin of the s-plane and other two complex poles at the  $j\omega$ -axis. This makes the system marginally stable.

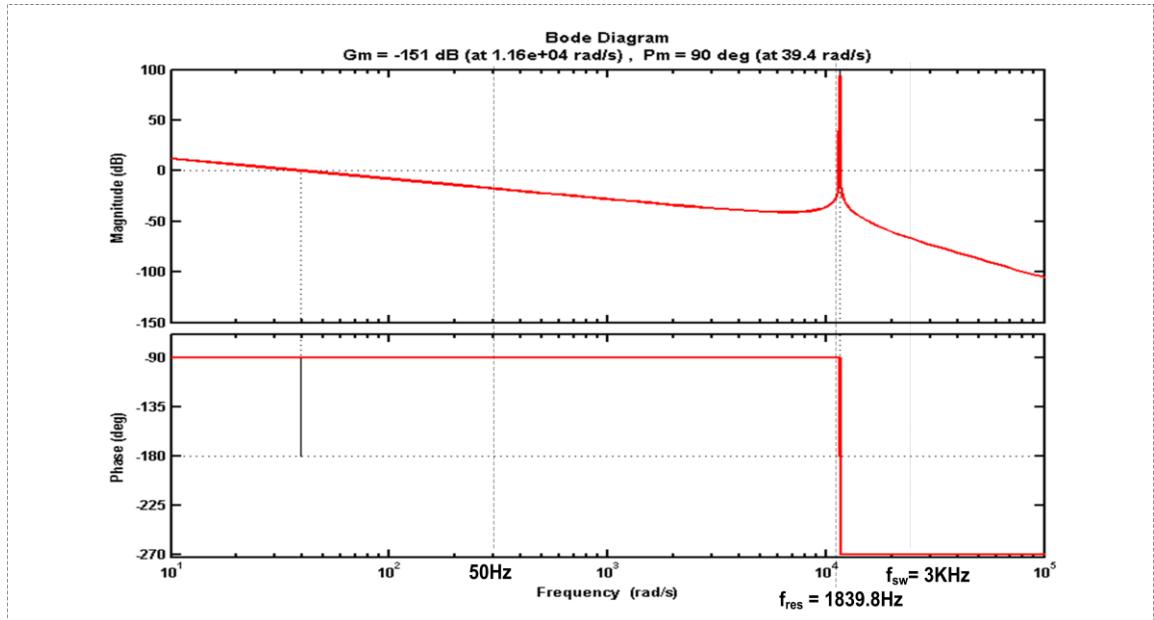


Fig 5-8: Bode plot of LCL filter without damping resistor

In bode plot of LCL filter without damping resistor, we can observe that

- Both the gain margin ( $G_m$ ) and phase margin ( $P_m$ ) are having opposite signs, which resembles the system instability.
- In magnitude plot, a peak is occurring at resonant frequency which causes the abrupt increase in gain margin of system and causes oscillations and makes system unstable.
- In phase plot, at resonant frequency there is a phase shift of 180 degrees due to the sudden shift of phase plot from -90 degrees to -270 degrees. This changes the system behaviour.

To achieve stable operation of SPWM inverter, the resonance due to LCL filter and the oscillations need to be damped. Hence, we use damping resistor.

### 5.5(b) Stability analysis of LCL filter with damping resistance

Open loop transfer function of LCL filter with damping resistance is given as:

$$G_d(s) = \frac{I_g}{V_i} = \frac{C_f R_d s + 1}{L_i C_f L_g s^3 + C_f (L_i + L_g) R_d s^2 + (L_i + L_g) s}$$

Where  $I_g$  = Grid side current

$V_i$  = Inverter output voltage

$R_d$  = Damping resistor

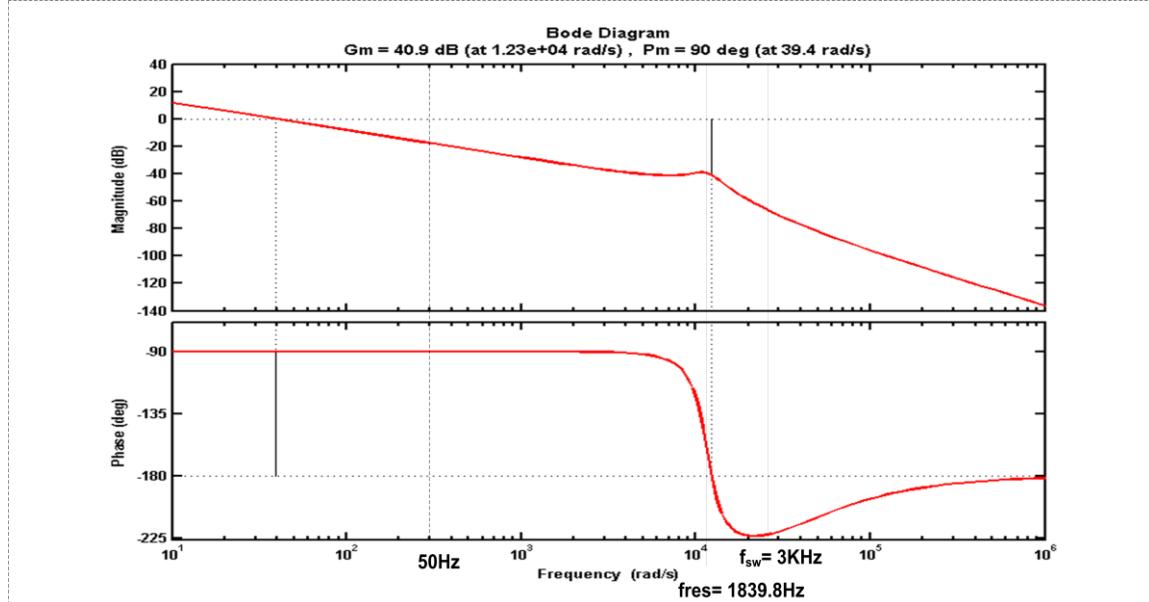
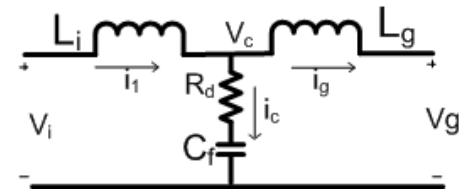


Fig 5-9: Bode plot of LCL filter with damping resistor

In bode plot of LCL filter with damping resistor, we can observe that

- Both the gain margin ( $G_m$ ) and phase margin ( $P_m$ ) are having same signs, which resembles that the system is stable.
- The bode plot has smoothed and free of unnecessary oscillations.
- In magnitude plot, the peak which was occurring earlier at resonant frequency has diminished by the addition of damping resistor. Addition of series damping resistor with capacitor improves stability of the system by attenuating the ripples at resonant frequency.
- In phase plot, at resonant frequency the phase shift of 180 degrees which was there earlier is rolled off.

**Hence, we can say that filter which we have designed is stable.**

## 6.CONCLUSION

Different topologies of single-phase as well as three-phase multi-level inverters have been studied. Of all the three different topologies Cascaded H-bridge topology is found to be superior and in our project analysis of CHB of different levels at various switching frequencies has been carried out.

Different SPWM techniques have been studied. In all the SPWM techniques, Carrier wave based PWM schemes are mostly used for Multi-level inverter topologies. Among the three Carrier wave based PWM schemes, Phase Opposite Disposition (POD) is found to have lesser %THD from our analysis. So, we have carried our further analysis on POD technique.

Effect of Carrier frequency on CHB topology has been studied and it can be concluded that on a particular level if switching frequency is increased, the %THD decreases.

Effect of modulation index ( $M_a$ ) has been studied and we can conclude that as  $M_a$  reduces from unity there is reduction in levels of output voltage. As we decrease the  $M_a$ , the fundamental decreases and %THD increases due to decrease in number of levels.

Passive filter topologies (L, LC and LCL) have been studied for multi-level inverters and with respect to filter requirements as well as %THD it is found that LCL filter is more preferable in conjunction with multi-level inverters. Filter design parameters for various levels as well as switching frequencies have been calculated from the conventional design formulas and their THD analysis has been carried out.

According to the IEEE standards, the permissible limit of individual harmonic distortion is up to 5%. But from the conventional filter design of LCL filter, it is observed that the %THD is much less than 5%. So, by maintaining the IEEE standards of %THD, the filter design parameters have been chosen arbitrarily. Hence from our analysis we can conclude that as we go on increasing the levels of multi-level inverter, filter requirements have been reduced so that its size and cost. But there is limitation in increasing levels as the circuit complexity increases with levels as well as size and cost increases. Similarly, it can be concluded that with increase in switching frequency again there is decrement in %THD with levels but the limitations of increasing switching frequency are increase in switching losses and EMI interference.

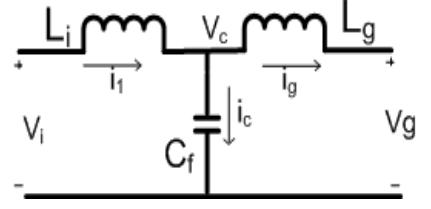
The stability analysis of designed LCL filter has been carried out and also it is found that pure LCL filter makes the system unstable and causes oscillations which has been inferred from the bode plots. So, to damp the oscillations a damping resistor should be used. Addition of series damping resistor with capacitor improves stability of the system by attenuating the ripples at resonant frequency.

Hence, it can be concluded that our designed LCL filter is stable.

## APPENDIX

For the LCL filter,

$$\begin{aligned}
 V_i(s) - sL_i i_L(s) - V_{c(s)} &= 0 \\
 -sL_g i_g(s) - V_{g(s)} + V_c(s) &= 0 \\
 V_{c(s)} &= \frac{i_c(s)}{C_f s} \\
 i_L(s) &= \frac{V_i(s) - V_{c(s)}}{sL_i}
 \end{aligned}$$



$$i_g(s) = \frac{V_c(s) - V_{g(s)}}{sL_g}$$

$$i_L(s) - i_{Lc}(s) = i_g(s)$$

$$i_L(s) - i_g(s) = i_c(s)$$

$V_i$  and  $V_g$  are two inputs,  $i_g(s)$  is the output.

Required T.F is  $\frac{i_g(s)}{V_i(s)}$

$$i_c(s) = s^2 L_g C_f i_g(s)$$

$$V_i(s) - sL_i i_L(s) - \frac{i_c(s)}{C_f s} = 0$$

$$V_i(s) - sL_i(i_c(s) + i_g(s)) - \frac{s^2 L_g C_f i_g(s)}{C_f s} = 0$$

$$V_i(s) - sL_i(i_c(s) + i_g(s)) - sL_g i_g(s) = 0$$

$$V_i(s) - sL_i i_g(s) - sL_i(s^2 L_g C_f i_g(s)) - sL_g i_g(s) = 0$$

$$V_i(s) = i_g(s)[s(L_i + L_g) + s^3 L_i L_g C_f]$$

And hence, we get

$$G_d(s) = \frac{i_g}{V_i} = \frac{1}{L_i C_f L_g s^3 + (L_i + L_g)s}$$

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