

SN65518, SN75518

VACUUM FLUORESCENT DISPLAY DRIVERS

SLDS004B - MARCH 1983 - REVISED MAY 1990

- Each Device Drives 32 Lines
 - 60-V Output Voltage Swing Capability
 - 25-mA Output Source Current Capability
 - High-Speed Serially Shifted Data Input
 - Latches on All Driver Outputs

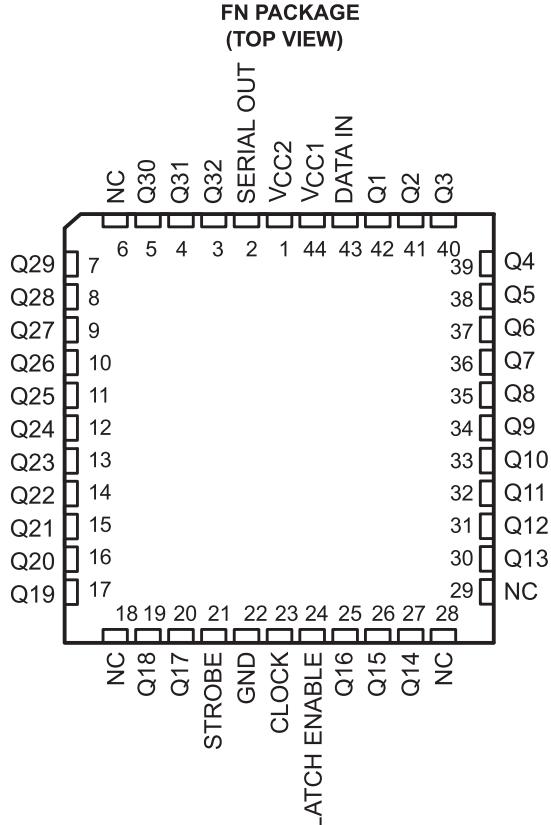
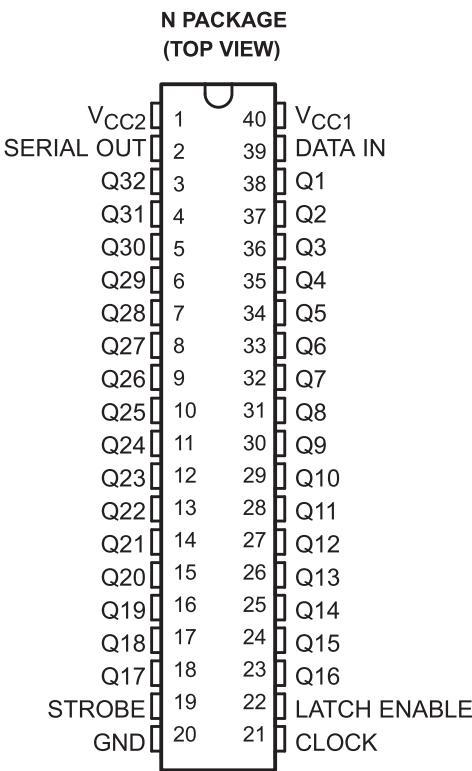
description

The SN65518 and SN75518 are monolithic BIDFET[†] integrated circuits designed to drive a dot matrix or segmented vacuum fluorescent display.

Each device consists of a 32-bit shift register, 32 latches, and 32 output AND gates. Serial data is entered into the shift register on the low-to-high transition of CLOCK. While LATCH ENABLE is high, parallel data is transferred to the output buffers through a 32-bit latch. Data present in the latch during the high-to-low transition of LATCH ENABLE is latched. When STROBE is low, all Q outputs are enabled. When STROBE is high, all Q outputs are low.

Serial data output from the shift register may be used to cascade additional devices. This output is not affected by LATCH ENABLE or STROBE.

The SN65518 is characterized for operation from -40°C to 85°C . The SN75518 is characterized for operation from 0°C to 70°C .



NC – No internal connection

[†]BIDFET – Bipolar, double-diffused, N-channel and P-channel MOS transistors on same chip. This is a patented process.

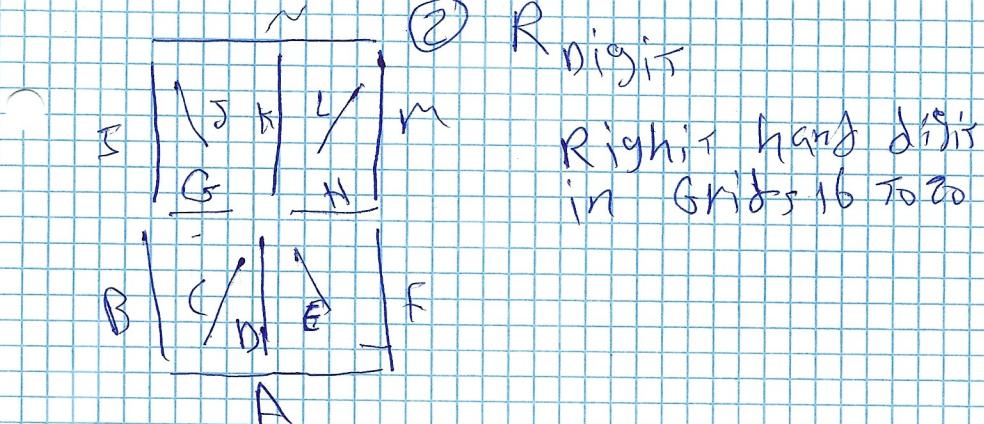
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

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$$A = \$2$$

$$B = \$4$$

$$C = \$6$$

$$D = \$8$$

$$E = \$10$$

$$F = \$12$$

$$G = \$15$$

$$H = \$17$$

$$I = \$20$$

$$J = \$22$$

$$K = \$24$$

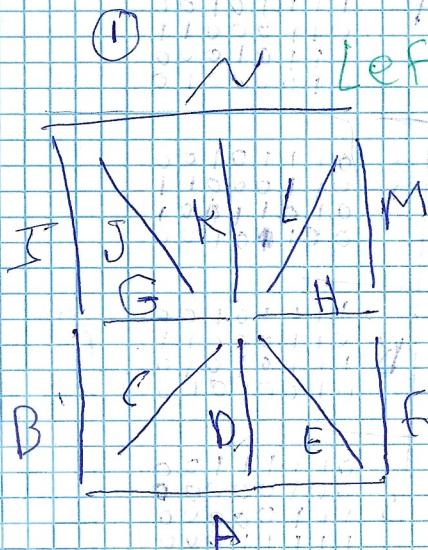
$$L = \$26$$

$$M = \$28$$

$$N = \$30$$

01110100
01100011
11100000
10000100

left hand digit
in Grids 16 to 20



$$D_u = S18$$

$$D_d = S13$$

$$A = S1$$

$$J = S21$$

$$B = S3$$

$$K = S23$$

$$C = S5$$

$$L = S25$$

$$D = S7$$

$$M = S27$$

$$E = S9$$

$$N = S29$$

$$F = S11$$

$$G = S14$$

$$H = 16$$

$$I = S19$$

	6 ₁	6 ₂	6 ₃	6 ₄	left digit data in Grids 16 To 20
1 =	16	0	16	0	
2 =	80	2	128	20	
3 =	64	18	128	20	
4 ≤	0	28	144	16	
5 ≤	64	18	144	4	
6 ≤	80	18	144	4	
7 ≤	0	16	(28)	20	
8 ≤	80	20	144	20	
9 ≤	0	18	144	20	
0 =	80	16	16	20	

~~115 155 115 815 215 115 015 65~~
 85 25 95 55 65 85 25 15

1 8

A

0	1	1	1	0	1	0	0
0	1	1	0	0	0	1	1
0	0	0	1	1	1	1	1
1	0	0	0	1	0	0	0

B

1	1	1	1	0	1	0	0
0	1	1	0	0	0	1	1
1	1	0	1	0	0	0	0
1	1	1	1	0	0	0	0

C

0	1	1	1	0	1	0	0
0	1	1	0	0	0	0	1
0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0

E

1	1	1	1	1	1	0	0
0	0	1	0	0	0	0	1
1	1	1	0	1	0	0	0
0	1	1	1	1	1	0	0

F

1	1	1	1	1	1	1	0	0
0	1	0	0	0	0	0	1	1
1	1	1	0	1	0	0	0	0
0	1	0	0	0	0	1	0	0

G

0	1	1	1	0	1	0	0
0	1	1	0	0	0	0	1
0	1	1	1	0	0	0	0
1	0	1	1	1	1	0	0

H

1	0	0	0	1	1	0	0
0	1	1	0	0	0	1	1
1	1	1	1	0	0	0	0
1	1	0	0	0	1	0	0

byte[0] D2 D4 D5 D6

byte[1] D0 D1 D5 D6

byte[2] D0 D1 D2 D3 D4

byte[3] D3 D7

byte[4] D2 D4 D5 D6 D7

byte[5] D0 D1 D5 D6

byte[6] D3 D5 D6 D7

byte[7] D4 D5 D6 D7

byte[8] D2 D4 D5 D6

byte[9] D0 D5 D6

byte[10] D3

byte[11] D3 D4 D5 D7

byte[12] D2 > D7

byte[13] D1 D4

byte[14] D3 D5 D6 D7

byte[0] D2 > D7

byte[1] D0 D4

byte[2] D3 D5 D6 D7

byte[3] D1 D6

byte[4] D2 D4 D5 D6

byte[5] D0 D4 D5

byte[6] D3 D4 D5 D6

byte[7] D2 D3 D4 D5 D7

byte[8] D2 D3 D7

byte[9] D1 D5 D6

byte[10] D3 > D7

byte[11] D2 D6 D7

Grid 15

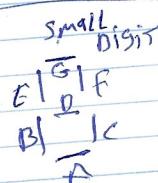
S₁ VOL

S₂ -FS₃

S₁₁ = MUTE

S₁₉ = 'dB

S₂₀ = G, E, C, A



S₂₁ = F, B

S₂₂ = D

S₂₃ = ...

S₂₄ = ADAPTIVE DRC

S₂₅ = VIRTUAL

S₂₆ = SL

S₂₆ = SW

S₂₈

S₂₇ = SR

S₂₈ = PBL

S₂₉ = SB

S₃₀ = SBR

\xrightarrow{G} Digit ① L

E \xrightarrow{D} F

B \xrightarrow{I} C

A

S₄ = A

S₇ = D

S₅ = B

S₈ = E

S₆ = C

S₉ = F

S₁₀ = G

S₁₁ = G

\xrightarrow{G} Digit ② R

E \xrightarrow{D} F

B \xrightarrow{I} C

F

S₁₂ = A

S₁₅ = D

S₁₃ = B

S₁₆ = E

S₁₄ = C

S₁₇ = F

S₁₈ = G

Grid 16

~~123~~

S2 CINEMA DSP

1 S10
2 S8
3 S6
4 S4

S12 BLUETOOTH simple

S13

zone 1
2 AC

S17

S20

S15

zone 1
3 BE

S18

S22

S24 sleep

S26 party

S28 TUNED

S20 STEREO

S31 ENHANCER

Grid 20

S13 = HDMI

S18 charge

S31 2

S32 1

S33 OUT

S34 ECO

S35 ...

S36 ...

S37 ...

1 = E, B

2 = G, F, D, B, A

3 = G, F, D, C, A

$$G/F = 192$$

$$B/A = 22$$

4 = E, F, D, C

5 = G, E, D, C, A

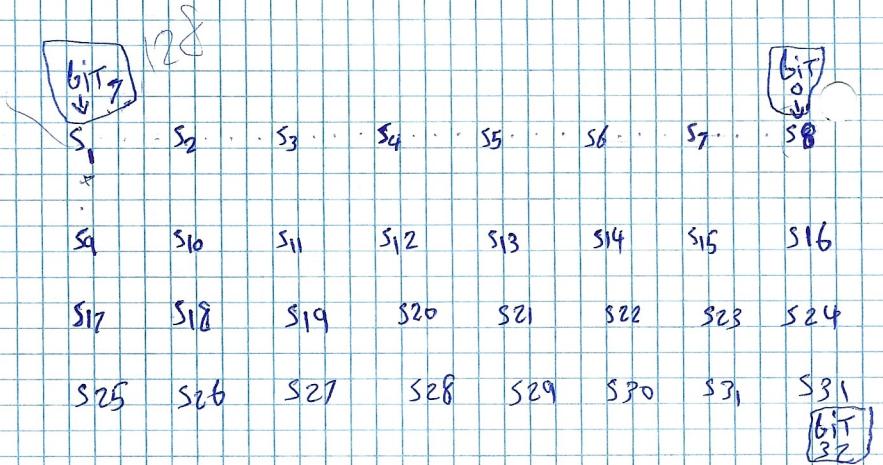
6 = G, E, D, B, A, C

7 = G, F, C

8 = G, F, C, A, B, E, D

9 = G, F, D, E, C

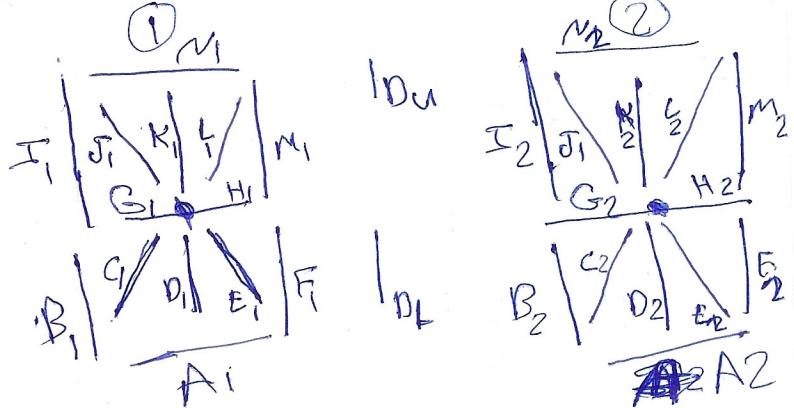
0 = G, F, C, A, B, E



S = Segments pins in VFD

using SN 75518 shift register

32 bits



S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉
A ₁	A ₂	B ₁	B ₂	C ₁	C ₂	D ₁	D ₂	E ₁
S ₁₀	S ₁₁	S ₁₂	S ₁₃	S ₁₄				
E ₂	F ₁	F ₂	B ₂	G ₁				
S ₁₅	S ₁₆	S ₁₇	S ₁₈	S ₁₉				
G ₂	H ₁	H ₂	D ₄	I ₁				
S ₂₀	S ₂₁	S ₂₂	S ₂₃	S ₂₄				
I ₂	J ₁	J ₂	K ₁	K ₂				
S ₂₅	S ₂₆	S ₂₇	S ₂₈	S ₂₉				
L ₁	L ₂	M ₁	M ₂	M ₁				

S₃₀
N₂

CHARGE

HDMI

OUT 1/2

ECO



ENHANCER

STEREO

TUNED

PARTY

SLEEP

MUTE

ZONE

[2 A]

[3 B]

VOL.

100.8
dB

CINEMA

DSP



ADAPTIVE DRC VIRTUAL

PPG

SL SW SR

SBL SB SBR

SW101
INFO

SW103
MEMORY

SW105
PRESET

SW107
PRESET

SW109
FM

SW111
AM

SW113
TUNING

SW115
TUNING

V1001

E229910-A9U
PY-1 94V-0
LF
Sn-Ag-Cu

SCENE1
BD/DVD
SW112

SCENE2
TV
SW114

SCENE3
CD
SW116

SCENE4
RADIO
SW118

