COL215: Digital Logic and System Design

Software Assignment - 2

Circuits with D Flip Flops and Area Optimisation

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ALGORITHM

A:- Calculating Longest Combinational Path Delay in Circuits with D Flip Flops

In this algorithm, we use memorisation (dynamic programming)

1. Parsing and storing of the circuit

- From the file "gate delays.txt, parse the input and store the gate information in the form of five lists, one for each type of gate(AND2, OR2, NAND2, NOR2 and INV2). In these lists, 3 pairs are stored, sorted in the increasing order of the gate delays.
- Create five lists: primary inputs, primary outputs, internal_signals, dff_inputs and dff_outputs and four dictionaries: out circuit graph, out generator gate, out delay evaluated, and out delay.
- Read and parse the circuit specifications from the circuit.txt file.
- Store primary inputs, primary outputs, signals, dff inputs and dff outputs in lists: primary_inputs, primary_outputs, internal_signals, dff_inputs and dff_outputs.
- Store circuit specifications in out_circuit_graph and out_generator_gate dictionaries:
  i. out_circuit_graph stores signals as keys and a tuple of corresponding generating signals as values.
  ii. The information about the DFF gates is not stored in the previous step.
  iii. out_generator_gate stores signal as keys and corresponding generating gate as values.
  iv. For example, if signal C is generated from signals A and B by a NAND2 gate, then (C, (A, B)) is a key-value pair of out_circuit_graph.
  v. (C, NAND2) is a key-value pair of out_generator_gate.
  vi. Initially, out_delay_evaluated is true for primary inputs and dff_outputs and false otherwise.
  vii. Initially, out_delay is 0 for inputs and None otherwise.

2. Function to find output delays

   The function find_out_delay() is called on every DFF input and primary output, and the results are stored in a list res. When find_out_delay(x) is called:
   - If the value of out_delay[x] is already evaluated, return it (in constant time).
   - If not, find the maximum delay of child nodes (y) and add it to the delay of the gate that generates signal x.
   - Store the value in out_delay[x] and mark that out_delay[x] has been evaluated.
   - Return out_delay[x].

3. Time Complexity
   The time complexity of this algorithm is O(no of gates + no of signals). As we are traversing every gate and every edge exactly once, this time complexity is achieved.

B:- Area Optimisation

1. Exact solution (slower:- for circuits with less gates)
   - In exact solution, we take all possible permutations of gates, which is equal to 3 ^ (n), where n is the total number of gates in the circuit
   - We calculate the delay for the longest combinational path delay for each permutation.
   - We calculate the area for that permutation only when the longest combinational path delay is less than the delay constraint given to us.
   - We calculate the minimum of all these areas, which is the required answer.
   - **Time complexity**:- Since we are considering all possible permutations, which is 3 ^ n, and in every case, the time for finding the longest combinational delay and its total area is O(no of gates+ no of edges), so the time complexity of (no of gates+ no of edges) * (3 ^ no of gates).
2. Approximate solution (faster:- for circuits with more gates)
   - We find a way to get some length n permutations of {0, 1, 2} with repetitions.
   - We begin with a permutation with all zeroes stored as a string.
   - From these, in the i^{th} iteration of a loop, we perturb the i^{th} position of the string, replacing zeroes by 1 and 2. We check if the longest delay is within the delay constraint. Then, it is included in the list of strings. If it is, then we calculate the area. If this area is smaller than the minimum area, then this area is made minimum.
   - If the delay is more, then the string is not included in the list
   - But we don't take all the possible permutations. We take only some 50*(i+1) permutations that we get first in the i^{th} loop so that we don't consider an exponential order of possibilities.
   - **Time Complexity:-** In the i^{th} iteration, we can only accommodate 50*(i+1) many permutations. So, in total n iterations, we consider O(n^2) many possibilities. And for every possibility, all other factors like max combinational path and gate area computation take O(n) time. Hence overall time complexity is O(n^3)

TEST CASES

- **Test case 1:-** This test case was given with the question statement as an example.
- **Test case 2:-** It takes into account when an input signal is directly given as an input to a DFF.
- **Test case 3:-** This test case has a very high delay constraint, which means that always the gates with the minimum area (max delay) must have been used, which is indeed what we got as the answer.
- **Test case 4:-** This test case has a delay constraint lower than the longest combinational delay calculated in part a, indicating no possible solution, which is expected as we get infinite (inf) as the answer.
- **Test case 5:-** It has a delay constraint just greater than the longest combinational delay calculated in part a, which means always the gates with minimum delay (maximum area) should have been used, which is what we got.
- **Test case 6:-** This test case has a DFF in a loop.
- **Test case 7:-** This test case incorporates a hypothetical case when all the gates will have a zero delay, so all the combinational paths, so the longest combinational path, would have zero delay. Also, any non-negative delay can be achieved by gates of minimum area (as all delays are zero), which is indeed what we got.
- **Test case 8:-** It also considers a hypothetical case when all the gates take no area on the circuit, so area required will always be zero, no matter what delay constraint is (given it to be greater than the longest combinational path delay).
- **Test case 9:-** It considers the case when two DFFs are connected in series in the circuit.
- **Test case 10:-** It is a big and complex test case incorporating multiple corner cases from previous test cases.