COL202: Digital Logic and System Design

Hardware Assignment-0
AND Gate

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PROBLEM DESCRIPTION

Design and implement a circuit that takes two inputs from the switches of the BASYS3 FPGA board and outputs the AND operation of the two inputs into a LED output of the board.

THEORY- (AND Gate)

An AND gate gives a HIGH(1) output if and only if all the inputs are HIGH; otherwise, it gives a LOW(0) output.

The truth table for two inputs AND gate is:-

INPUT		OUTPUT
a	b	c = a AND b
0	0	0
0	1	0
1	0	0
1	1	1

DESIGN DECISIONS:

- We have taken inputs a and b from the switches V17 and V16, respectively. If a switch is ON (or OFF), it corresponds to a HIGH (LOW) state.
- We have displayed the output c on LED U16. If the LED is ON(OFF), it corresponds to a HIGH(LOW) output.

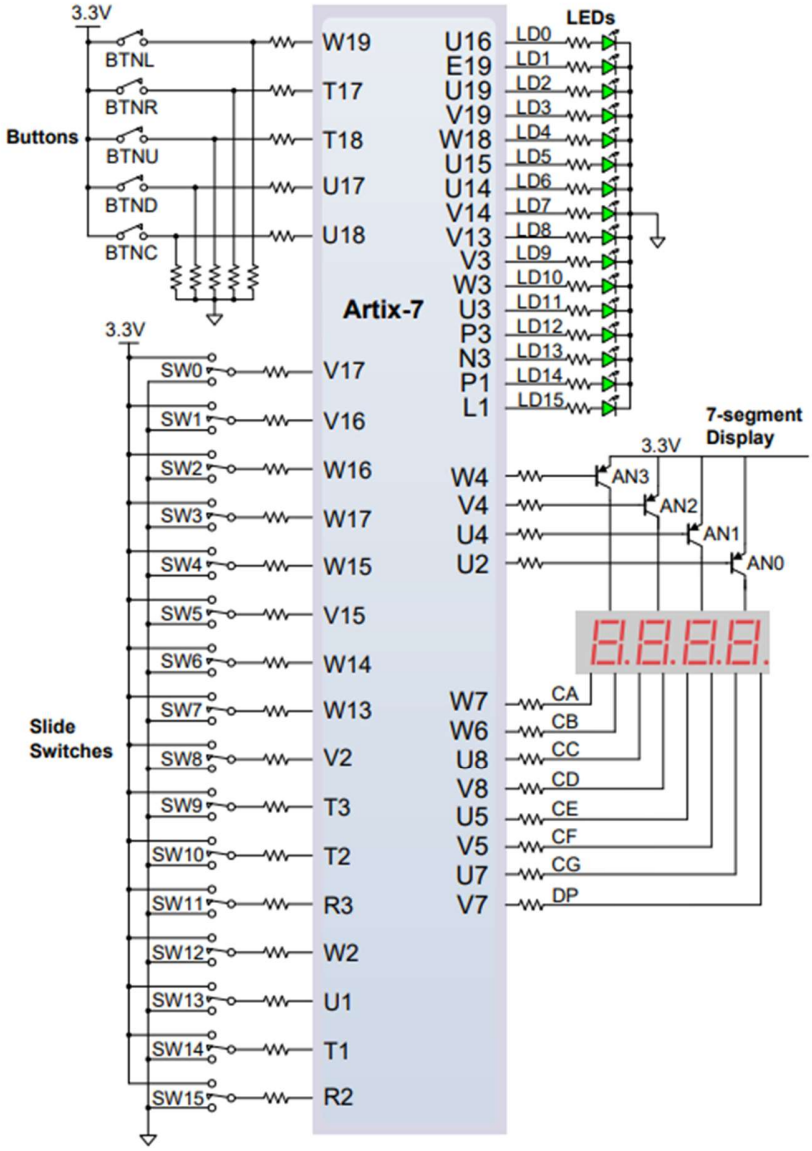


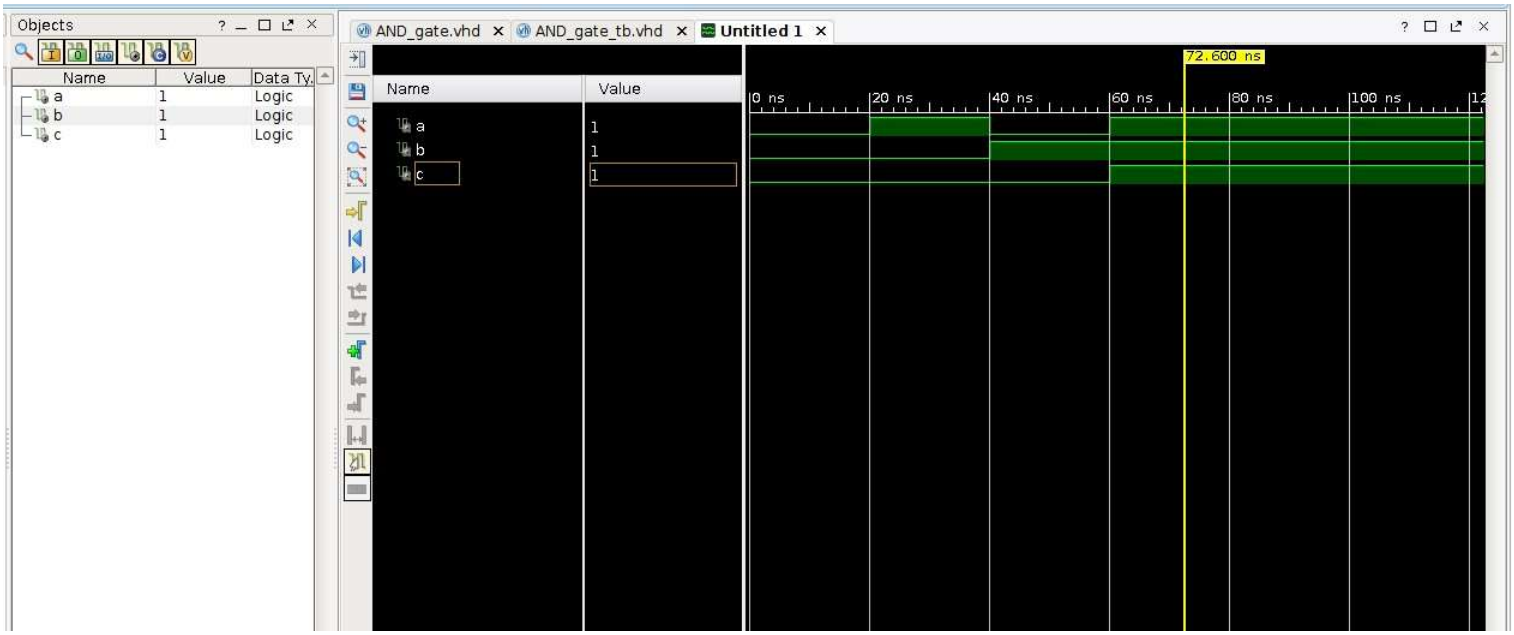
Fig1: General purpose I/O devices on BASYS3 board.

LAB WORK

1. We opened Vivado, created a new project to develop a source file(AND_gate.vhd), added a constraint file basys3.xdc, and selected the part number xc7a35tcpg236-1.
2. Source code:-
   We updated the source file as uploaded with this report.

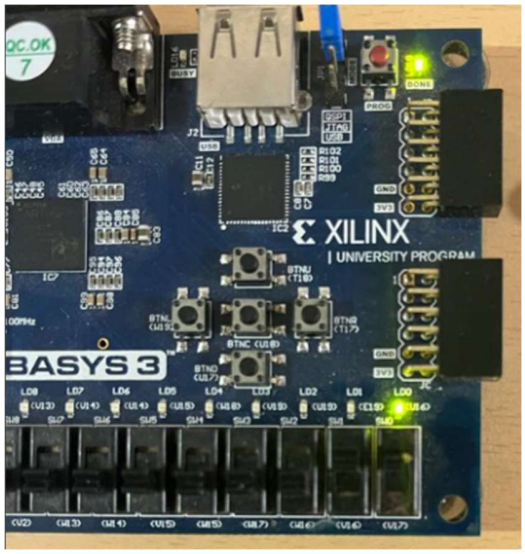
3. Simulation of the Design:-
   For the design simulation, we created a testbench file named AND_gate_tb.vhd as uploaded.
   After the simulation is completed, this simulation file is disabled.
4. Constraint file
   We updated the constraint file as uploaded so that the inputs a and b are taken, and output c is displayed as planned in the design.
5. Synthesis of design
   We click on Run Synthesis, then on Run Implementation, Generate the Bitstream, Auto connect the BASYS3 board and program the device.
   Now, we can give inputs to the BASYS3 board with switches and get AND output on the LED.

Simulation Snapshots

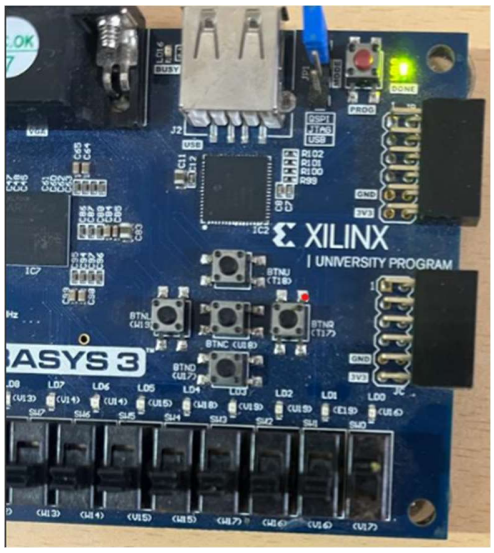


On running the simulation, we got this output form, which matches the expected output of the AND gate.

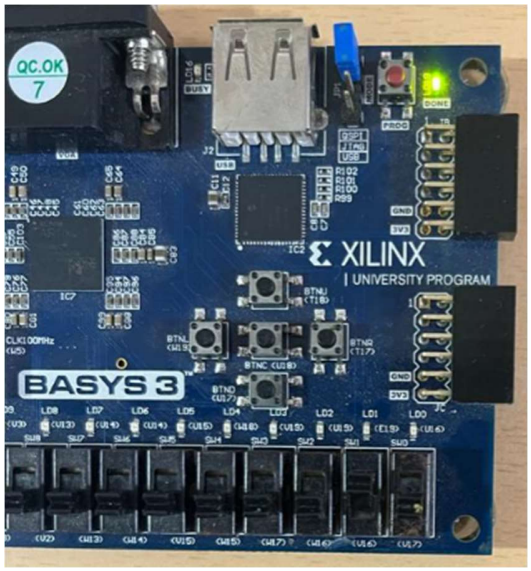
Synthesis Report



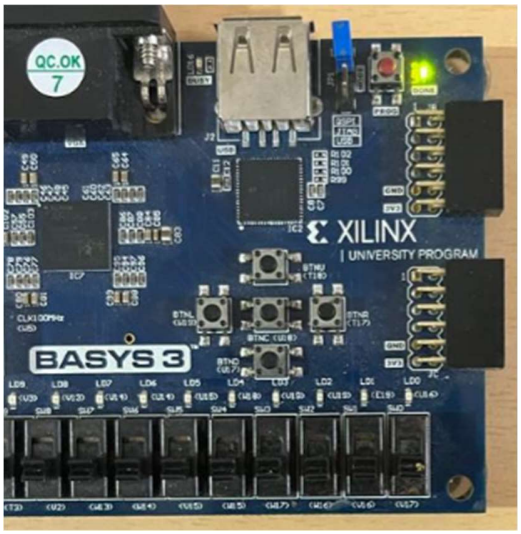
$a = 1 , b = 1 , c = 1$



$a = 1 , b = 0 , c = 0$



$a = 0 , b = 1 , c = 0$



$a = 0 , b = 0 , c = 0$

The experimentally obtained output matches the expected result.