COL215: Digital Logic and System Design

Hardware Assignment - 3

Image Filter Calculator using FSM

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PROBLEM DESCRIPTION

- To implement a 3 × 3 image filter operator with inputs as an image and a filter kernel and display the final filtered image on the screen using a VGA controller.

VHDL CODE STRUCTURE

FSM

- The FSM controls the signals cycle, task, rst, wr, hpos, vpos, clk25, and the address of the two ROMs and the RAM.
- Signal rst controls when the answer(obtained from MAC) must be assigned to be zero.
- Signal task controls which operation is going on currently. task is 0 for reading the kernel, 1 for calculating the maximum and minimum values of the answer, 2 for storing the normalised answer to the RAM and 3 for displaying from the RAM.
- wr controls the reading and writing from the RAM. When wr is 1, only writing to the RAM is done, and when wr is 0, only reading from the RAM is done.

MAC

- When rst = 0, i.e. the loop for calculating the answer is in between the 3*3 block, the answer gets updated accordingly at each clock cycle, else when rst = 0, answer remains to be 0 always.

```
architecture Behavioral of MAC is
    signal internal_ans : integer := 0;
begin
    ans <= internal_ans;
    process(clk, rst)
    begin
        if(rising_edge(clk)) then
            if rst = '1' then
                internal_ans <= 0;
            else
                internal_ans <= internal_ans + k*i;
            end if;
        end if;
```

```
    end process;

end Behavioral;
```

RENDERER

Using the signals from the RAM, the renderer calculates and updates the maximum and minimum values of the answer, reads from the ROM, and writes the normalised answer to the RAM. It also controls displaying from the VGA port.

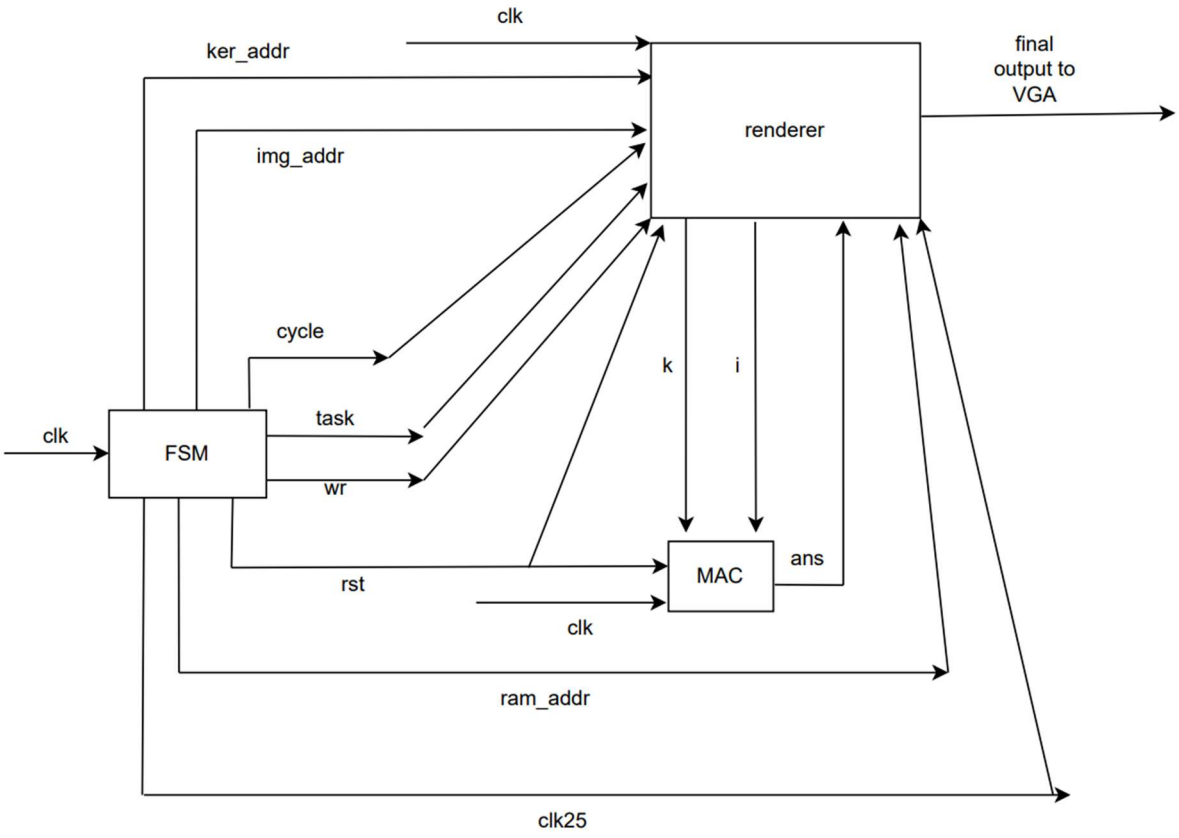
BASYS3 File mappings

```
## Clock signal
set_property PACKAGE_PIN W5 [get_ports clk]
        set_property IOSTANDARD LVCMOS33 [get_ports clk]
        create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5}
[get_ports clk]

## Switches
set_property PACKAGE_PIN V17 [get_ports {reset}]
        set_property IOSTANDARD LVCMOS33 [get_ports {reset}]

##VGA Connector
set_property PACKAGE_PIN G19 [get_ports {r[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {r[3]}]
set_property PACKAGE_PIN H19 [get_ports {r[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {r[2]}]
set_property PACKAGE_PIN J19 [get_ports {r[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {r[1]}]
set_property PACKAGE_PIN N19 [get_ports {r[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {r[0]}]
set_property PACKAGE_PIN N18 [get_ports {g[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g[3]}]
set_property PACKAGE_PIN L18 [get_ports {g[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g[2]}]
set_property PACKAGE_PIN K18 [get_ports {g[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g[1]}]
set_property PACKAGE_PIN J18 [get_ports {g[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {g[0]}]
set_property PACKAGE_PIN J17 [get_ports {b[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b[3]}]
set_property PACKAGE_PIN H17 [get_ports {b[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b[2]}]
```

```
set_property PACKAGE_PIN G17 [get_ports {b[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b[1]}]
set_property PACKAGE_PIN D17 [get_ports {b[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b[0]}]
set_property PACKAGE_PIN P19 [get_ports hsync]
        set_property IOSTANDARD LVCMOS33 [get_ports hsync]
set_property PACKAGE_PIN R19 [get_ports vsync]
        set_property IOSTANDARD LVCMOS33 [get_ports vsync]
```



Block diagram