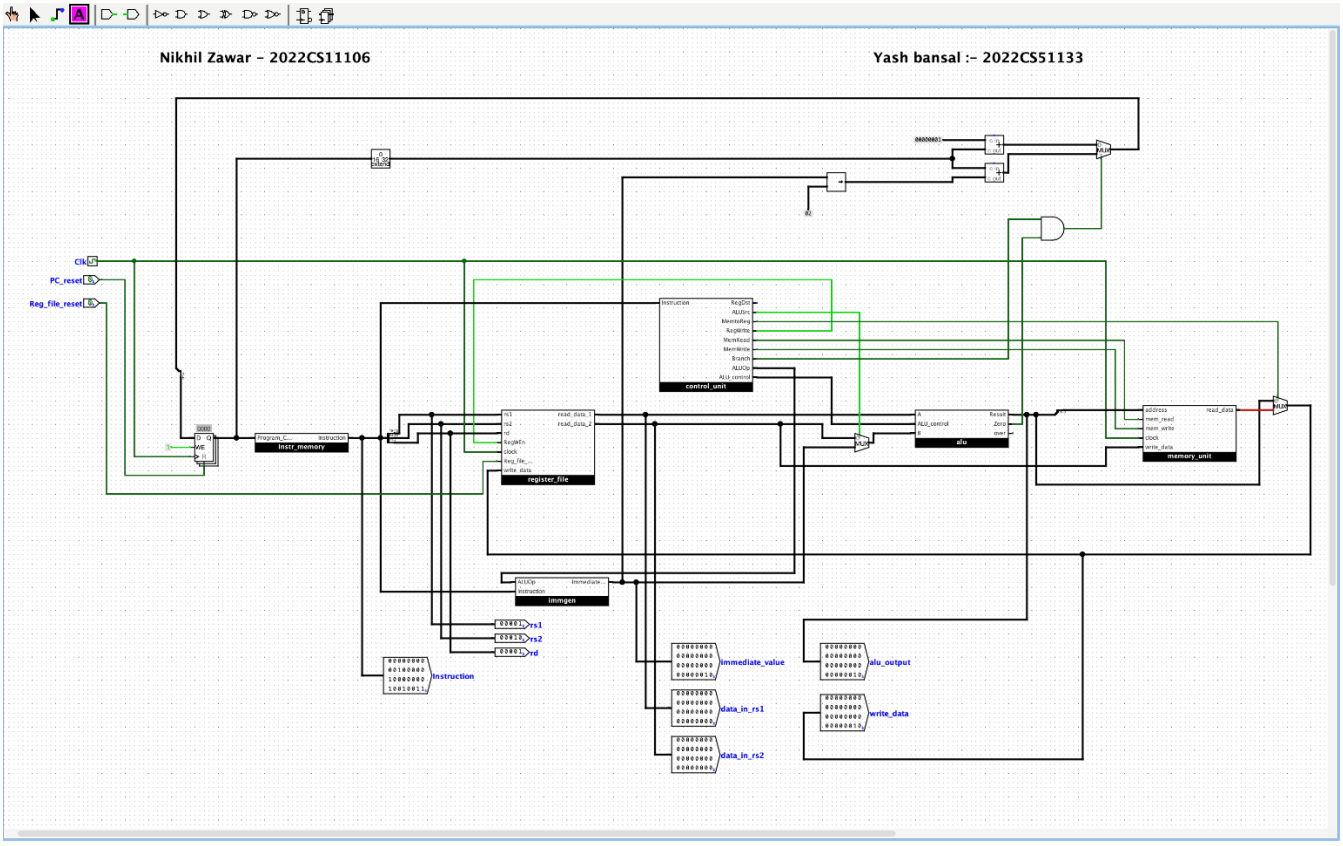
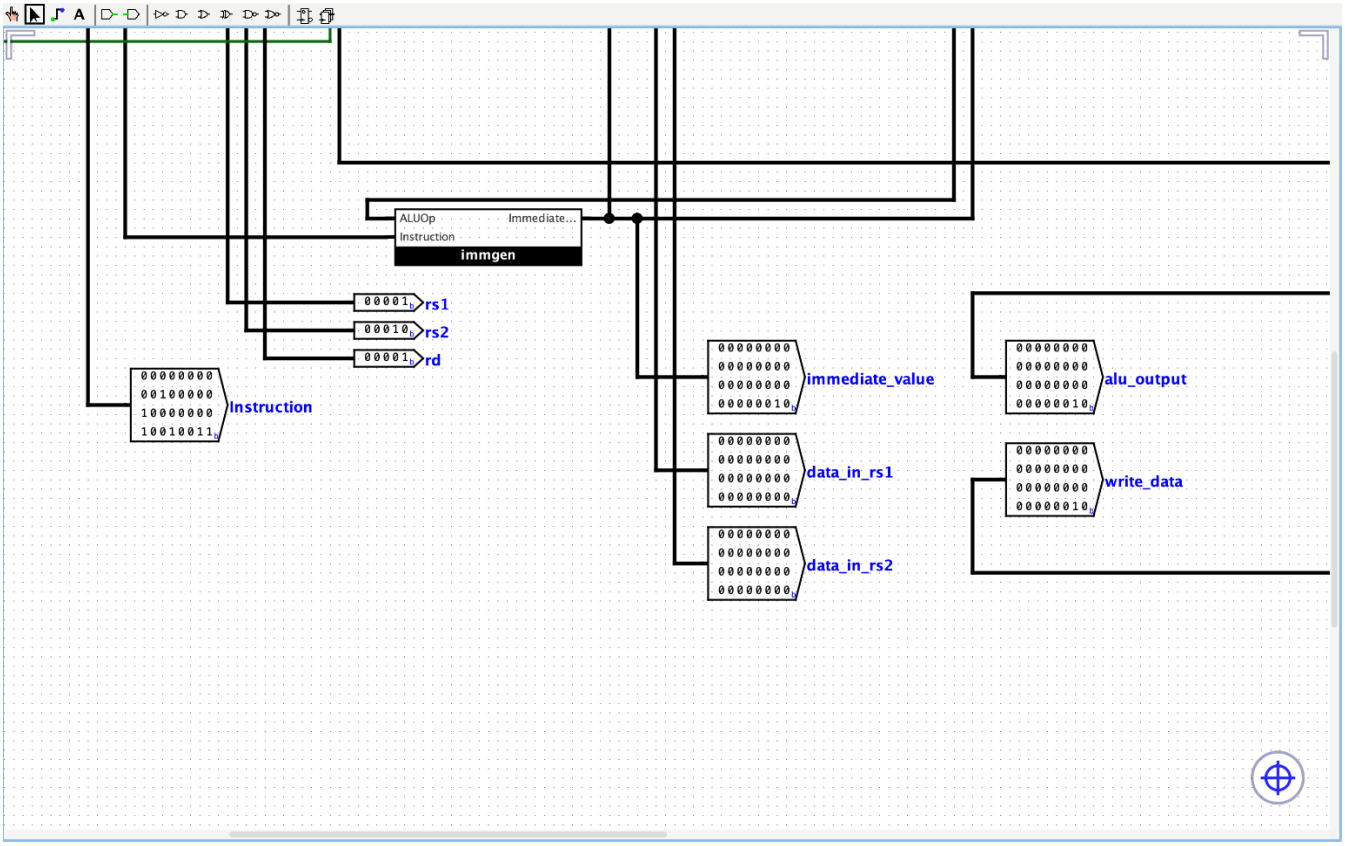
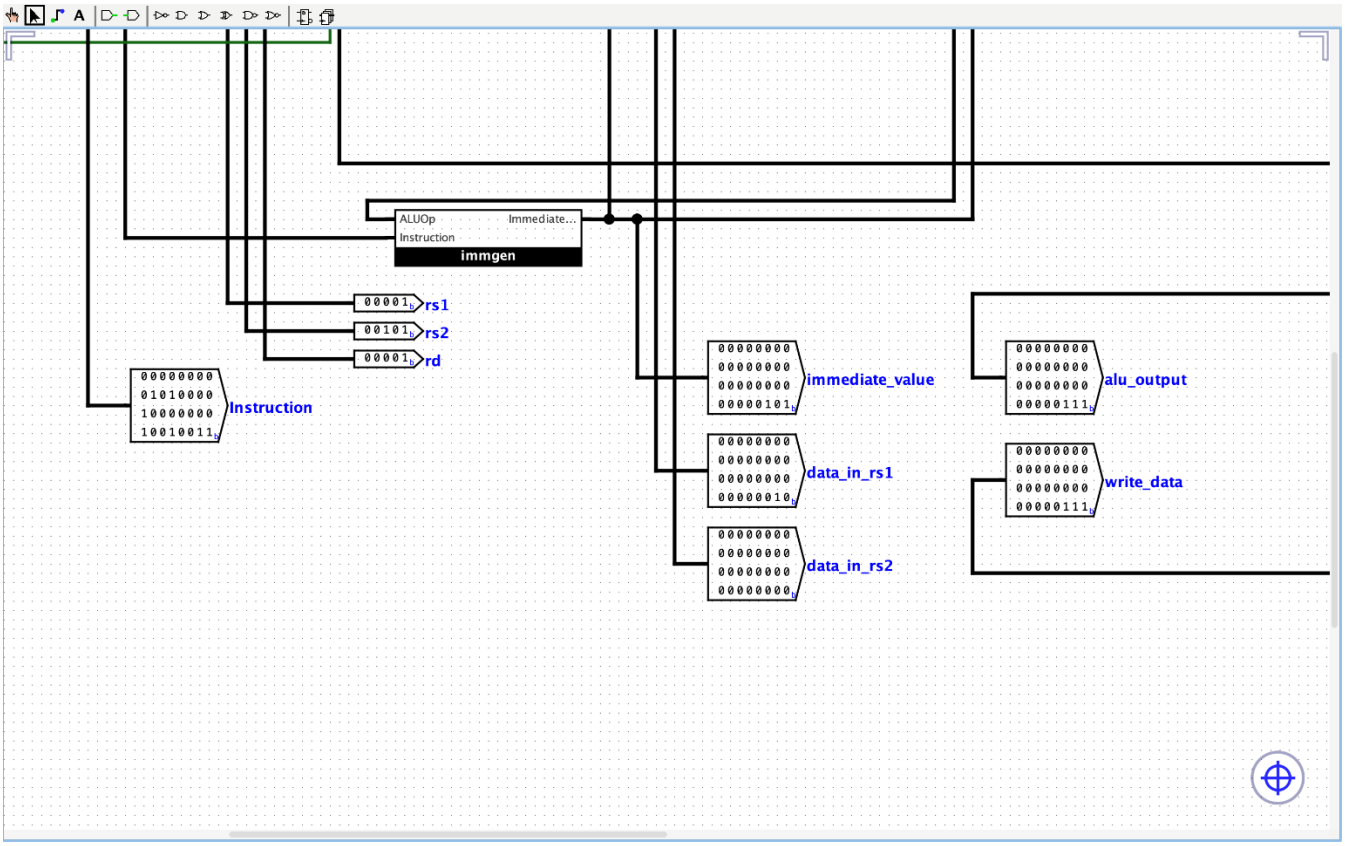


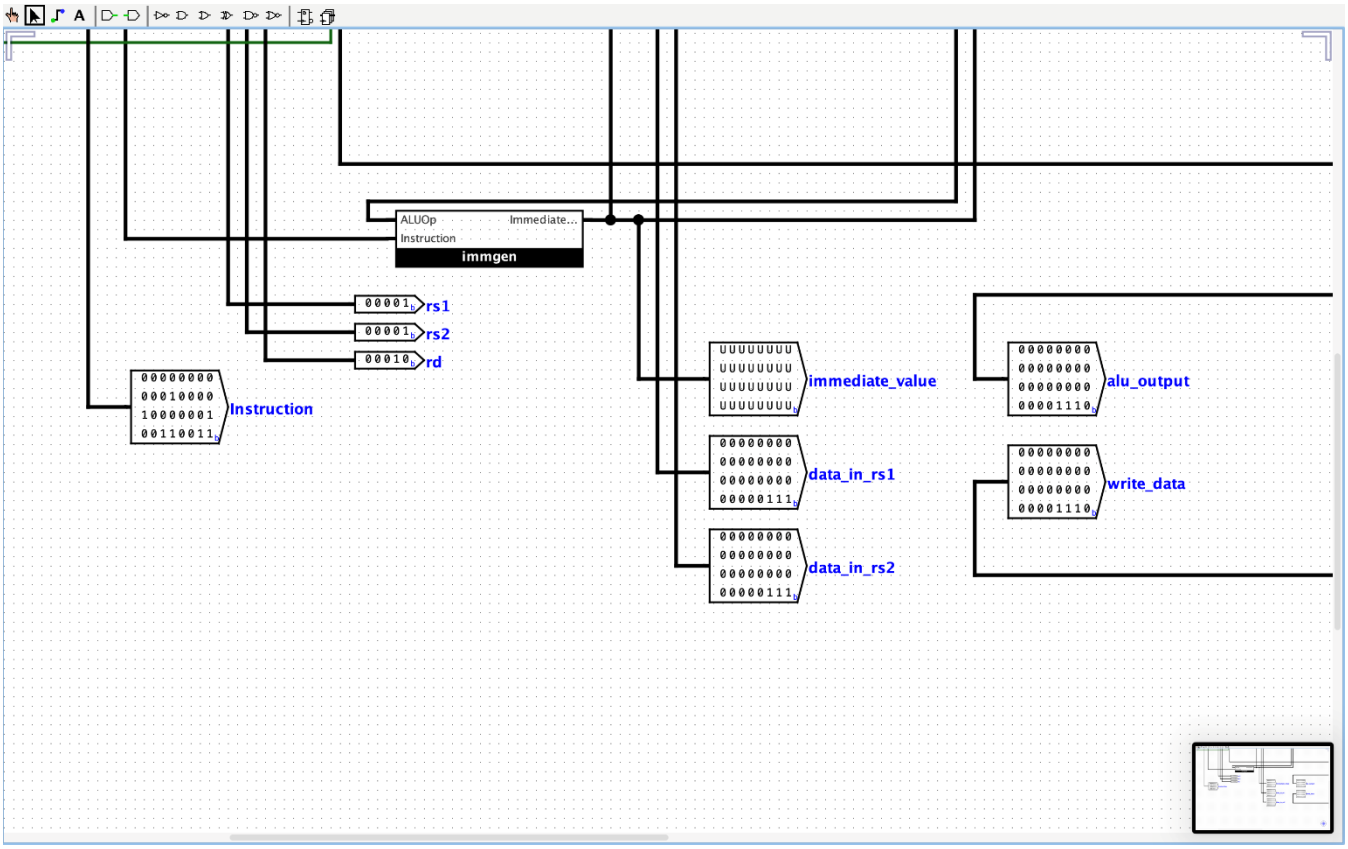
Final Processor



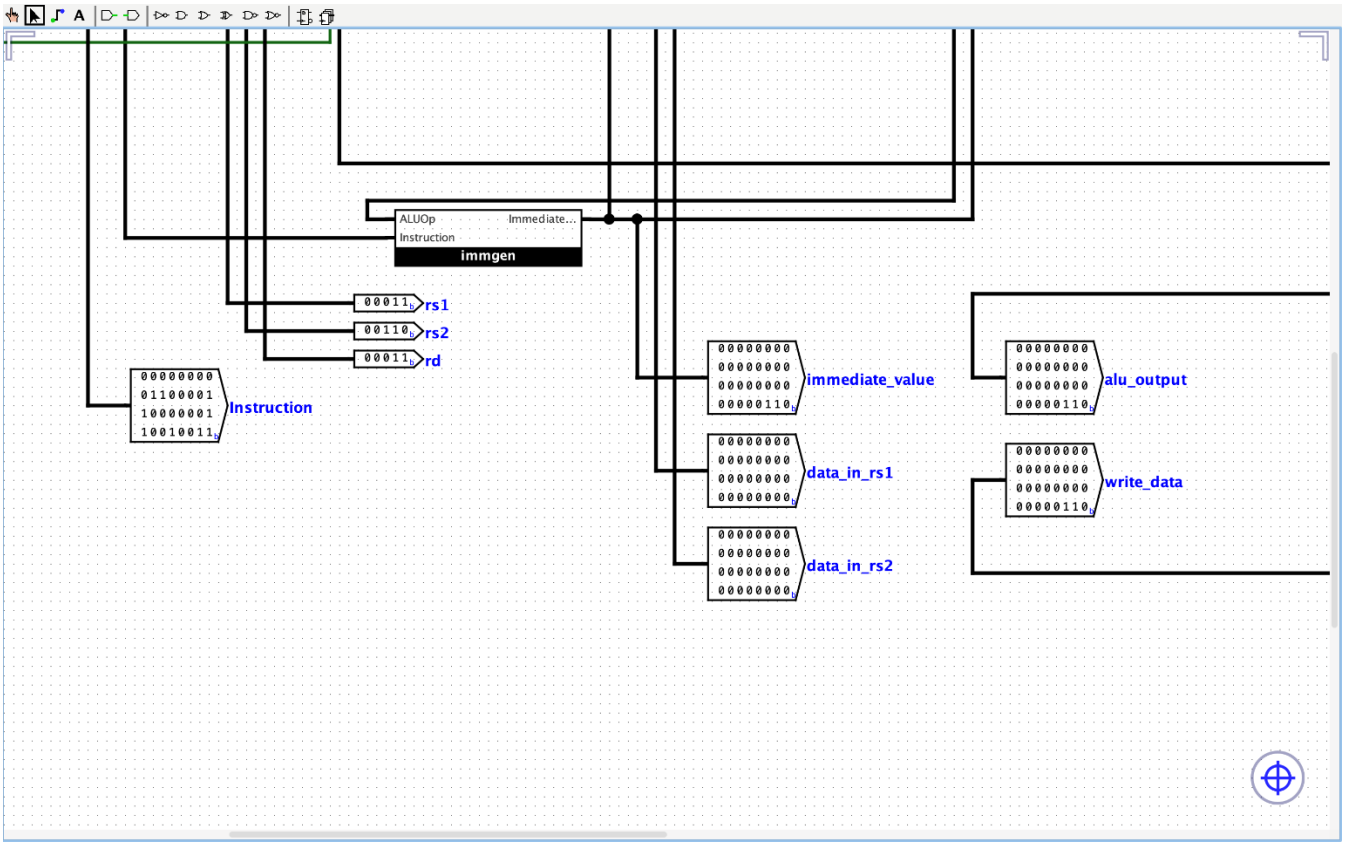
addi x1 x1 2



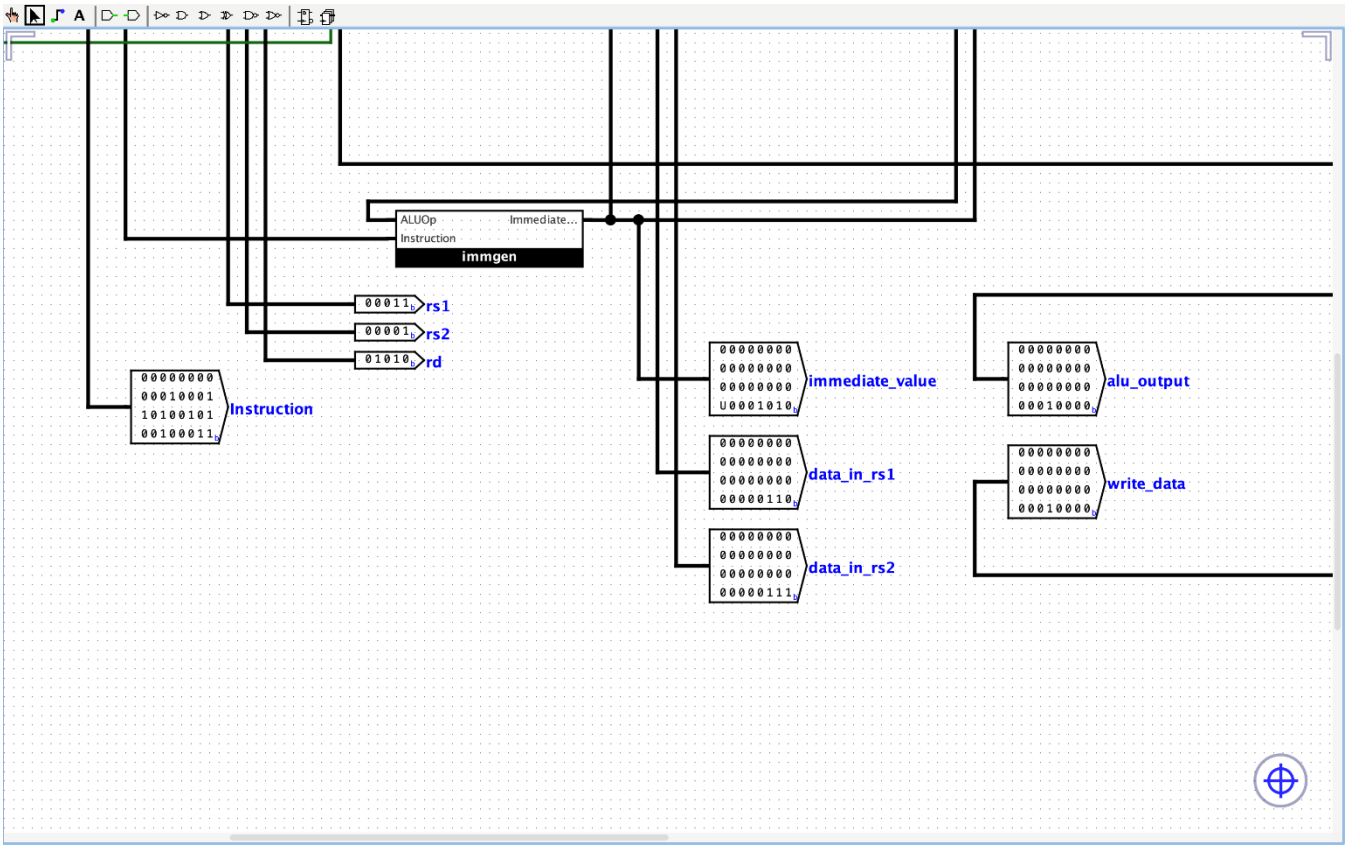
addi x1 x1 5



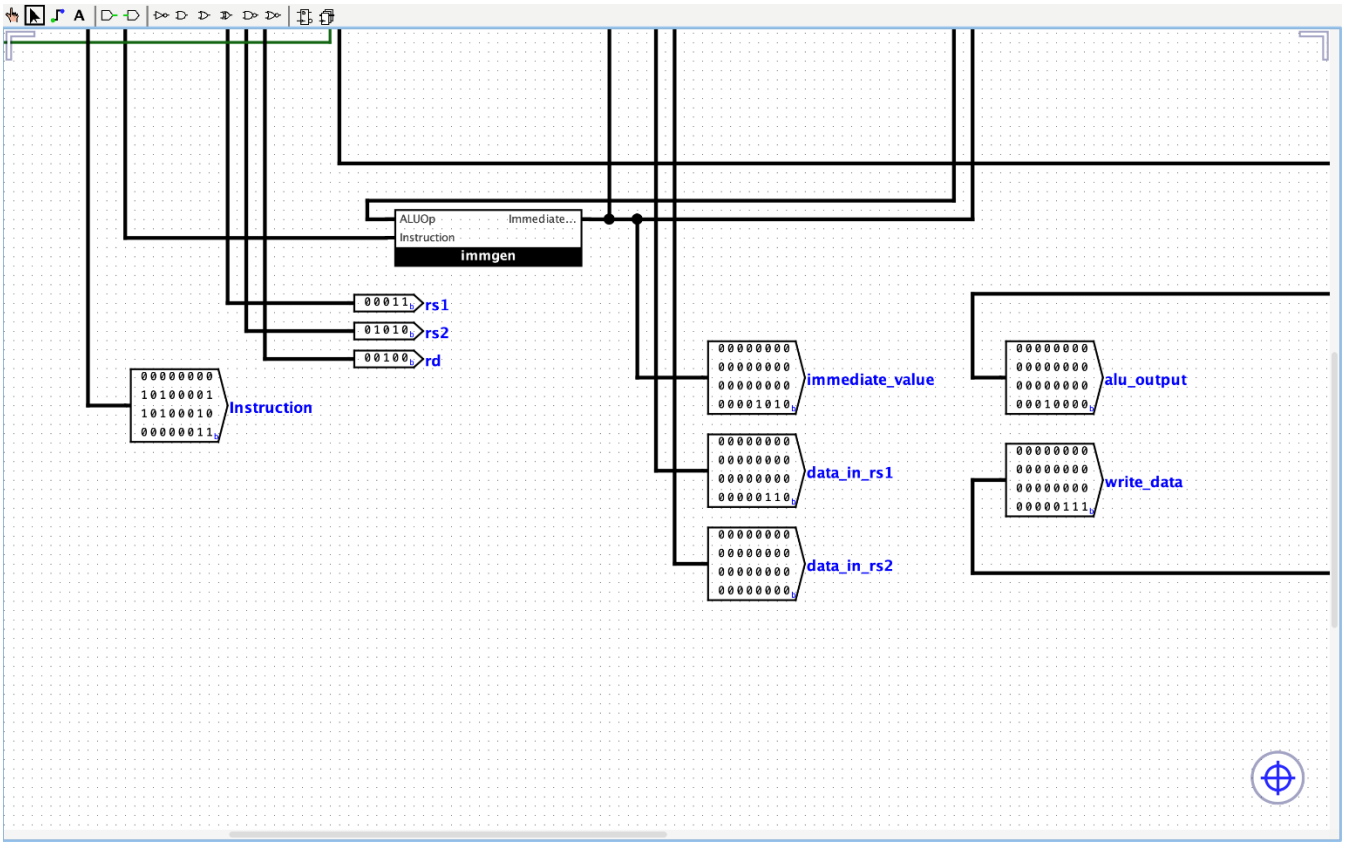
add x2 x1 x1



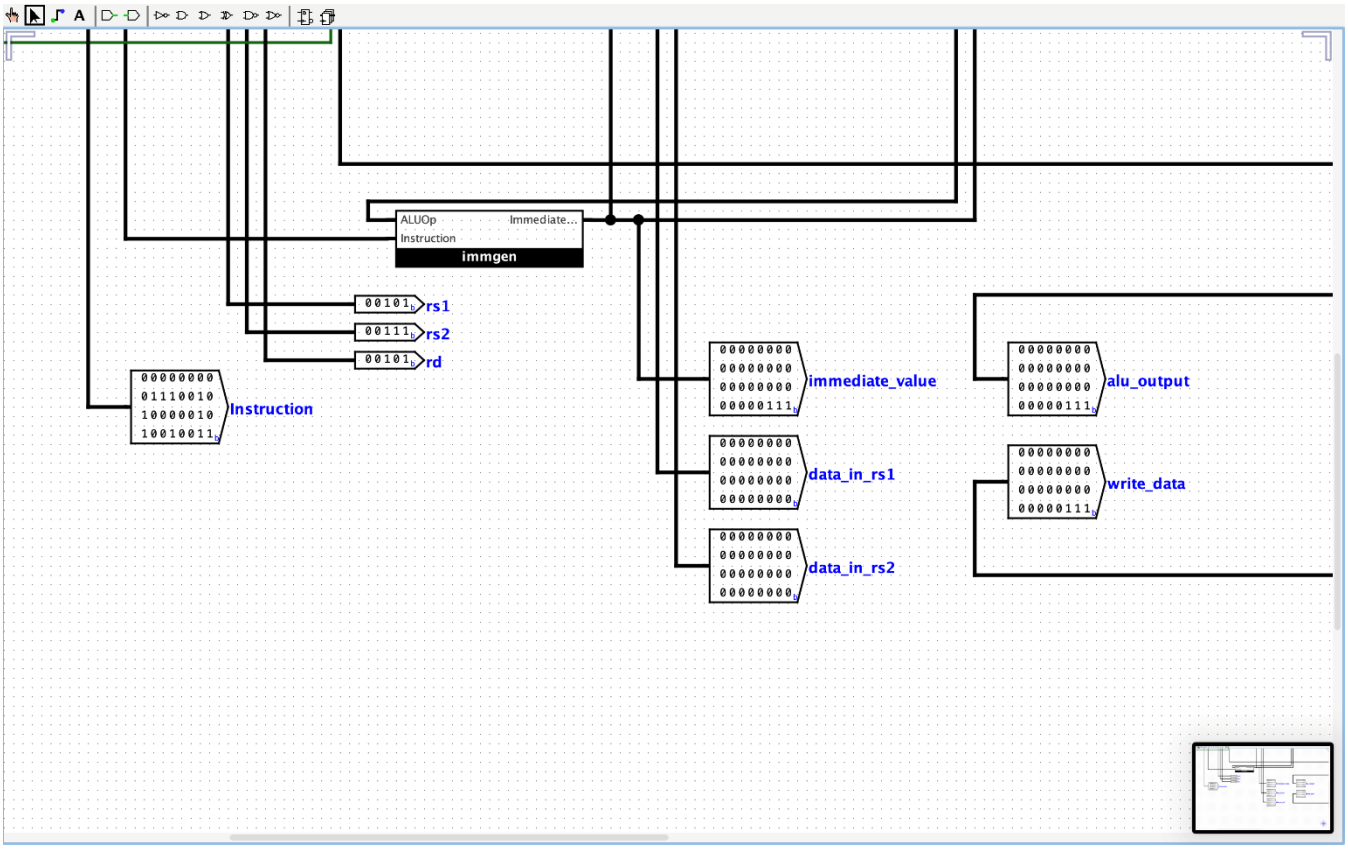
addi x3 x3 6



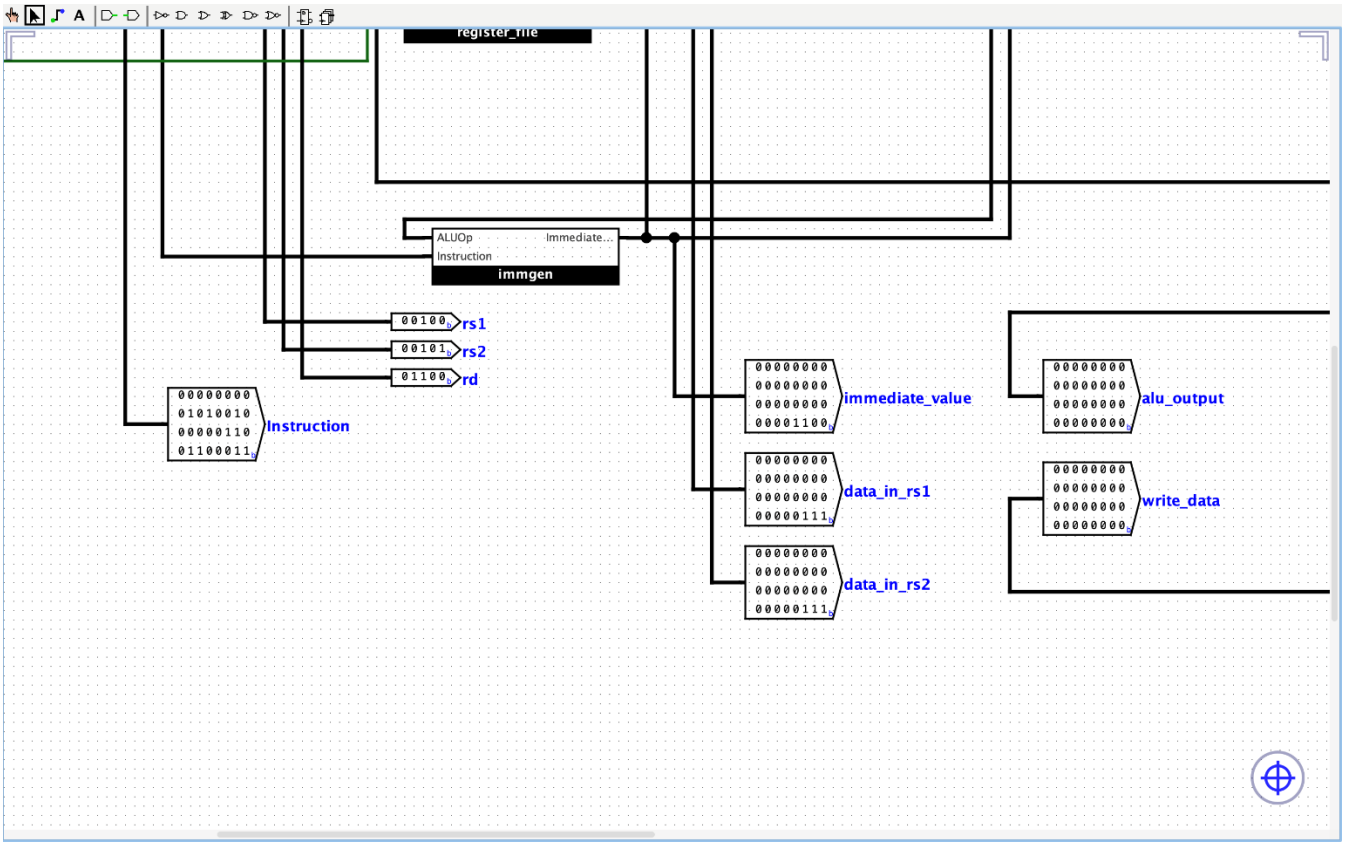
sw x1 10(x3)



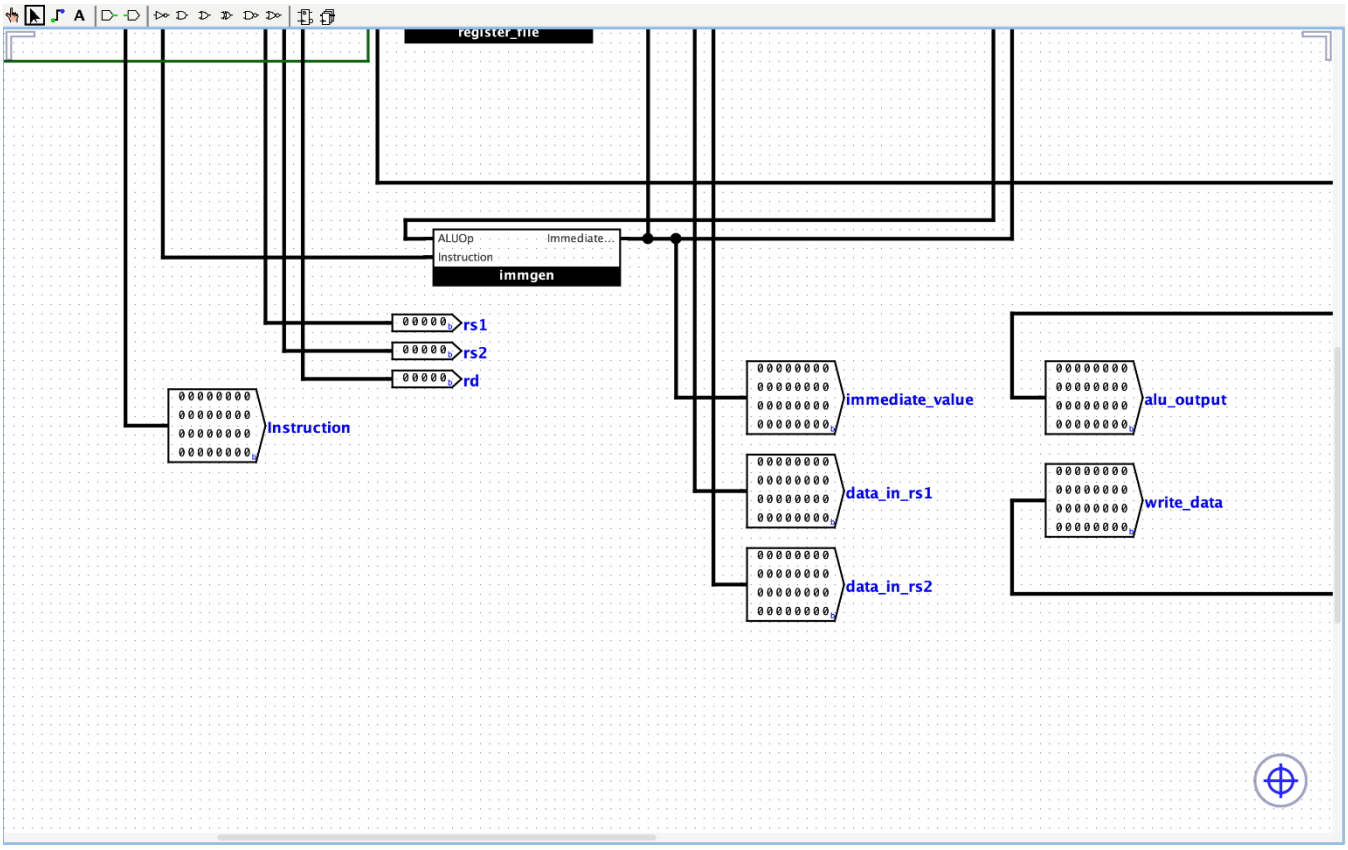
lw x4 10(x3)



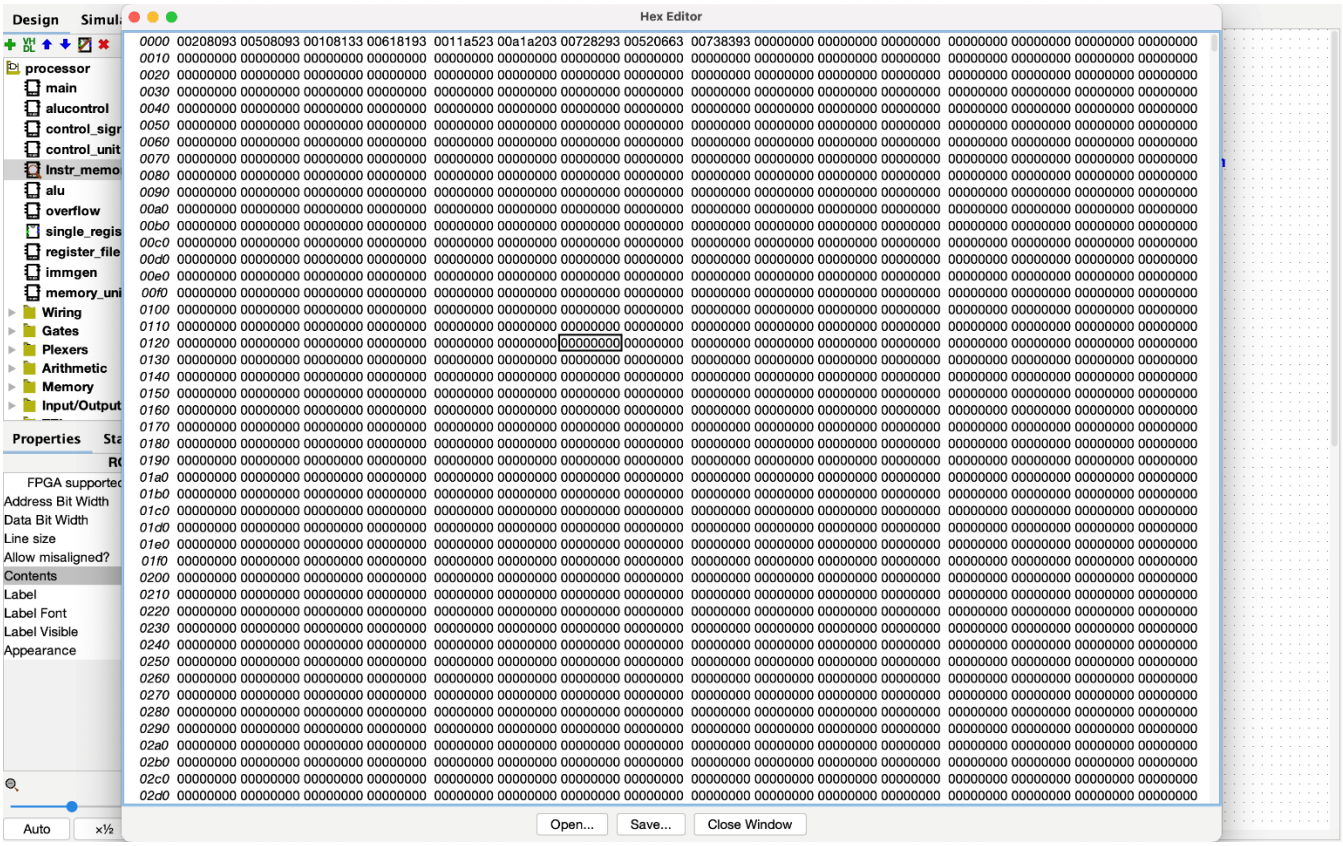
addi x5 x5 7



beq x4 x5 6



End program



Instruction Memory