Project-1 [CMOS Inverter]

A Project Submitted

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(Section-A)

Under the Supervision of

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In Partial Fulfilment of

the requirements for the course of

EE1124 (Analog Electronics)

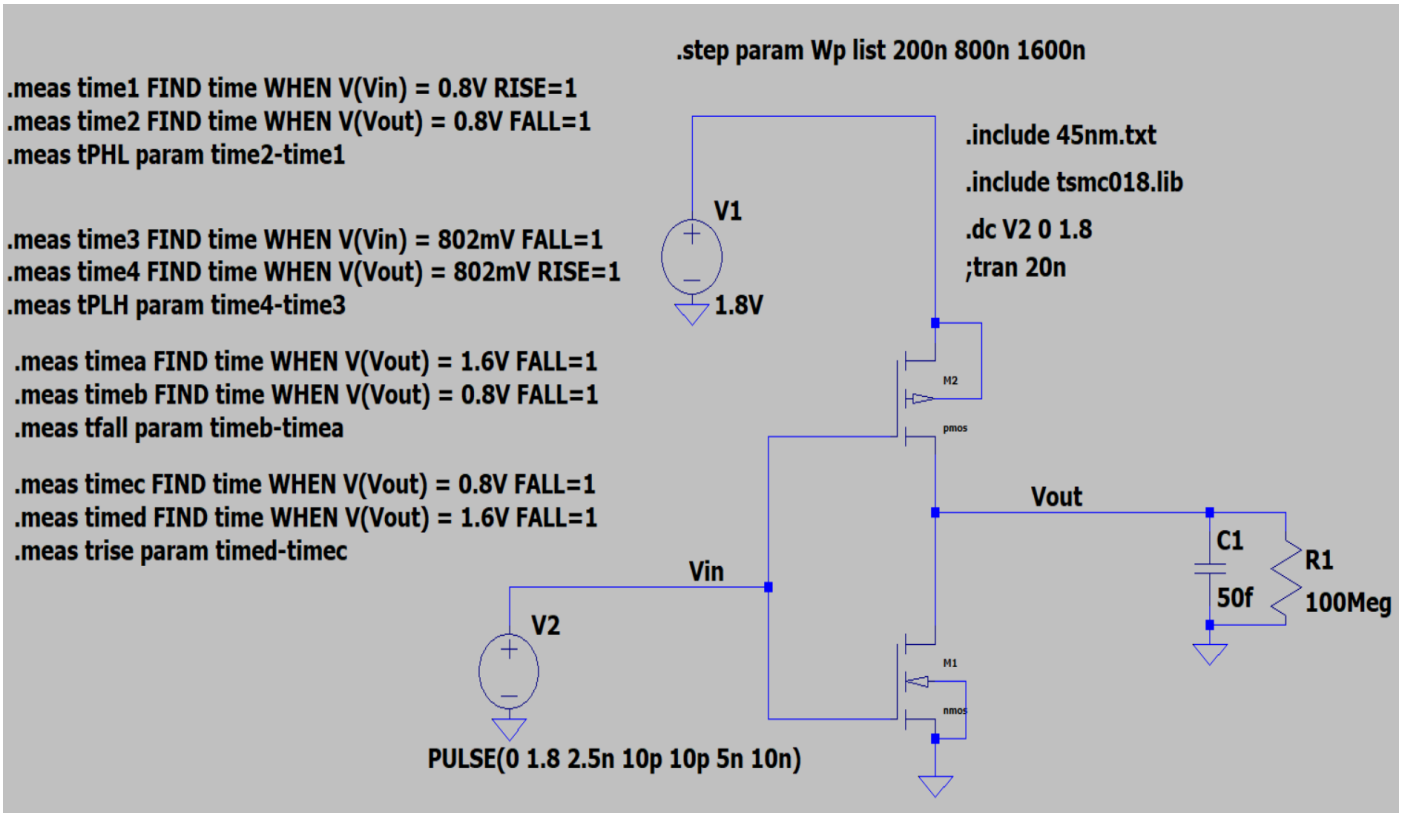
To the

Institute of Engineering And Technology (IET)

J.K Lakshmipat University Jaipur

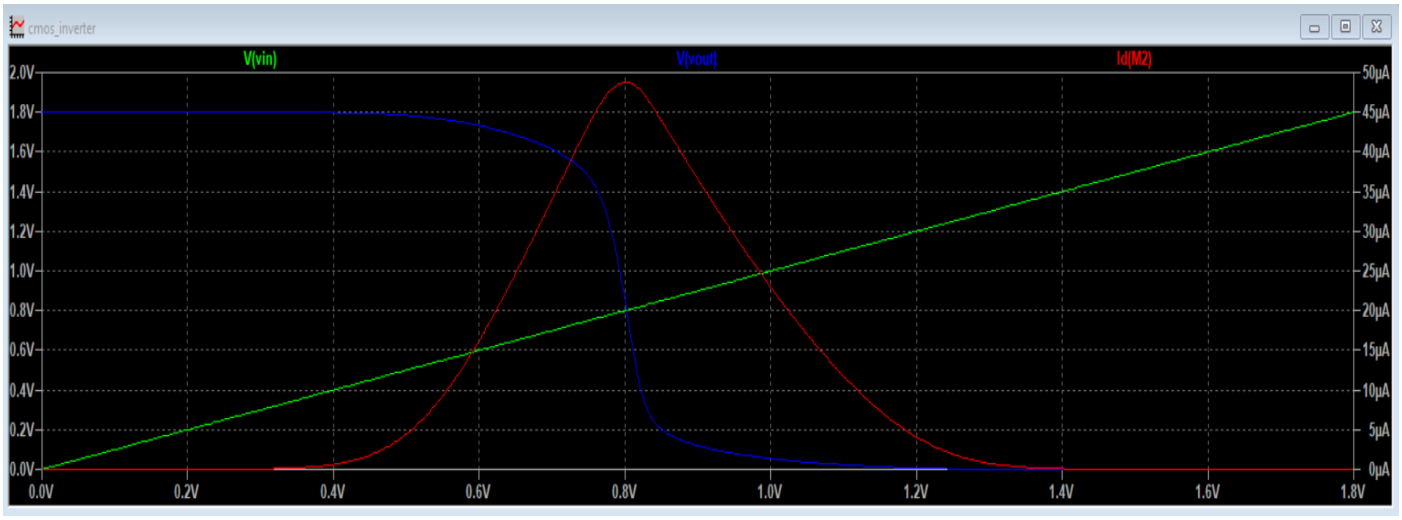
Aim: To design a CMOS Inverter on LTspice and to see various factors like: noise margin, switching threshold, Static and Dynamic Power Loss, Rise and Fall time, Propogation Delay, Working of inverter at different Length and Width etc.

Schematic:

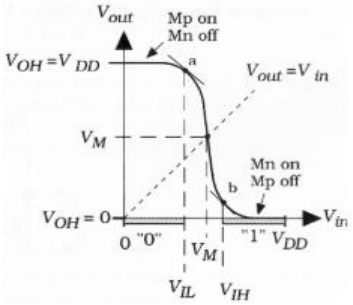


DC Analysis:

Ques1: How will you determine NML and NMH from voltage transfer characteristics (VTC)?



Noise Margin: To determine the Noise margin we need the following parameters:



Vil (Voltage input low), **Vih** (Voltage input high),**Vol** (Voltage output Low), **Voh** (Voltage output high)
Where **Vil** is the maximum input voltage that is still recognized as a **logical LOW** by a digital circuit represented as point **'a'** in the given figure.

Vih is the maximum input voltage that is still recognized as a **logical HIGH** by a digital circuit represented as point **'b'** in the given figure.

Whereas **Voh = Vdd** (or a <= Voh <= Vdd) and **Vol = 0** (or 0 <= Vol <= b)

After calculation of the required parameters **Noise margin High** (Vnmh) is calculated as: **Voh – Vih** and **Noise Margin Low** is calculated as: **Vil – Vol**

In our case:

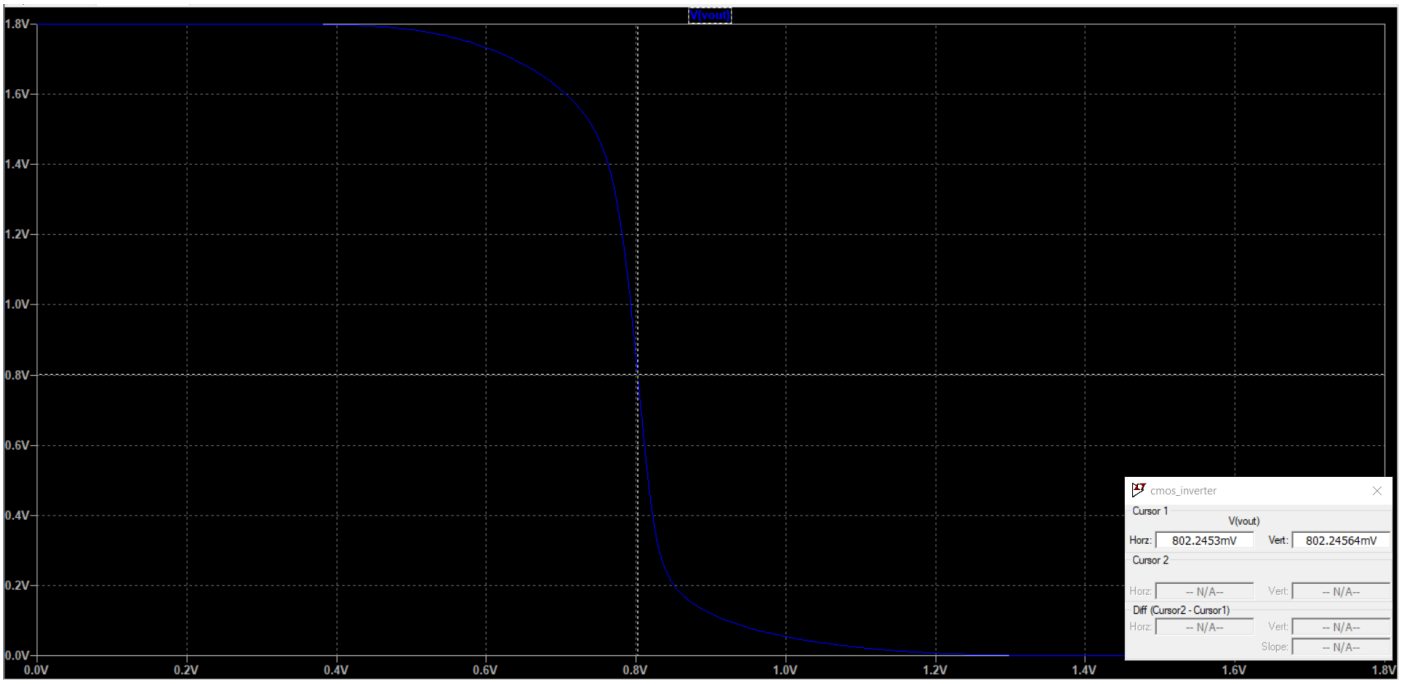
Vil = 0.7V ; **Vih** = 0.870V ; **Vol** = 0V ; **Voh** = 1.8V

Noise Margin High = Vnmh = Voh – Vih = 1.8V – 0.870V = **0.930V**

Noise Margin Low = Vnml = Vil – Vol = 0.7V – 0V = **0.7V**

Switching Threshold: It is that point where the both Nmos and Pmos are in the ON State or we can say the point where the Vin = Vout is known as the Switching Threshold.

Vin = Vout **= 802.2454 mV**



Ques2: Calculate the following:
Rise Time, Fall time, Edge Rate, High-to-Low Propogation delay, Low-to-High propogation delay, Propogation delay.

Soln. Rise Time: Time Required by the Output Voltage (Vout) to rise from its 10% value to the 90% of its Value is known as the Rise Time (tr).

Fall Time: Time Required by the Output Voltage (Vout) to fall from its 90% value to the 10% of its Value is known as the Fall Time (tf).

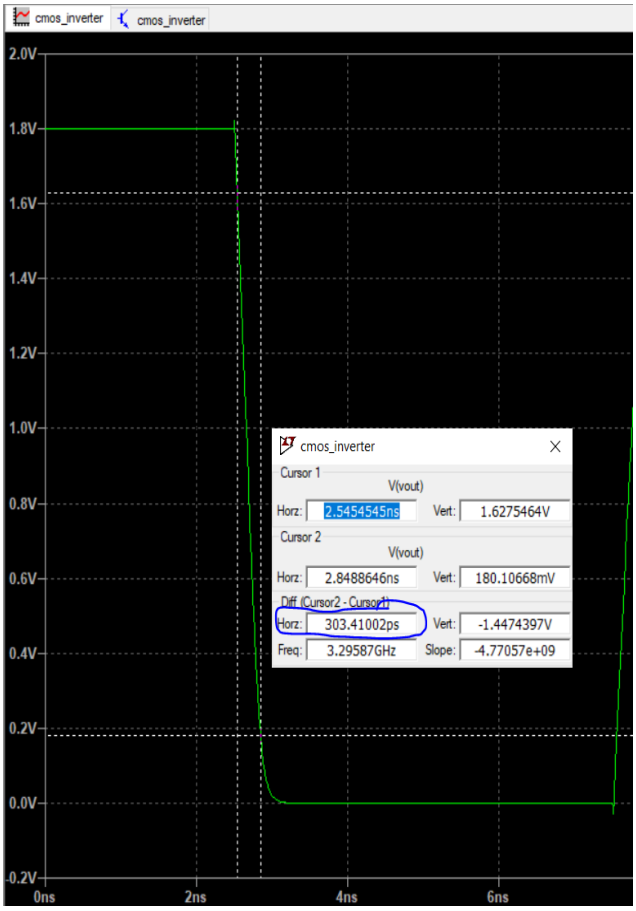
Edge Rate (trf): It is the Average of the Rise time and Fall time.

High-to-Low Propogation delay (tpHL): It is the Delay between the Vin and Vout at the Switching Threshold point when the Vout is Falling.

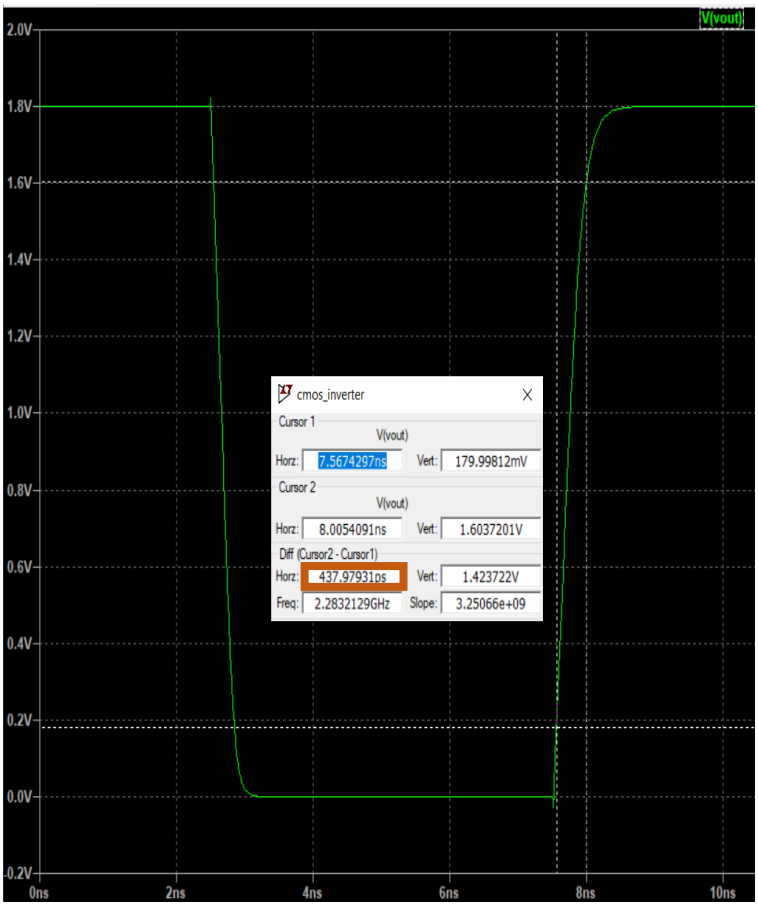
Low-to-High Propogation delay (tpLH): It is the Delay between the Vin and Vout at the Switching Threshold point when the Vout is Rising.

Propogation Delay (tp): It is the **average** of the **High-to-Low** and **Low-to-High** Propogation delay.

Fall Time (303.41ps)



Rise Time (437.97ps)



Verification by running .meas Statement in LT spice:

```
timea: time=2.55045e-09 at 2.55045e-09
timeb: time=2.69947e-09 at 2.69947e-09
tfall: timeb-timea=1.49016e-10
timec: time=2.69947e-09 at 2.69947e-09
timed: time=2.55045e-09 at 2.55045e-09
trise: timed-timec=-1.49016e-10


Date: Wed Apr  9 11:45:00 2025
Total elapsed time: 0.229 seconds.
```

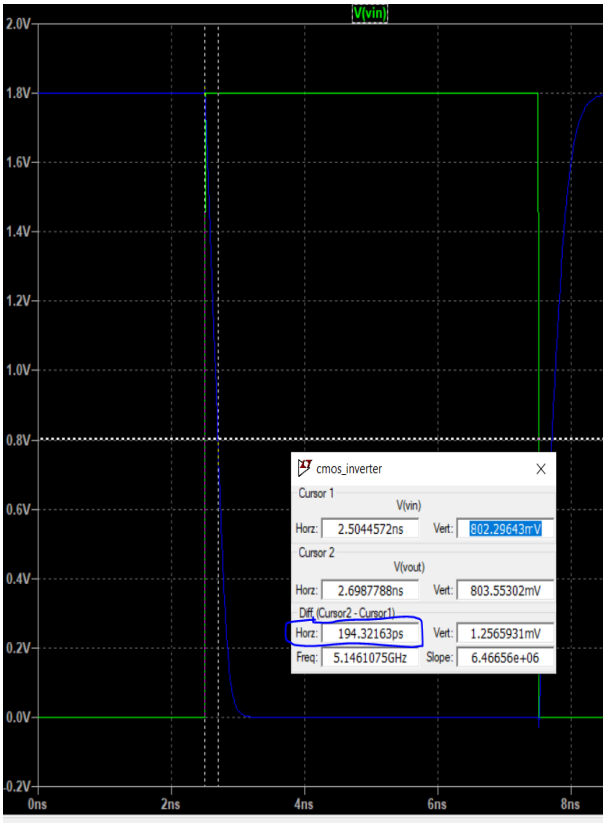
```
.meas timea FIND time WHEN V(Vout) = 1.6V FALL=1
.meas timeb FIND time WHEN V(Vout) = 0.8V FALL=1
.meas tfall param timeb-timea

.meas timec FIND time WHEN V(Vout) = 0.8V FALL=1
.meas timed FIND time WHEN V(Vout) = 1.6V FALL=1
.meas trise param timed-timec
```

Fall Time (tf) = 149.016 ps ; Rise Time (tr) = 149.016ps

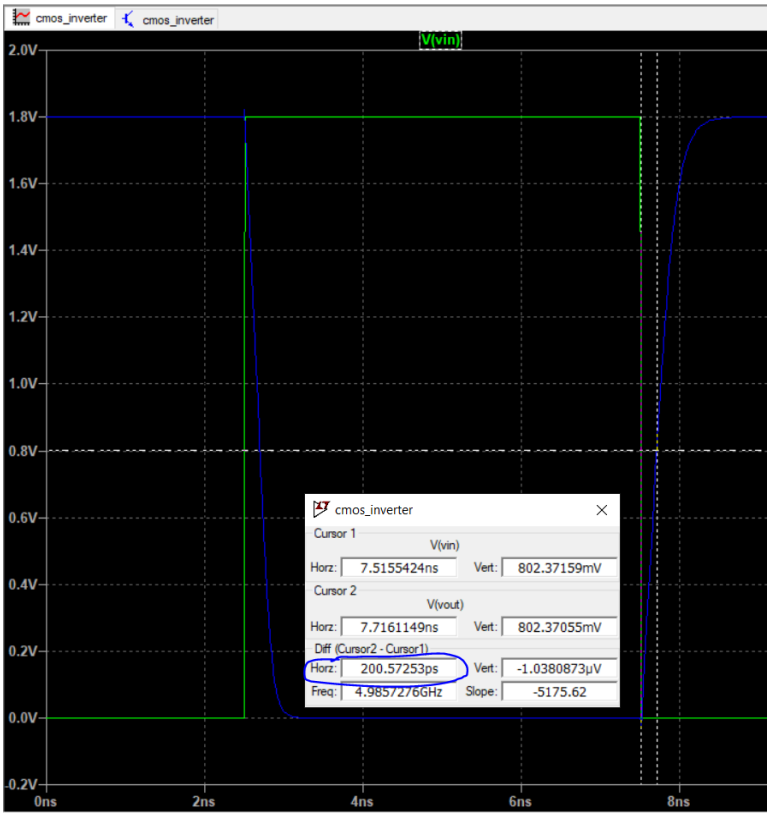
Trf = (tf + tr)/2 = (149.016 + 149.016)/2 = 149.016ps

As, we can see our answer is nearly matches to the calculated value using the .meas statement. However it is difficult to manually set the cursor at the specific point so the slight variation occurs.

Delay High to Low: 194.32 ps (approx.)



Delay Low to High: 200.57 ps (approx.)



tpHL = 194.32 ps ; tpLH = 200.57 ps

Propogation Delay (tp) = (tpHL + tpLH)/2 = (194.32 + 200.57)/2 = **197.445 ps**

Verification by running .meas Statement in LT spice:

```
.meas time1 FIND time WHEN V(Vin) = 0.8V RISE=1
.meas time2 FIND time WHEN V(Vout) = 0.8V FALL=1
.meas tPHL param time2-time1


.meas time3 FIND time WHEN V(Vin) = 802mV FALL=1
.meas time4 FIND time WHEN V(Vout) = 802mV RISE=1
.meas tPLH param time4-time3
```

SPICE Error Log: C:\Users\HP\AppData\Local\LTspice\cmos_inverter.log

```
Circuit: * C:\Users\HP\AppData\Local\LTspice\cmos_inverter.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

time1: time=2.50444e-09 at 2.50444e-09
time2: time=2.69947e-09 at 2.69947e-09
tphl: time2-time1=1.95021e-10
time3: time=7.51554e-09 at 7.51554e-09
time4: time=7.71602e-09 at 7.71602e-09
tplh: time4-time3=2.00477e-10
```

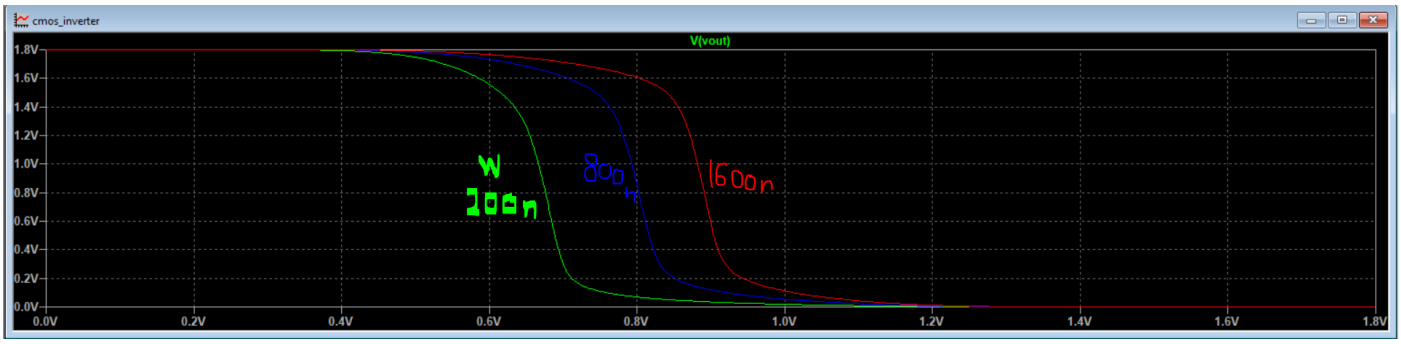
As, we can see our answer is nearly matches to the calculated value using the .meas statement.

Ques3: If you increase the size of the pMOS transistor with respect to the nMOS transistor, what change do you expect in the VTC and why?

Soln. If we increase the Size of the Pmos transistor (means we can change the area of the pmos by changing the Width of the Pmos only because changing the length make different length from the nmos which is not practically possible because pmos is build on the nmos by making a well so there length must be same) with respect to the nmos the **VTC curve** will shifts towards the **right** which means that it actually **increases** the **Switching threshold**.

This happens Because:

1) Due to **Mobility Difference** of the **Electrons** and the **Holes** where holes are generally **2.5 times slower** than the electrons. That's why the area of the Pmos is increased by a factor of **2 to 3** because **increasing the area** will **reduce the resistance** and **increase the Current**.
2) Also, by increasing the area of Pmos will favours keeping the **output high for longer time** which allows us to study the factors like: Noise margin High/Low. If **it area is low** or VTC shifts towards the left it make the **Device more sensitive to the noise** when dealing with high input due to **not** storing the **Output high** for longer time.



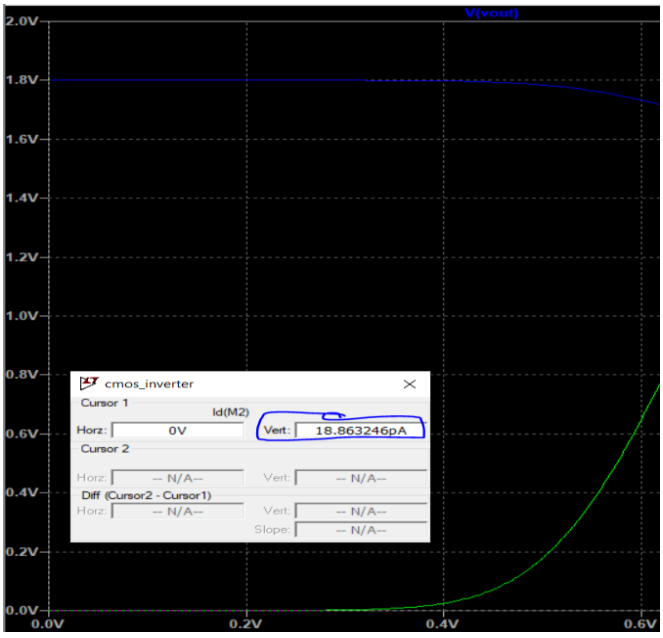
Here, we can see by increasing the area the VTC curve shifts to the Right side and if area decreases then it Shifts to the Left side if we take the reference curve of width=800n.

Ques4: Calculate the Static and Dynamic power loss of the CMOS Inverter.

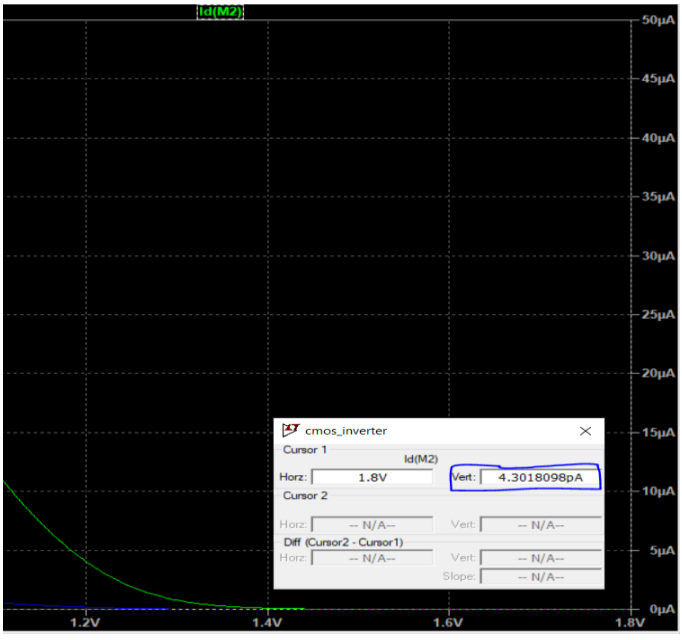
Soln. Static Power Loss: Power loss when the MOSFET (Pmos or Nmos) is in the off state and there is some **leakage current** is present in it is known as **Static Power Loss**.

<u>Leakage Current Due to:</u>

Due to N-MOS:



Due to P-MOS:



In the above Graphs, Leakage current due to **NMOS** is **18.86pA** because it is obtained when the input Voltage is 0 the **NMOS is in OFF** state and PMOS is in ON State but when the **Vin is High** the Leakage Current in **PMOS is 4.30pA** because at that time NMOS is ON and **PMOS is OFF**.

Static Power Loss:

In NMOS: Power Loss = 18.86pA * 1.8V = **33.948pWatt**

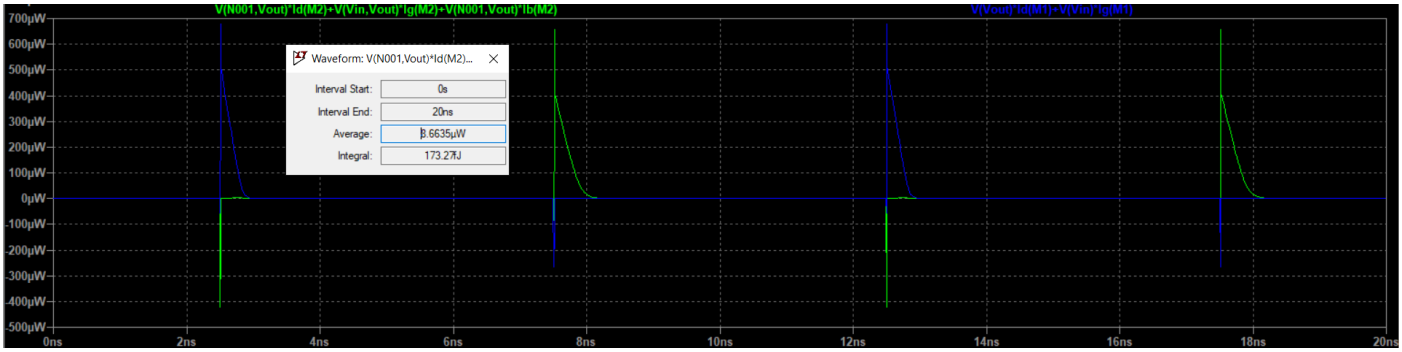
In PMOS: Power Loss = 4.30pA * 1.8V = **7.74pWatt**

Dynamic Power Loss: Power loss occurs when the MOSFET switches between the ON and OFF state mainly when the both PMOS and NMOS are ON in the partial state. It is also caused by the charging/Discharging of the parasitic capacitances (Cgd, Cgs, Cds).

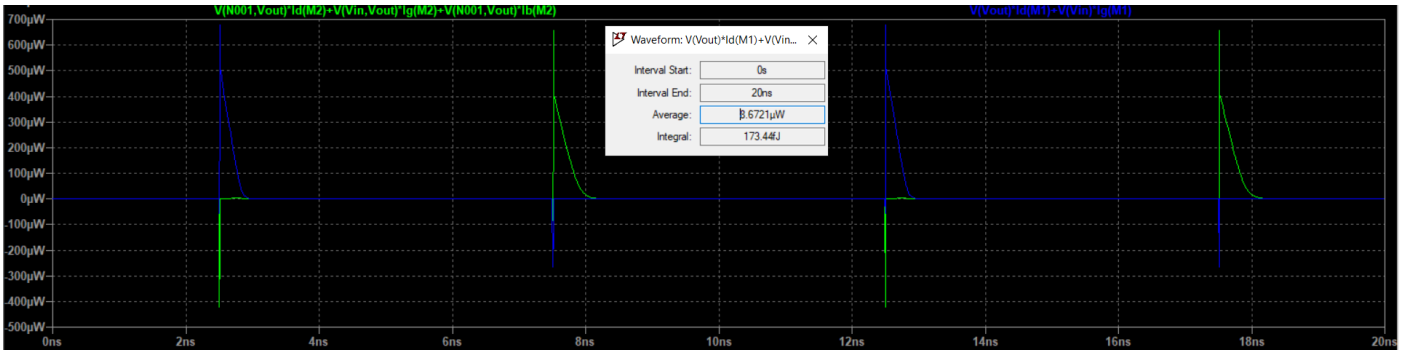
Instantaneous Power Simulation:

Dynamic Power loss in PMOS = 8.6653 uW (where green line shows the instantaneous power in PMOS)

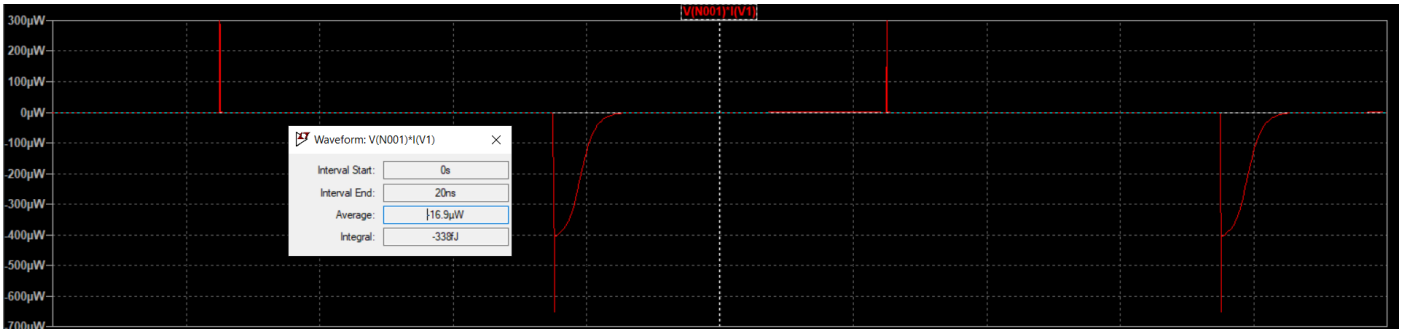
Calculated by **alt+click** on the **PMOS** (gives **Instantaneous Power**) then **ctrl+click** on the **trace name** gives the **average power dissipated**.



Dynamic Power Loss in Nmos: 8.6721 uW



Power given by Source: -16.9 uW (-ve because source is supplying power to the PMOS and NMOS not consuming)



When the **input** goes from **high to low** the **output** goes from **0 to 1** where approximately **16 micro watt** of **power is taken** from the **source** out of which **8 microwatt** gets **dissipated as heat** in the **PMOS** and remaining **8microwatts** will used in **charging the capacitor**.

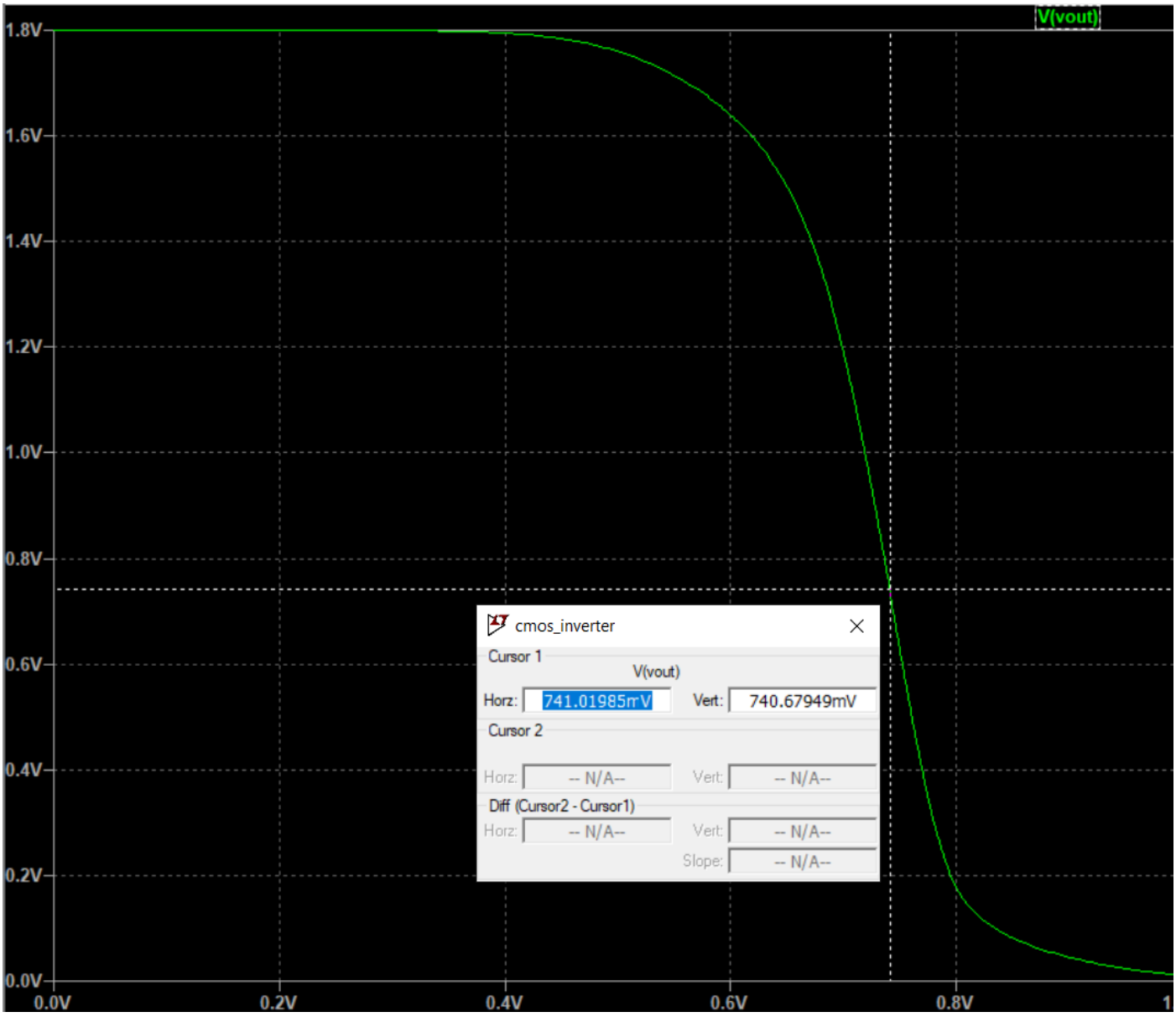
When the **input** goes from **low to high** the **output** goes from **1 to 0** where the **stored power** by the capacitor is taken **by the NMOS** and is **dissipated as heat** in the NMOS.

Ques5: Compare the switching characteristics of 180nm, 90nm and 45nm CMOS inverter.

Soln. For 180nm technology node we have done above.

When Technology Node is 90nm:

Switching threshold: 741mV



Noise Margin:

Vil = 0.611V Vih = 0.811V Voh = 1.8V Vol = 0V

NML = Vil – Vol = 0.611V

NMH = Voh – Vih = 0.989V

Rise Time, Fall Time and Propogation Delay:

```
.meas time1 FIND time WHEN V(Vin) = 0.8V RISE=1
.meas time2 FIND time WHEN V(Vout) = 0.8V FALL=1
.meas tPHL param time2-time1


.meas time3 FIND time WHEN V(Vin) = 802mV FALL=1
.meas time4 FIND time WHEN V(Vout) = 802mV RISE=
.meas tPLH param time4-time3

 .meas timea FIND time WHEN V(Vout) = 1.6V FALL=1
 .meas timeb FIND time WHEN V(Vout) = 0.8V FALL=1
 .meas tfall param timeb-timea

 .meas timec FIND time WHEN V(Vout) = 0.8V FALL=1
 .meas timed FIND time WHEN V(Vout) = 1.6V FALL=1
 .meas trise param timed-timec
```

```
SPICE Error Log: C:\Users\HP\AppData\Local\LTspice\cmos_inverter.log
Circuit: * C:\Users\HP\AppData\Local\LTspice\cmos_inverter.asc

Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Ignoring BSIM parameter XL
Ignoring BSIM parameter XW
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Warning: Pd = 0 is less than W.
Warning: Ps = 0 is less than W.
Direct Newton iteration for .op point succeeded.

time1: time=2.50444e-09 at 2.50444e-09
time2: time=2.61164e-09 at 2.61164e-09
tphl: time2-time1=1.072e-10
time3: time=7.51554e-09 at 7.51554e-09
time4: time=7.62596e-09 at 7.62596e-09
tplh: time4-time3=1.10419e-10
timea: time=2.52854e-09 at 2.52854e-09
timeb: time=2.61164e-09 at 2.61164e-09
tfall: timeb-timea=8.31085e-11
timec: time=2.61164e-09 at 2.61164e-09
timed: time=2.52854e-09 at 2.52854e-09
trise: timed-timec=-8.31085e-11


Date: Thu Apr 10 12:08:25 2025
Total elapsed time: 0.163 seconds.

tnom = 27
```

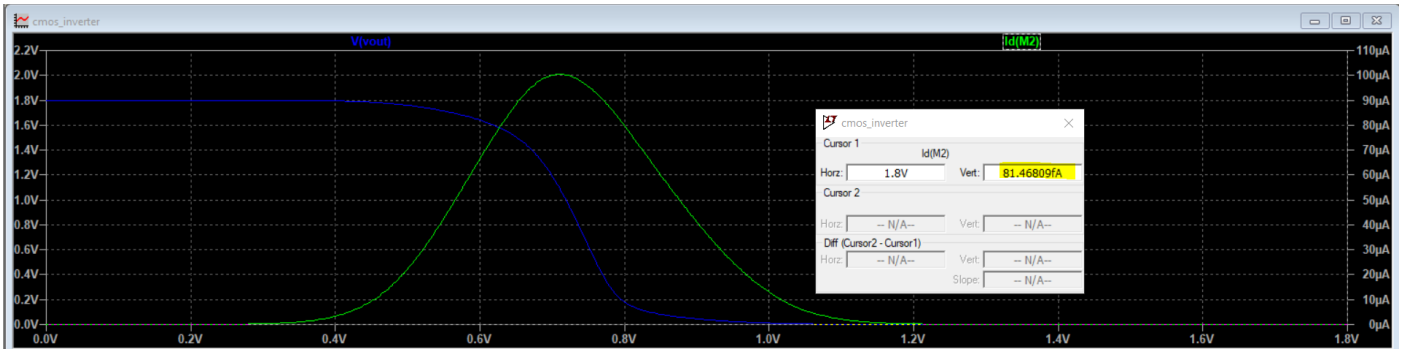
Trise = 83.10 ps and tfall = 83.10 ps **Edge rate = 83.10ps**

Tphl = 107.2ps and tplh = 110.4ps

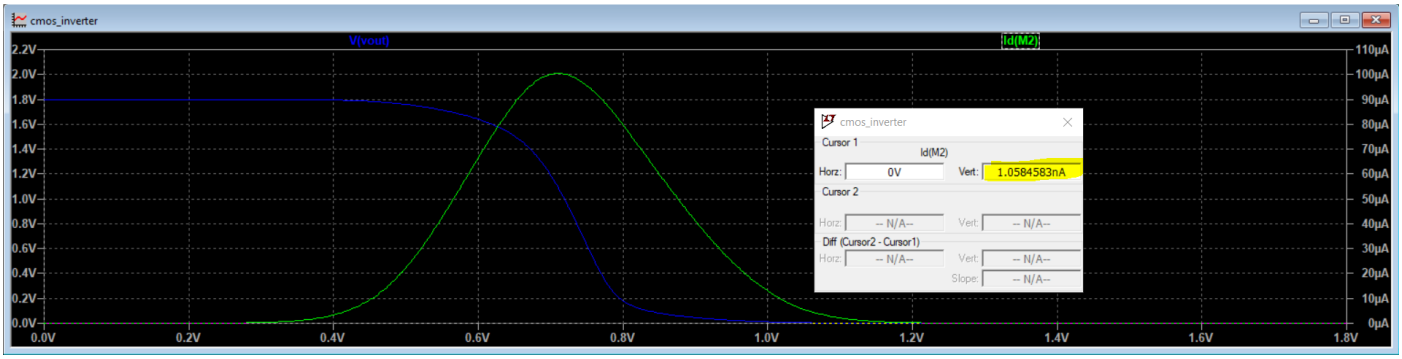
Propogation delay = (107.2 + 110.4)/2 = **108.8ps**

Static Power Loss:

Due to PMOS: 0.081pA * 1.8V = 0.1458pW

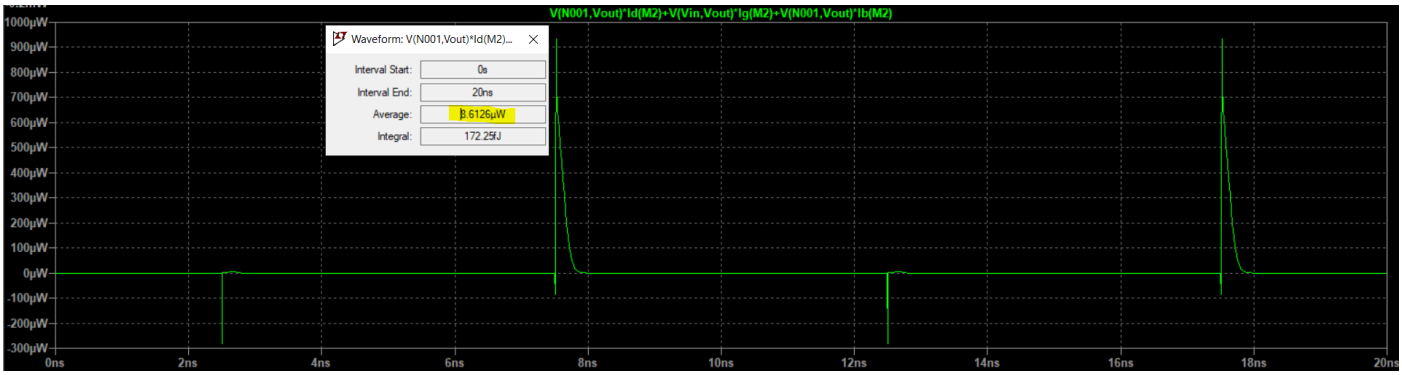


Due to NMOS: 1058.45pA * 1.8 = 1905.21pW

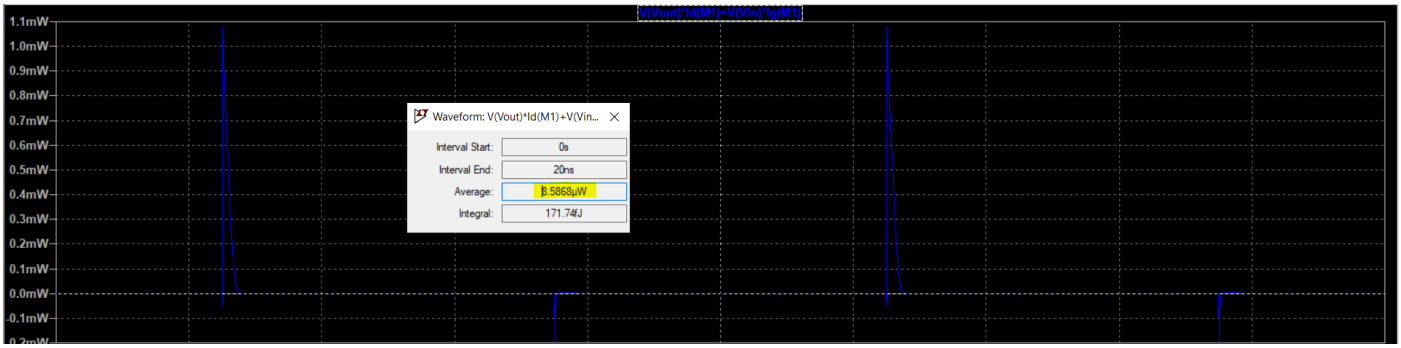


Dynamic Power Loss:

Due to PMOS: 8.612 microwatt

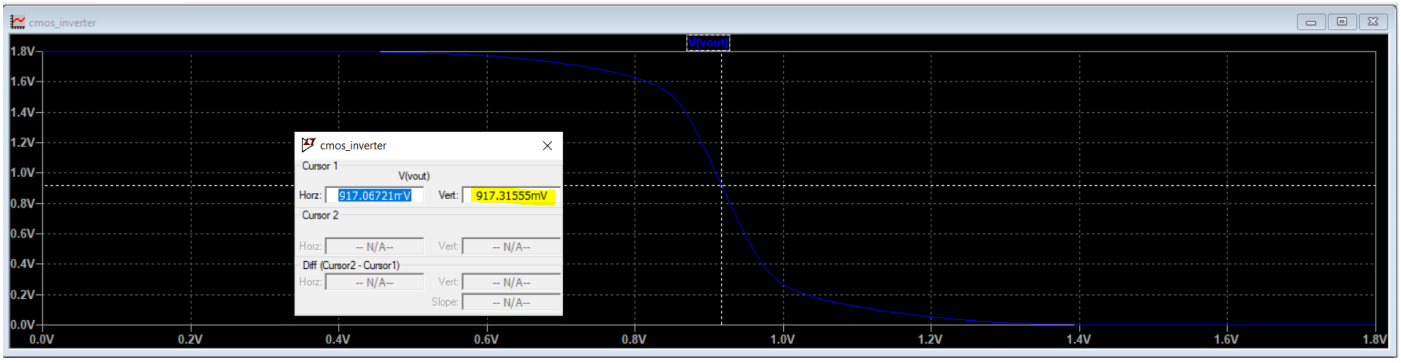


Due to NMOS: 8.58 microwatt



When Technology Node is 45nm:

Switching Threshold: 917.31mV



Noise Margin:

Vil = 0.805V Vih = 1.016V Voh = 1.8V Vol = 0V

NML = Vil – Vol = 0.805V

NMH = Voh – Vih = 0.784V

Rise Time, Fall Time and Propogation Delay:

```
.meas time1 FIND time WHEN V(Vin) = 0.8V RISE=1
.meas time2 FIND time WHEN V(Vout) = 0.8V FALL=1
.meas tPHL param time2-time1

.meas time3 FIND time WHEN V(Vin) = 802mV FALL=1
.meas time4 FIND time WHEN V(Vout) = 802mV RISE=1
.meas tPLH param time4-time3

.meas timea FIND time WHEN V(Vout) = 1.6V FALL=1
.meas timeb FIND time WHEN V(Vout) = 0.8V FALL=1
.meas tfall param timeb-timea

.meas timec FIND time WHEN V(Vout) = 0.8V FALL=1
.meas timed FIND time WHEN V(Vout) = 1.6V FALL=1
.meas trise param timed-timec
```

```
Circuit: * C:\Users\HP\AppData\Local\LTspice\cmos_inverter.asc

Direct Newton iteration for .op point succeeded.

time1: time=2.50444e-09 at 2.50444e-09
time2: time=2.60702e-09 at 2.60702e-09
tphl: time2-time1=1.02573e-10
time3: time=7.51554e-09 at 7.51554e-09
time4: time=7.57911e-09 at 7.57911e-09
tplh: time4-time3=6.35617e-11
timea: time=2.52762e-09 at 2.52762e-09
timeb: time=2.60702e-09 at 2.60702e-09
tfall: timeb-timea=7.9393e-11
timec: time=2.60702e-09 at 2.60702e-09
timed: time=2.52762e-09 at 2.52762e-09
trise: timed-timec=-7.9393e-11


Date: Thu Apr 10 12:42:37 2025
Total elapsed time: 0.188 seconds.

tnom = 27
temp = 27
method = modified trap
totiter = 2238
traniter = 2232
tranpoints = 1092
accept = 1080
rejected = 12
matrix size = 13
```

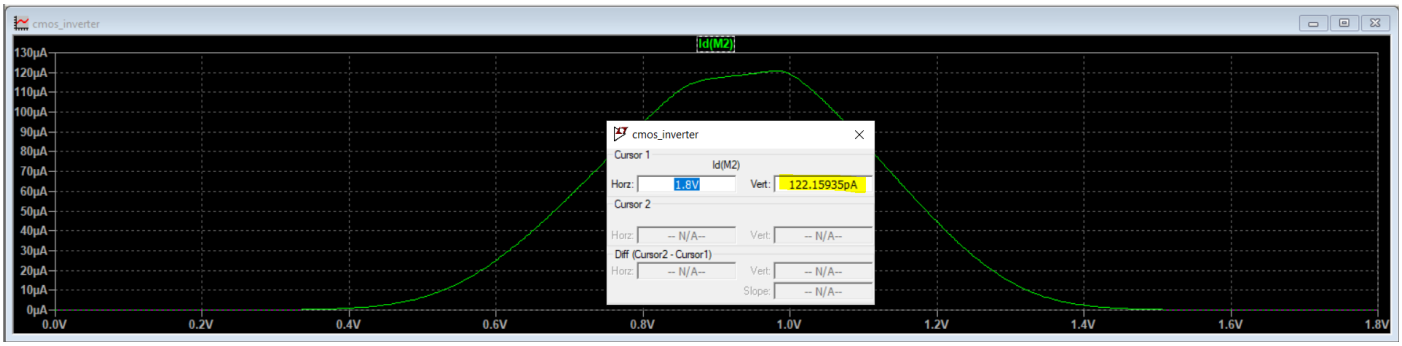
Trise = 79.39 ps and tfall = 79.39 ps **Edge rate = 79.39ps**

Tphl = 102.57ps and tplh = 63.56ps

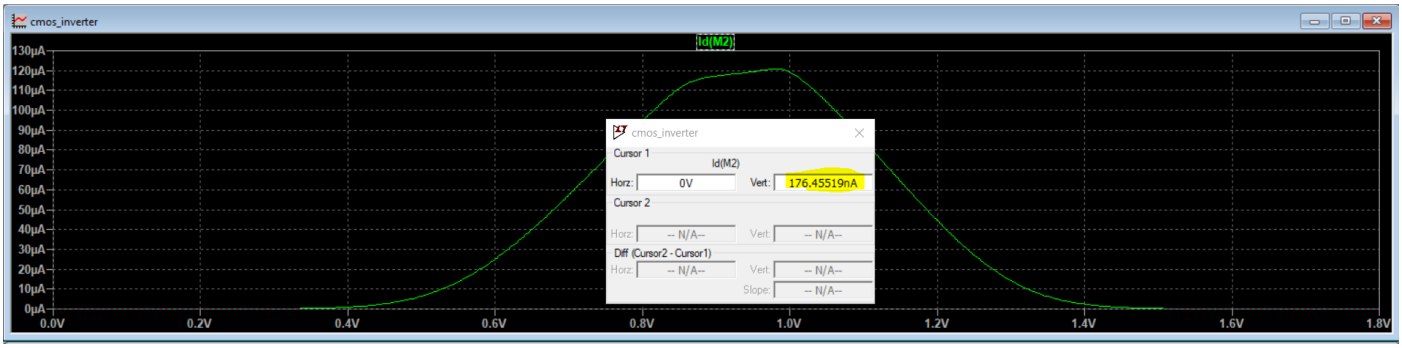
Propogation delay = (102.57 + 63.56)/2 = **83.065ps**

Static Power Loss:

Due to PMOS: 122.15pA * 1.8V = 219.87pW

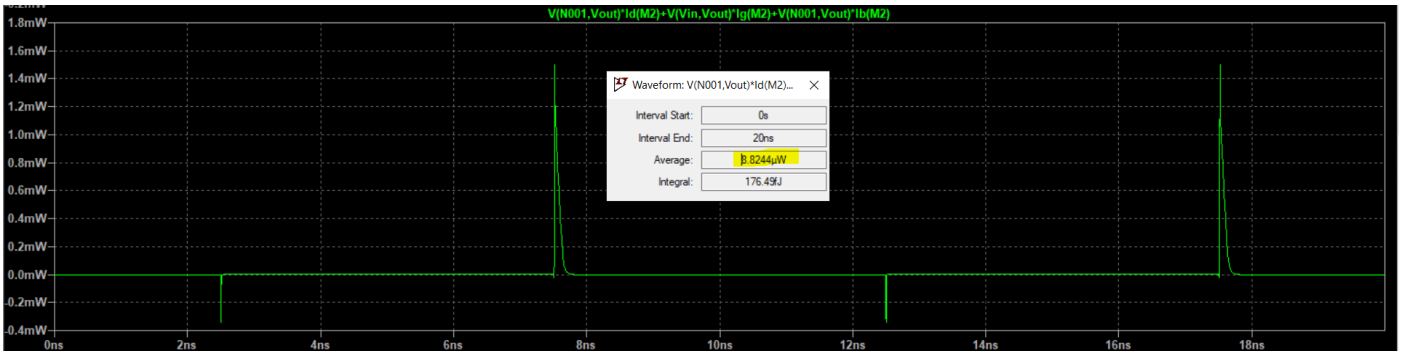


Due to NMOS: 176.45nA * 1.8V = 317.61nW

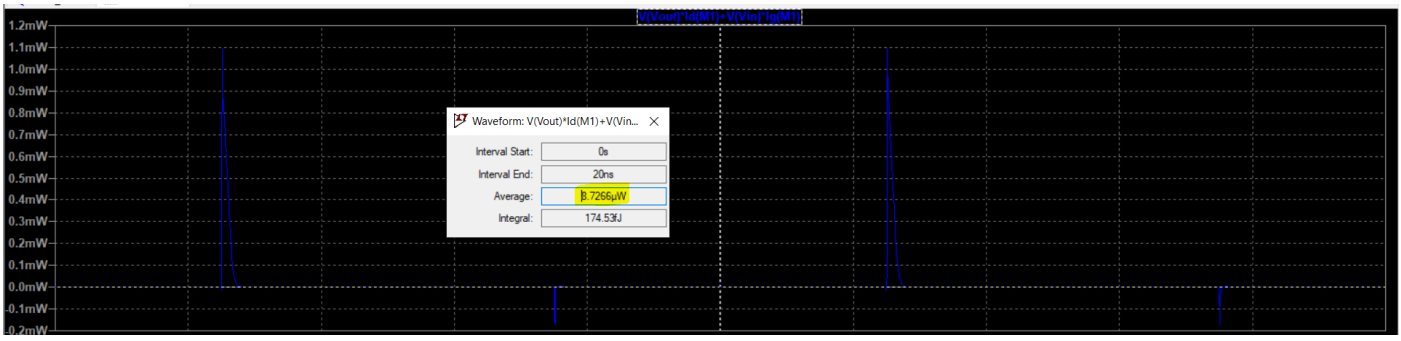


Dynamic Power Loss:

Due to PMOS: 8.824 microwatt



Due to NMOS: 8.726microwatt



Comparison:

Switching Threshold: As channel length decreases from 180nm to 90nm, the switching threshold Vm shifts left due to moderate NMOS strengthening. However, at 45nm, strong short-channel effects drastically increase NMOS drive, shifting Vm right, closer to VDD. This non-linear trend is due to increasing dominance of short-channel effects at smaller nodes.

Noise Margin: As we reduce the channel length from 180nm to 45nm, the noise margins change in a non-uniform way. At 180nm, the inverter has strong and balanced noise margins. But at 90nm and 45nm, due to effects like leakage and lower threshold voltage, the input voltage levels shift, which causes the high and low noise margins to change. Overall, as the size gets smaller, the circuit becomes more sensitive to noise, especially in detecting logic '1' correctly.

Rise time, Fall time an Propogation Delay: As the channel length increases, the MOSFET becomes weaker, which slows down how quickly the output can switch. This results in **slower edge transitions** and **higher propagation delay**, making the circuit respond more slowly to input changes.

Static Power Loss: As the channel length decreases from 180nm to 45nm, static power loss increases significantly—especially in NMOS transistors. At smaller nodes, **leakage currents rise sharply** due to short-channel effects and reduced threshold voltage. This results in much higher static power loss at 45nm, with NMOS leakage dominating the total power dissipation.

Dynamic Power Loss: As the channel length decreases from 180nm to 45nm, the dynamic power loss in both NMOS and PMOS shows a slight increase. This happens because shorter channel lengths lead to **higher switching speeds** and **increased capacitance charging frequency**, causing **more dynamic power consumption**. At 45nm, both NMOS and PMOS show the highest power loss due to faster transitions and higher activity.