Project-3 [Differential Ampilifier Design]

A Project Submitted

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(Section-A)

Under the Supervision of

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In Partial Fulfilment of

the requirements for the course of

EE1124 (Analog Electronics)

To the

Institute of Engineering And Technology (IET)

J.K Lakshmipat University Jaipur

Aim: To design the differential amplifier according to the given parameters of the Mosfet and verify the gain is matching with the given gain.

Given Parameters:

How to meet the design targets?

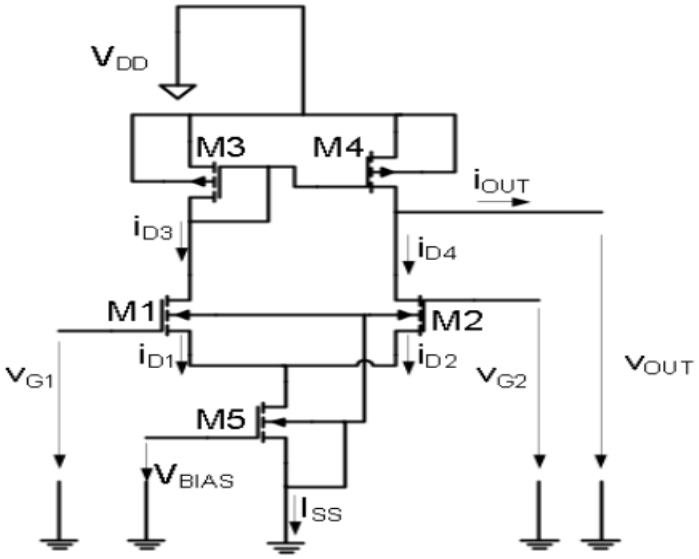
Assume we have the following specification and we use the 0.8µm sample technology

$V_{DD} = -V_{SS} = 2{,}5V$
$SR \geq 10V/\mu s$
$f_{-3dB} \geq 100kHz (C_L = 5pF)$
$-1{,}5V \leq ICMR \leq 2V$
$A_{diff} = 100$
$P_{diss} \leq 1mW$

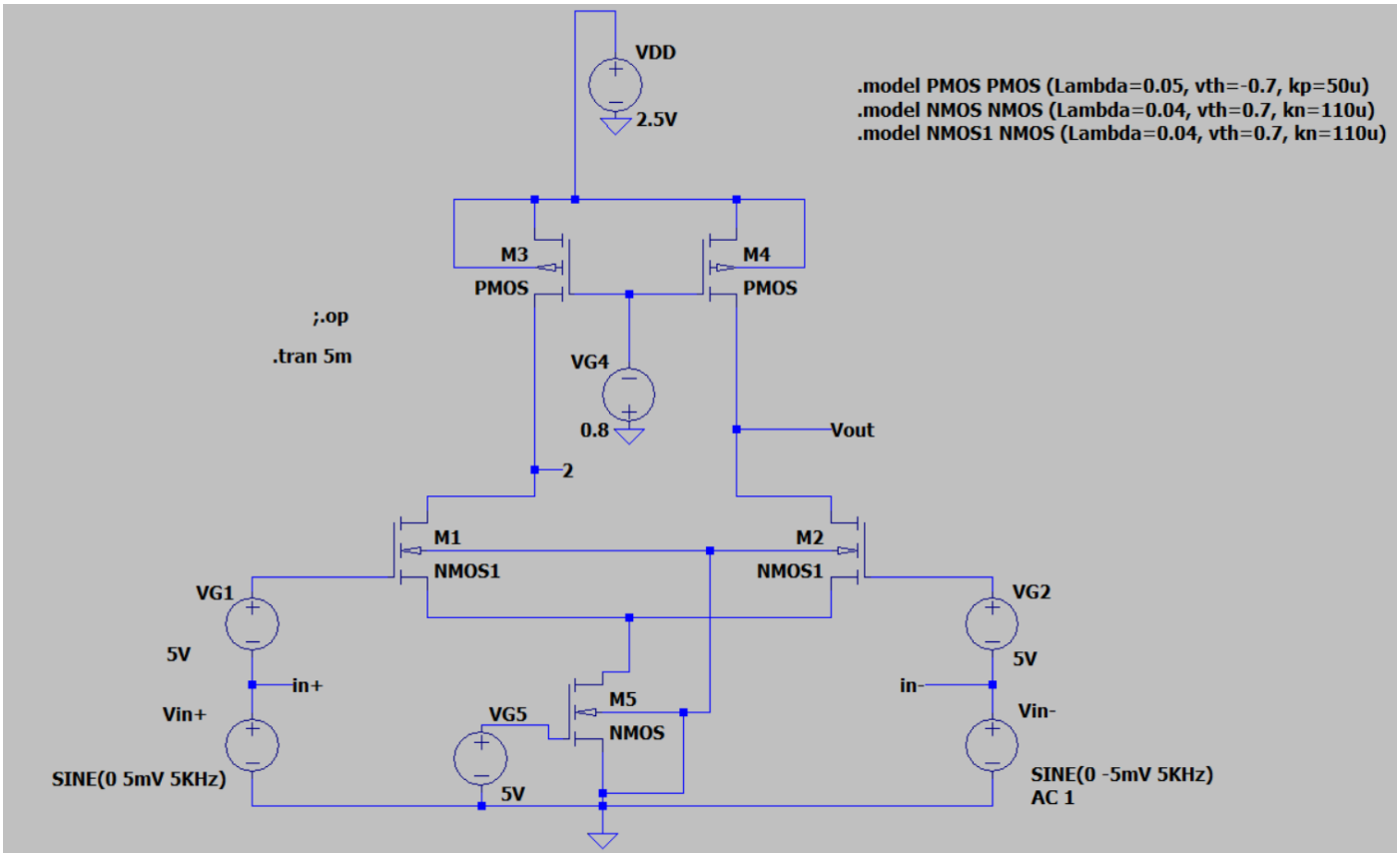
0.8µm CMOS Sample Technology

Parameter	Parameterwerte NMOS	PMOS	Einheit
V_{th0}	$0{,}7 \pm 0{,}15$	$-0{,}7 \pm 0{,}15$	V
K'	$110 \pm 10\%$	$50 \pm 10\%$	$\mu A/V^2$
γ	0,4	0,57	$V^{1/2}$
λ	$0{,}04 \mid_{L=1\mu m}$ $0{,}01 \mid_{L=2\mu m}$	$0{,}05 \mid_{L=1\mu m}$ $0{,}01 \mid_{L=2\mu m}$	V^{-1}
$2\lvert\phi_F\rvert$	0,7	0,8	V

Circuit:



Schematic:



Theortical Designing:

0.8μm

Param	NMOS	PMOS
V_{tho}	0.7 ± 0.15	−0.7 ± 0.15
K'	110 ± 10%	50 ± 10%
γ	0.4	0.57
λ	0.04 | L=1μm	0.05 | L=1μm
	0.01 | L=2μm	0.01 | L=2μm
$2\lvert\phi_F\rvert$	0.7	0.8

$V_{DD} = -V_{SS} = 2.5V$

$SR \geq 10\ V/\mu s$

$f_{-3db} \geq 100kHz\ (C_L = 5pF)$

$-1.5V \leq ICMR \leq 2V$

$A_{diff} = 100$

$P_{diss} \leq 1mW$

$\rightarrow SR \leq \frac{I_5}{C_L} \Rightarrow I_5 \geq \frac{10V}{\mu s} \times 5pF = 10\times10^6 \times 5\times10^{-12} \geq 50\mu A$

$\rightarrow P_{diss} \geq I_D \times V_{DD} \Rightarrow I_D \leq \frac{1\times10^{-3}}{2.5} \times 1 = \frac{1000\times10^{-6}}{2.5} \leq 400\mu A$

Overall circuit current $I_D \leq 400\mu A$

$Sq\ I_5 = \frac{I_D}{2} \Rightarrow I_5 \leq 200\mu A$

$I_{D_1} + I_{D_2} = I_5$ so, $I_{D_1} = I_{D_2} = \leq 100\ \mu A$

$\rightarrow R_{out} \leq \frac{1}{2\pi f_{3db} C_L}$ to get $f_{3db} \geq 100kHz$

$\leq \frac{1\times10^{+12}}{2\pi\times100\times10^3\times5} = \frac{10^7}{31.4} = \frac{10000\times10^3}{31.4} = 318.47\times10^3$

$R_{out} \leq 318\ K\Omega$

Actual $R_{out} = \frac{2}{(\lambda_n+\lambda_p)I_5} \leq \frac{2}{(0.04+0.05)\times200} \times 10^6 = 111.11\ K\Omega$

$R_{out} \leq 111.11\ K\Omega$ (Less than $318\ K\Omega$) OK ✓

→ Calculating I_5 considering channel length modulation factors.

$r_{out} = \frac{1}{\lambda I_D}$ $R_{out} = \left(\frac{1}{0.04 I_D} \parallel \frac{1}{0.05 I_D}\right)$

$R_{out} = \frac{0.04\times0.05}{I_D(0.04+0.05)} = \frac{0.0222}{I_D} \leq 318K\Omega$.

$I_5, I_D \geq 70\mu A$

To get some marging we take $I_5 = 100\mu A$

$Sq\ I_{D_1} = I_{D_2} = 50\mu A$

→ Calculating W/L Ratio of PMOS.

$V_{IC}(Max) = V_{DD} - V_{SG3} + V_{TN1}$

(V_{SG3}: PMOS current mirror)

$2 = 2.5 - V_{SG3} + (0.7) \Rightarrow -V_{SG3} = -1.2$, $\boxed{V_{SG3} = 1.2\,V}$

$I_{D3} = I_{D1} = \frac{1}{2} \times K_P \times \frac{W_3}{L_3} \times (V_{SG3} - V_{TP})$

$50 = \frac{1}{2} \times 50 \times \frac{W_3}{L_3} (-1.2 + 0.7)^2$

$\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{2}{(-0.5)^2} = 8$, $\boxed{W_3 = W_4 = 6.4\mu m}$ ✓

$L_3 = L_4 = L_1 = L_2 = 8\mu m$

→ Calculating W/L Ratio of NMOS

$A_V = \frac{V_{out}}{V_{id}} = \frac{g_{md}}{g_{ds2} + g_{ds4}}$ [g_{ds2} & g_{ds4} bcoz Vout is taken from NMOS 2 & 4 only.]

$g_{md} = g_{m1} = g_{m2} = \sqrt{2 K_n' I_{D1,2} \frac{W_1}{L_1}} = \sqrt{K_n' I_{SS} \frac{W_1}{L_1}}$

$g_{ds2} + g_{ds4} = (\lambda_N + \lambda_P) I_{D1,2} = (\lambda_N + \lambda_P)(I_{SS}/2)$

So, $A_V = \frac{2\sqrt{\mu_N C_{ox} \frac{W_1}{L_1}}}{(\lambda_N + \lambda_P)\sqrt{I_{SS}}} = \frac{2\sqrt{110 \frac{W_1}{L_1} \frac{\mu A}{V^2}}}{(0.04 + 0.05)\sqrt{100\mu A}} = 23.31 \sqrt{\frac{W_1}{L_1}} = 100\,V_A$

$\sqrt{\frac{W_1}{L_1}} = \frac{100}{23.31} \Rightarrow \frac{W_1}{L_1} = \frac{W_2}{L_2} = 18.40$

$\boxed{W_1 = W_2 = 14.72\mu m}$ ✓

→ Calculating W/L Ratio for I_5

$V_{IC}(min) = V_{SS} - V_{DS5}(sat) + V_{GS2}$

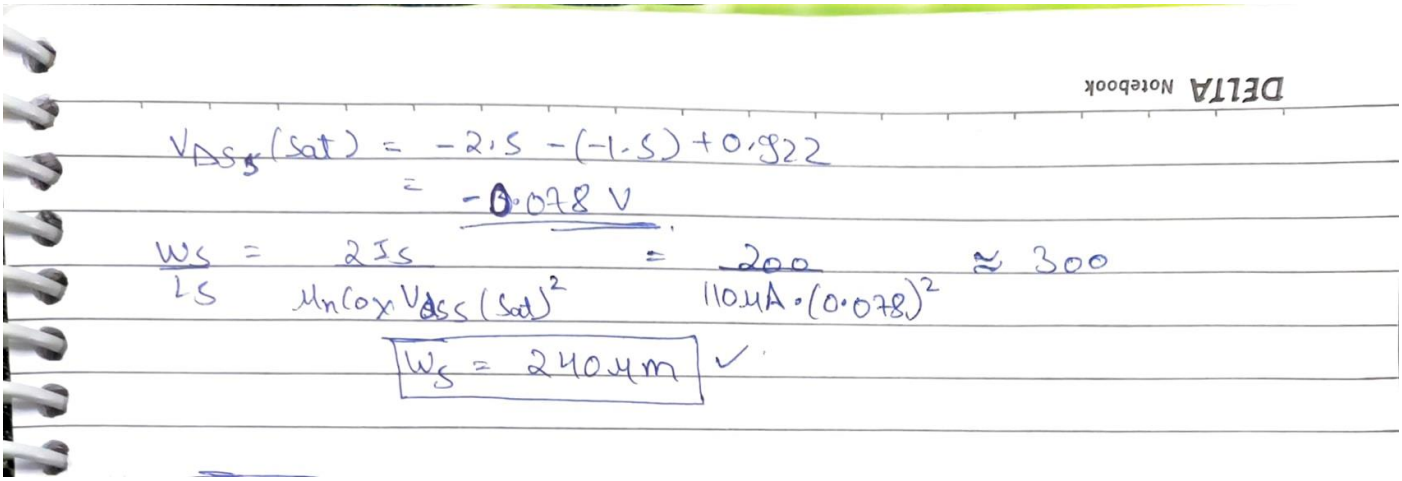
$V_{DS5}(sat) = V_{SS} - V_{IC}(min) + V_{GS2}$

$= -2.5 - (-1.5) + V_{GS2}$?

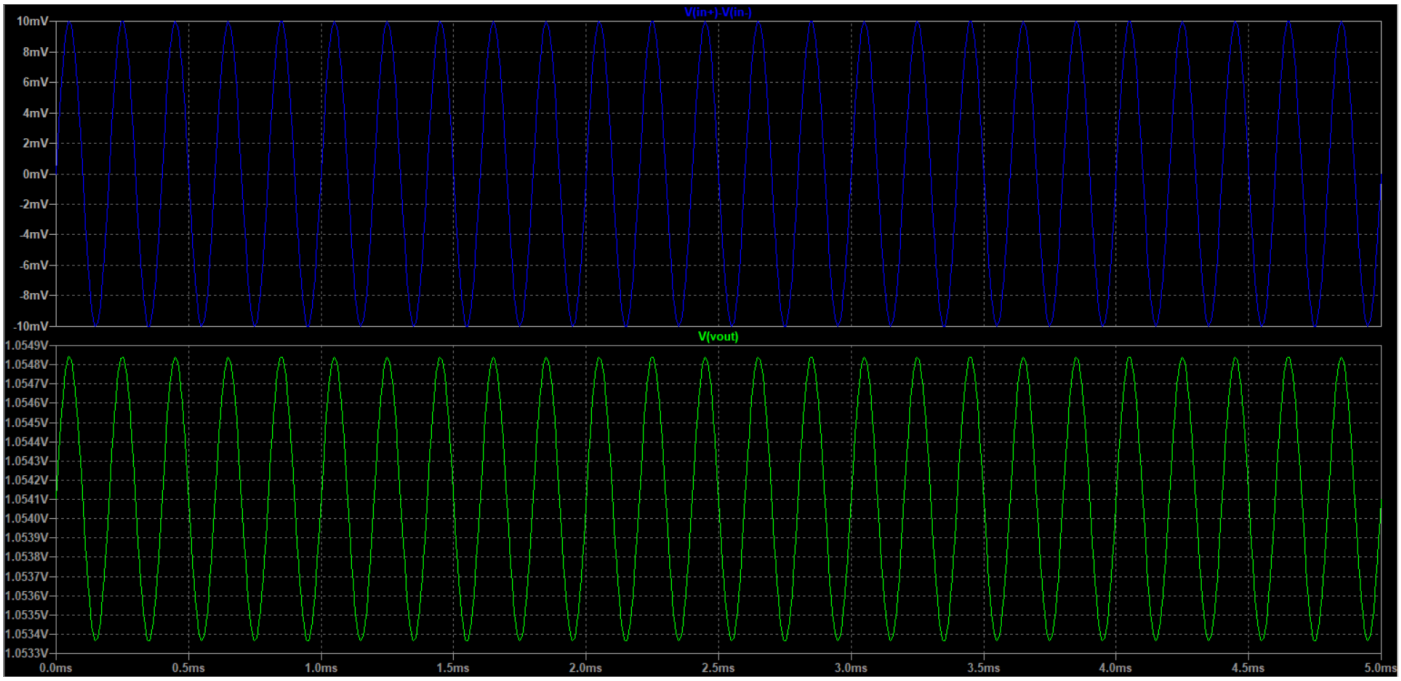
$I_2 = \frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_{GS2} - V_{TN})^2$

$V_{GS2} = \sqrt{\frac{2 I_2 L_2}{\mu_n C_{ox} W_2}} + V_{TN} = \sqrt{\frac{2 \times 50}{110 \times 18.4}} + 0.7 = 0.222 + 0.7$

$\boxed{V_{GS2} = 0.922\,V}$



Verification of Gain:



Gain = Vout/ ((Vin+)-(Vin-)) = 1.054V/10mV = **105.4 V/V**

Here, we can see that our given gain for designing part that is **100 V/V** is approximately equal to the gain comes through the simulation of the circuit by putting the value of width and length that comes through calculation.

NOTE:

We have taken the value of VGS of NMOS 5 greater than 0.7v because if we take it lower than this our NMOS will not in ON Situation which results in not generating the current and leads to wrong value for the Gain.

Also, we need to supply the negative voltage at the PMOS Current mirror because we know that PMOS works only when the negative voltage is applied.