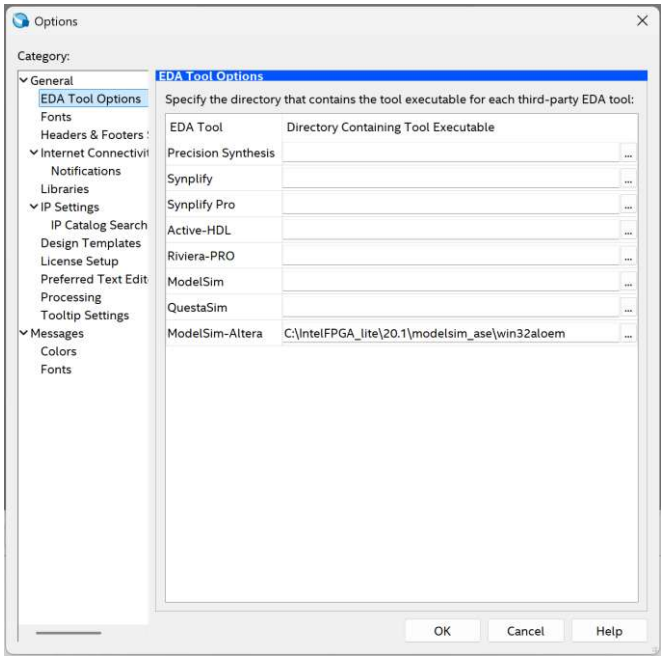
**Part A: Installing Quartus & ModelSim (Intel FPGA Edition)**

1. **Download Quartus Prime Lite Edition**
    - Go to Intel FPGA Download Center.
    - Select **Quartus Prime Lite Edition** (free version).
    - Click Here to Install.
2. **Select Components to Download**
    - Quartus Prime (mandatory).
    - ModelSim Intel FPGA Starter Edition (mandatory for simulation).
3. **Install the Software**
    - Run the Quartus installer and follow on-screen instructions.
    - Then install **ModelSim Intel FPGA Starter Edition**.
4. **Configure EDA Tool Options**
    1. In Quartus, go to **Tools** → **Options**
    2. Select **EDA Tool Options** from the left pane
    3. Under **Simulation**, locate **ModelSim-Altera**
    4. Set the path to:**C:\intelFPGA_lite\21.1\modelsim_ase\win32aloem**
    5. Click **Apply**, then **OK.**



**Part B: Preparing Project Files**

1 . Ensure you have the following files:

- asyncfifo.v → Asynchronous FIFO RTL design.
- fifo_mem.v →FIFO Memory RTL Design
- synchronizer.v →Synchronizer RTL Design
- rptr_handle.vr → Read Pointer Handler RTL Design
- wptr_handler.v →Write Pointer Handler RTL Design
- asyncfifo_tb.v → Testbench file.

Keep them in the same project folder (e.g., D:\Async_FIFO).

2. Set **asyncfifo.v** as **Top Level Entity**

1. Go to **Assignments → Settings**

2.In the left pane, click **General**

3.In the **Top-level entity field,** type: asyncfifo

4.Click **OK** to save.

3. Click the **Start Compilation** button on the toolbar

4.After Successful Compilation of the asyncfifo.v, simulate the testbench.

1.Go to **Assignments** → **Settings**.

2.In the left pane, expand **EDA Tool Settings** → **Simulation**.

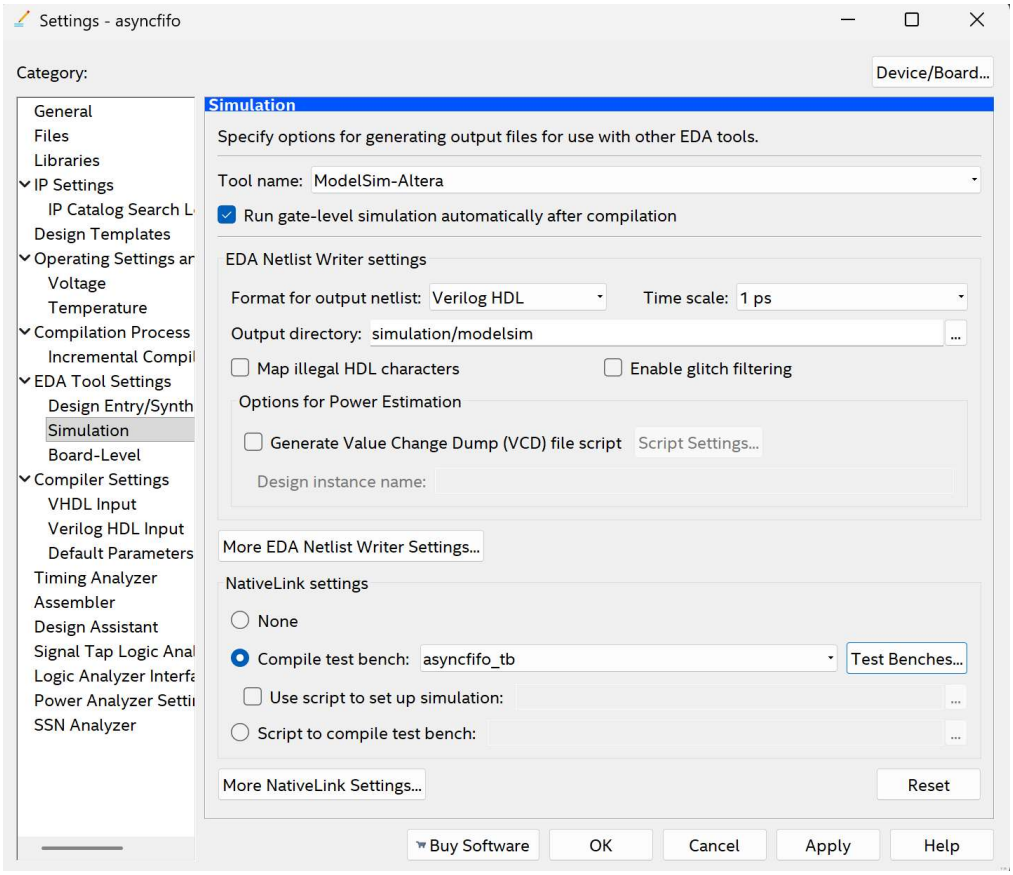
3.Set the following options:

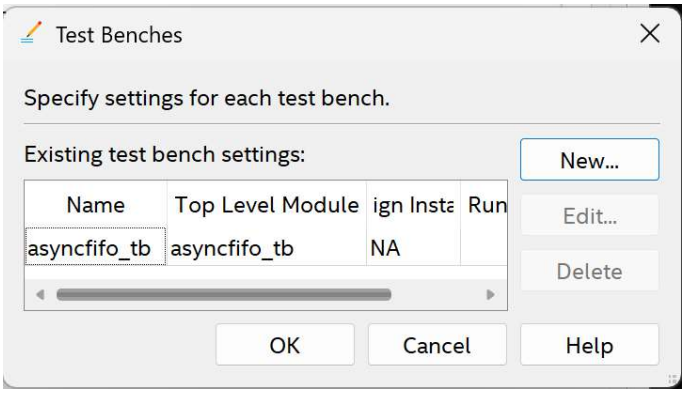
- **Tool name**: ModelSim-Altera
- **Format for output netlist**: Verilog HDL
- **Time scale**: 1 ps
- **Output directory**: simulation/modelsim
- **Test bench name**: asyncfifo_tb

4.Click on **compile testbench** → **Test Benches** →**new** →select **asyncfifo_tb.v**

5.Click **Apply**, then **OK.**

5.Go to **Tools** → **Run Simulation Tool** → **RTL Simulation.**


Settings - asyncfifo
Category:
Device/Board...
General
Files
Libraries
IP Settings
IP Catalog Search L
Design Templates
Operating Settings ar
Voltage
Temperature
Compilation Process
Incremental Compil
EDA Tool Settings
Design Entry/Synth
Simulation
Board-Level
Compiler Settings
VHDL Input
Verilog HDL Input
Default Parameters
Timing Analyzer
Assembler
Design Assistant
Signal Tap Logic Anal
Logic Analyzer Interfa
Power Analyzer Setti
SSN Analyzer
Simulation
Specify options for generating output files for use with other EDA tools.
Tool name: ModelSim-Altera
Run gate-level simulation automatically after compilation
EDA Netlist Writer settings
Format for output netlist: Verilog HDL
Time scale: 1 ps
Output directory: simulation/modelsim
Map illegal HDL characters
Enable glitch filtering
Options for Power Estimation
Generate Value Change Dump (VCD) file script
Script Settings...
Design instance name:
More EDA Netlist Writer Settings...
NativeLink settings
None
Compile test bench: asyncfifo_tb
Test Benches...
Use script to set up simulation:
Script to compile test bench:
More NativeLink Settings...
Reset
Buy Software
OK
Cancel
Apply
Help


Test Benches
Specify settings for each test bench.
Existing test bench settings:
New...
Name
Top Level Module
ign Insta
Run
Edit...
asyncfifo_tb
asyncfifo_tb
NA
Delete
OK
Cancel
Help