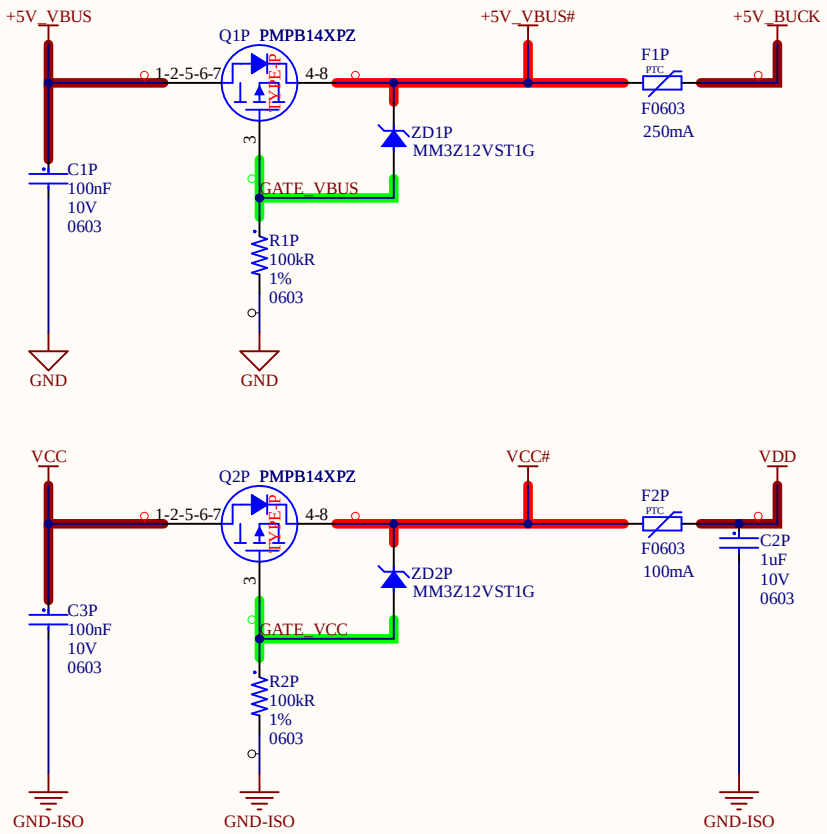


Title: *Power_Path*		**Author:** Alcatraz	**DHNLAB PVT LTD**
Size: A4	**Prj:** USB-SMB-ISO-CP2112	**Approved:** Alcatraz	*DHANBAD*
		PUBLIC	*JHARKHAND*
Date: 06-12-2024 18:06:42	Sheet 1 of 6	**Edited:** 03-12-2024	*INDIA*
Git Hash: 471		**Variant:** [No Variations]	*ASIA*
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\1_Power_Path.SchDoc		**SW Version:** 24.10.1.45	

SGM2019-ADJ
Populate R0L, R1L and R2L

SGM2019-3.3
Only Populate R2L With 100nF Cap
DNP - R0L, R1L

HT7833
DNP - R0L, R1L and R2L

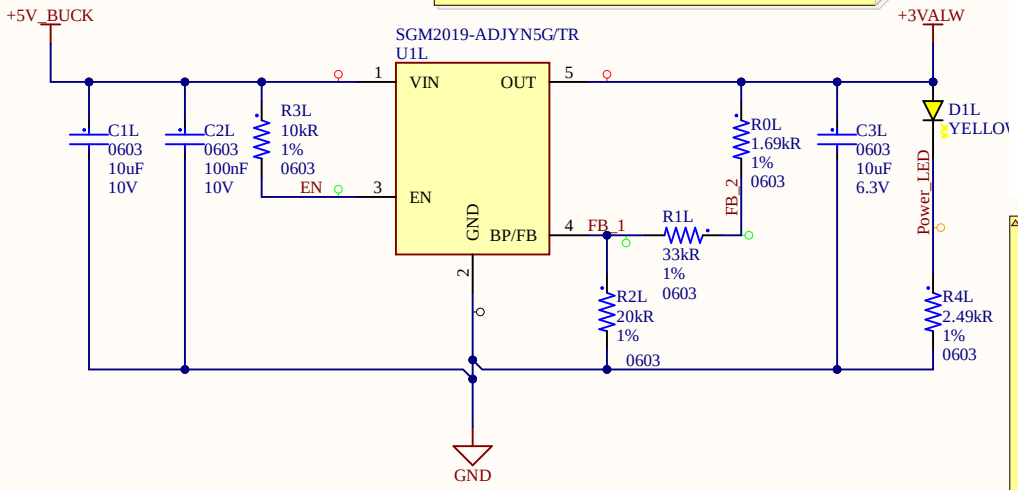
SGM2019-ADJYN5G/TR
Vout = 3.3V
Register Values For
R0L, R1L and R2L
R1L=R0B+R1L

Values From Datasheet

Standard 1% Resistor Values for Common Output Voltages of Adjustable Voltage Version

V_{OUT} (V)	R_1 (kΩ)	R_2 (kΩ)
1.2	0	63.4
1.5	10.5	42.2
1.8	34	63.4
2.8	84.5	63.4
3.0	63.4	42.2
3.3	73.2	42.2
3.6	84.5	42.2
4.2	105	42.2

NOTE: $V_{OUT} = (R_1 + R_2)/ R_2 \times 1.207$



Here are the calculated values of R1L (in kΩ) for VOUT= 3.3 V with different R2L values:
IF R0L= 0Ω
R2L=10kΩ:R1L≈17.34kΩ
R2L=20kΩ:R1L≈34.68kΩ
R2L=30kΩ:R1L≈52.02kΩ
R2L=40kΩ:R1L≈69.36kΩ
R2L=50kΩ:R1L≈86.70kΩ
R2L=60kΩ:R1L≈104.04kΩ
R2L=70kΩ:R1L≈121.38kΩ
R2L=80kΩ:R1L≈138.72kΩ
R2L=90kΩ:R1L≈156.06kΩ
R2L=100kΩ:R1L≈173.41kΩ

Title: LDO		**Author:**	Alcatraz
		Approved:	Alcatraz
Size: A4	**Prj:** USB-SMB-ISO-CP2112		PUBLIC
		Edited:	06-12-2024
Date: 06-12-2024 18:06:42	Sheet 2 of 6	**Variant:**	[No Variations]
Git Hash: 476		**SW Version:**	24.10.1.45
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\2_LDO.SchDoc			

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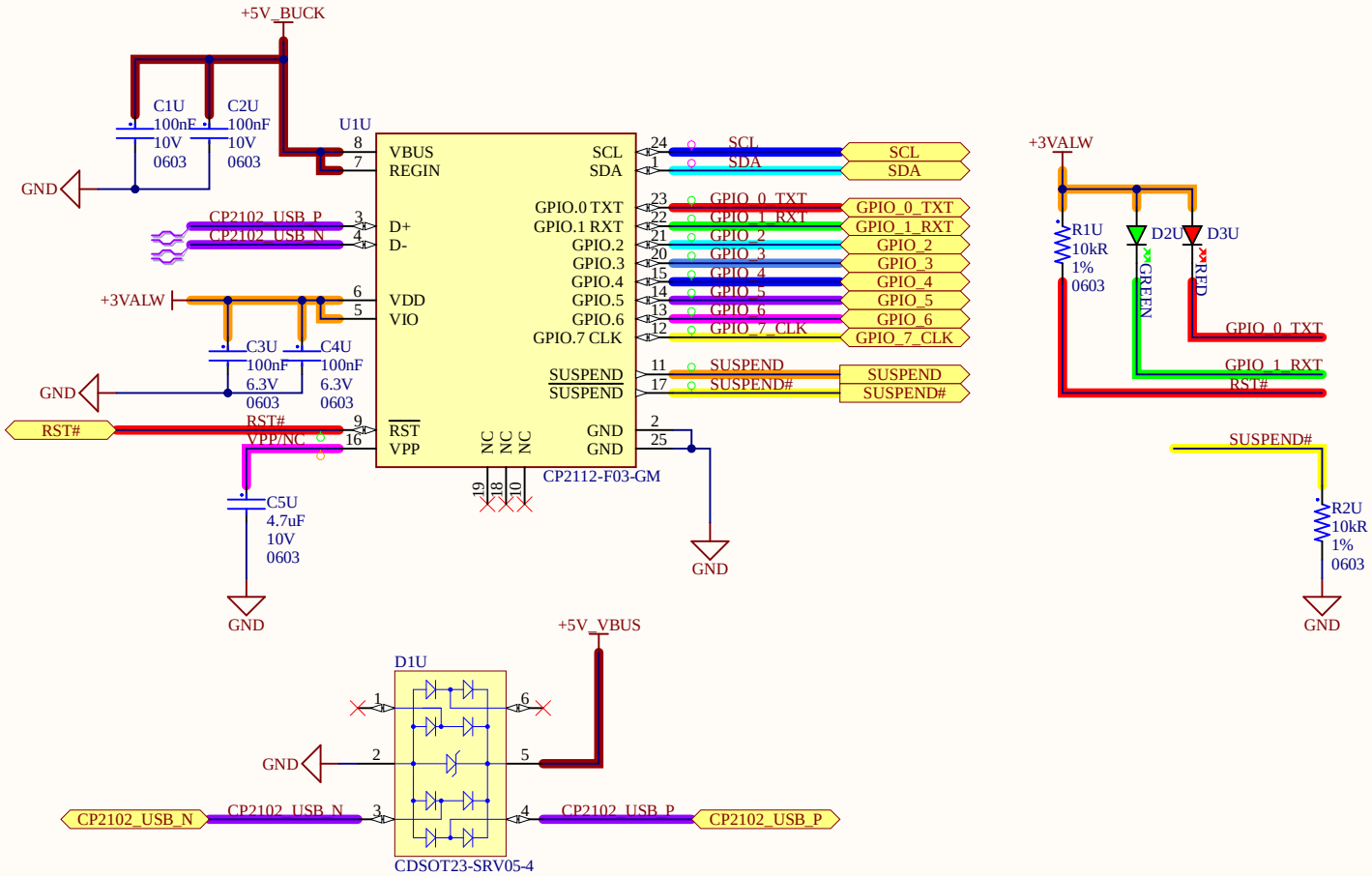
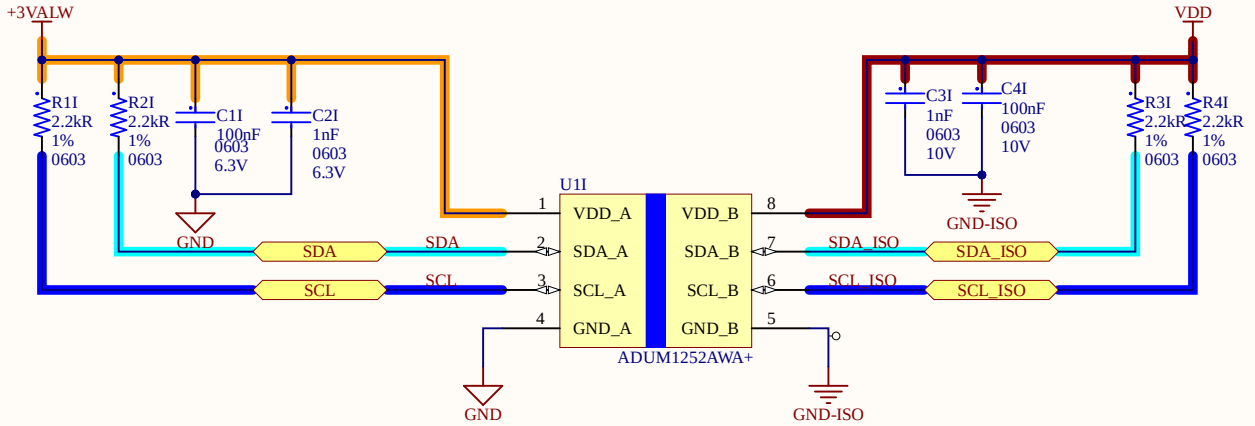
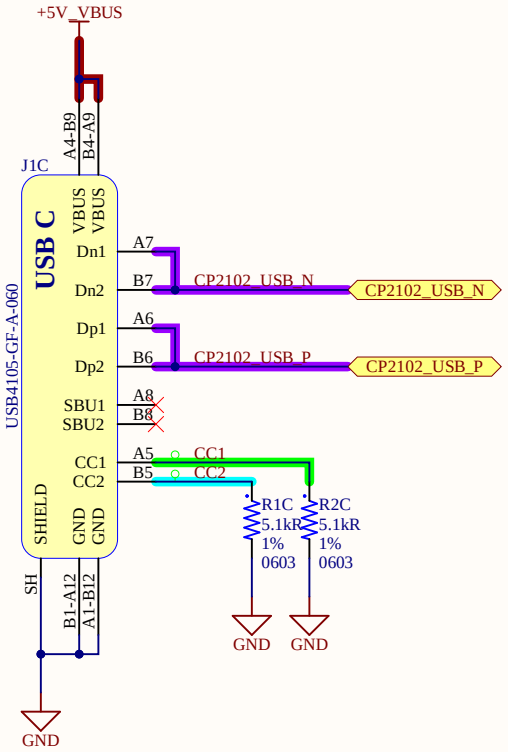
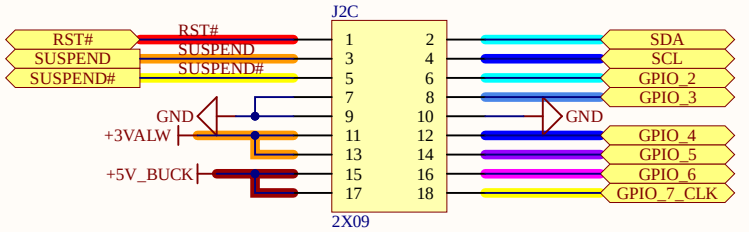


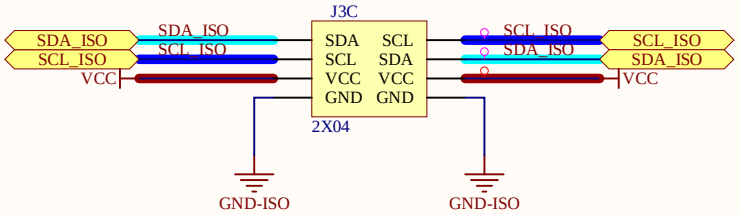
Title: *USB_TO_UART*		**Author:** Alcatraz	**DHNLAB PVT LTD**
Size: A4	**Prj:** USB-SMB-ISO-CP2112	**Approved:** Alcatraz	*DHANBAD*
		PUBLIC	*JHARKHAND*
Date: 06-12-2024 18:06:43	Sheet 3 of 6	**Edited:** 22-11-2024	*INDIA*
Git Hash: 420		**Variant:** [No Variations]	*ASIA*
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\3_USB_TO_UART.SchDoc		**SW Version:** 24.10.1.45	



Title: ***Digital_Isolator***		**Author:** Alcatraz	**DHNLAB PVT LTD**
Size: A4	**Prj:** USB-SMB-ISO-CP2112	**Approved:** Alcatraz	*DHANBAD*
		PUBLIC	*JHARKHAND*
Date: 06-12-2024 18:06:43	Sheet 4 of 6	**Edited:** 22-11-2024	*INDIA*
Git Hash: 425		**Variant:** [No Variations]	*ASIA*
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\4_Digital_Isolator.SchDoc		**SW Version:** 24.10.1.45	







Title: Connector		**Author:** Alcatraz	**DHNLAB PVT LTD**
Size: A4	**Prj:** USB-SMB-ISO-CP2112	**Approved:** Alcatraz	*DHANBAD*
		PUBLIC	*JHARKHAND*
Date: 06-12-2024 18:06:43	Sheet 5 of 6	**Edited:** 22-11-2024	*INDIA*
Git Hash: 420		**Variant:** [No Variations]	*ASIA*
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\6_Connector.SchDoc		**SW Version:** 24.10.1.45	

Title: ***MountingHoles***		**Author:** Alcatraz	**DHNLAB PVT LTD** *DHANBAD* *JHARKHAND* *INDIA* *ASIA*
Size: A4	**Prj:** USB-SMB-ISO-CP2112	**Approved:** Alcatraz	
		PUBLIC	
Date: 06-12-2024 18:06:43	Sheet 6 of 6	**Edited:** 22-11-2024	
Git Hash: 420		**Variant:** [No Variations]	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\7_MountingHoles.SchDoc		**SW Version:** 24.10.1.45	