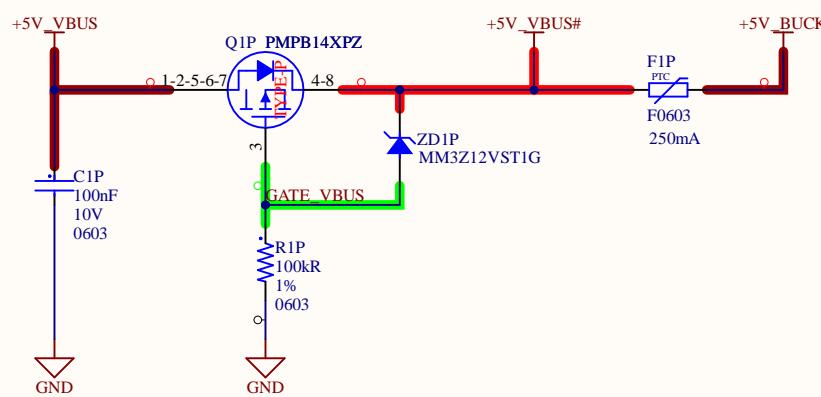
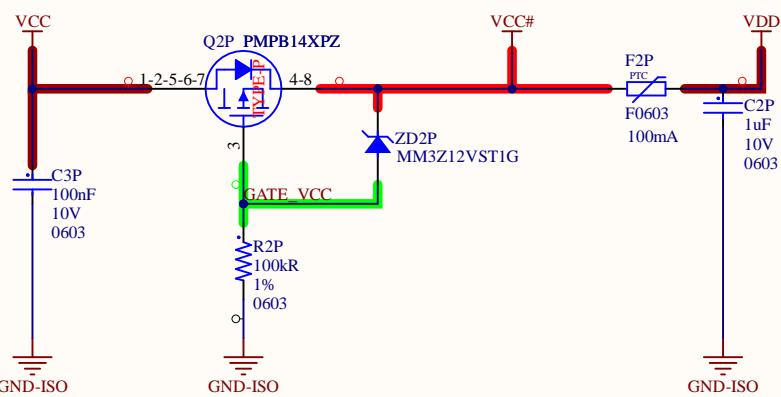


A



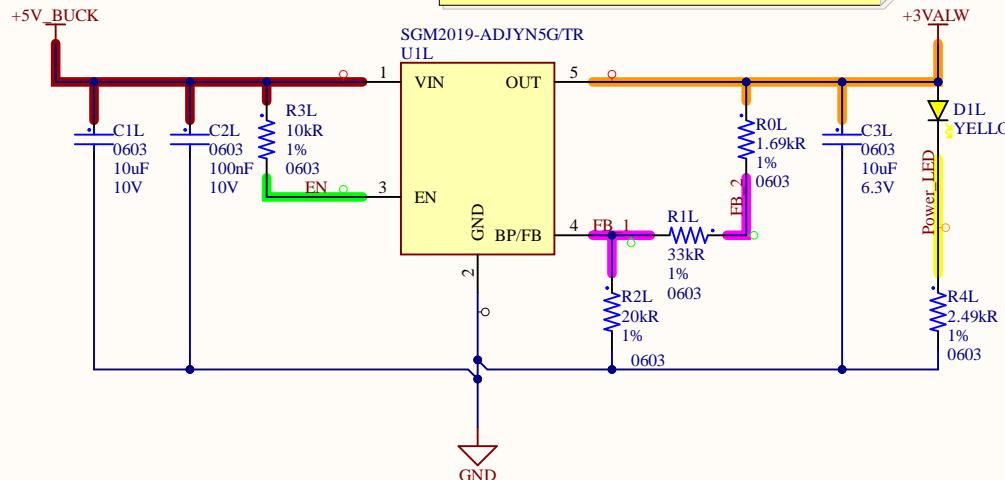
B



C

<b>Title:</b> Power_Path	<b>Author:</b> Alcatraz	<b>DHNLAB PVT LTD</b> <b>DHANBAD</b> <b>JHARKHAND</b> <b>INDIA</b> <b>ASIA</b>
<b>Size:</b> A4	<b>Approved:</b> Alcatraz	
<b>Prj:</b> USB-SMB-ISO-CP2112	<b>PUBLIC</b>	
<b>Date:</b> 06-12-2024 14:28:26	<b>Edited:</b> 03-12-2024	
<b>Git Hash:</b> 471	<b>Variant:</b> [No Variations]	
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\1_Power_Path.SchDoc	<b>SW Version:</b> 24.10.1.45	





**SGM2019-ADJYN5G/TR**  
Vout = 3.3V  
Register Values For R0L, R1L and R2L  
R1L=R0B+R1L

### Values From Datasheet

Vout(V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)
1.2	0	63.4
1.5	10.5	42.2
1.8	34	63.4
2.8	84.5	63.4
3.0	63.4	42.2
3.3	73.2	42.2
3.6	84.5	42.2
4.2	105	42.2

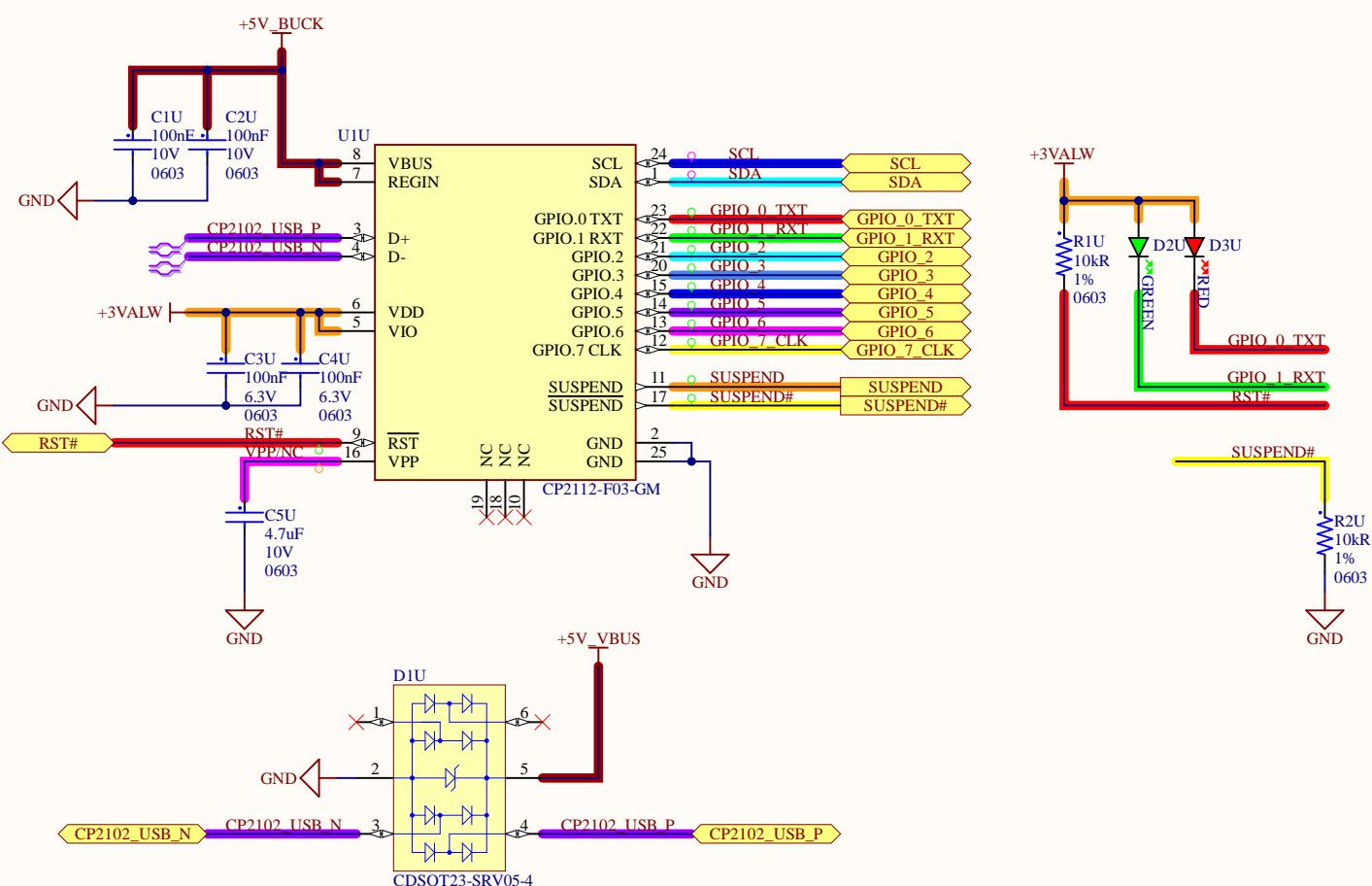
NOTE:  $V_{OUT} = (R_1 + R_2)/R_2 \times 1.207$

Here are the calculated values of R1L (in kΩ) for VOUT= 3.3 V with different R2L values:  
IF R0L= 0Ω  
R2L=10kΩ:R1L≈17.34kΩ  
R2L=20kΩ:R1L≈34.68kΩ  
R2L=30kΩ:R1L≈52.02kΩ  
R2L=40kΩ:R1L≈69.36kΩ  
R2L=50kΩ:R1L≈86.70kΩ  
R2L=60kΩ:R1L≈104.04kΩ  
R2L=70kΩ:R1L≈121.38kΩ  
R2L=80kΩ:R1L≈138.72kΩ  
R2L=90kΩ:R1L≈156.06kΩ  
R2L=100kΩ:R1L≈173.41kΩ

Title: <b>LDO</b>	Author: Alcatraz	DHNLAB PVT LTD
Approved: Alcatraz	PUBLIC	DHANBAD
Size: A4	Edited: 22-11-2024	JHARKHAND
Prj: USB-SMB-ISO-CP2112	Variant: [No Variations]	INDIA
Date: 06-12-2024 14:28:26	SW Version: 24.10.1.45	ASIA
Sheet 2 of 6		
Git Hash: 421		
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\2_LDO.SchDoc		



A



<b>Title: USB_TO_UART</b>		<b>Author:</b> Alcatraz	<b>DHNLAB PVT LTD</b> DHANBAD JHARKHAND INDIA ASIA
<b>Size:</b> A4 <b>Prj:</b> USB-SMB-ISO-CP2112		<b>Approved:</b> Alcatraz	
<b>Date:</b> 06-12-2024 14:28:26 <b>Sheet:</b> 3 of 6		<b>Edited:</b> 22-11-2024	
<b>Git Hash:</b> 420		<b>Variant:</b> [No Variations]	
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\3_USB_TO_UART.SchDoc		<b>SW Version:</b> 24.10.1.45	



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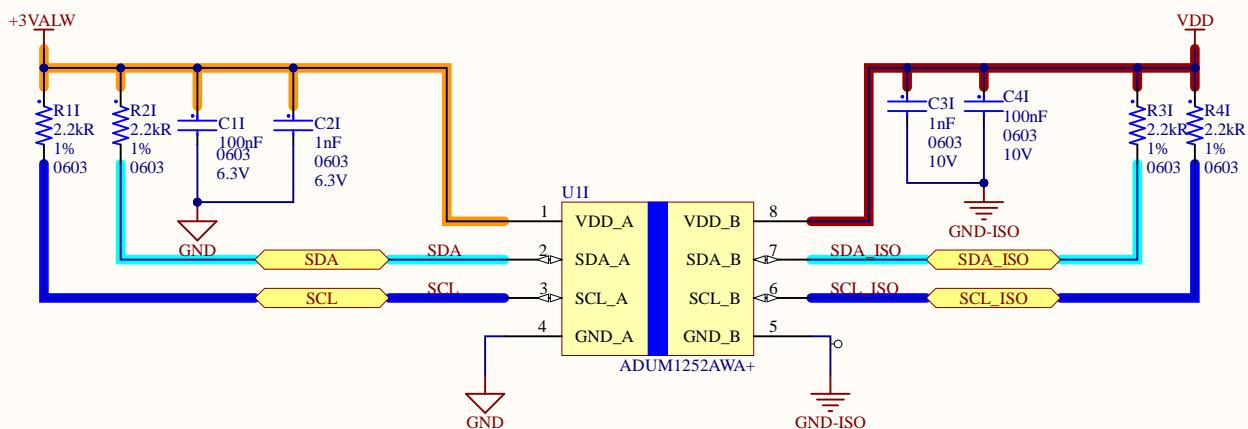
D

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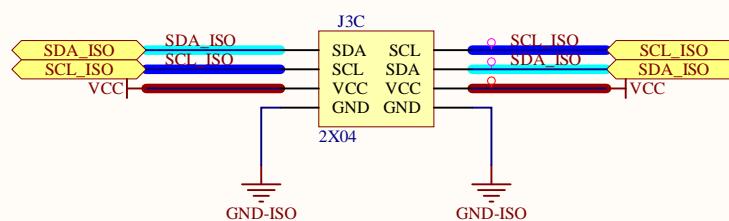
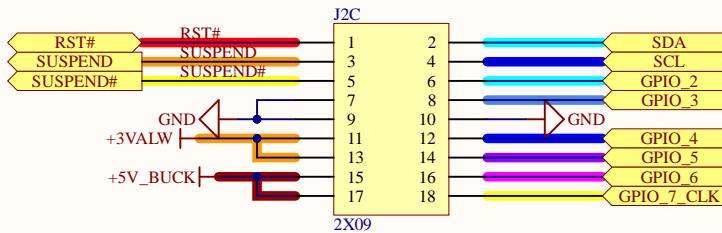
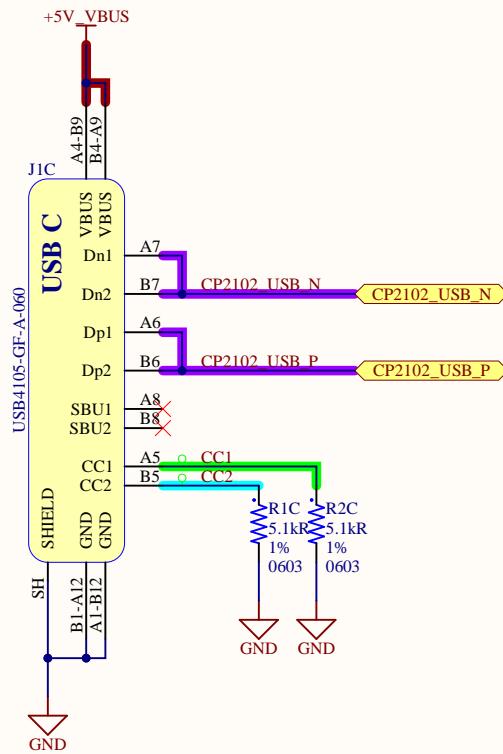
D



<b>Title:</b> <i>Digital_Isolator</i>		<b>Author:</b> Alcatraz	<b>DHNLAB PVT LTD</b>
<b>Size:</b> A4 <b>Prj:</b> USB-SMB-ISO-CP2112		<b>Approved:</b> Alcatraz	<b>DHANBAD</b>
		<b>Edited:</b> PUBLIC	<b>JHARKHAND</b>
		<b>Date:</b> 06-12-2024 14:28:26 <b>Sheet:</b> 4 of 6	<b>INDIA</b>
		<b>Variant:</b> [No Variations]	<b>ASIA</b>
<b>Git Hash:</b> 425		<b>SW Version:</b> 24.10.1.45	
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\4_Digital_Isolator.SchDoc			



A



<b>Title:</b> Connector		<b>Author:</b> Alcatraz	<b>DHNLAB PVT LTD</b> DHANBAD JHARKHAND INDIA ASIA
<b>Size:</b> A4 <b>Prj:</b> USB-SMB-ISO-CP2112		<b>Approved:</b> Alcatraz	
<b>Date:</b> 06-12-2024 14:28:26 <b>Sheet:</b> 5 of 6		<b>Edited:</b> 22-11-2024	
<b>Git Hash:</b> 420		<b>Variant:</b> [No Variations]	
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\6_Connector.SchDoc		<b>SW Version:</b> 24.10.1.45	



A

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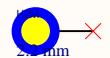
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D



<b>Title:</b> MountingHoles		<b>Author:</b> Alcatraz	<b>DHNLAB PVT LTD</b> DHANBAD JHARKHAND INDIA ASIA
Size: A4	Prj: USB-SMB-ISO-CP2112	Approved: Alcatraz	
Date: 06-12-2024	14:28:26	Edited: 22-11-2024	
Git Hash: 420		Variant: [No Variations]	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-SMB-ISO-CP2112\7_MountingHoles.SchDoc		SW Version: 24.10.1.45	



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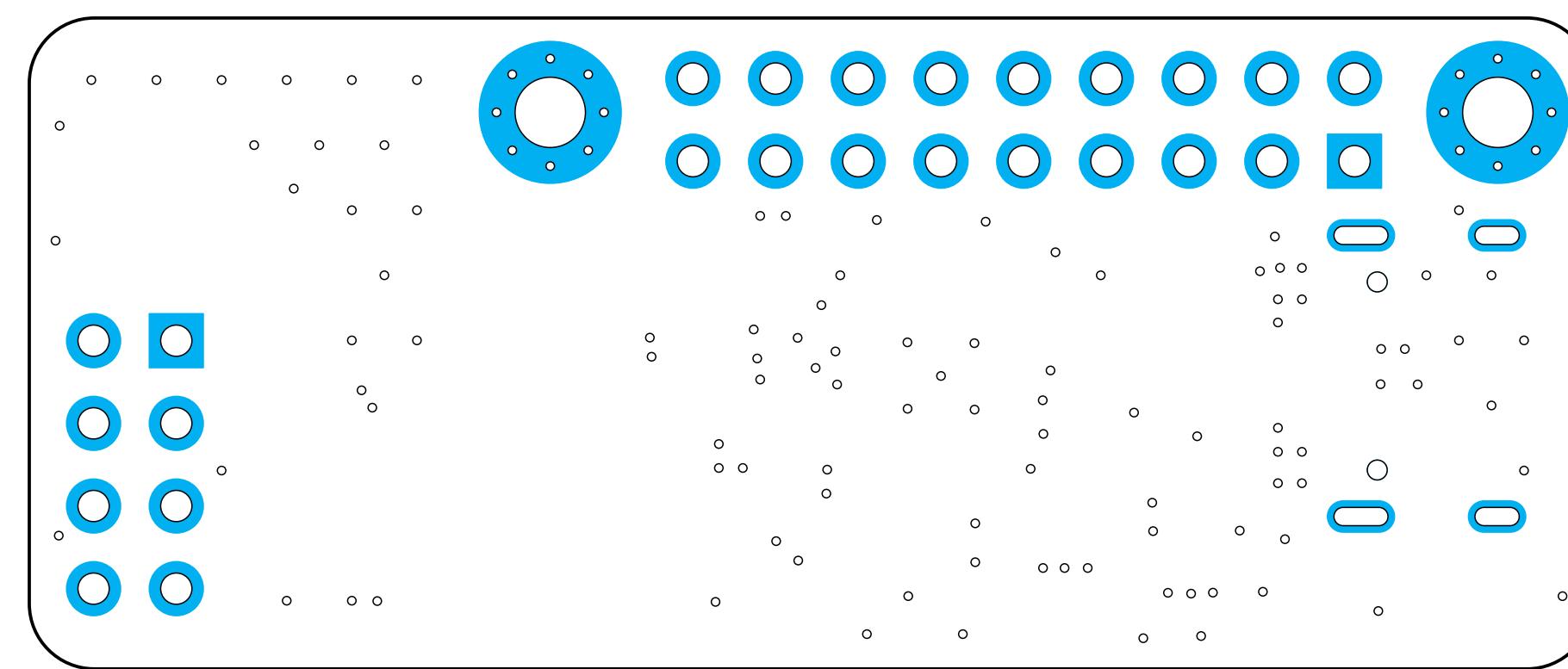
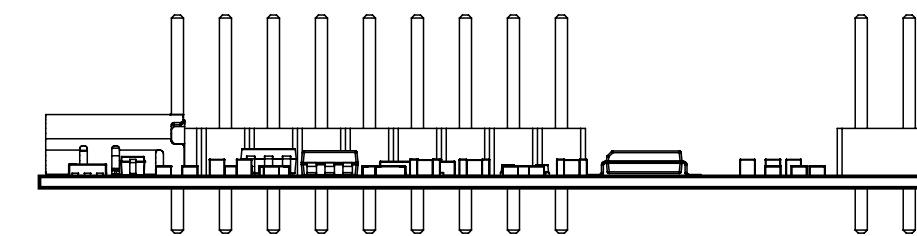
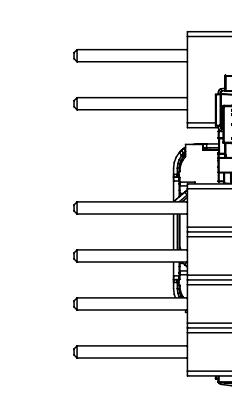
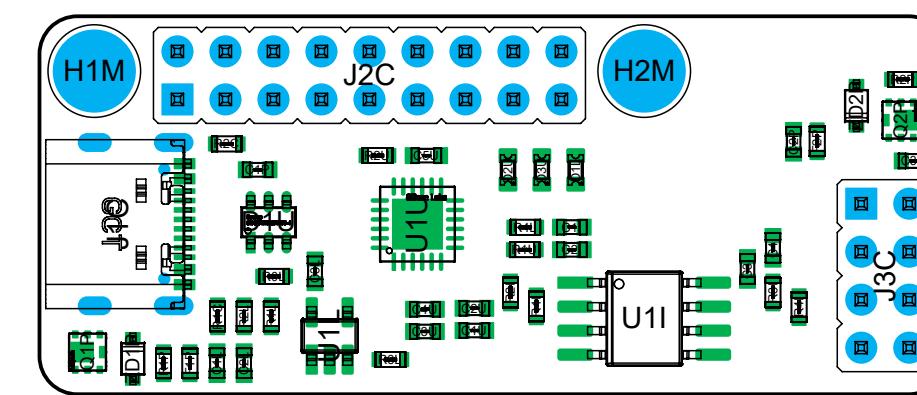
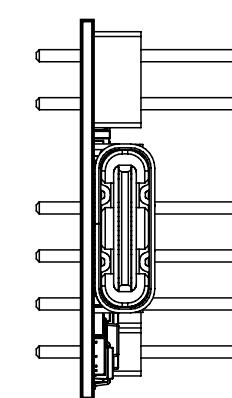
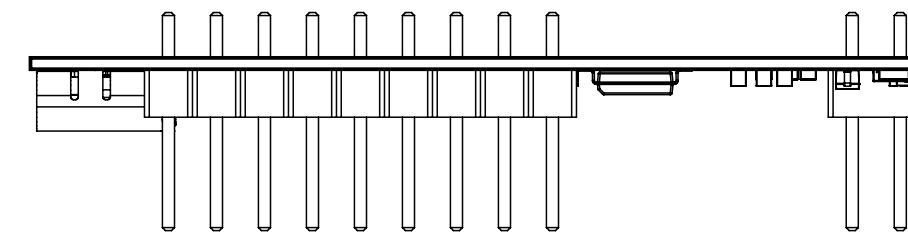
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## Note:

- 1 Text element with square border.
- 2 Text element with no border
- 3 Text element with circle border

THE INFORMATION CONTAINED IN  
THIS DRAWING IS THE SOLE  
PROPERTY OF  
. ANY REPRODUCTION IN PART OR  
AS A WHOLE WITHOUT THE  
WRITTEN PERMISSION OF IS  
PROPRIETARY AND CONFIDENTIAL

		UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	NAME	DATE	TITLE
		TOLERANCES: FRACTIONAL ± ANGULAR: MACH ± BEND ±	DRAWN	06-12-2024	
		TWO PLACE DECIMAL ±	CHECKED		
		THREE PLACE DECIMAL ±	ENG APPR.		
		INTERPRET GEOMETRIC TOLERANCING PER:	MFG APPR.		
		MATERIAL	Q.A.		COMMENTS:
	NEXT ASSY	USED ON	FINISH		
			APPLICATION	DO NOT SCALE DRAWING	
	SCALE: 1:1	WEIGHT:		SHEET 1 OF 1	

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# PCB MANUFACTURING SPECIFICATIONS

## "=ProjectTitle"

### SPECIFICATIONS

NOTE #	NOTE
1	ALL SPECIFICATIONS REFERENCED ARE OF THE REVISION SPECIFIED IN THE TITLE BLOCK
2	SUPPLIER SHALL NOT MODIFY THE DESIGN OR APPROVED STACK-UP WITHOUT WRITTEN PERMISSION
3	ALL MATERIALS SHALL BE RoHS COMPLIANT AND FINAL PRODUCT SHALL BE ACCEPTABLE TO USE IN RoHS ASSEMBLY. RoHS LOGO SHALL BE MARKED IN SILKSCREEN INK BY THE SUPPLIER WHERE INDICATED BY THE TEXT "PLACE MARKINGS HERE"
4	COPPER FOIL: REFER TO LAYER STACK LEGEND FOR Cu THICKNESS DETAILS. ALL Cu THICKNESSES ARE FINISHED AND INCLUDE BASE FOIL PLUS Cu PLATING ON PLATED LAYERS
5	ELECTRICAL TEST: ALL PRINTED CIRCUITS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS/SHORTS USING PROVIDED NETLIST. REJECTED PRINTED BOARDS MUST BE CLEARLY MARKED WITH NON-CONDUCTIVE, PERMANENT INK.
6	MARKINGS: VENDOR MARKING AND DATE/LOT CODES SHALL BE LOCATED ON THE BOARD IN THE RESERVED AREA AS SPECIFIED IN THE GERBER LAYER "PCBM_NOTES" BY THE TEXT "PLACE MARKINGS HERE".
7	MARKINGS: THE SIDE ONTO WHICH PLACE THE MARKINGS IS AT THE SUPPLIER DISCRETION UNLESS OTHERWISE NOTED ONTO THE LAYER "PCBM_NOTES"
8	SUPPLIER SHALL CHECK PCBM_NOTES LAYER BEFORE ASKING FOR CLARIFICATIONS
9	MANUFACTURE TENTED/PLUGGED VIAS AS SPECIFIED IN THE GERBER FILES

### SPECIFICATIONS

LENGTH	20.00mm
WIDTH	48.00mm
LAYERS	2
MATERIAL	FR-4
MATERIAL MIN TG	130-140
TRACK WIDTH/CLEARANCE	10 mils / 10 mils
THICKNESS	0.6mm
COPPER THICKNESS	35um (1oz)
SOLDERMASK	YES, TOP AND BOTTOM
SOLDERMASK COLOR	GREEN
SILKSCREEN	YES, TOP AND BOTTOM
SILKSCREEN COLOR	WHITE
SURFACE FINISH	HASL LEAD FREE
GOLD FINGERS	NO
CHAMFERING	YES
IMPEDANCE CONTROL	YES
HALF-CUT/CASTELLATED HOLES	NO
BURIED/BLIND VIAS	NO
VIAS FILLED WITH RESIN	NO
CARBON MASK	NO
COUNTERSINKS/COUNTERBORES	NO
Z-AXIS MILLING	NO
PEELABLE SOLDERMASK	NO

### Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
	Surface Material	0.02mm	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.04mm		Signal	GTL
	Core	0.50mm	FR-4	Dielectric	
Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	0.02mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.60mm

NON-COPPER LAYER THICKNESS FOR REFERENCE ONLY  
LAYERS OF TYPE "INTERNAL PLANE" ARE NEGATIVE

Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 23-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 06-12-2024 02:28	FMSheet 1 of 3	Address Line 3
Git Hash: 433 [No modification]	SW version: 24.10.1.45	Address Line 4
File:C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_MANUFACTURING_USE		

[YOUR LOGO  
HERE]

A

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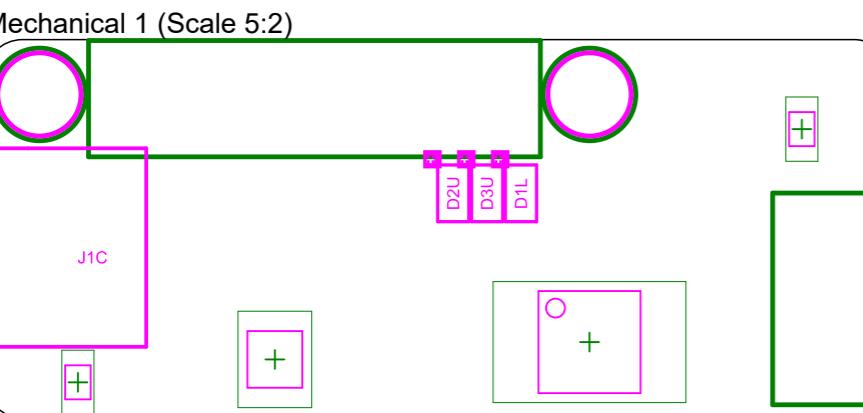
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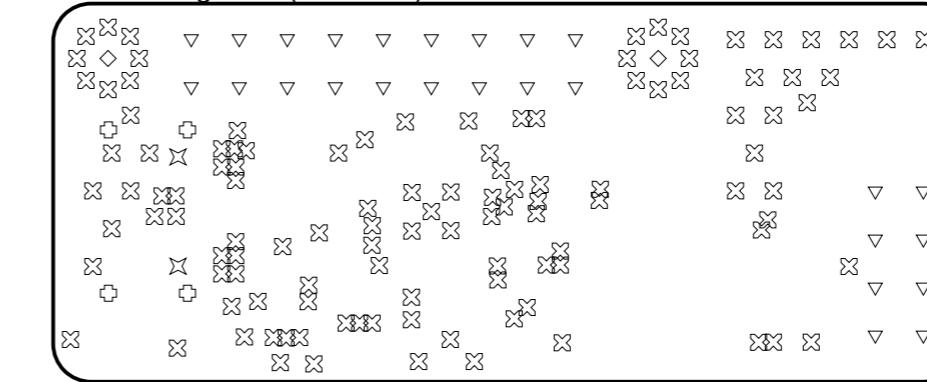
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1



2

Drill Drawing View (Scale 5:2)

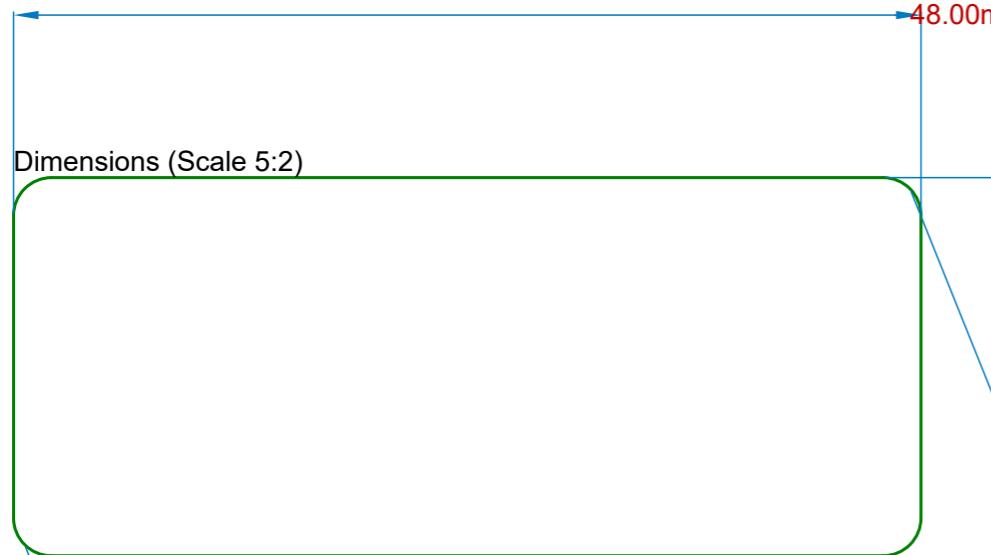


3

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
×	119	0.30mm	Есть	
+	4	0.60mm	Есть	
☒	2	0.65mm	Нет	
▽	26	1.00mm	Есть	
◇	2	2.20mm	Есть	
153 Total				

4



4

**ALWAYS CAREFULLY READ  
THE NOTES ON THIS LAYER!**

5

Title: =ProjectTitle	Author:	CONFIDENTIAL
Approved:		
Size: A3	Edited: 23-11-2024	
Prj: =ProjectTitle	Variant: [No Variations]	
Unit: mm	SW version: 24.10.1.45	
Date: 06-12-2024 02:28	FMSheet 2 of 3	
Git Hash: 433 [No modification]		
File:C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_MANUFACTURING_USE		

[YOUR LOGO  
HERE]

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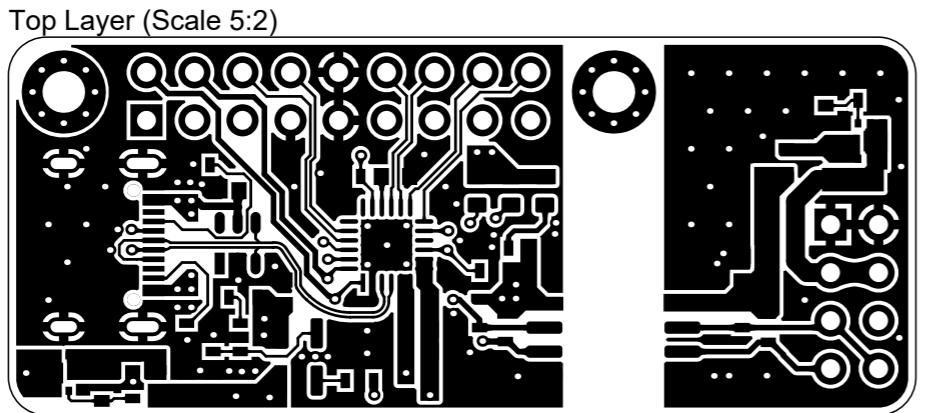
D

E

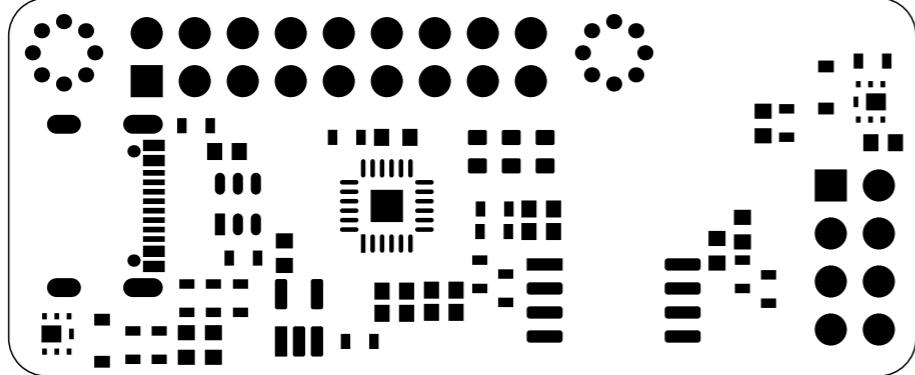
F

G

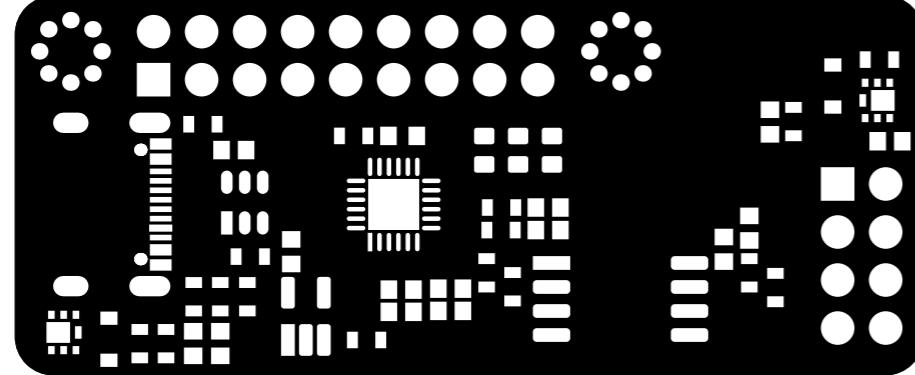
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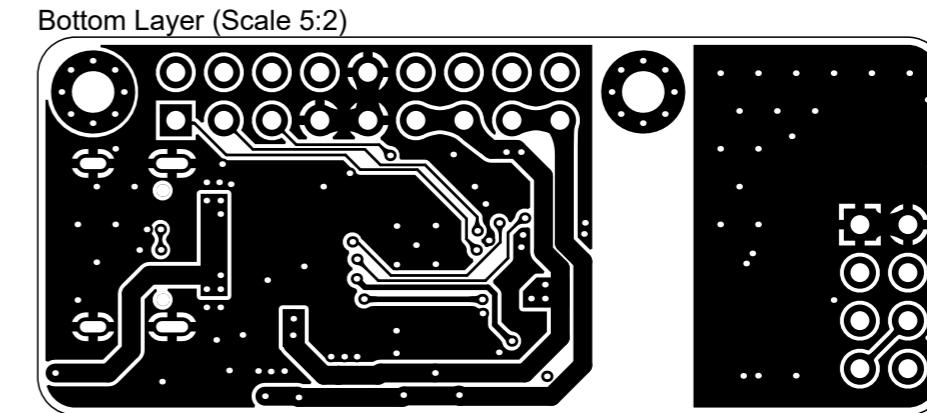
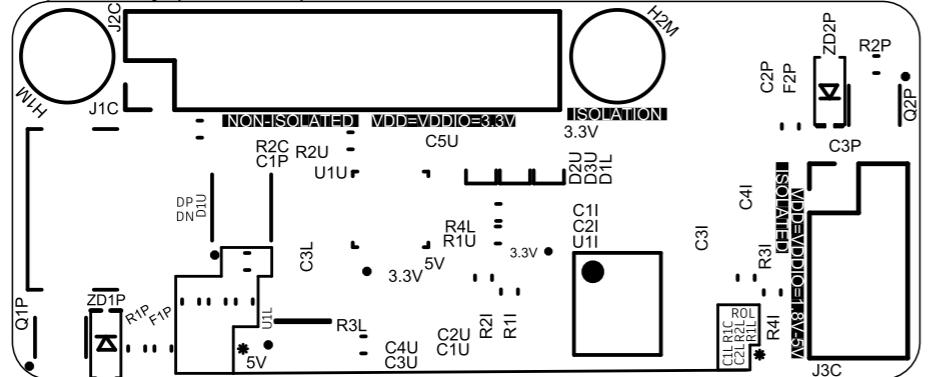
### Top Paste (Scale 5:2)



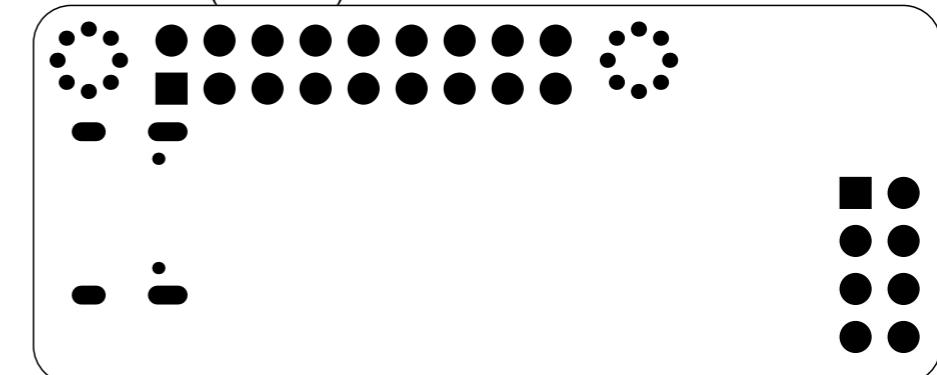
Top Solder (Scale 5:2)



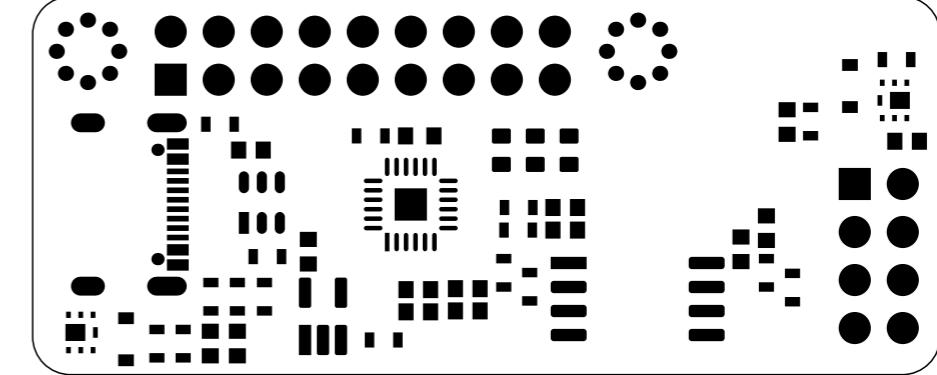
### Top Overlay (Scale 5:2)



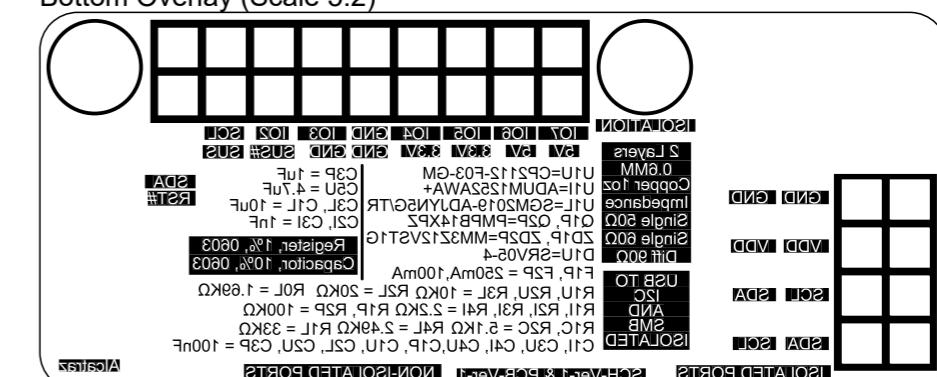
Bottom Paste (Scale 5:2)



Top Paste (Scale 5:2)



Bottom Overlay (Scale 5:2)



<b>Title:</b> =ProjectTitle		<b>Author:</b>	<b>CONFIDENTIAL</b>	
<b>Size:</b> A3	<b>Prj:</b> =ProjectTitle	<b>Approved:</b>	<b>My Company</b>	
<b>Unit:</b> mm		<b>Edited:</b> 23-11-2024	Address Line 1	
		<b>Variant:</b> [No Variations]	Address Line 2	
<b>Date:</b> 06-12-2024 02:28	EWSheet 3 of 3	<b>SW version:</b> 24.10.1.45	Address Line 3	
<b>Git Hash:</b> 433 [No modification]			Address Line 4	
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB MANUFACTURING USE				

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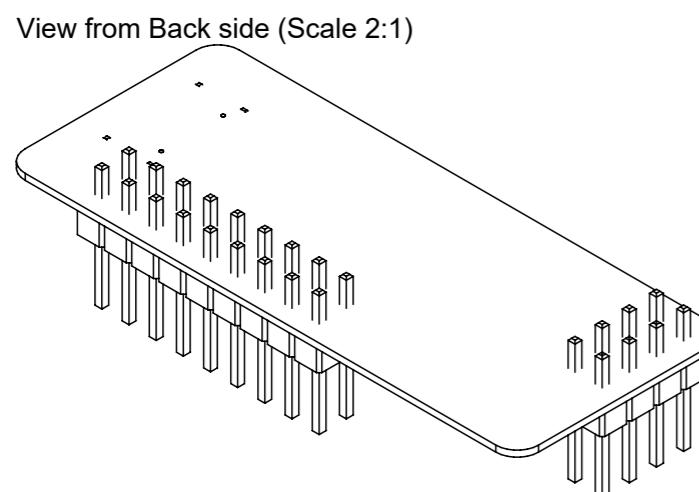
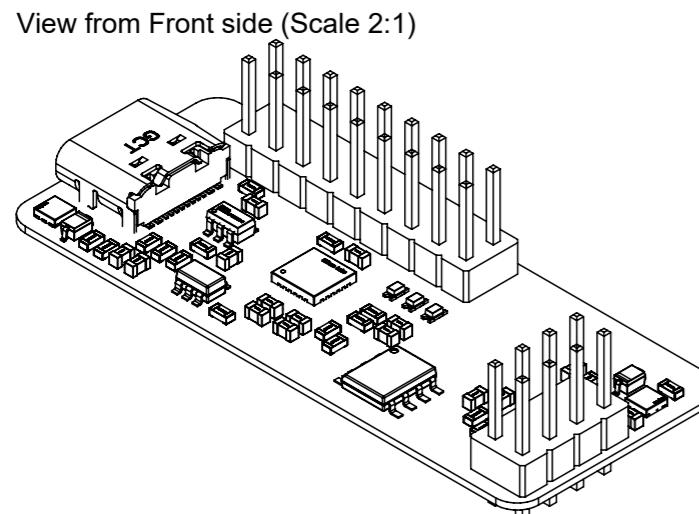
# PCB ASSEMBLY SPECIFICATIONS

## "=ProjectTitle"

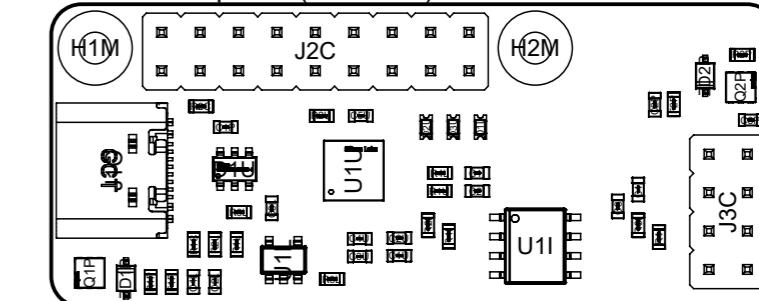
### Variant: "[No Variations]"

#### SPECIFICATIONS

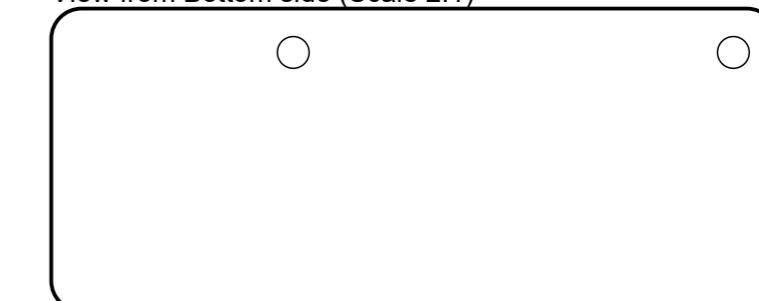
NOTE #	NOTE
1	ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION UNLESS OTHERWISE NOTED
2	SUPPLIER SHALL NOT MODIFY THE DESIGN WITHOUT WRITTEN PERMISSION
3	REFER TO EXCEL BOM FOR UP-TO-DATE INFORMATION
4	THE BOM IN THIS DOCUMENT IS PURELY AN AID TO ASSEMBLY OPERATIONS AND MAY NOT HAVE THE MOST UP-TO-DATE DATA OR ALL APPROVED COMPONENT ALTERNATIVE.



View from Top side (Scale 2:1)



View from Bottom side (Scale 2:1)



Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 23-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 06-12-2024 02:28	FMSheet 1 of 9	Address Line 3
Git Hash: 433 [No modification]	SW version: 24.10.1.45	Address Line 4
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_ASSEMBLY_USB-SMB		[YOUR LOGO HERE]

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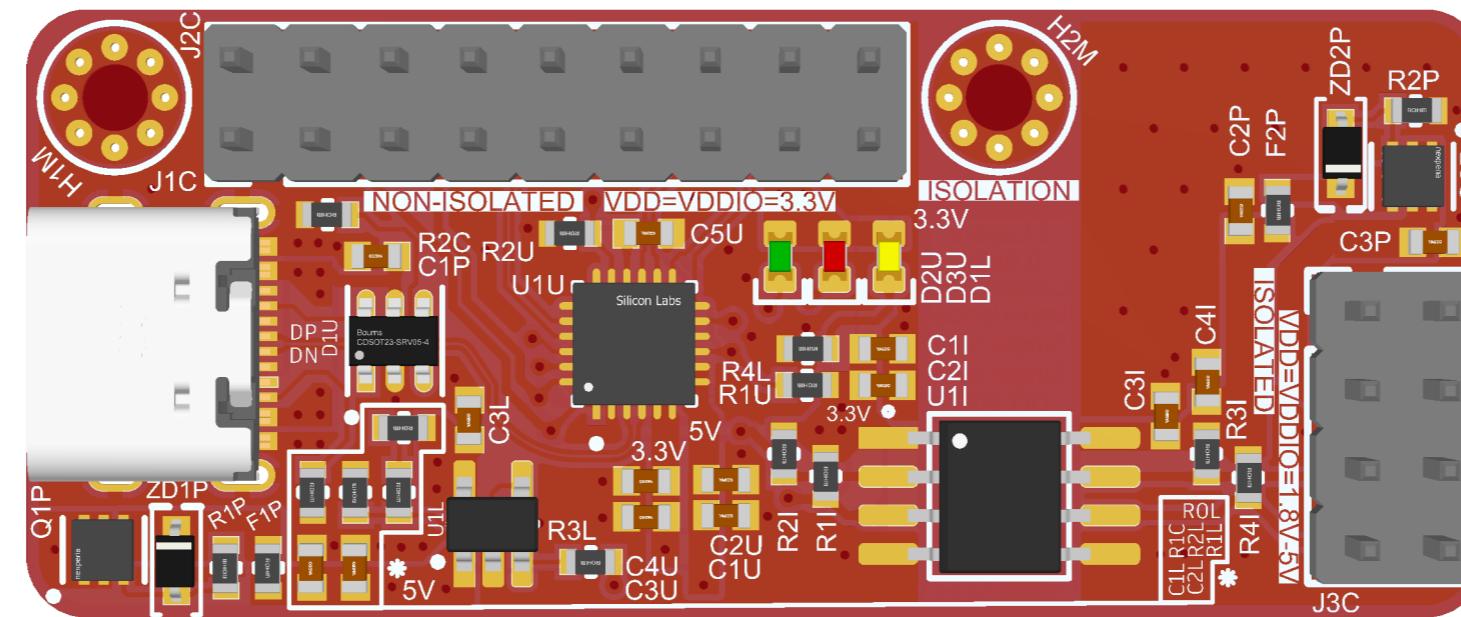
5

5

6

6

Realistic View TOP



<b>Title:</b> =ProjectTitle	<b>Author:</b>	<b>CONFIDENTIAL</b>
<b>Size:</b> A3	<b>Approved:</b>	<b>My Company</b>
<b>Unit:</b> mm	<b>Edited:</b> 23-11-2024	Address Line 1
<b>Prj:</b> =ProjectTitle	<b>Variant:</b> [No Variations]	Address Line 2
<b>Date:</b> 06-12-2024 02:28	<b>FMSheet:</b> 2 of 9	Address Line 3
<b>Git Hash:</b> 433 [No modification]	<b>SW version:</b> 24.10.1.45	Address Line 4
<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_ASSEMBLY_USB-SMB		

**[YOUR LOGO HERE]**

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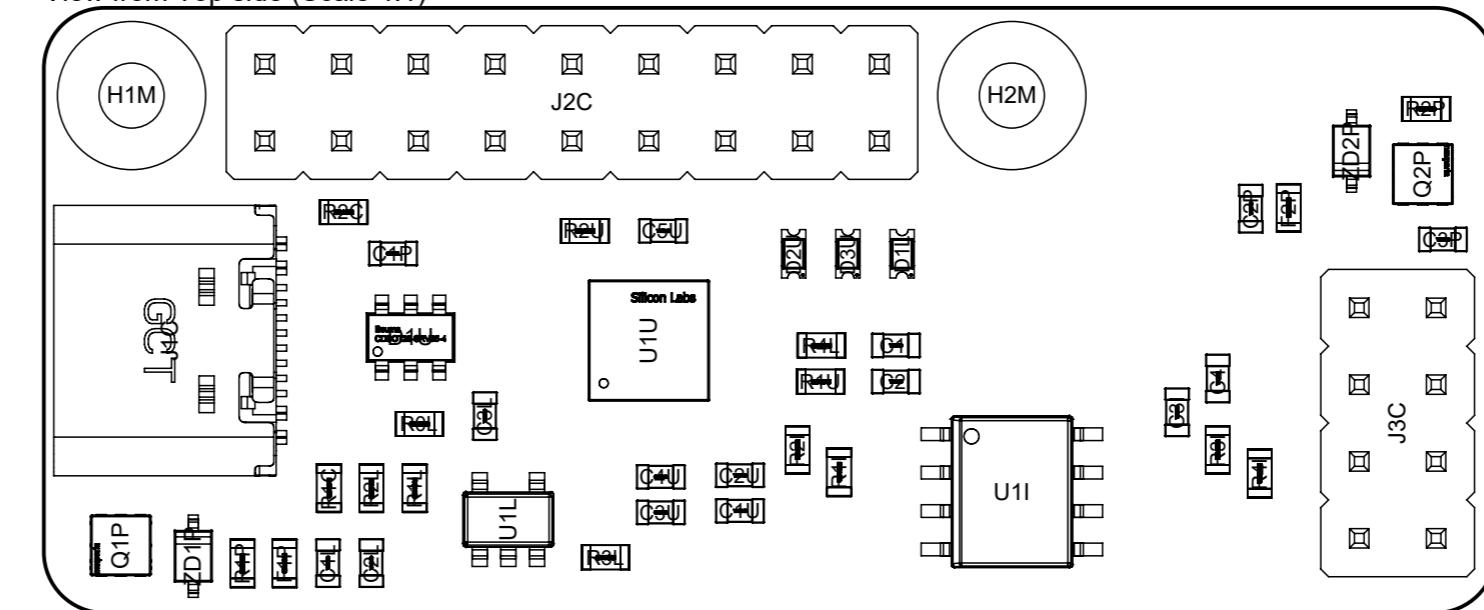
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2

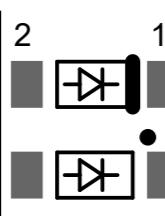
3

3

View from Top side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ( )



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

Title: =ProjectTitle

Author:

**CONFIDENTIAL**

Size: A3 Prj: =ProjectTitle

Approved: Edited: 23-11-2024

My Company

Unit: mm Date: 06-12-2024 02:28 FMSheet 3 of 9

Variant: [No Variations] SW version: 24.10.1.45

Address Line 1

Git Hash: 433 [No modification]

Address Line 2

File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB\_ASSEMBLY\_USB-SMB

Address Line 3

Address Line 4

**[YOUR LOGO HERE]**

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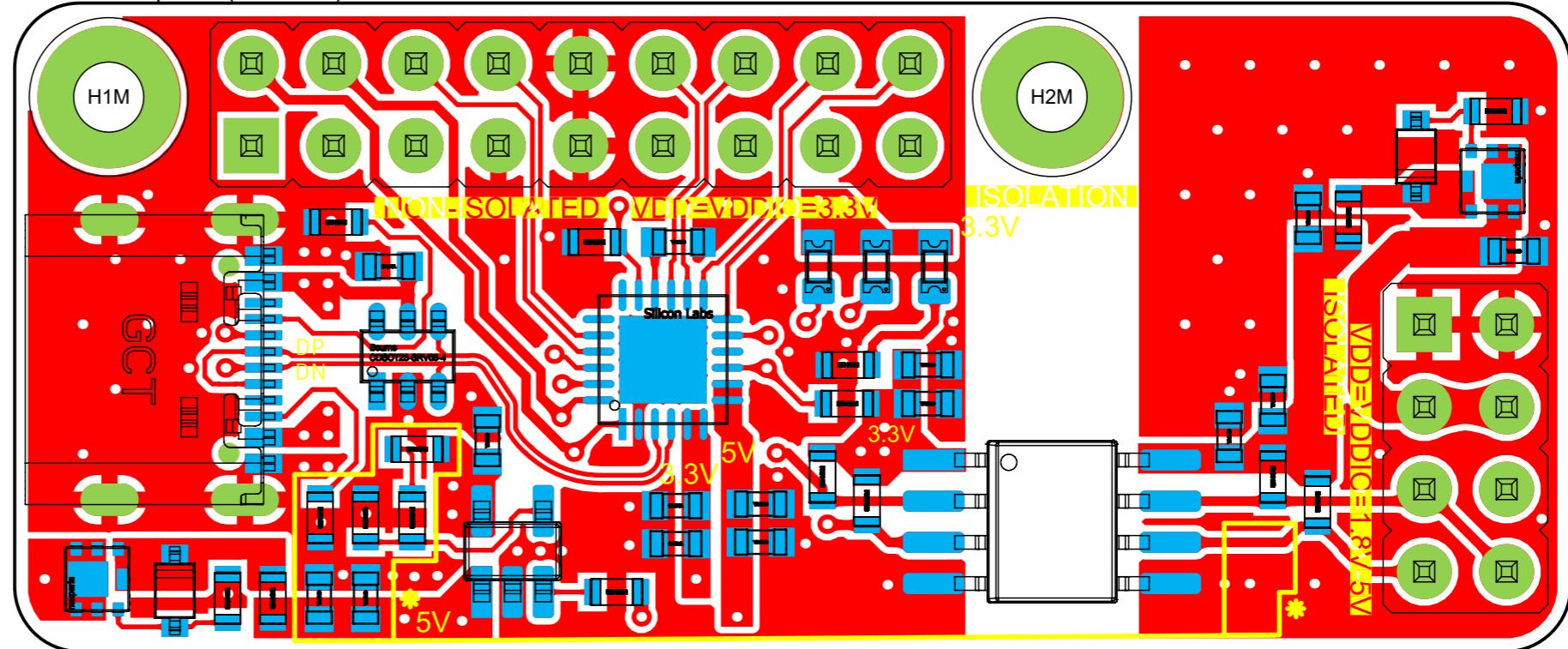
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4

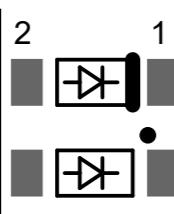
5

6

View from Top side (Scale 5:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ( )



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

Title: =ProjectTitle

Author:

**CONFIDENTIAL**

Size: A3 Prj: =ProjectTitle

Approved: Edited: 23-11-2024

My Company

Unit: mm Date: 06-12-2024 02:28 FileSheet 4 of 9

Variant: [No Variations] SW version: 24.10.1.45

Address Line 1

Git Hash: 433 [No modification]

Address Line 2

File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB\_ASSEMBLY\_USB-SMB

Address Line 3

Address Line 4

**[YOUR LOGO HERE]**

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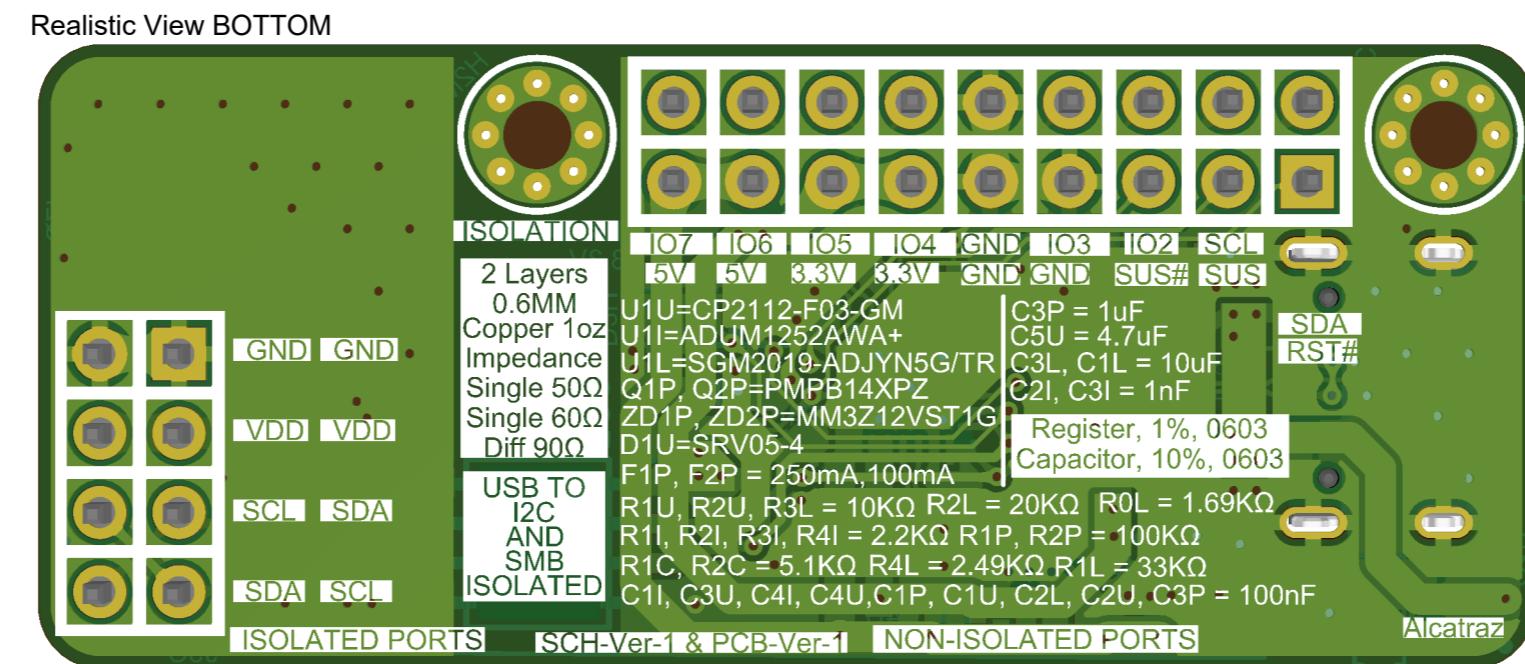
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<b>Title:</b> =ProjectTitle	<b>Author:</b>	<b>CONFIDENTIAL</b>
<b>Size:</b> A3	<b>Approved:</b>	<b>My Company</b>
<b>Unit:</b> mm	<b>Edited:</b> 23-11-2024	Address Line 1
<b>Prj:</b> =ProjectTitle	<b>Variant:</b> [No Variations]	Address Line 2
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<b>File:</b> C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_ASSEMBLY_USB-SMB		

[YOUR LOGO  
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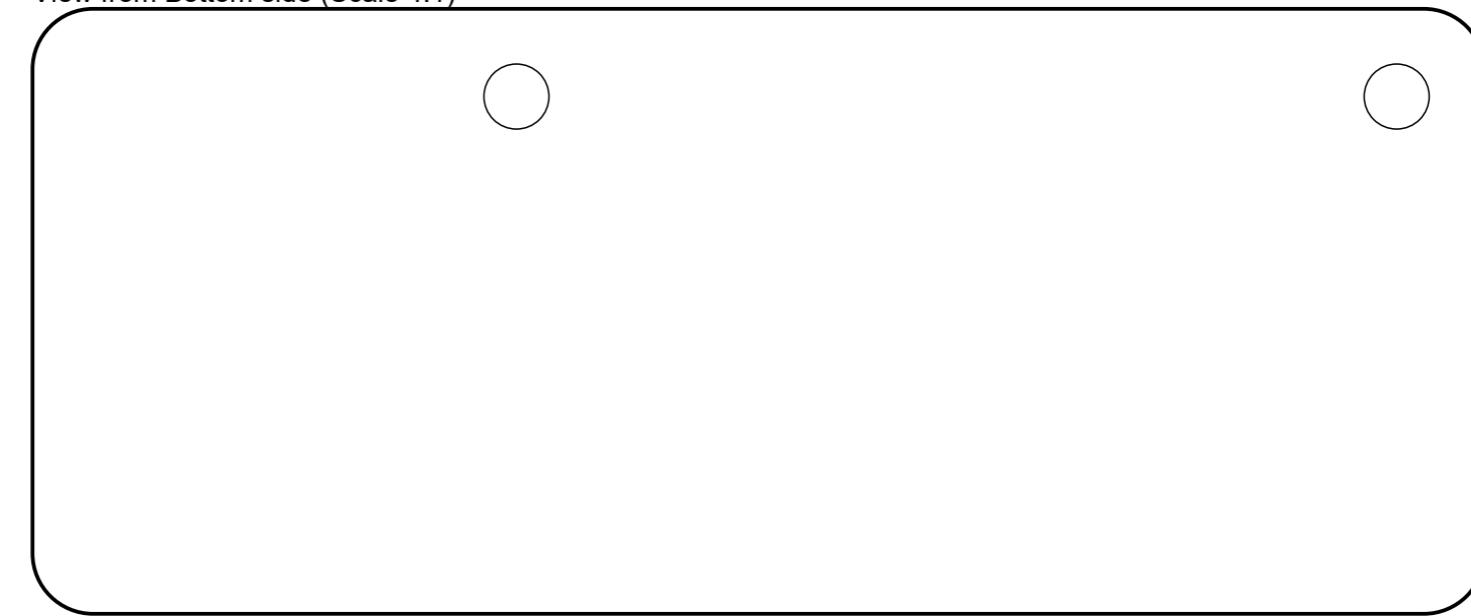
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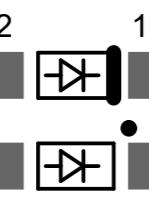
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View from Bottom side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ( )



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (*)

Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 23-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 06-12-2024 02:28	FMSheet 6 of 9	Address Line 3
Git Hash: 433 [No modification]	SW version: 24.10.1.45	Address Line 4
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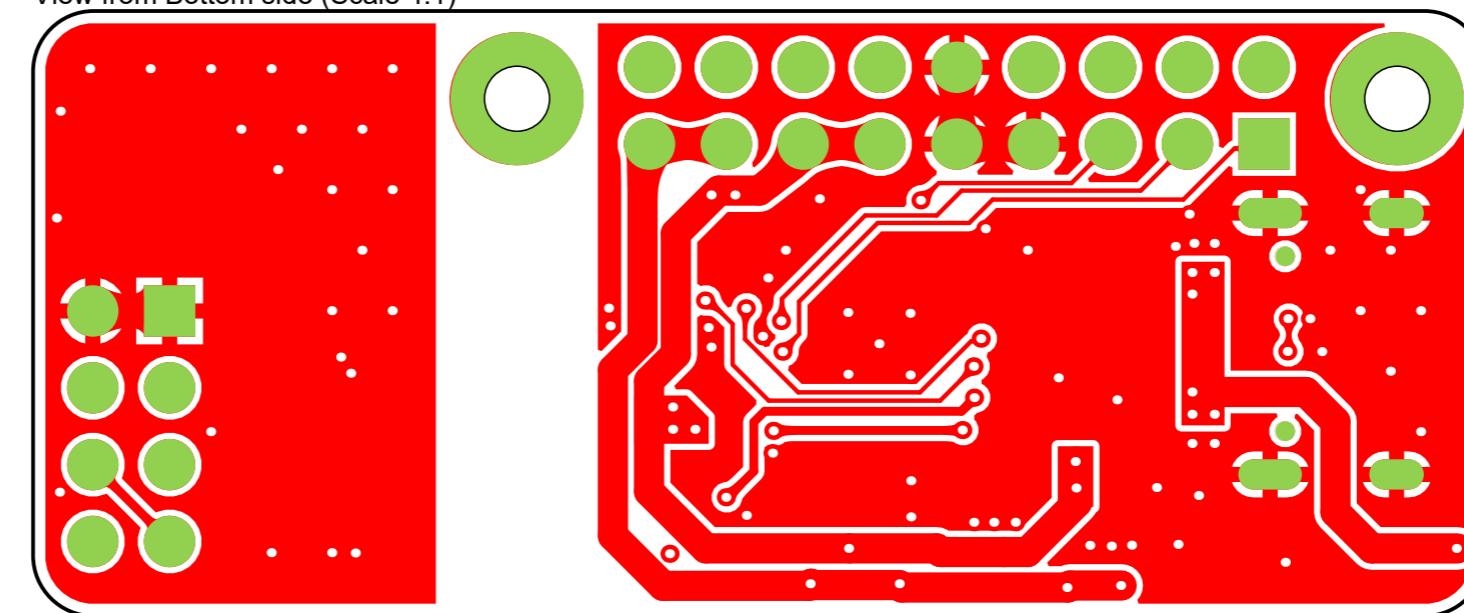
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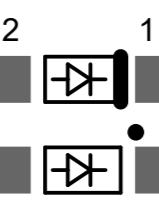
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View from Bottom side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ( )



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

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Size: A3	Approved:	
Unit: mm	Edited: 23-11-2024	My Company
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 1
Date: 06-12-2024 02:28	FMSheet 7 of 9	Address Line 2
Git Hash: 433 [No modification]	SW version: 24.10.1.45	Address Line 3
		Address Line 4
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YOUR LOGO  
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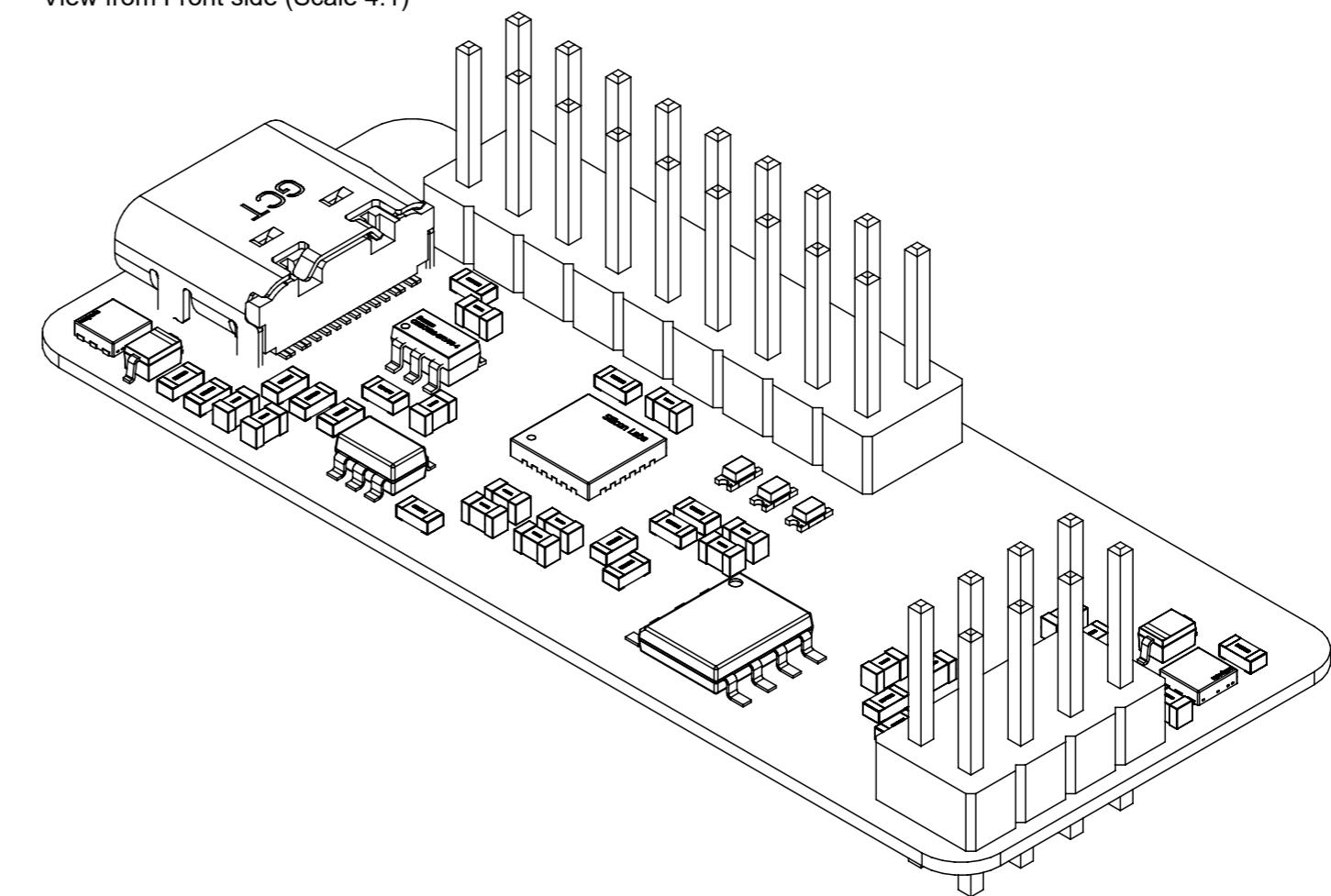
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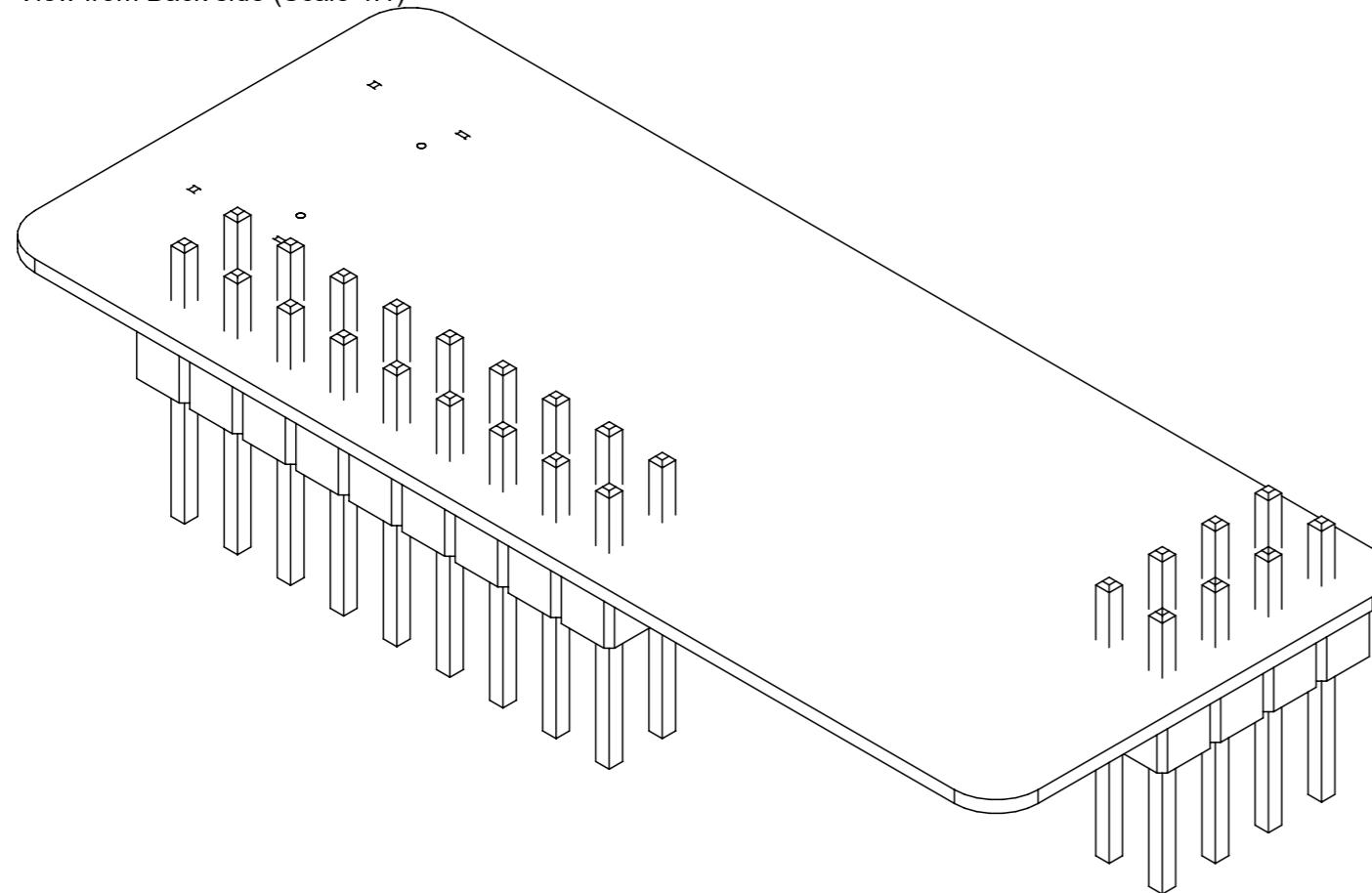
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View from Front side (Scale 4:1)



View from Back side (Scale 4:1)



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Size: A3	Approved:	My Company
Prj: =ProjectTitle	Edited: 23-11-2024	Address Line 1
Unit: mm	Variant: [No Variations]	Address Line 2
Date: 06-12-2024 02:28	FMSheet 8 of 9	Address Line 3
Git Hash: 433 [No modification]	SW version: 24.10.1.45	Address Line 4
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_ASSEMBLY_USB-SMB		

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## Bill Of Materials

Line #	Description	Designator	Quantity	Manufacturer Part Number 1	Part Number	Layer
2	Cap Cer 0.1uF 6.3V X7R 0603	C1I, C3U, C4U	3	KGM15AR70J104KM		
	Multilayer Ceramic Capacitor, 10 uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C1L	1			
	Multilayer Ceramic Capacitor, 0.1 uF, 10 V, ± 10%, X7R, 0603 [1608 Metric]	C1P, C1U, C2L, C2U, C3P, C4I	6	C0603C104K8RAC786 7		
	Cap Ceramic 0.001uF 6.3V COG 10% SMD 0603 125°C Paper T/R	C2I	1	06036A102KAT2A		
	Ceramic Capacitor, Multilayer, Ceramic, 10V, 10% +Tol, 10% -Tol, X5R, 15% TC, 1uF, 0603	C2P	1			
	Cap Ceramic 0.001uF 10V X7R 10% SMD 0603 125°C Paper T/R	C3I	1			
	Multilayer Ceramic Capacitor, 10 uF, 6.3 V, ± 10%, X5R, 0603 [1608 Metric]	C3L	1	CL10A106KQ8NNNC		
	Multilayer Ceramic Capacitor, 4.7 uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C5U	1	CL10A475KP8NNNC		
3	LED 0603 YELLOW SMD	D1L	1			
	TVS DIODE 5V 15V SOT23-6	D1U	1			
	LED 0603 GREEN SMD	D2U	1			
	LED 0603 RED SMD	D3U	1			
	Fuse PPTC SMD 0603	F1P	1			
	Fuse PPTC SMD 0603	F2P	1			
	USB Connector Type C SMT 16 Pin (Power pins joints = 12 pins)	J1C	1			
		J2C	1			
		J3C	1			
	PMPB14XPZ	Q1P, Q2P	2	PMPB14XPZ		
4	Surface Mount Thick Film Chip Resistor 0603 Case 1.69K Ohms 1% Tolerance 100 PPM	R0L	1	MCR03EZPFX1691		
	SMD Chip Resistor, 5.1 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1C, R2C	2	CRCW06035K10FKEA		
	SMD Chip Resistor, 2.2 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1I, R2I, R3I, R4I	4	RC0603FR-072K2L		
	Res Thick Film 0603 33K Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD Automotive T/R	R1L	1	ERJ-3EKF3302V		
	SMD Chip Resistor, 100 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1P, R2P	2	AC0603FR07100KL		
	SMD Chip Resistor, 10 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1U, R2U, R3L	3	RC0603FR-0710KL		
	SMD Chip Resistor, 20 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R2L	1	CR0603-FX-2002ELF		
5	Res Thick Film 0603 2.49K Ohm 1% 1/10W ±100ppm/°C Molded SMD SMD Paper T/R	R4L	1			
	Ultra-Low Power, Bidirectional I2C Isolator with Extended VDD, Idle-Bus Hot-Swap and Low VOL	U1I	1	ADUM1252AWA+		
	LDO U-Reg Adj 0, 3A SOT23-5	U1L	1	SGM2019-ADJYN5G/TR		
	IC HID USB-TO-SMBUS BRIDGE 24QFN	U1U	1			
	MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323   ON Semiconductor MM3Z12VST1G	ZD1P, ZD2P	2			

Please consider LCSC (立创商城) as our first supplier

BOM FOR REFERENCE ONLY

ALWAYS REFER TO THE LATEST EXCEL BOM PROVIDED

Title: =ProjectTitle		Author:	CONFIDENTIAL
Size: A3	Prj: =ProjectTitle	Approved:	My Company Address Line 1 Address Line 2 Address Line 3 Address Line 4
Unit: mm		Edited: 23-11-2024	
Date: 06-12-2024 02:28	MSheet 9 of 9	Variant: [No Variations]	
Git Hash: 433 [No modification]		SW version: 24.10.1.45	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\PCB_ASSEMBLY_USB-SMB			

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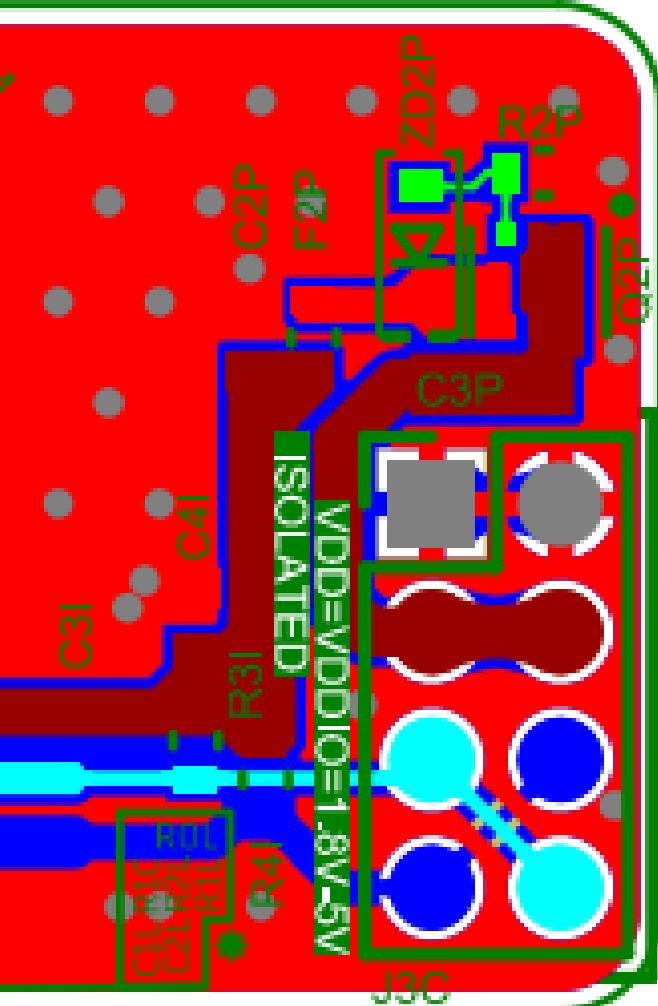
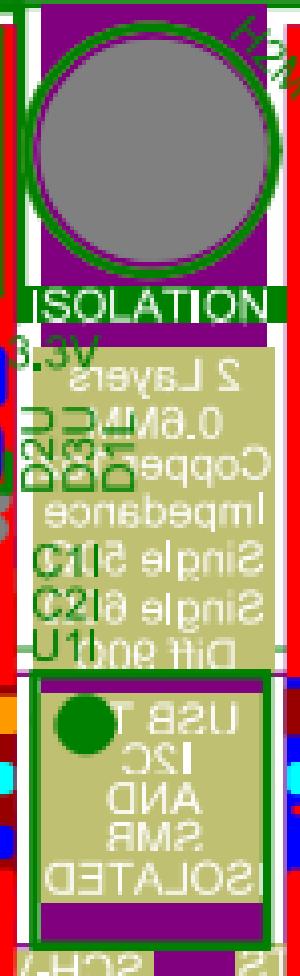
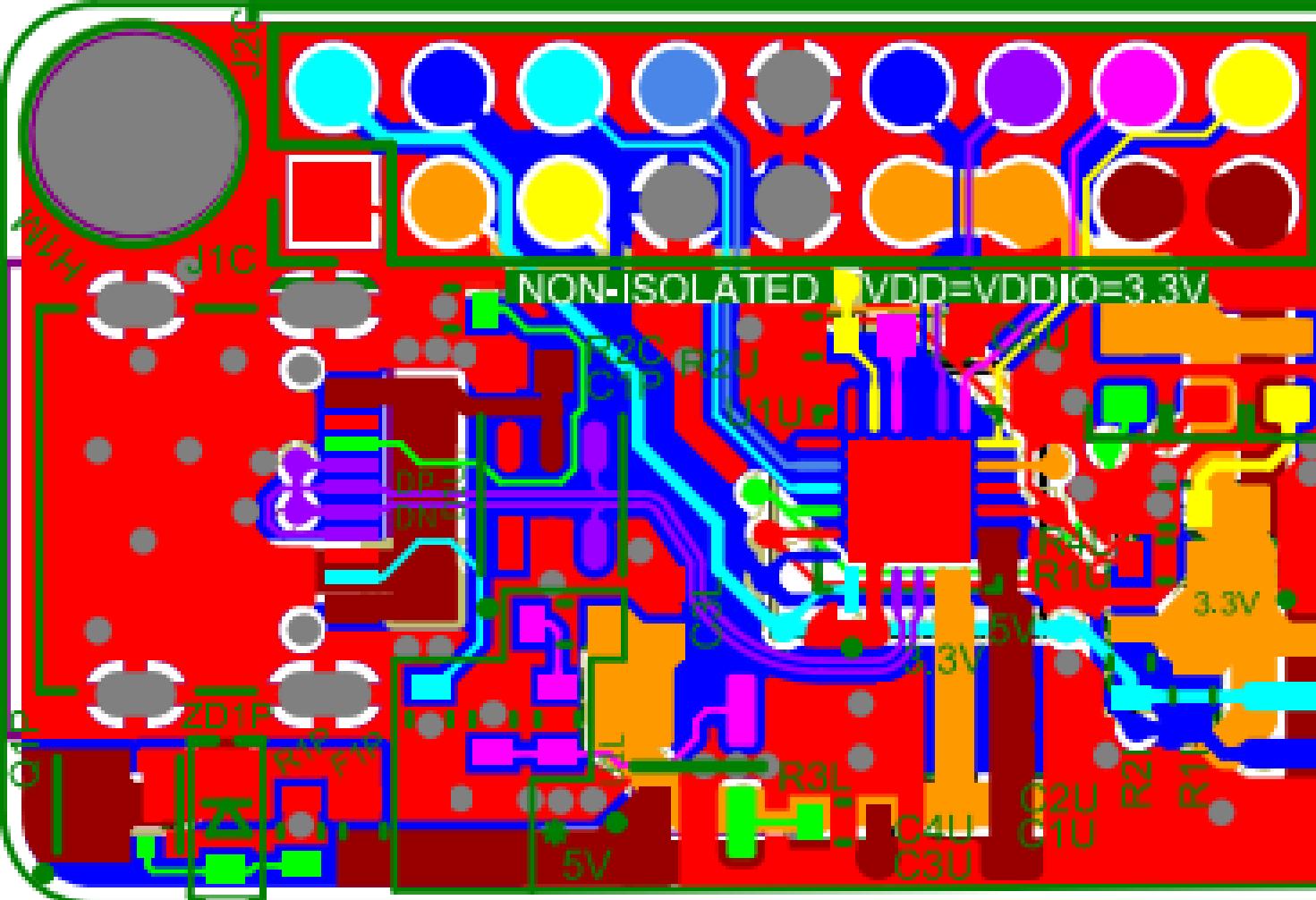
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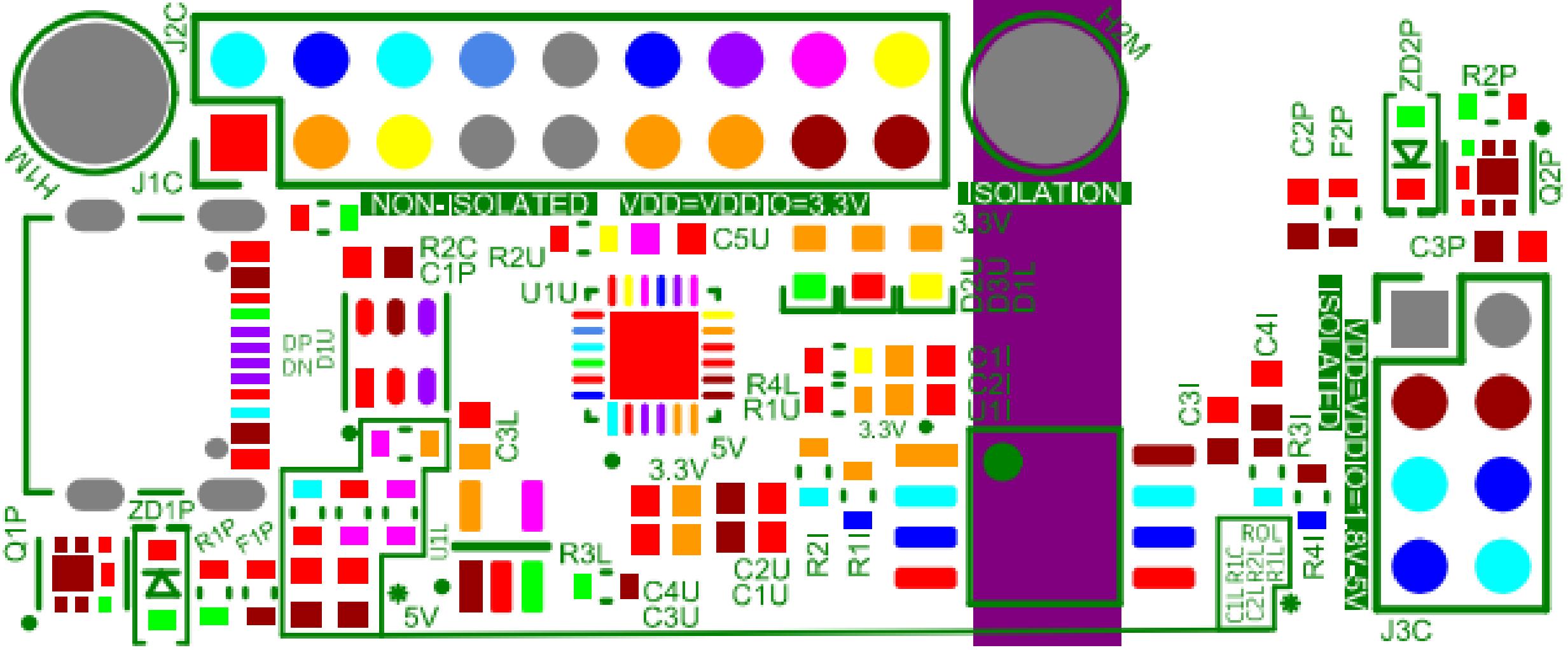
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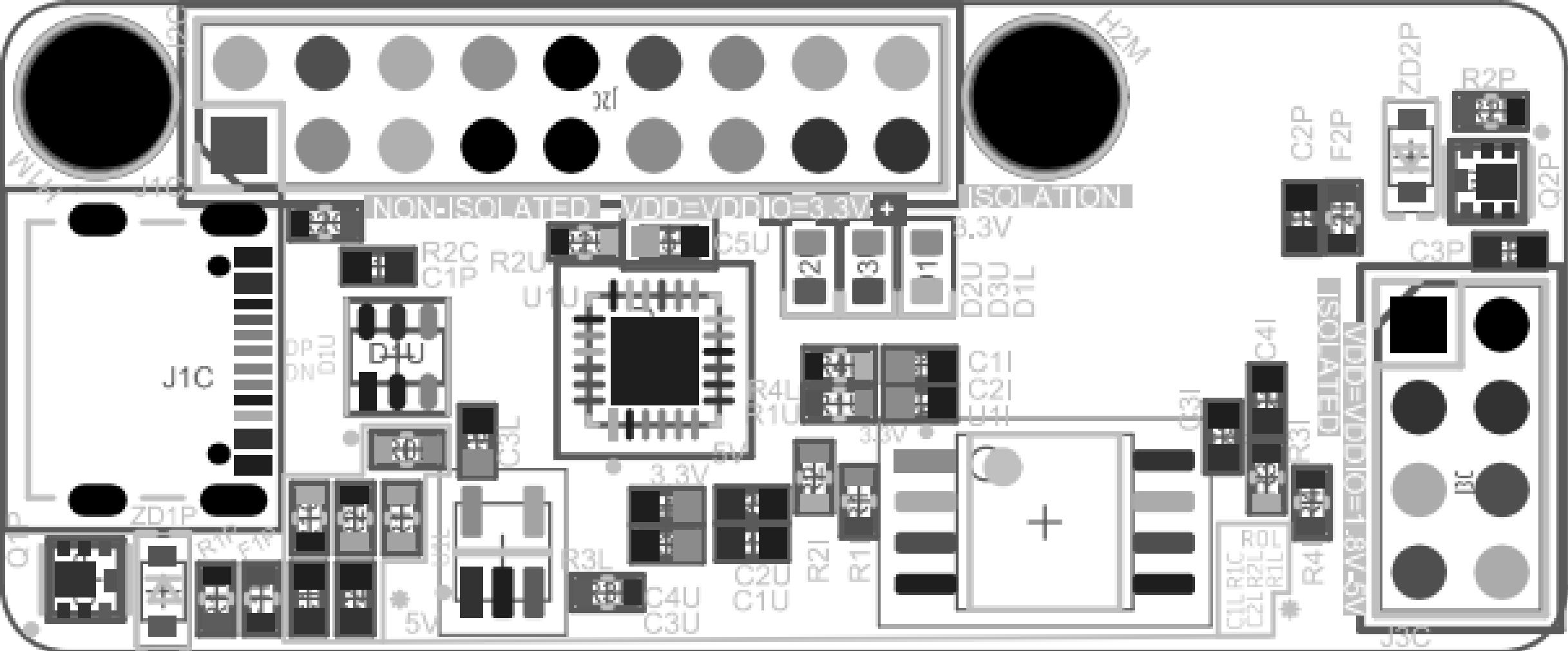




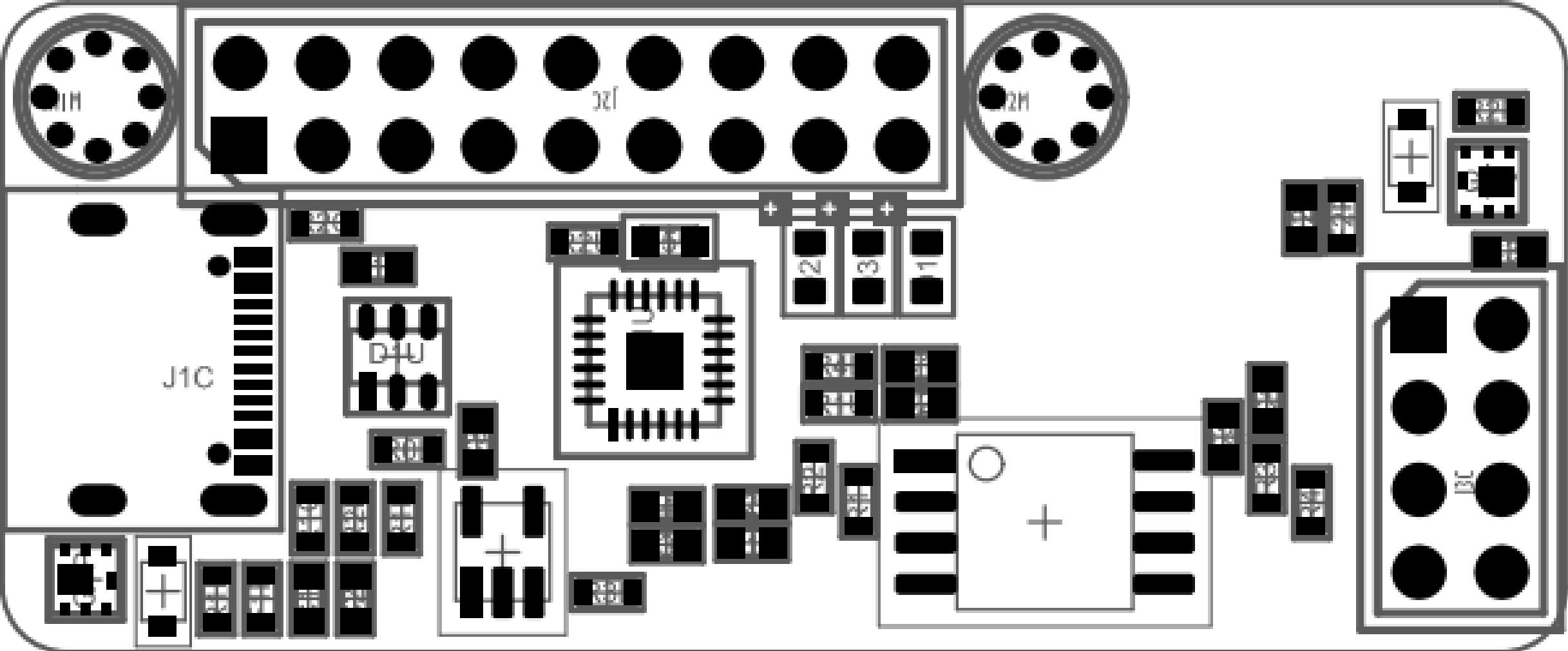


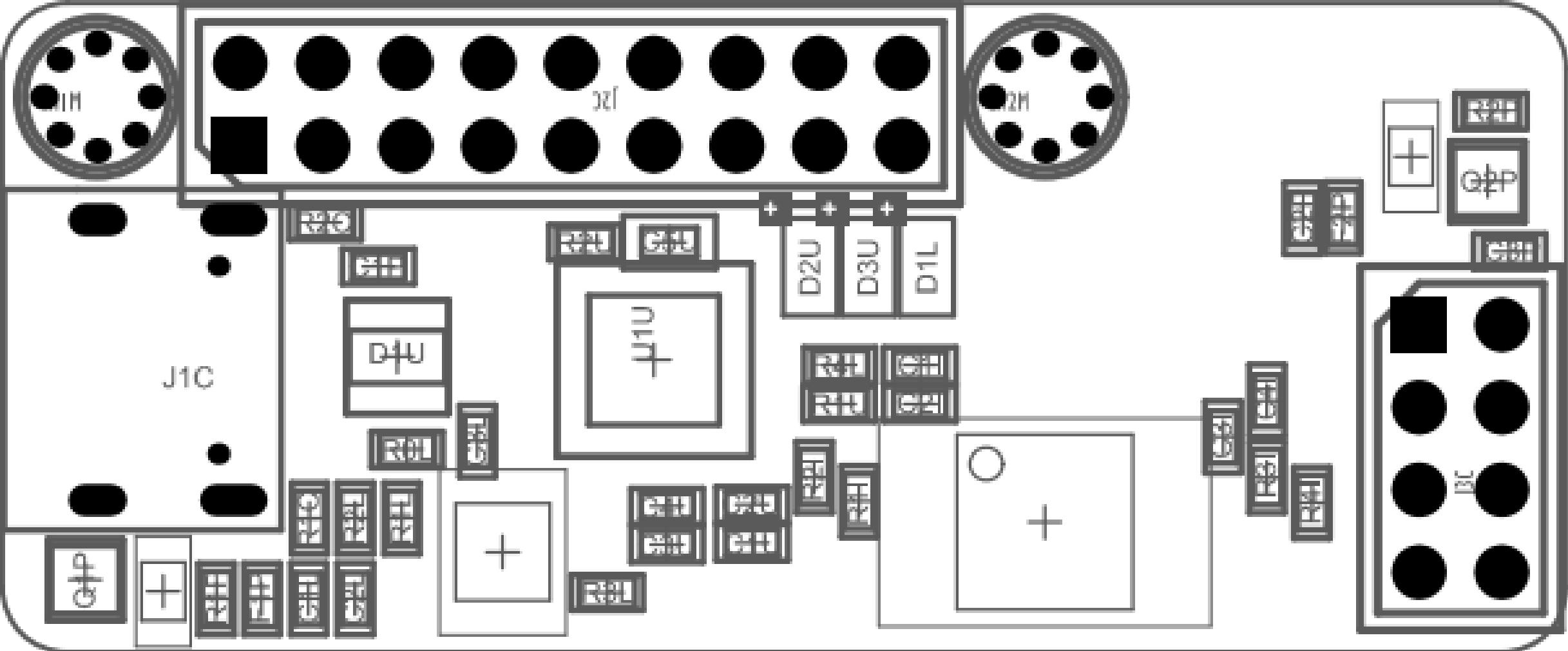


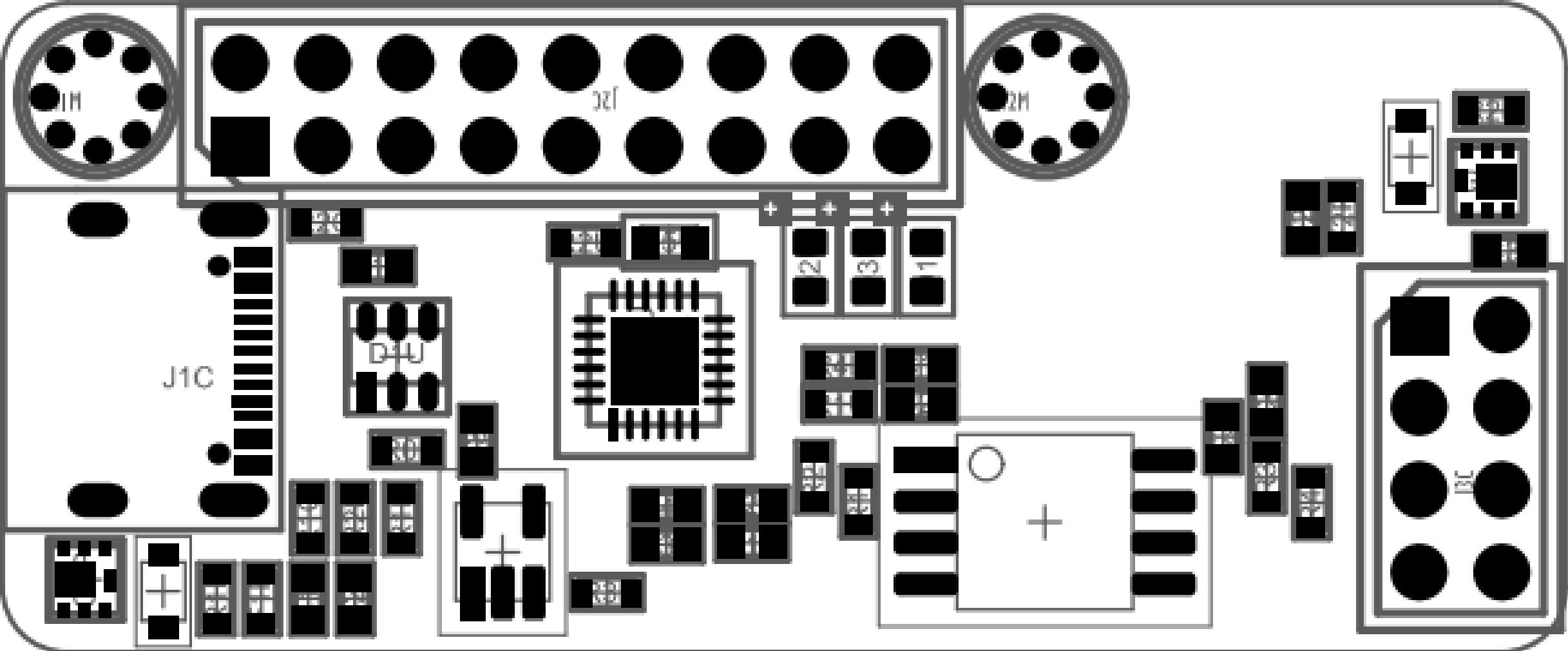


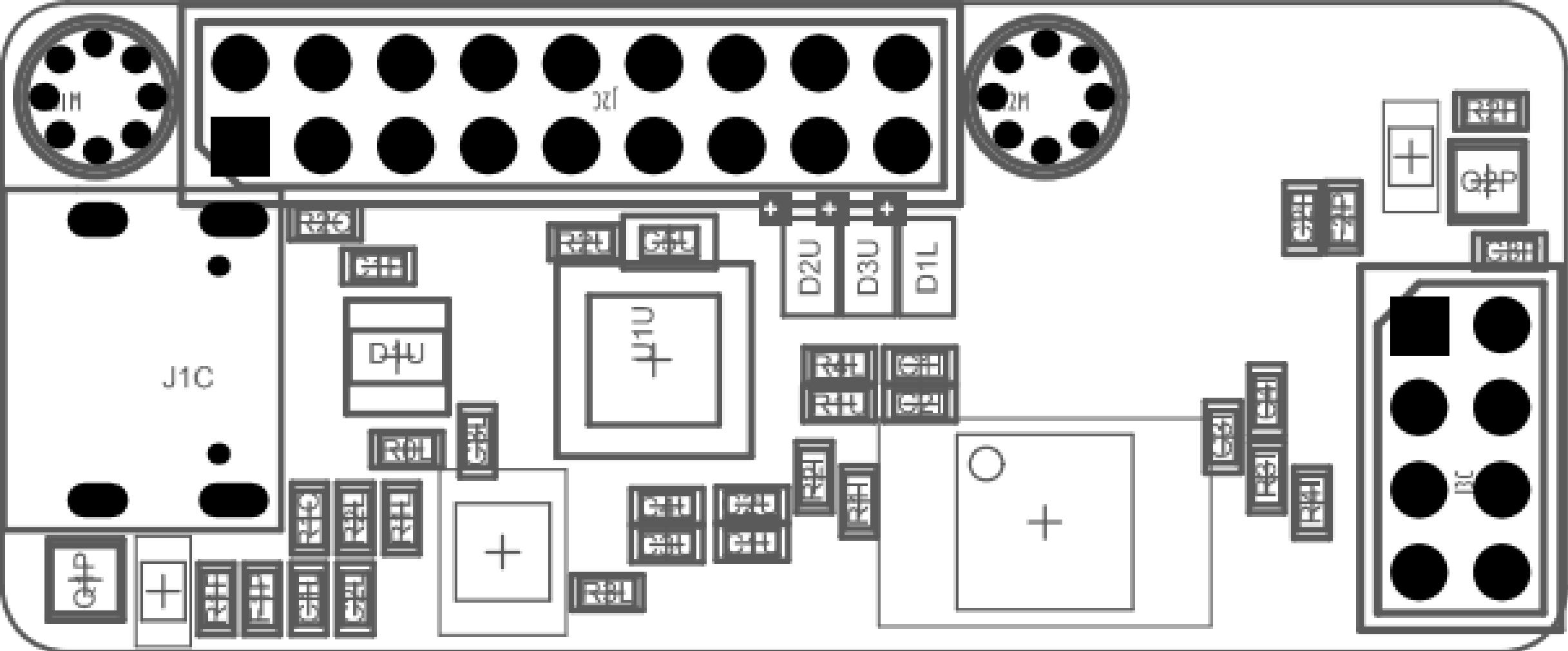


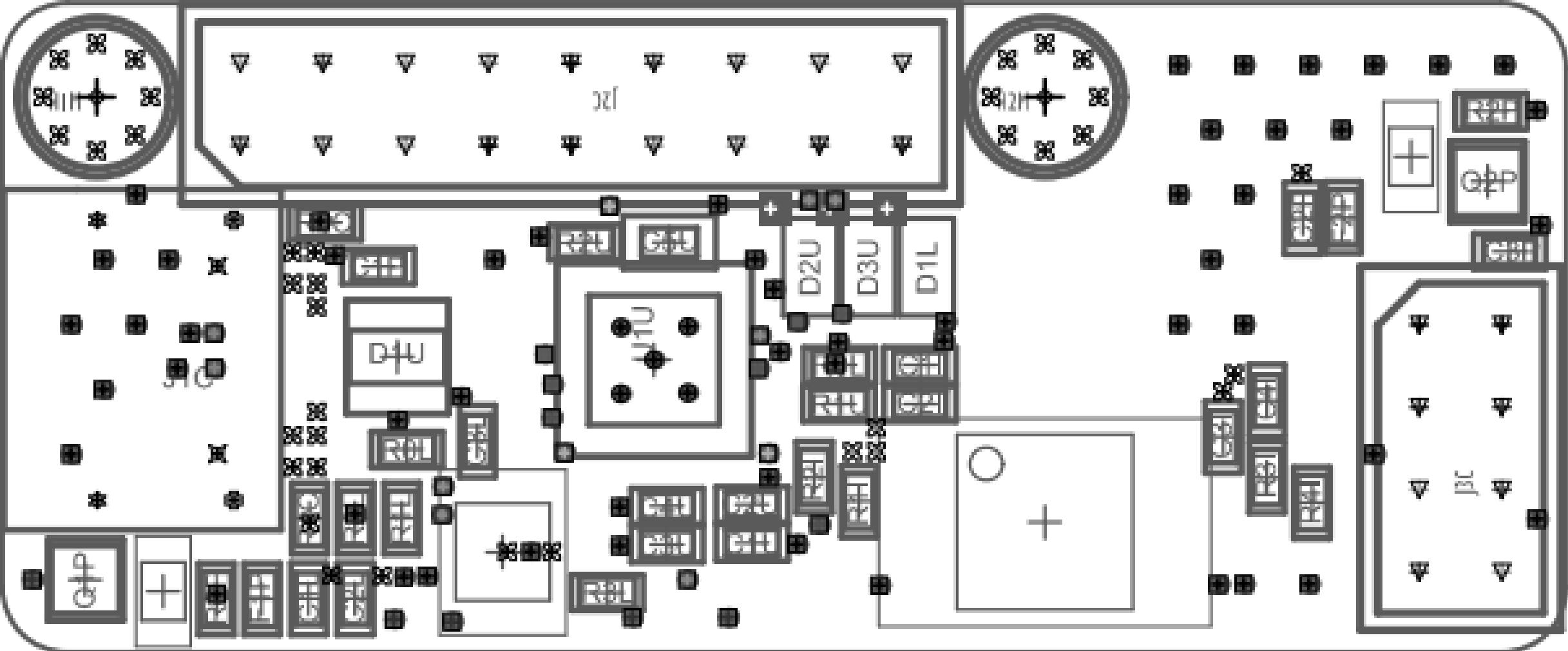


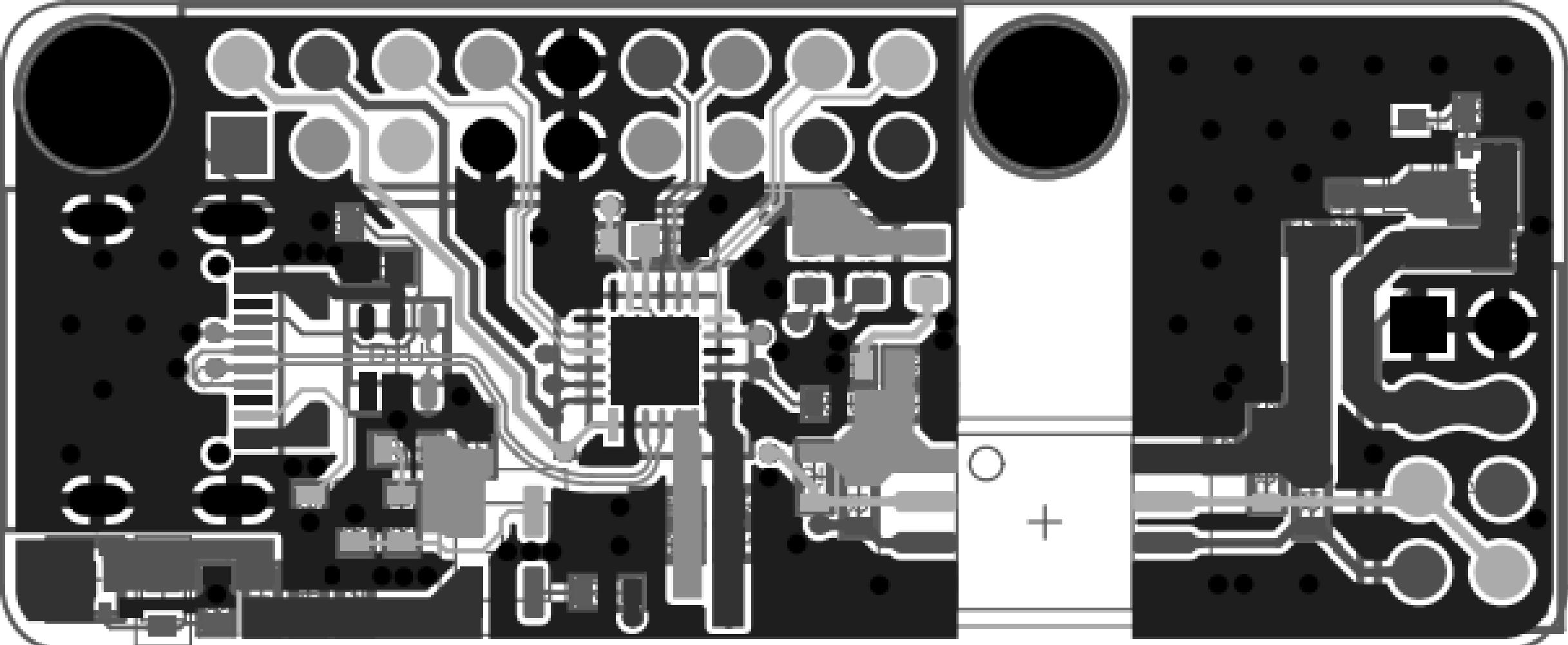


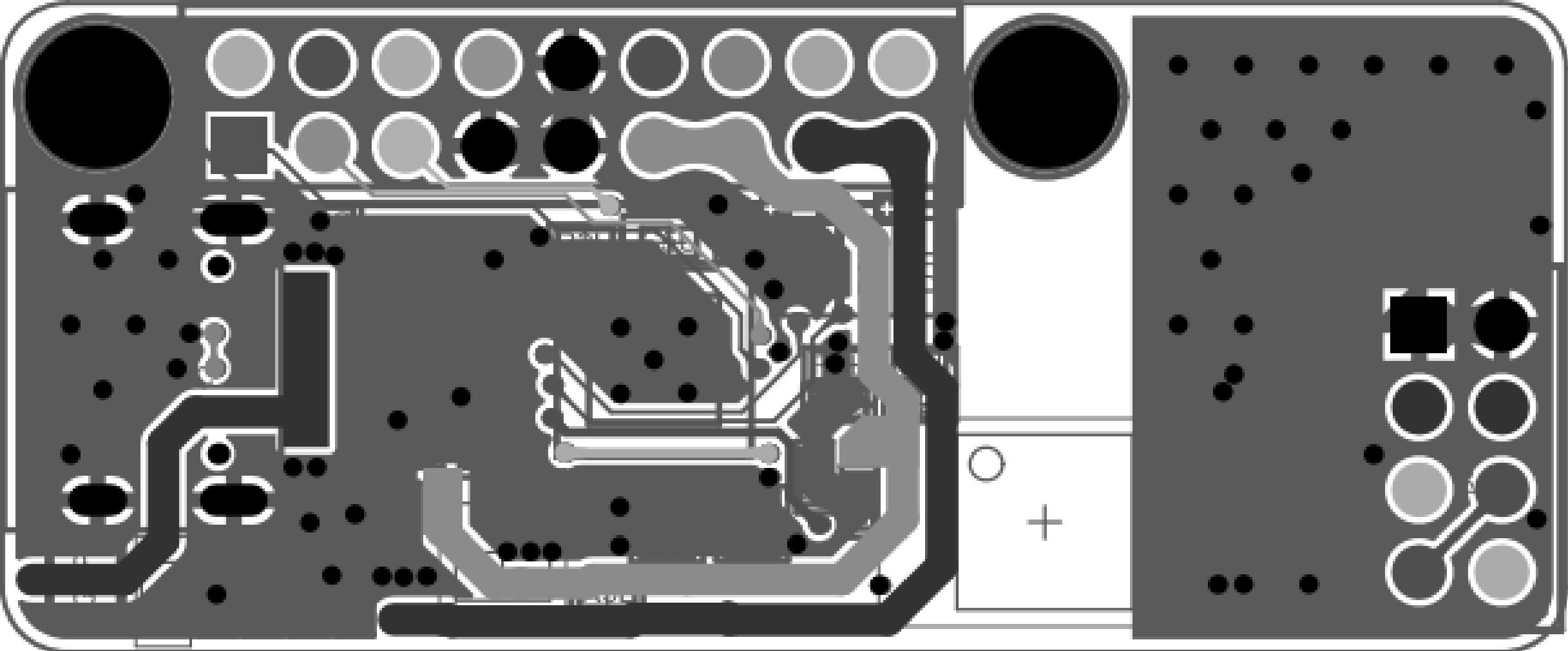


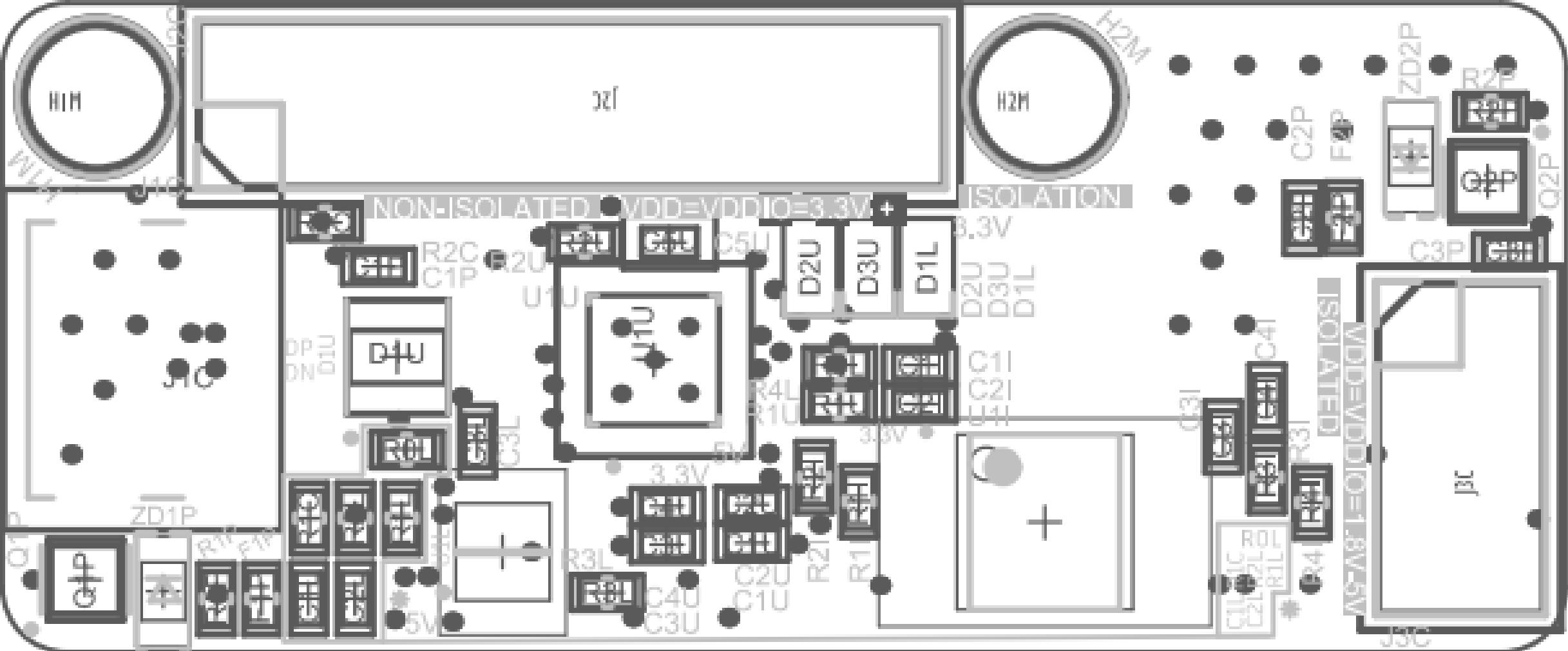


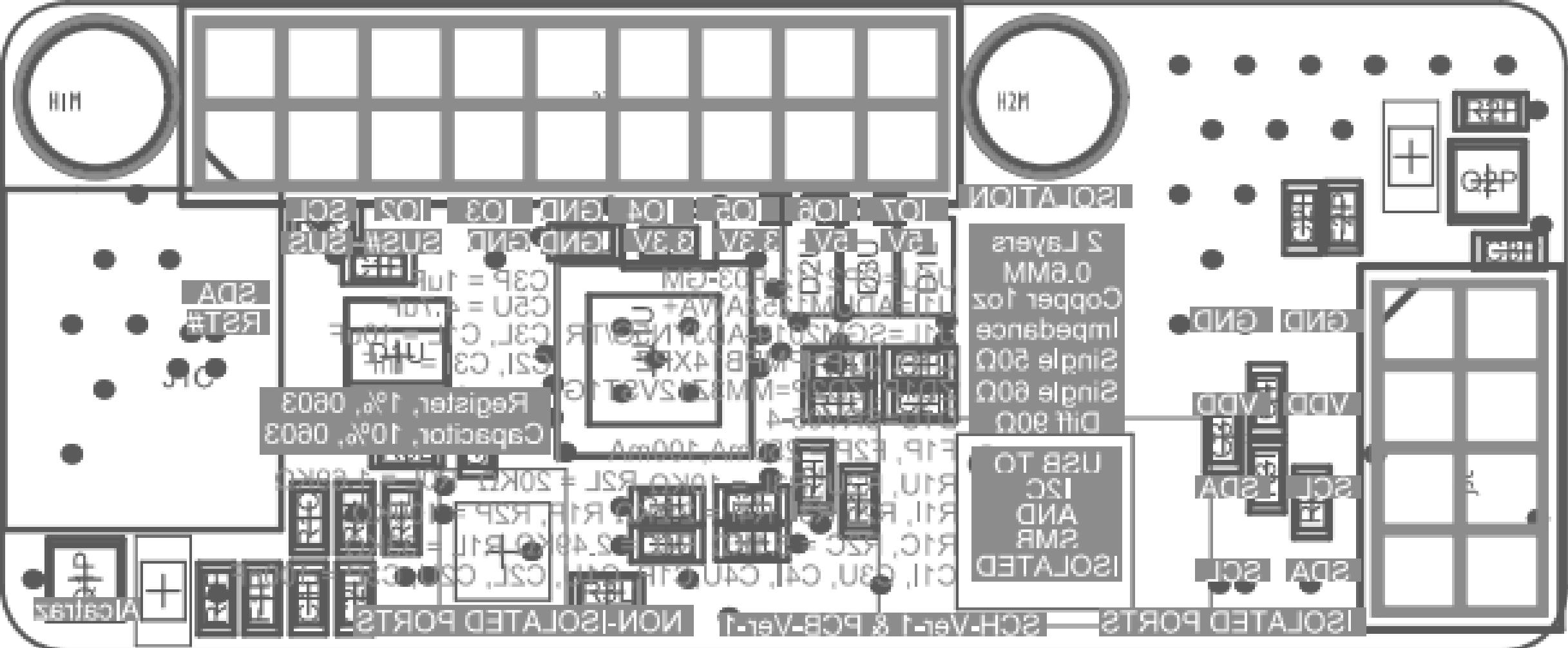


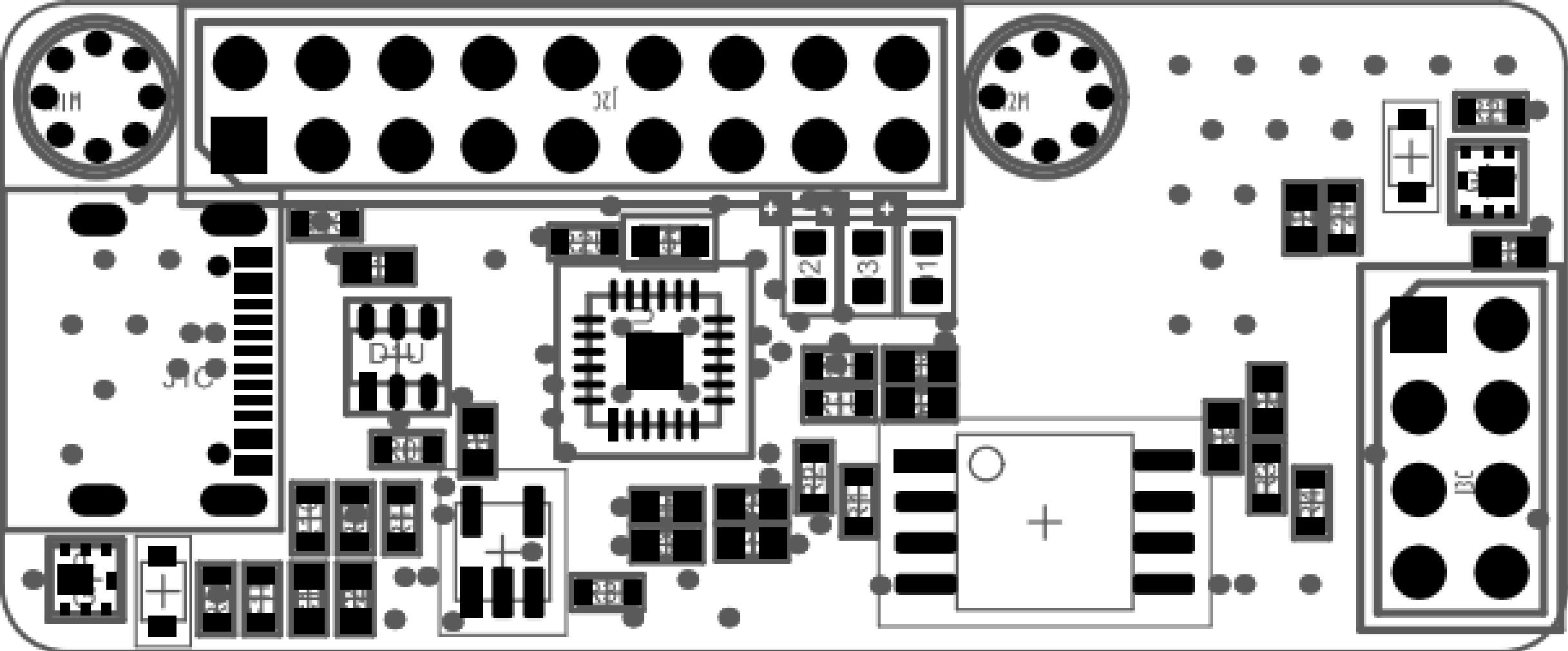


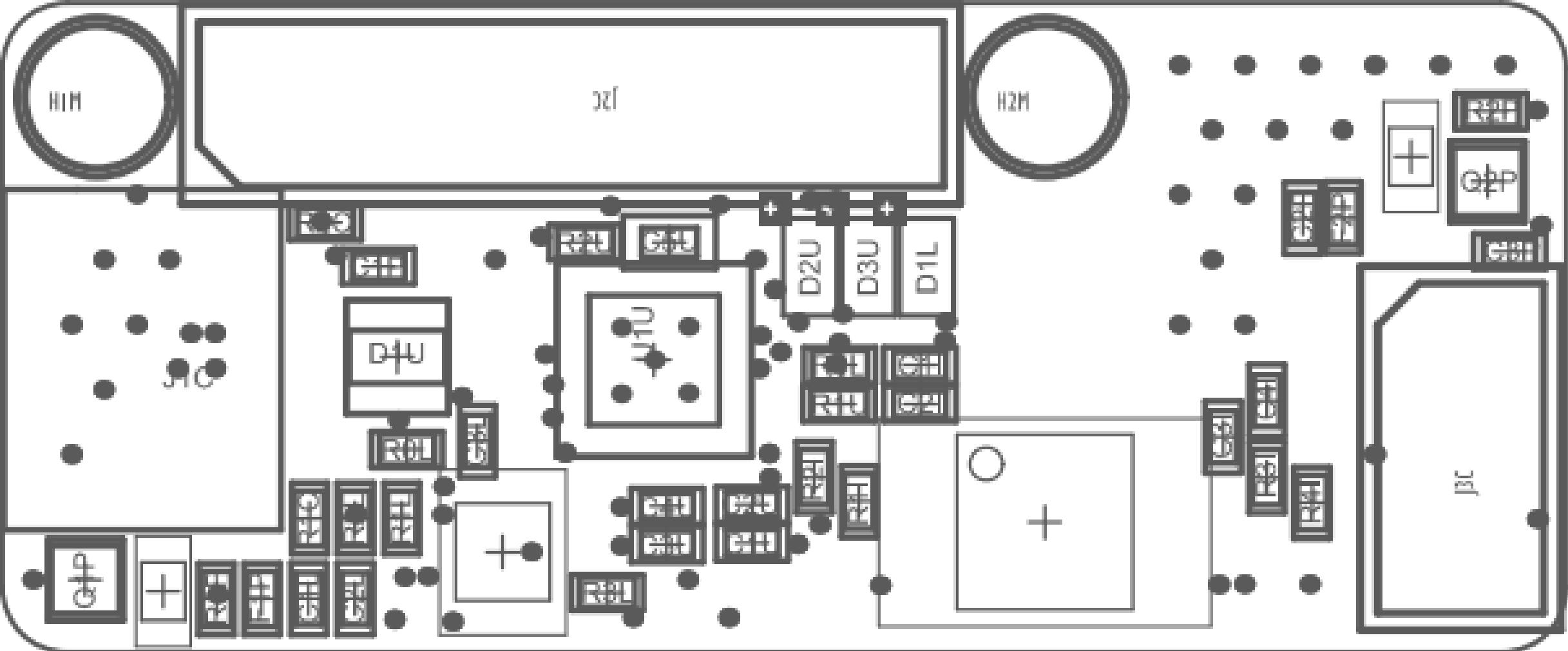


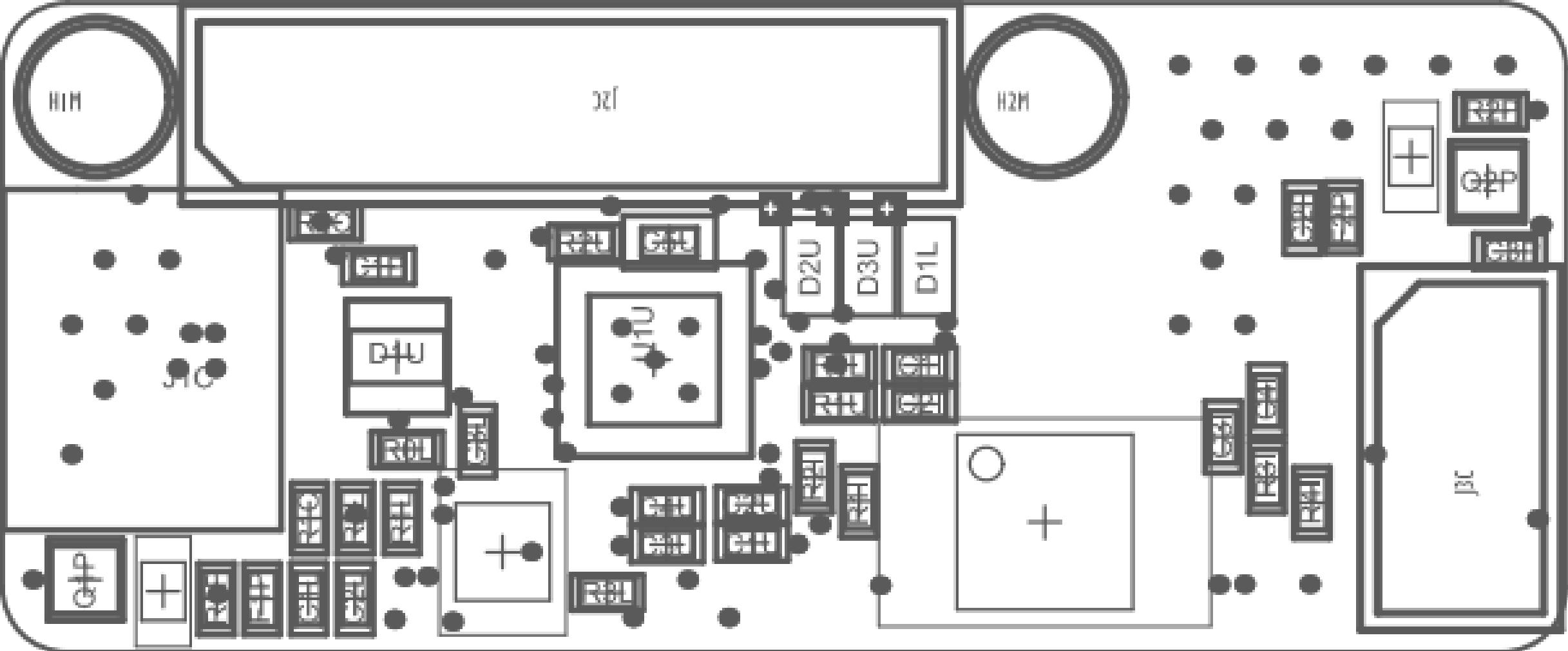


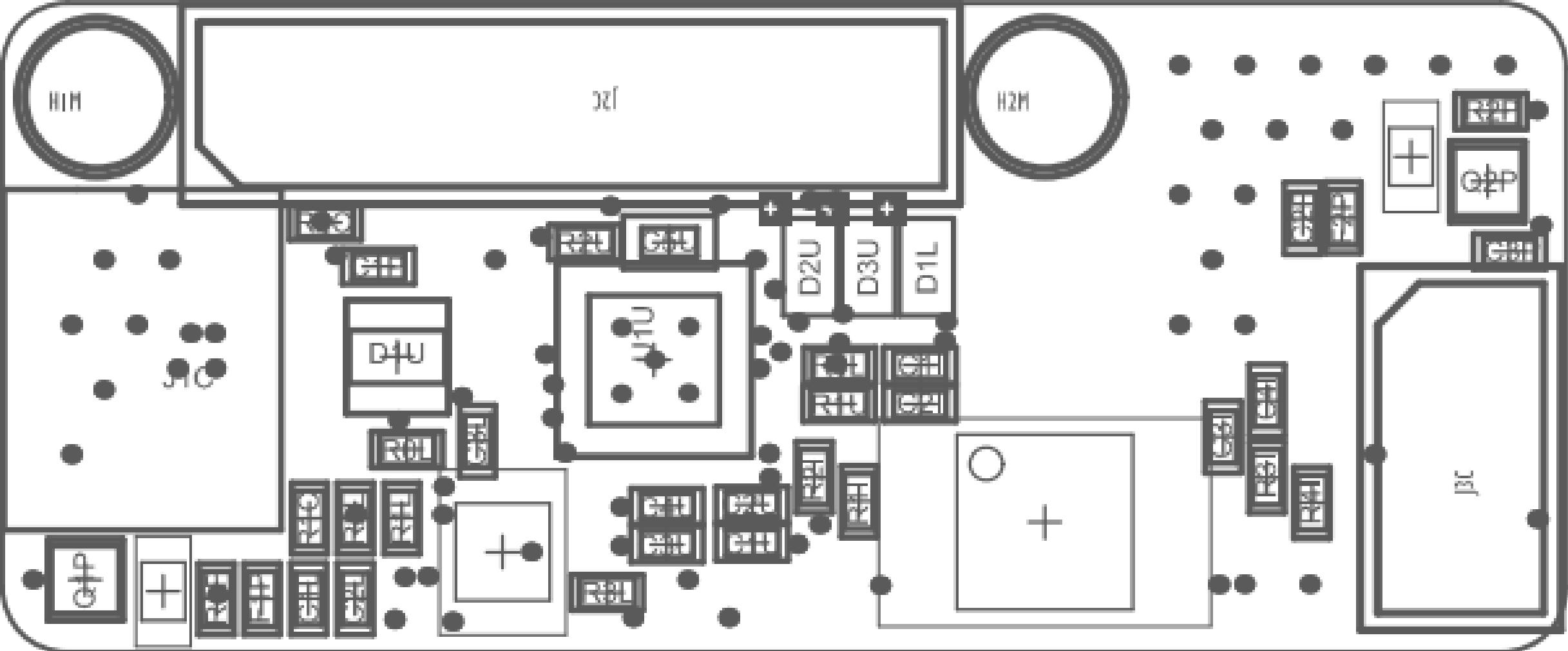


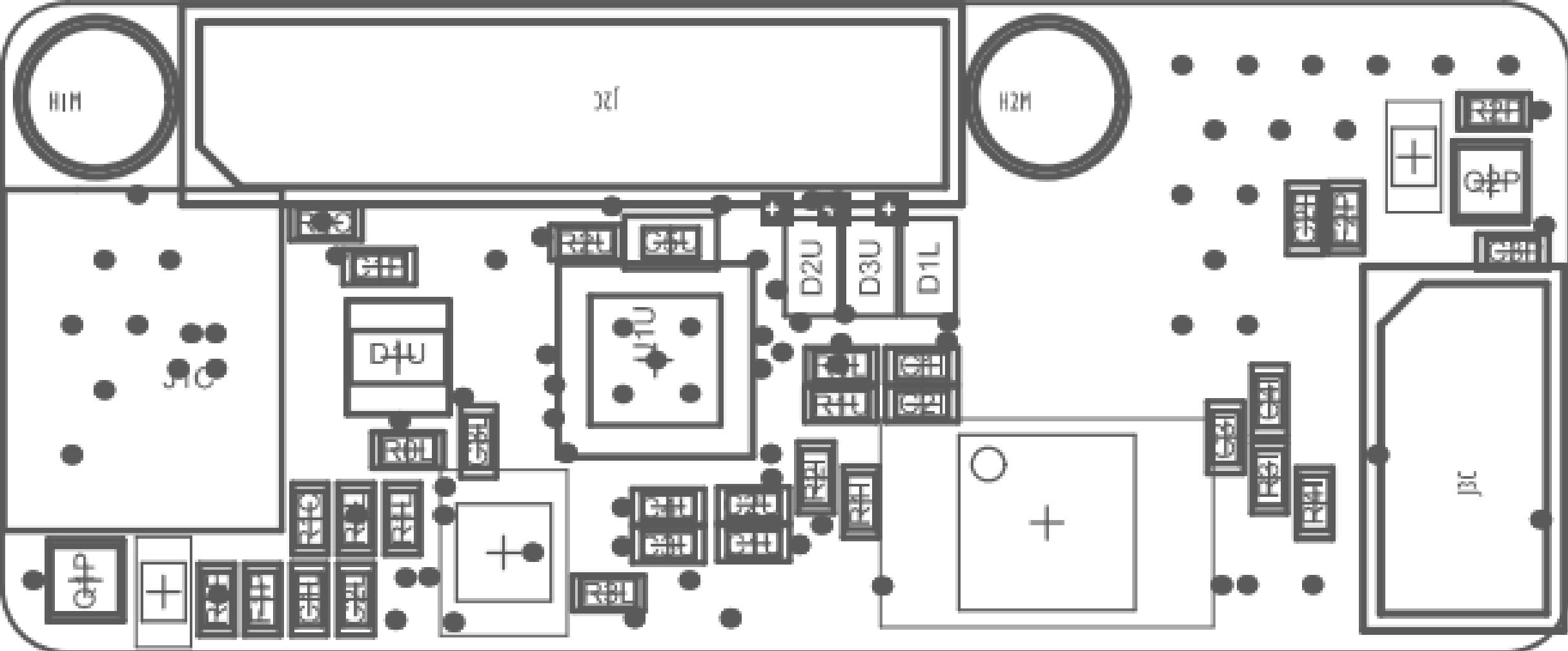


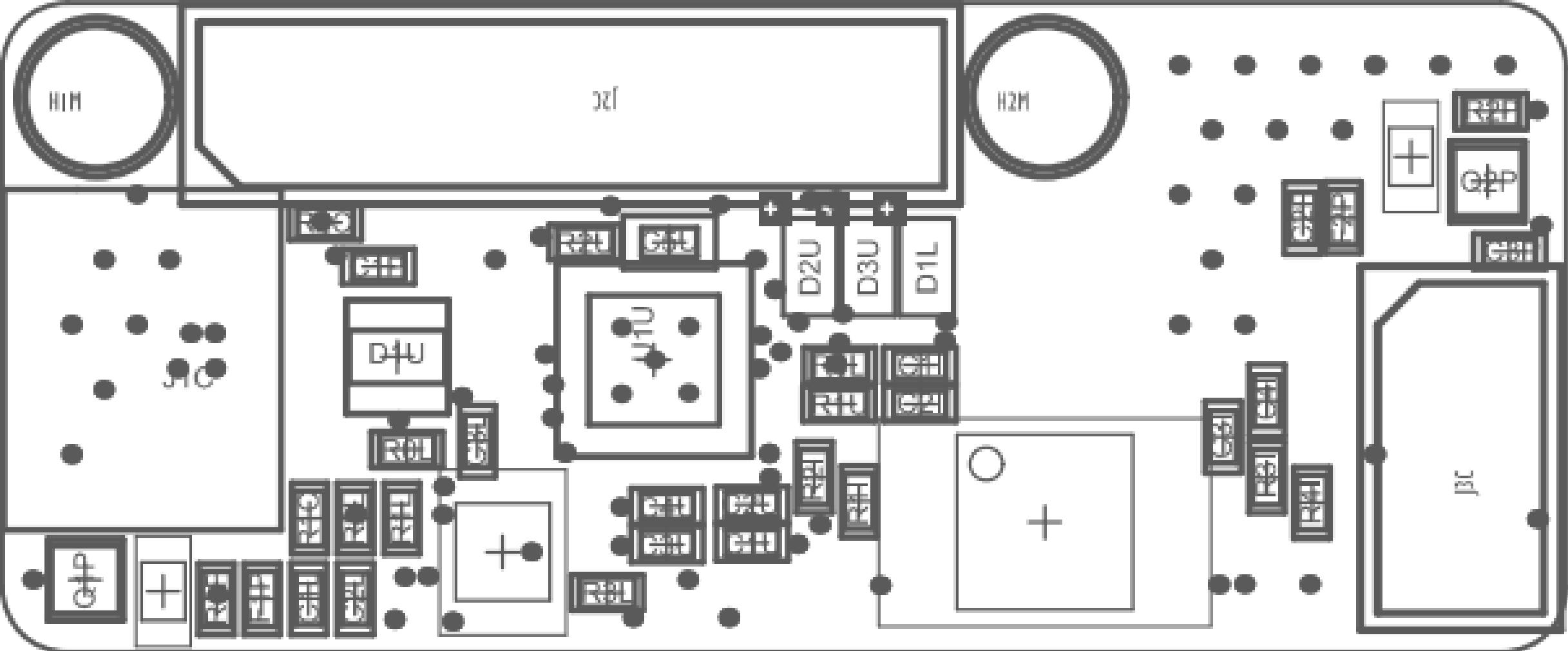


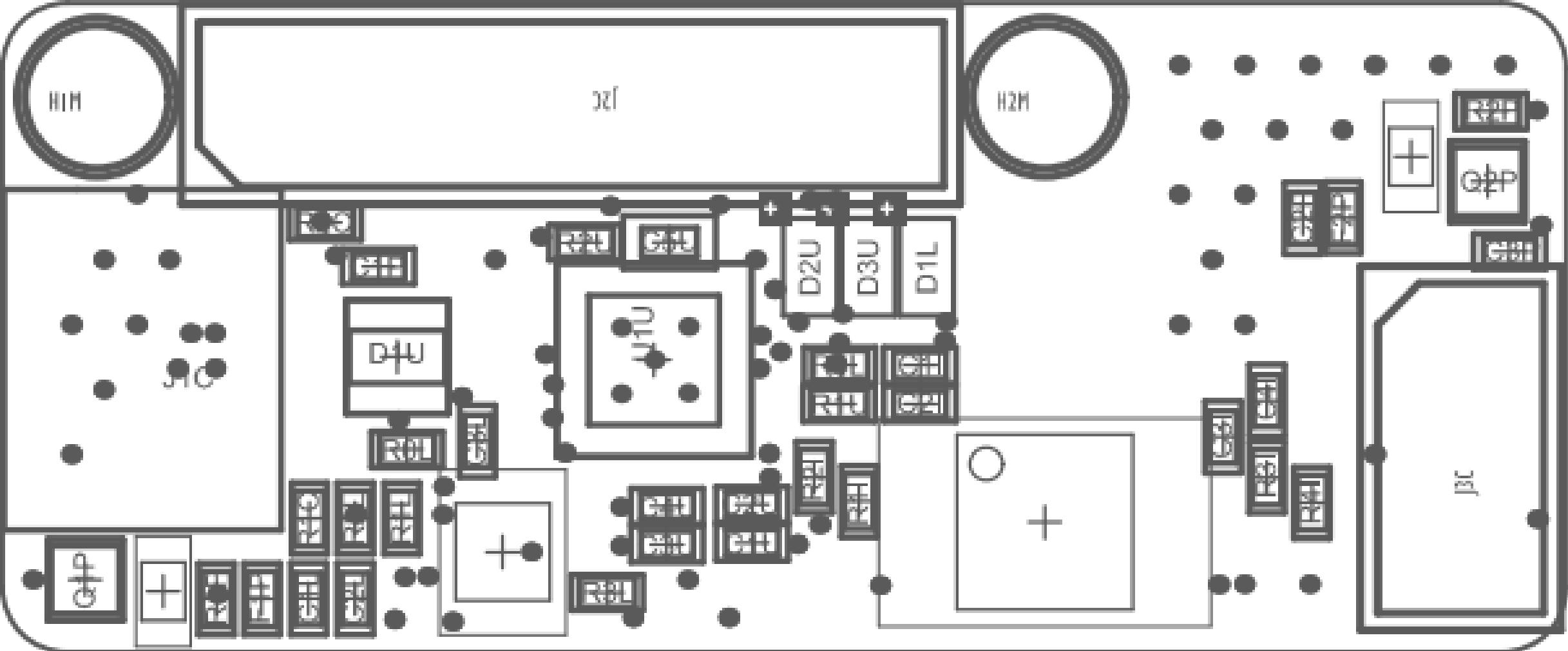


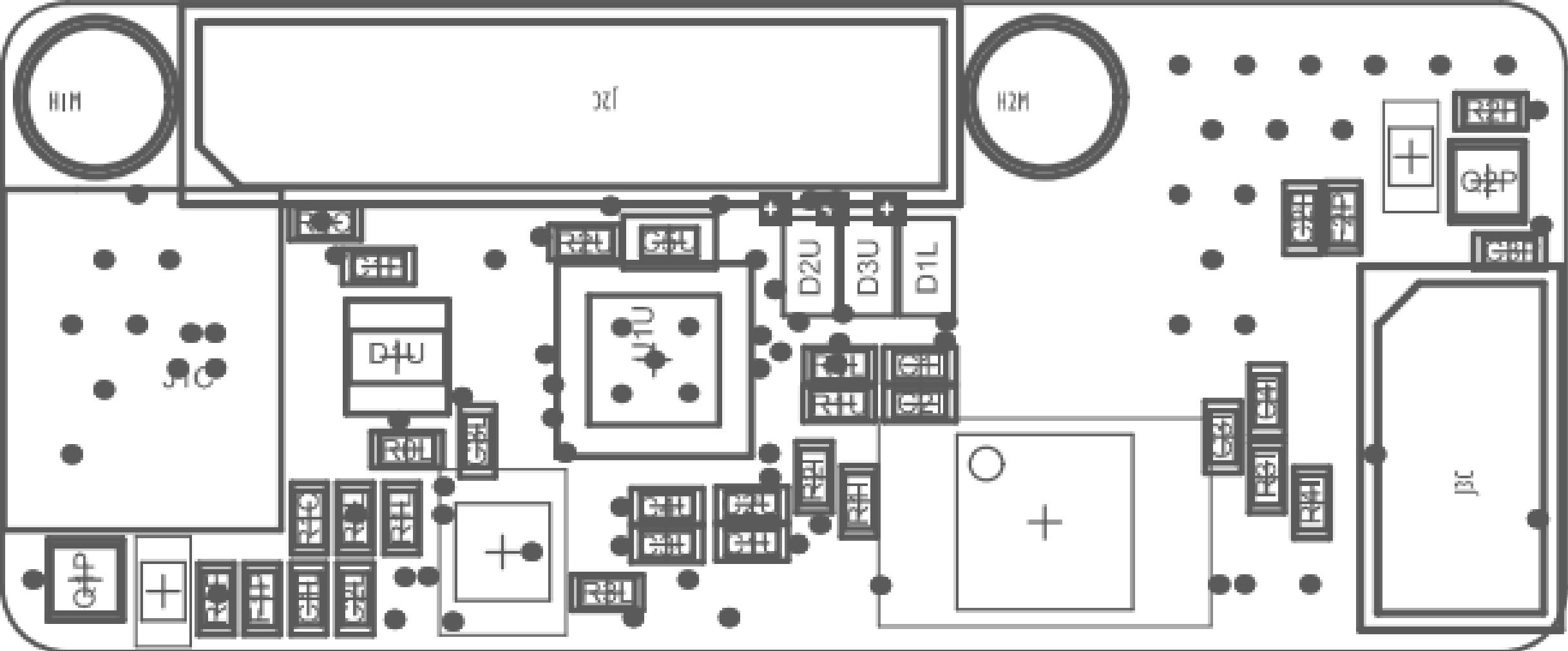


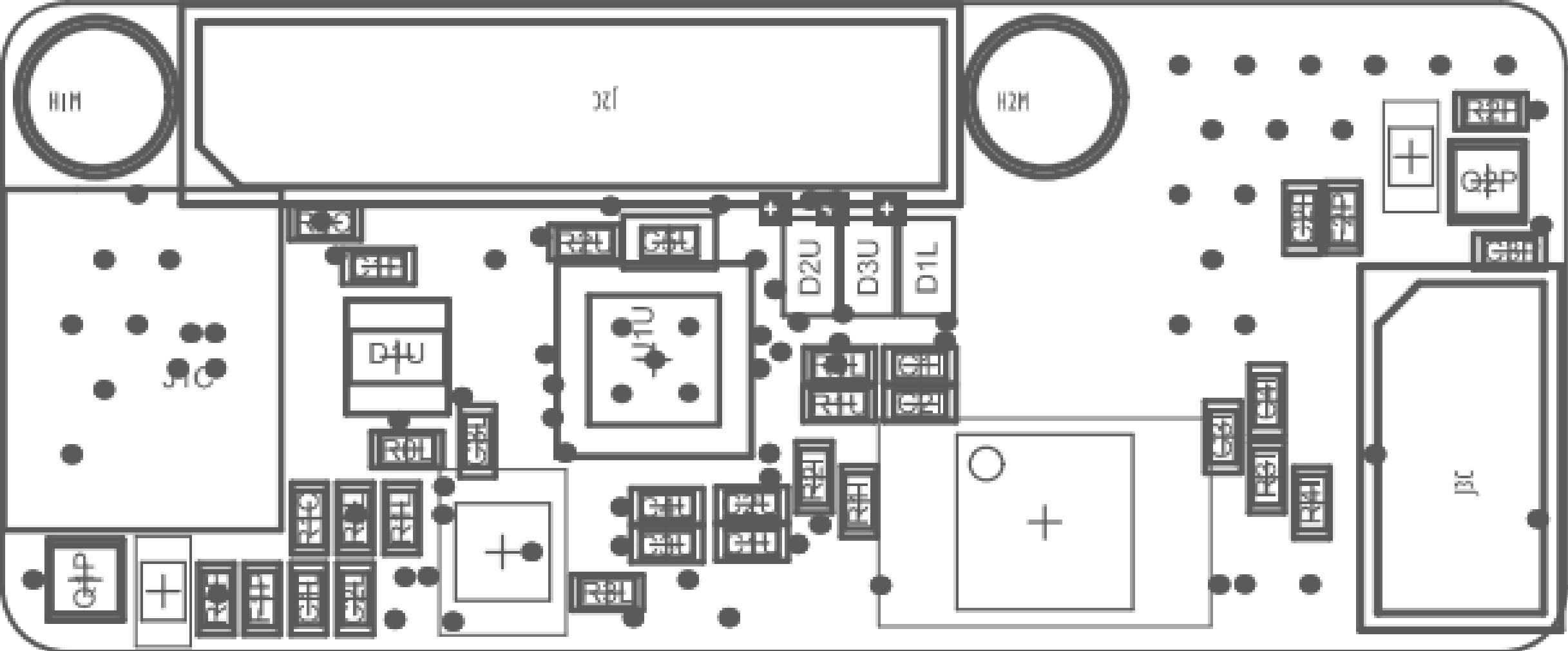


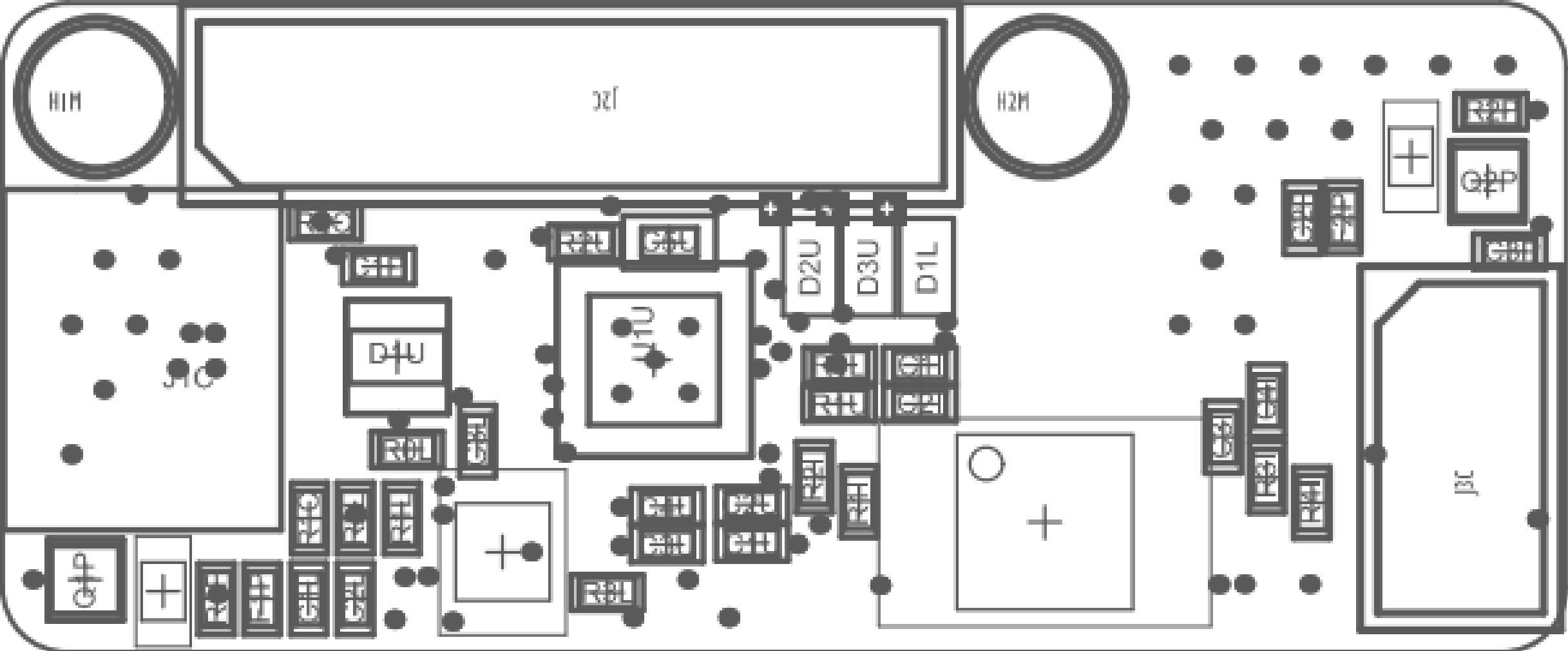


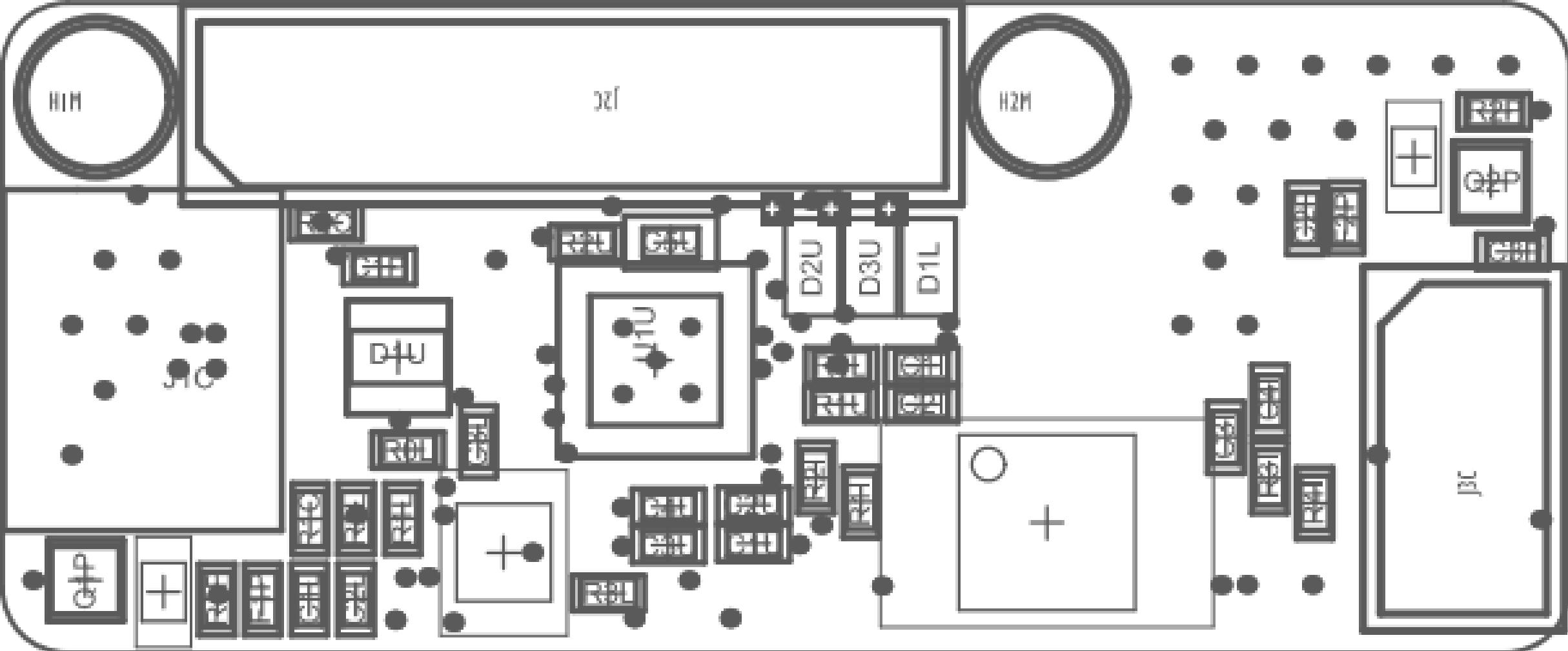


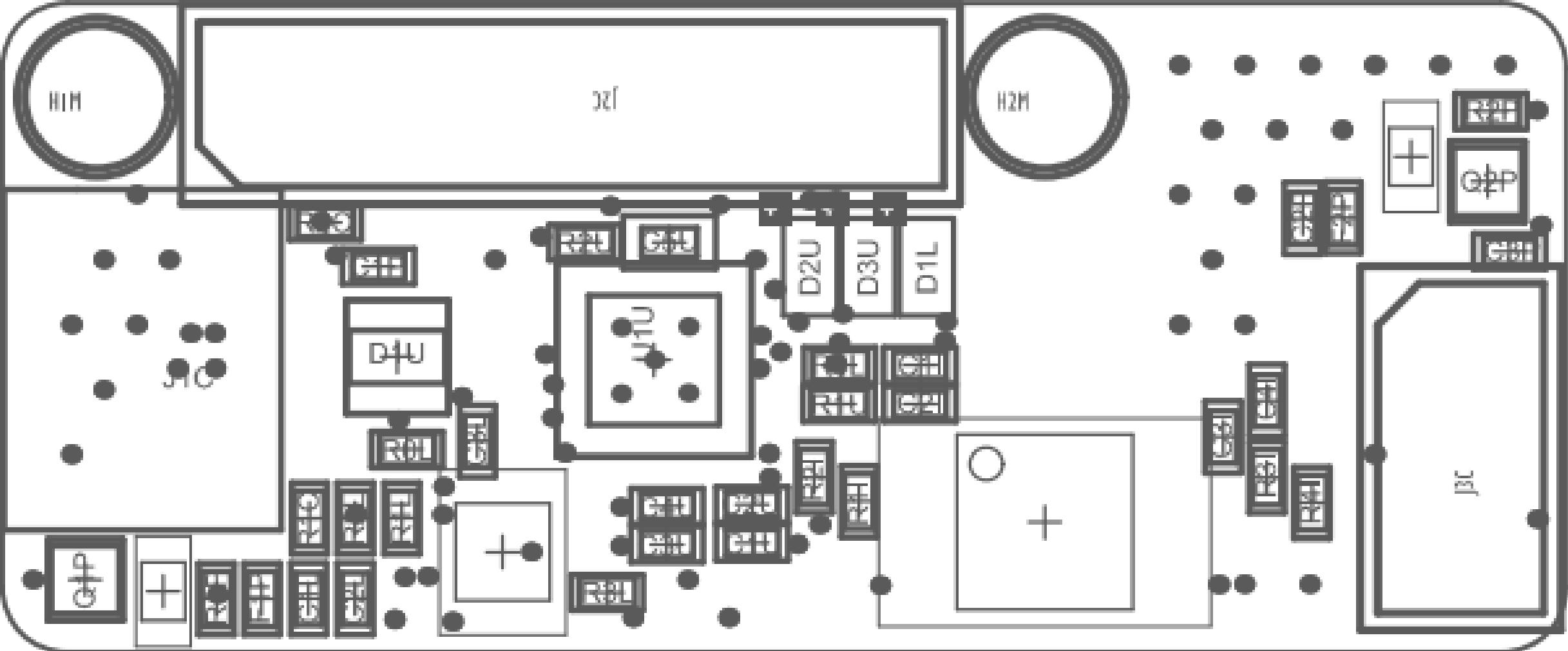


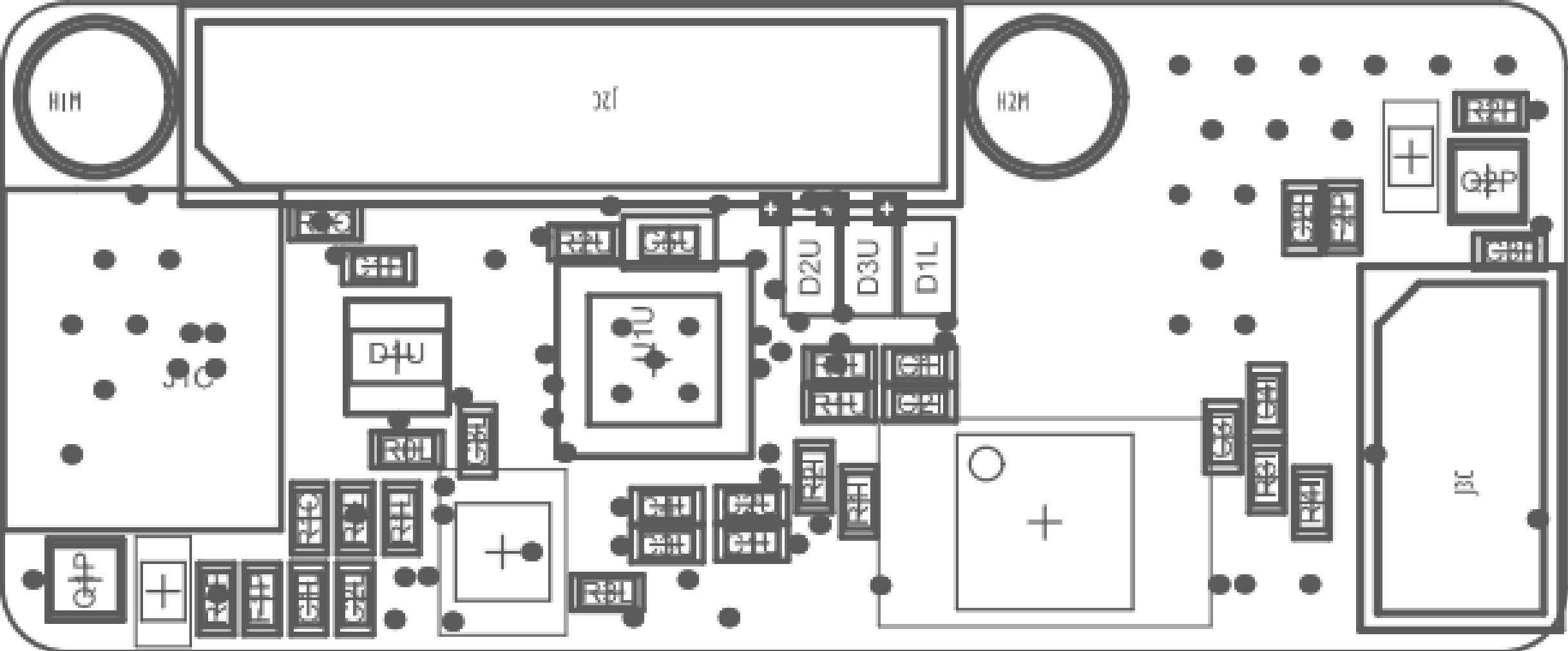


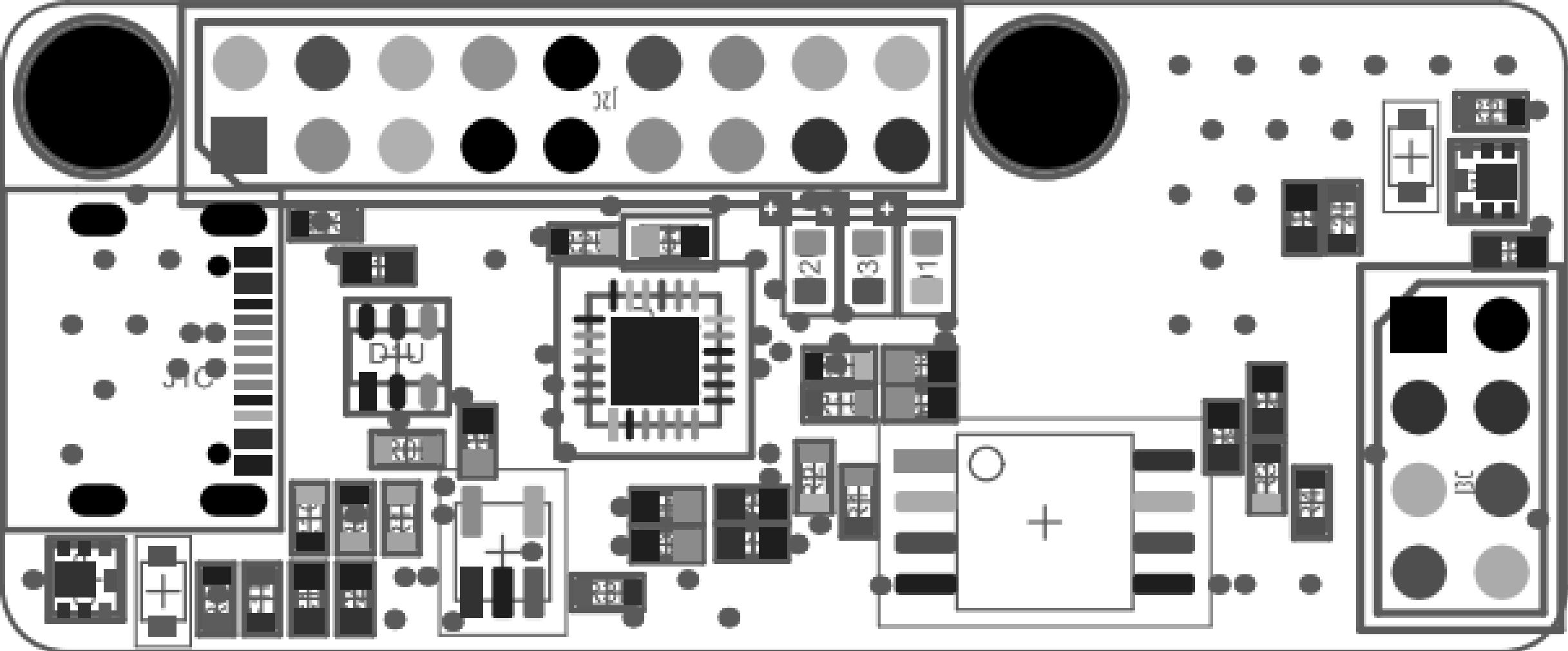


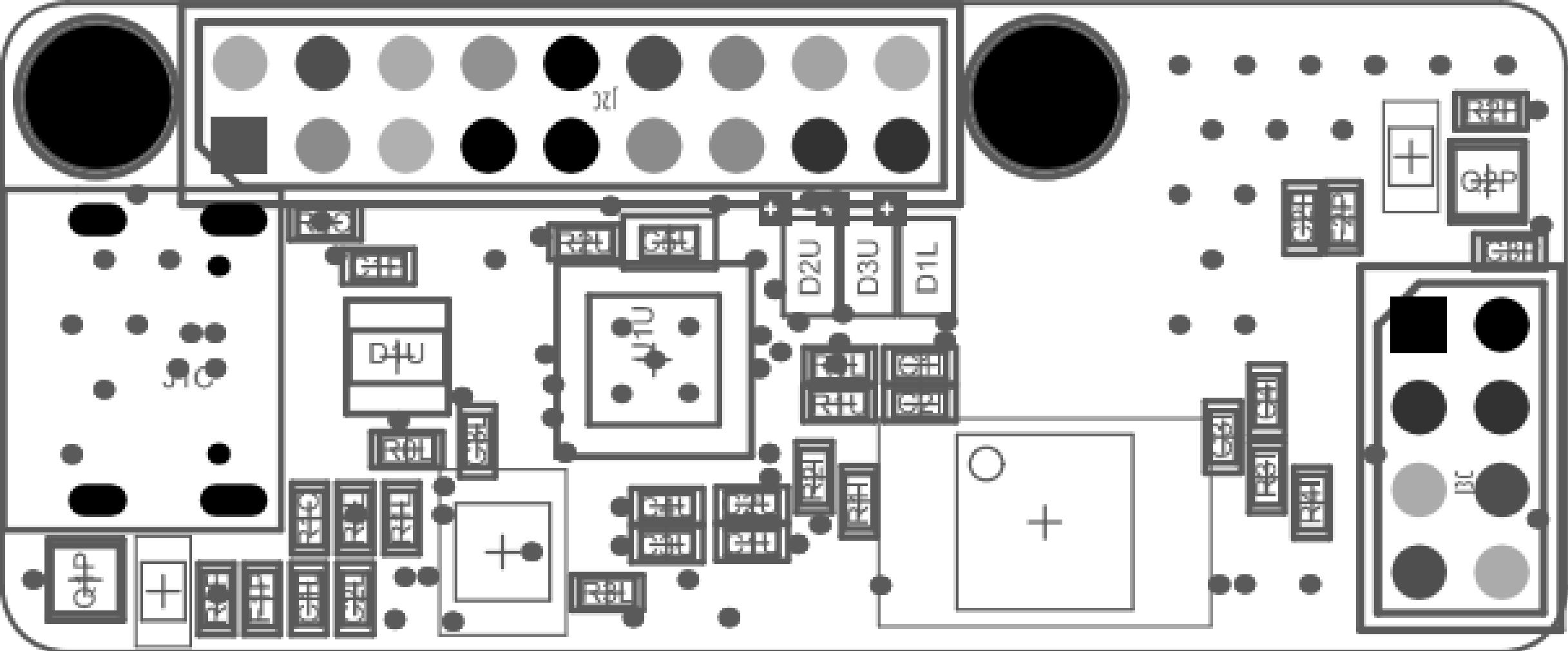


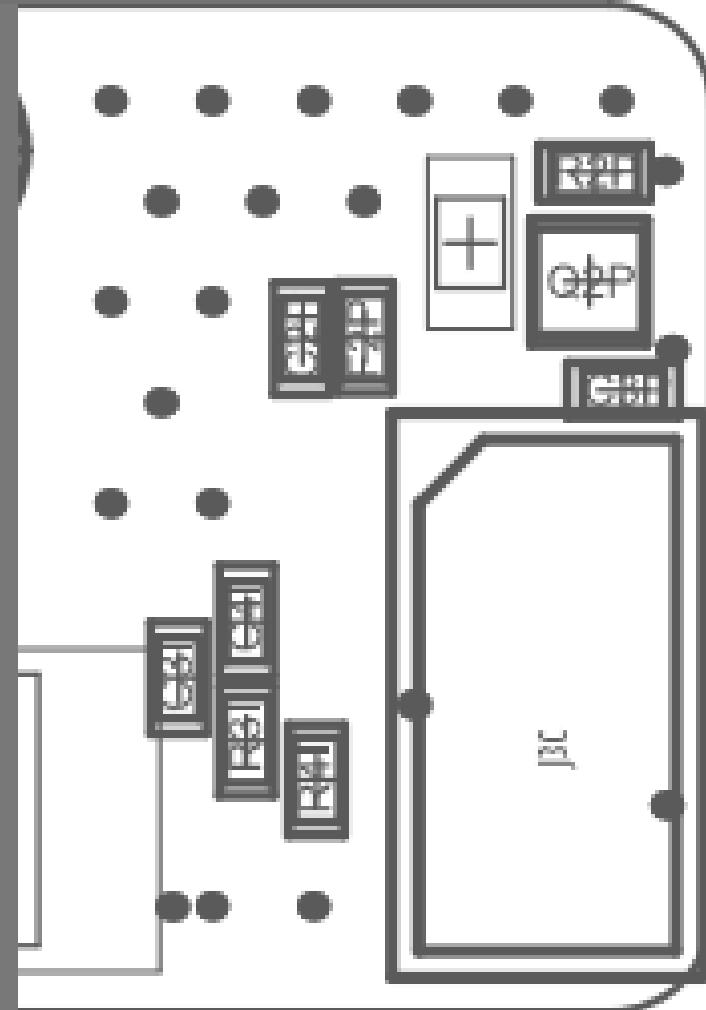
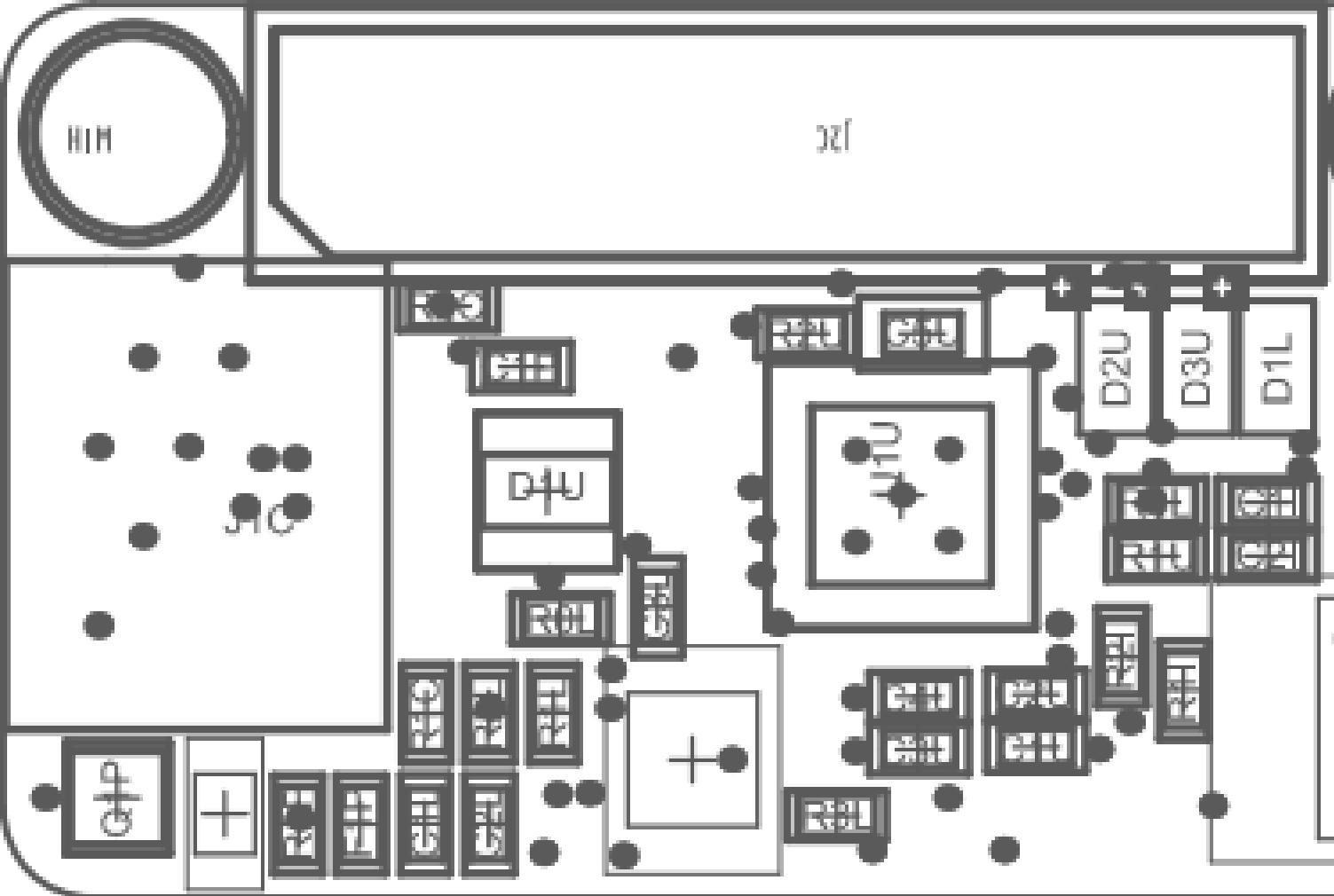


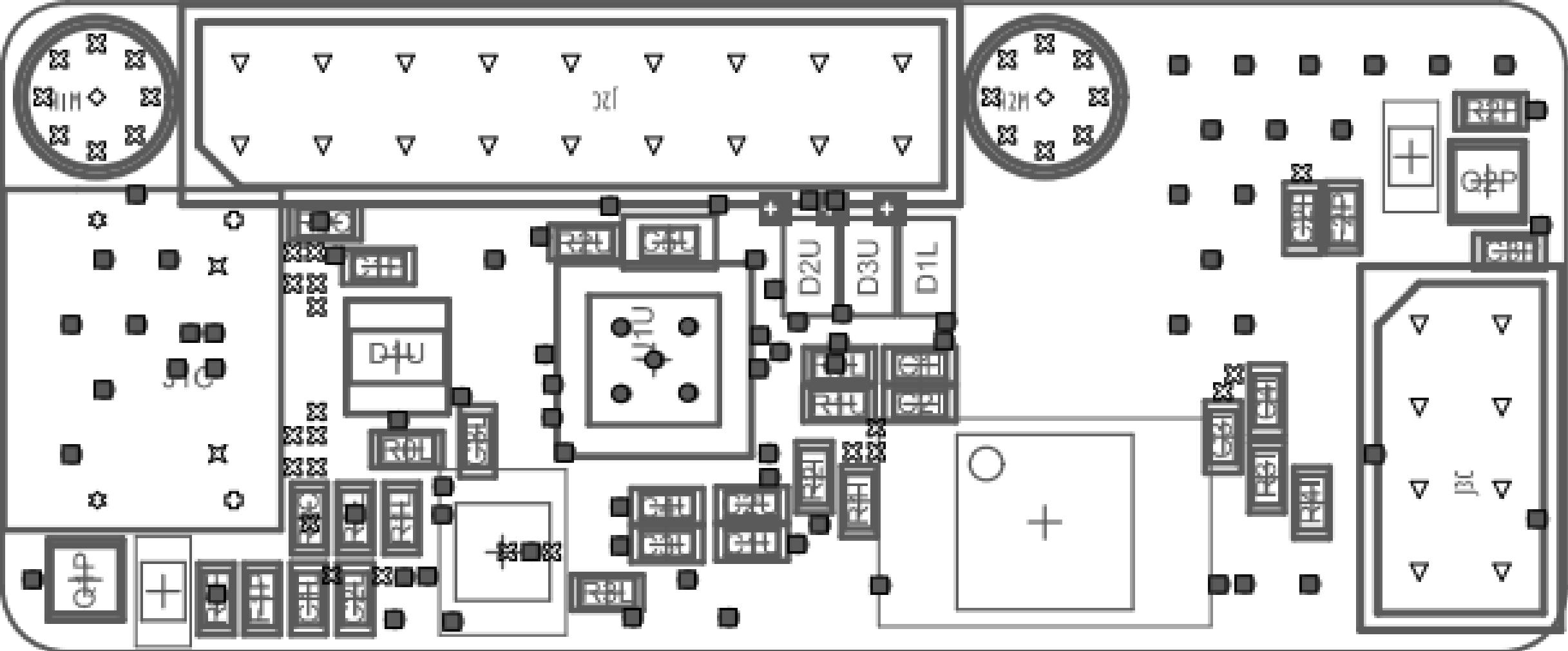


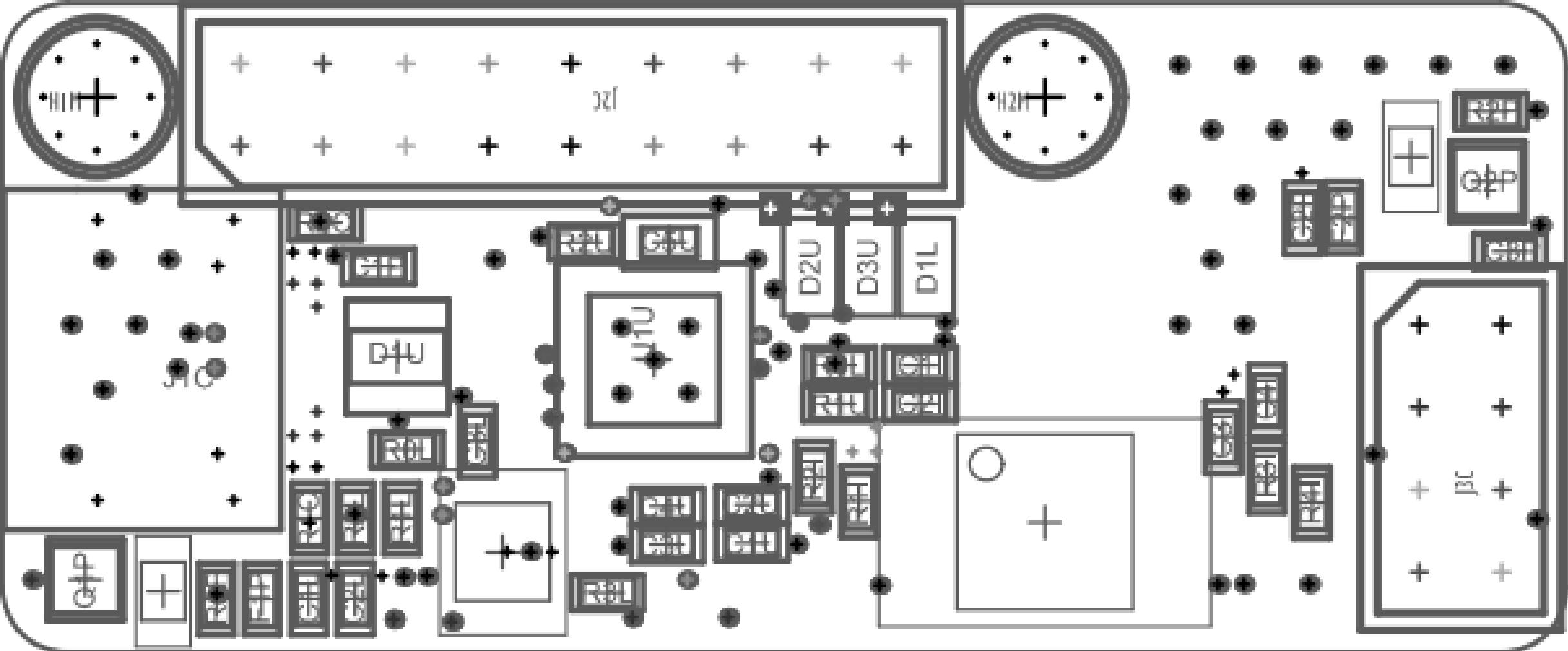


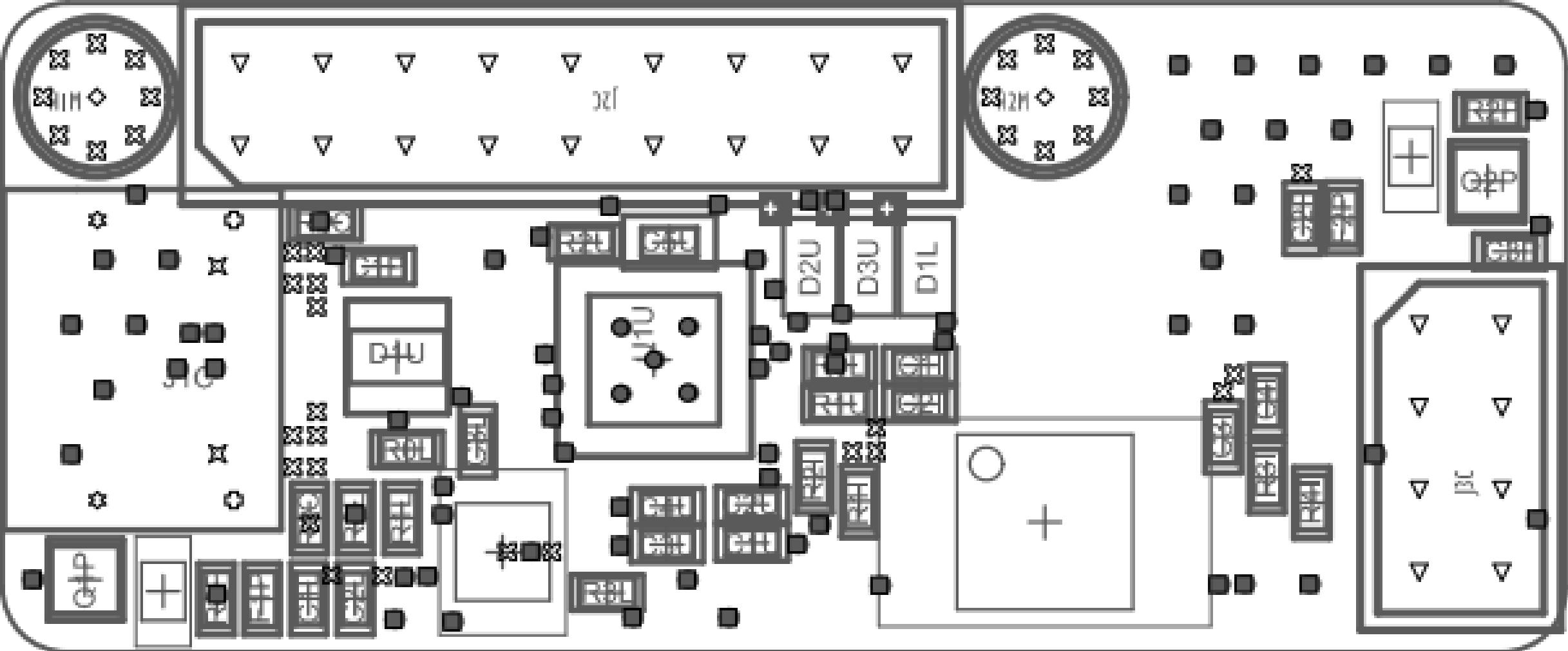


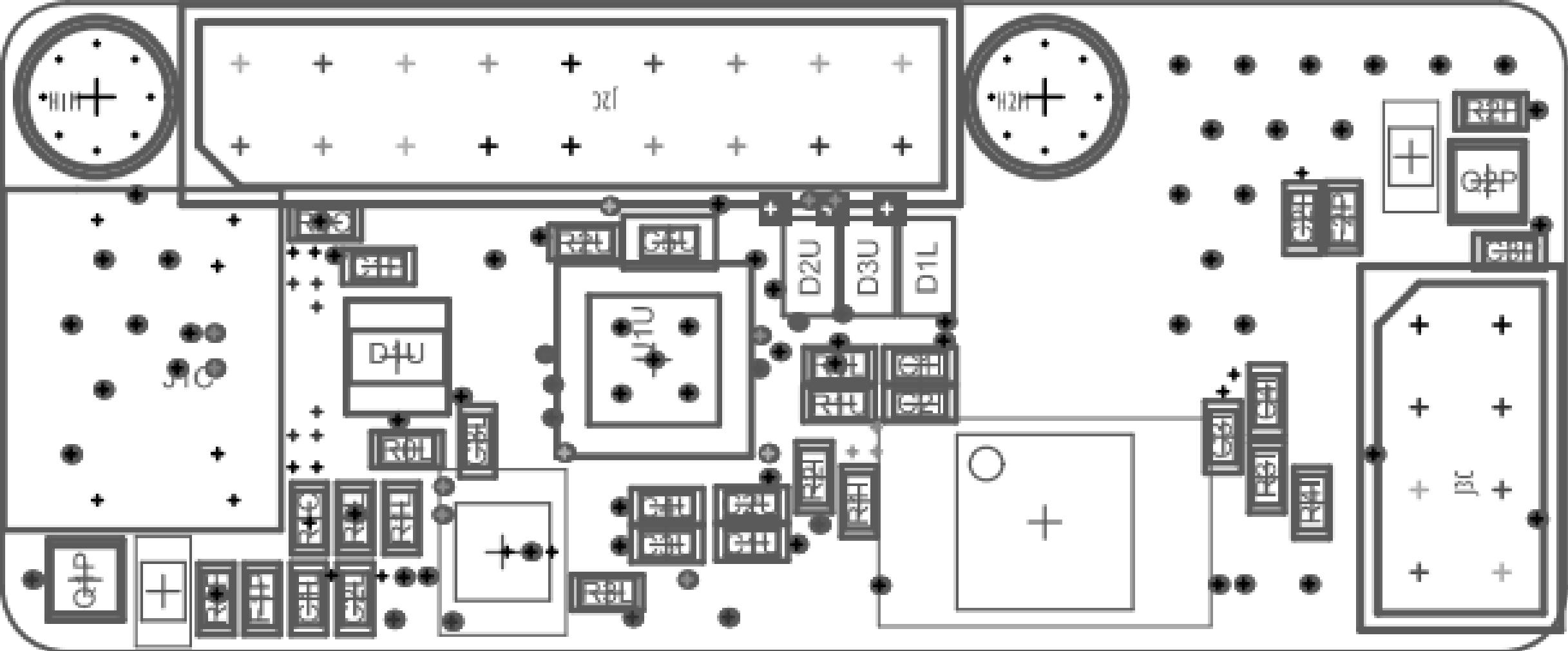












Comment	Description	Designator	Footprint	LibRef	Quantity	Manufacturer Part Number	Value	Tolerance	Voltage Rating
KGM15AR70/104K4M	Cap Cor 0.1uF 6.3V X7R 0603	C11, C3U, C4U	C0603-IPC_C_No_Silk	100nF_6.3V	3	KGM15AR70/104K4M	100nF		
C160BX5R1A106K080AC	Multilayer Ceramic Capacitor, 10 uF, 10 V, ±10%, X5R, 0603 [1608 Metric]	C1I	C0603-IPC_C_No_Silk	10uF_10V	1	C160BX5R1A106K080AC	10uF	10%	10V
C0603C104K8RACTU	Multilayer Ceramic Capacitor, 0.1 uF, 10 V, ±10%, X7R, 0603 [1608 Metric]	C1P, C1U, C2L, C2U, C3P, C4I	C0603-IPC_C_No_Silk	100nF_10V	6	C0603C104K8RACTU	100nF	10%	10V
06036A102KAT2A	Cap Ceramic 0.001uF 6.3V COG 10% SMD 0603 125°C Paper T/R	C2I	C0603-IPC_C_No_Silk	1nF_6.3V	1	06036A102KAT2A	1nF	10%	6.3V
C0603C105K8PACTU	Ceramic Capacitor, Multilayer, Ceramic, 10V, 10% +tol, 10% - Tol, X5R, 15%TC, 1uF, 0603	C2P	C0603-IPC_C_No_Silk	1uF_10V	1	C0603C105K8PACTU	1uF	10%	10V
CC0603KRX7R6BB102	Cap Ceramic 0.001uF 10V X7R 10% SMD 0603 125°C Paper T/R	C3I	C0603-IPC_C_No_Silk	1nF_10V	1	CC0603KRX7R6BB102	1nF	10%	10V
CL10A106K08NNNC	Multilayer Ceramic Capacitor, 10 uF, 6.3 V, ±10%, X5R, 0603 [1608 Metric]	C3I	C0603-IPC_C_No_Silk	10uF_6.3V	1	CL10A106K08NNNC	10uF	10%	6.3V
CL10A475KP8NNNC	Multilayer Ceramic Capacitor, 4.7 uF, 10 V, ±10%, X5R, 0603 [1608 Metric]	C5U	C0603-MFG_No_Silk	4.7uF_10V	1	CL10A475KP8NNNC	4.7uF	10%	10V
YELLOW	LED 0603 YELLOW SMD	D1I	LED_0603_YELLOW	LED_0603_YELLOW	1				
CD5OT23-SRV05-4	TVS DIODE 5V 15V SC72-6	D1U	SOT23-6-IPC_C	SRV05-4	1	CD5OT23-SRV05-4			
GREEN	LED 0603 GREEN SMD	D2U	LED_0603_GREEN	LED_0603_GREEN	1				
RED	LED 0603 RED SMD	D3U	LED_0603_RED	LED_0603_RED	1				
F0603	Fuse PPTC SMD 0603 F1P, F2P	R0603-MFG	FUSE_PPTC_0603		2		250mA, 100mA		
USB4105-GF-A-060	USB Connector Type-C SMT 16 Pin (Power pins joints = 12 pins)	J1C	USB-Type-C-16-Pin-SMT	USB-Type-C-16-Pin-SMT	1	USB4105-GF-A-060			
2X09		I2C	PinHeader_2x09_P2.5 4mm, Vertical	PinHeader_2x09_DU	1				
2X04		I3C	PinHeader_2x04_P2.5 4mm, Vertical	I2C_2X04_P2.54mm	1				
PMPB14XPZ	PMPB14XPZ	Q1P, Q2P	DFN2020MD-MFG	PMPB14XPZ	2	PMPB14XPZ			
MCR03EZPFX1691	Surface Mount Thick Film Chip Resistor 0603 Case 1.69K Ohms 1% Tolerance 100PPM	R0L	R0603-MFG	1.69K	1	MCR03EZPFX1691	1.69kR	1%	
CRCW06035K10FKEA	SMD Chip Resistor, 5.1 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1C, R2C	R0603-MFG	5.1K	2	CRCW06035K10FKEA	5.1kR	1%	75V
RC0603FR-072K2L	SMD Chip Resistor, 2.2 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1I, R2I, R3I, R4I	R0603-MFG	2.2K	4	RC0603FR-072K2L	2.2kR	1%	50V
ERJ-3EKF3302V	Res Thick Film 0603 33K Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD Automotive T/R	R1L	R0603-MFG	33K	1	ERJ-3EKF3302V	33kR	1%	75V
AC0603FR-07100KL	SMD Chip Resistor, 100 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1P, R2P	R0603-MFG	100K	2	AC0603FR-07100KL	100kR	1%	50V
RC0603FR-0710KL	SMD Chip Resistor, 10 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1U, R2U, R3L	R0603-MFG	10K	3	RC0603FR-0710KL	10kR	1%	75V
CR0603-FX-2002ELF	SMD Chip Resistor, 20 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R2L	R0603-MFG	20K	1	CR0603-FX-2002ELF	20kR	1%	50V
MCR03EZPFX2491	Res Thick Film 0603 2.49K Ohm 1% 1/10W ±100ppm/°C Molded SMD SMT Paper T/R	R4L	R0603-MFG	2.49K	1	MCR03EZPFX2491	2.49kR	1%	
ADUM1252AWA+	Ultra-Low Power, Bidirectional I2C Isolator with Extended VDD, Idle-Bus Hot-Swap and Low VOL	U1I	SOIC-W-8-IPC_A	ADUM1252AWA+	1	ADUM1252AWA+			
SGM2019-ADJYN5G/TR	DO-1U-I Reg Adj 0.3A SC72-5	U1U	TSOT-23-5-IPC-A	SGM2019-ADJYN5G/TR	1	SGM2019-ADJYN5G/TR			
CP2112-F03-GM	IC-HD USB TO-SMBUS BRIDGE 24OFN	U1U	CP2112-IPC_A	CP2112-F03-GM	1	CP2112-F03-GM			
MM3Z12VST1G	MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323 1N Semiconductor MM3Z12VST1G	ZD1P, ZD2P	SOD-323	MM3Z12VST1G	2	MM3Z12VST1G		2%	

## Design Rules Verification Report

Filename : C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-SMB-ISO-CP2112\USB-SMB-ISO-CP2112-V-1.F

Warnings 0

Rule Violations 0

### Warnings

Total	0
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Rule Violations	
Clearance Constraint (Gap=4mm) (InNetClass('PowerRails_HighVoltage_AC') Or	0
Clearance Constraint (Gap=0.254mm) (InComponentClass('Via_Plugged')), (IsPad)	0
Clearance Constraint (Gap=0.2mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (not IsBoardCutoutRegion)	0
Un-Routed Net Constraint ( All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.18mm) (Max =0.4mm) (Preferred=0.254mm) (InNetClass('Power_Signal'))	0
Width Constraint (Min=0.18mm) (Max =0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))	0
Width Constraint (Min=0.15mm) (Max =25.4mm) (Preferred=0.4mm) (InNetClass('GND'))	0
Width Constraint (Min=0.146mm) (Max =0.146mm) (Preferred=0.146mm) (InNetClass('Signal'))	0
Width Constraint (Min=0.15mm) (Max =25.4mm) (Preferred=0.3mm) (InNetClass('PowerRails_LowVoltage_DC'))	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max =0.102mm) (Preferred=0.102mm)	0
SMD To Corner (Distance=0.102mm) (NOT InNetClass('PowerRails_LowVoltage_DC') AND NOT	0
SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)	0
Power Plane Connect Rule(Direct Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.074mm) (IsVia)	0
Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass('7_MountingHoles'))	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole Size Constraint (Min=0.3mm) (Max =6.3mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)	0
Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)	0
Silk To Solder Mask (Clearance=0.15mm) (All), (All)	0
Silk to Silk (Clearance=0.102mm) (All), (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer'))	0
Height Constraint (Min=0mm) (Max =1816.048mm) (Preferred=12.7mm) (All)	0
Total	0

## Electrical Rules Check Report

Class	Document	Message
		Successful Compile for USB-SMB-ISO-CP2112.PrjPcb

Different Descriptions  
Schematic Object

MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323

MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323

PCB Object

ON Semiconductor MM3Z12VST1G [ZD1P]

ON Semiconductor MM3Z12VST1G [ZD2P]