

A

B

C

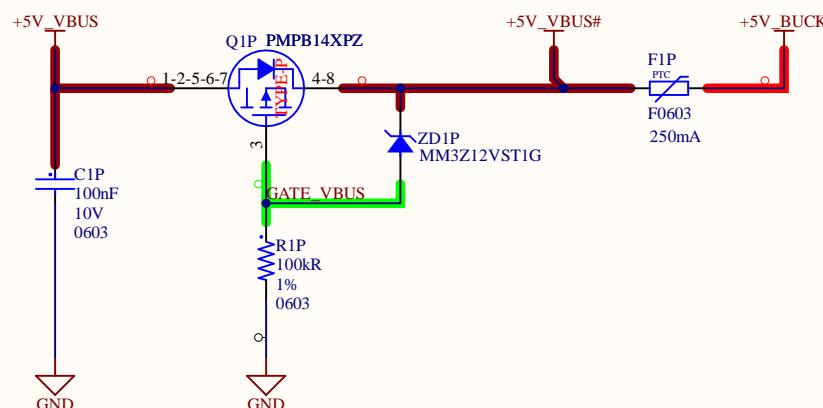
D

A

B

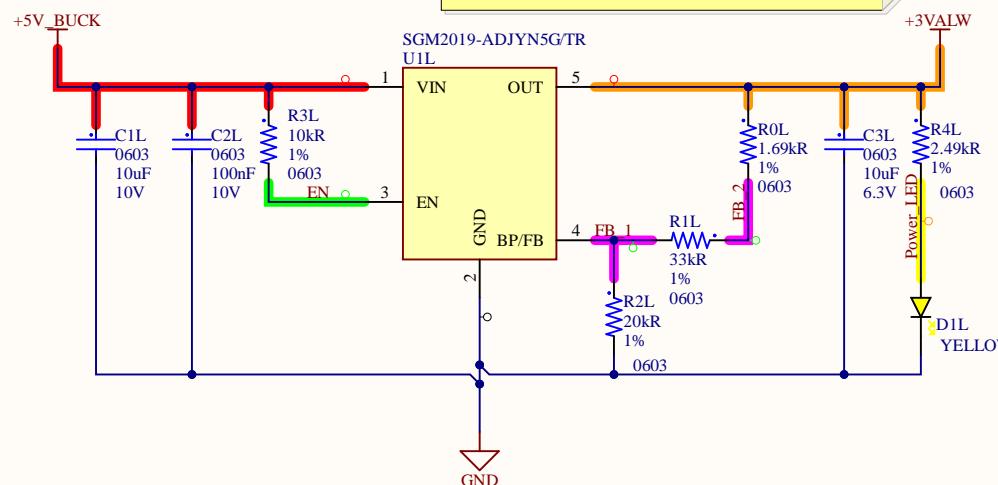
C

D



Title: Power_Path		Author: Alcatraz	DHNLAB PVT LTD DHANBAD JHARKHAND INDIA ASIA
Size: A4 Prj: USB-UART-ISO-CP2102		Approved: Alcatraz	
Date: 23-11-2024 03:04:33 Sheet 1 of 7		Edited: 22-11-2024	
Git Hash: 426		Variant: [No Variations]	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\1_Power_Path.SchDoc		SW Version: 24.10.1.45	





SGM2019-ADJYN5G/TR
Vout = 3.3V
Register Values For R0L, R1L and R2L
R1L=R0B+R1L

Values From Datasheet

Vout(V)	R1 (kΩ)	R2 (kΩ)
1.2	0	63.4
1.5	10.5	42.2
1.8	34	63.4
2.8	84.5	63.4
3.0	63.4	42.2
3.3	73.2	42.2
3.6	84.5	42.2
4.2	105	42.2

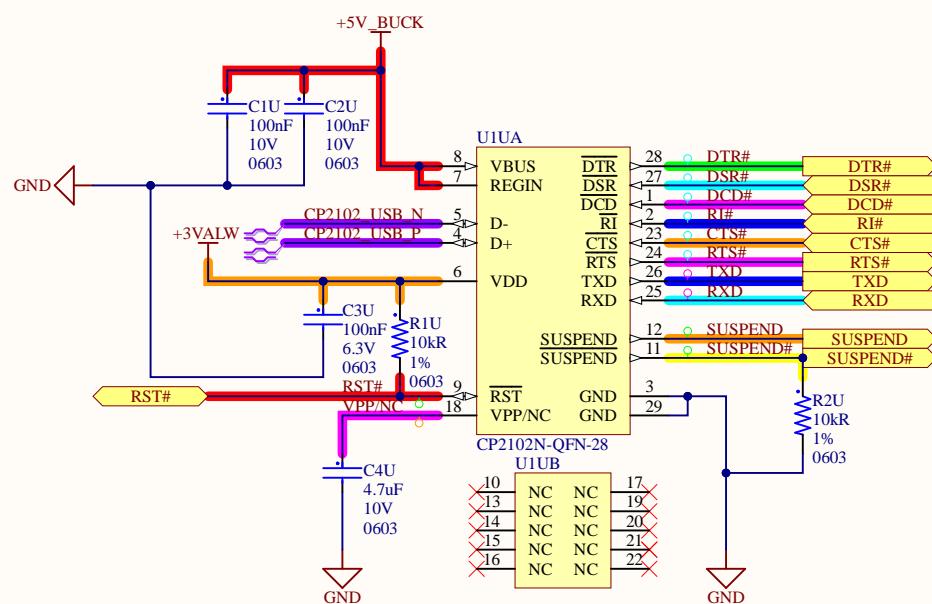
NOTE: $V_{OUT} = (R_1 + R_2) / R_2 \times 1.207$

Here are the calculated values of R1L (in kΩ) for VOUT= 3.3 V with different R2L values:
IF R0L= 0Ω
R2L=10kΩ:R1L≈17.34kΩ
R2L=20kΩ:R1L≈34.68kΩ
R2L=30kΩ:R1L≈52.02kΩ
R2L=40kΩ:R1L≈69.36kΩ
R2L=50kΩ:R1L≈86.70kΩ
R2L=60kΩ:R1L≈104.04kΩ
R2L=70kΩ:R1L≈121.38kΩ
R2L=80kΩ:R1L≈138.72kΩ
R2L=90kΩ:R1L≈156.06kΩ
R2L=100kΩ:R1L≈173.41kΩ

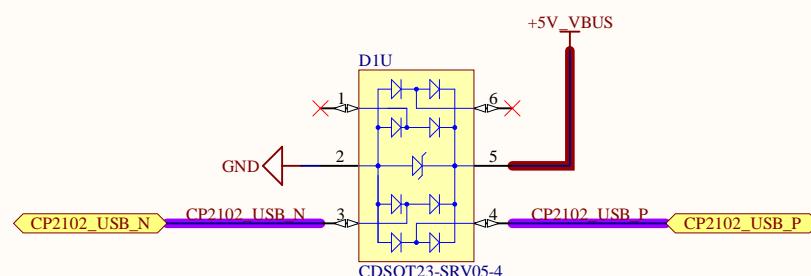
Title: LDO	Author: Alcatraz	DHNLAB PVT LTD
Approved: Alcatraz	PUBLIC	DHANBAD
Size: A4	Edited: 22-11-2024	JHARKHAND
Prj: USB-UART-ISO-CP2102	Variant: [No Variations]	INDIA
Date: 23-11-2024 03:04:33	SW Version: 24.10.1.45	ASIA
Sheet 2 of 7		
Git Hash: 426		
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\2_LDO.SchDoc		



A



B



C

D

Title: USB_TO_UART	Author: Alcatraz	DHNLAB PVT LTD
Approved: Alcatraz	PUBLIC	DHANBAD
Size: A4	Edited: 17-11-2024	JHARKHAND
Prj: USB-UART-ISO-CP2102	Variant: [No Variations]	INDIA
Date: 23-11-2024 03:04:33	SW Version: 24.10.1.45	ASIA
Sheet 3 of 7		
Git Hash: 394		
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Developmen\USB-UART-ISO-CP2102\3_USB_TO_UART.SchDoc		

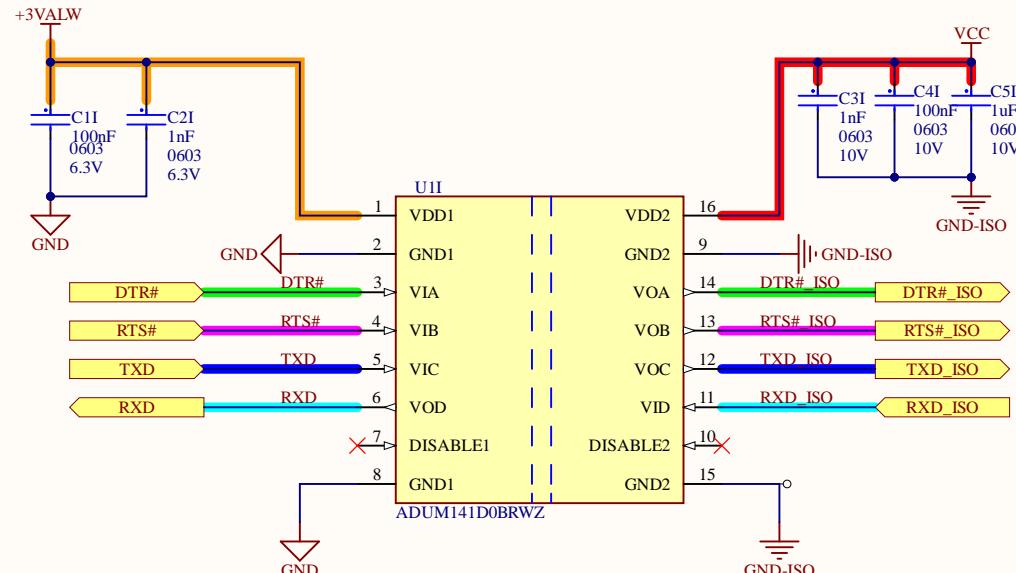


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Title: <i>Digital_Isolator</i>	Author: Alcatraz	DHNLAB PVT LTD DHANBAD JHARKHAND INDIA ASIA
Size: A4	Approved: Alcatraz	
	PUBLIC	
Date: 23-11-2024 03:04:33	Edited: 22-11-2024	
Git Hash: 427	Variant: [No Variations]	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Developmet\USB-UART-ISO-CP2102\4_Digital_Isolator.schDoc		

A

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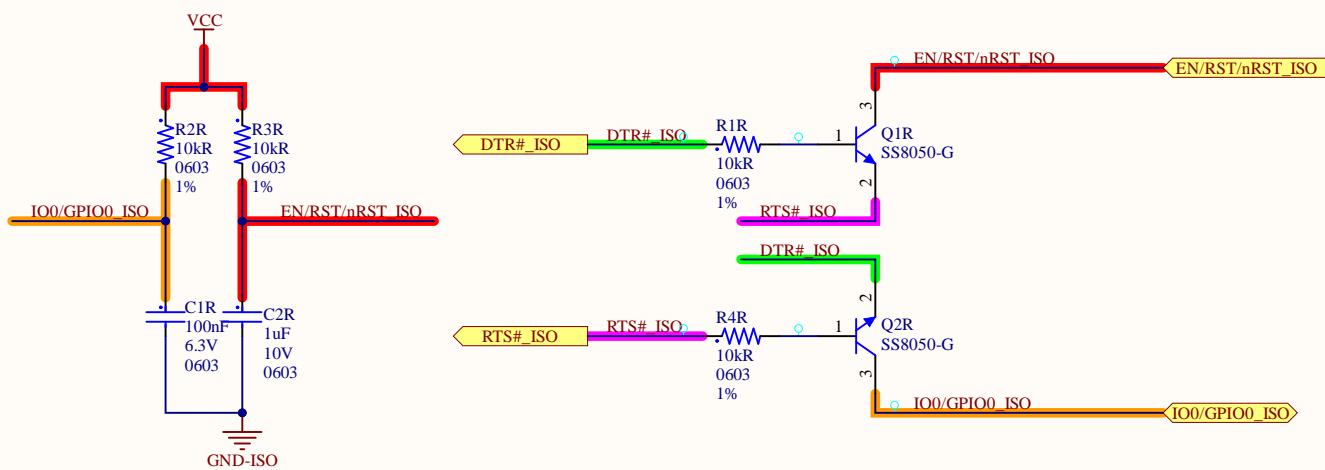
D

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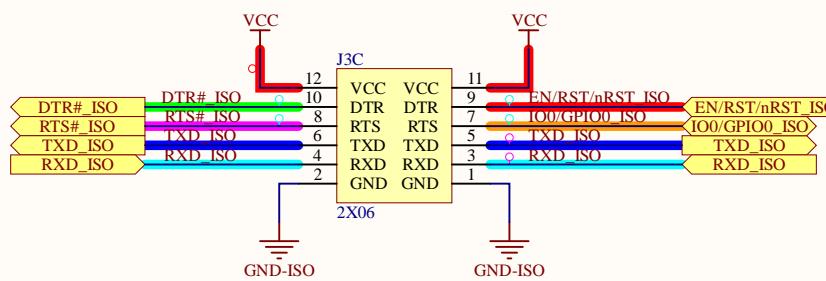
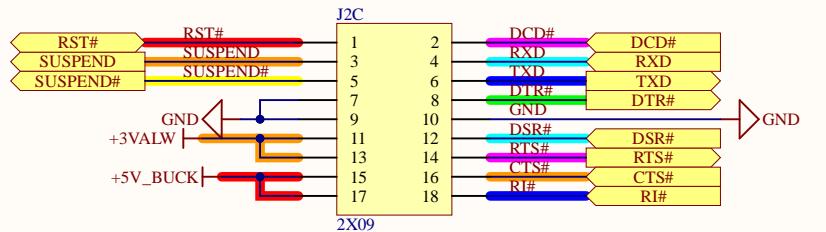
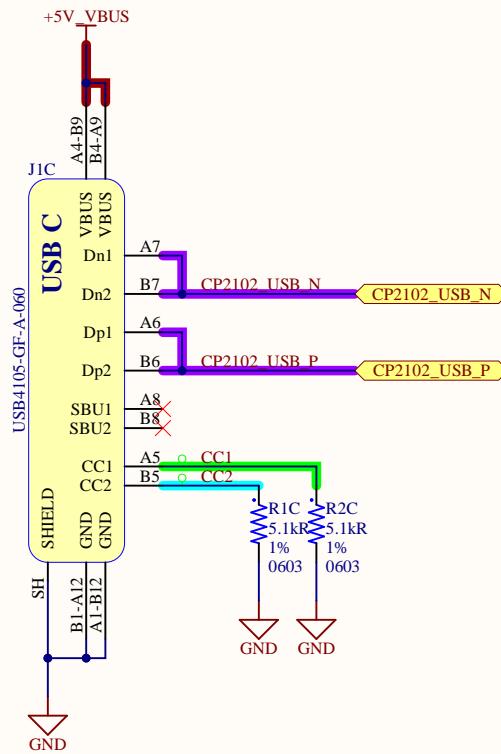
D



Title: <i>Auto_Reset</i>		Author: Alcatraz	DHNLAB PVT LTD DHANBAD JHARKHAND INDIA ASIA
Size: A4 Prj: USB-UART-ISO-CP2102		Approved: Alcatraz	
Date: 23-11-2024 03:04:33 Sheet: 5 of 7		Edited: 17-11-2024	
Git Hash: 394		Variant: [No Variations]	
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\5_Auto_Reset.SchDoc		SW Version: 24.10.1.45	



A



Title: Connector	Author: Alcatraz	DHNLAB PVT LTD
Size: A4	Approved: Alcatraz	DHANBAD
Prj: USB-UART-ISO-CP2102	Edited: PUBLIC	JHARKHAND
Date: 23-11-2024 03:04:33	Variant: [No Variations]	INDIA
Git Hash: 394	SW Version: 24.10.1.45	ASIA
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-UART-ISO-CP2102\6 Connector.SchDoc		



A

A

B

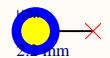
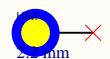
B

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C

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Title: MountingHoles		Author: Alcatraz	DHNLAB PVT LTD DHANBAD JHARKHAND INDIA ASIA
Size: A4	Prj: USB-UART-ISO-CP2102	Approved: Alcatraz	
Date: 23-11-2024	03:04:33	Edited: 19-11-2024	
Git Hash: 404		Variant: [No Variations]	
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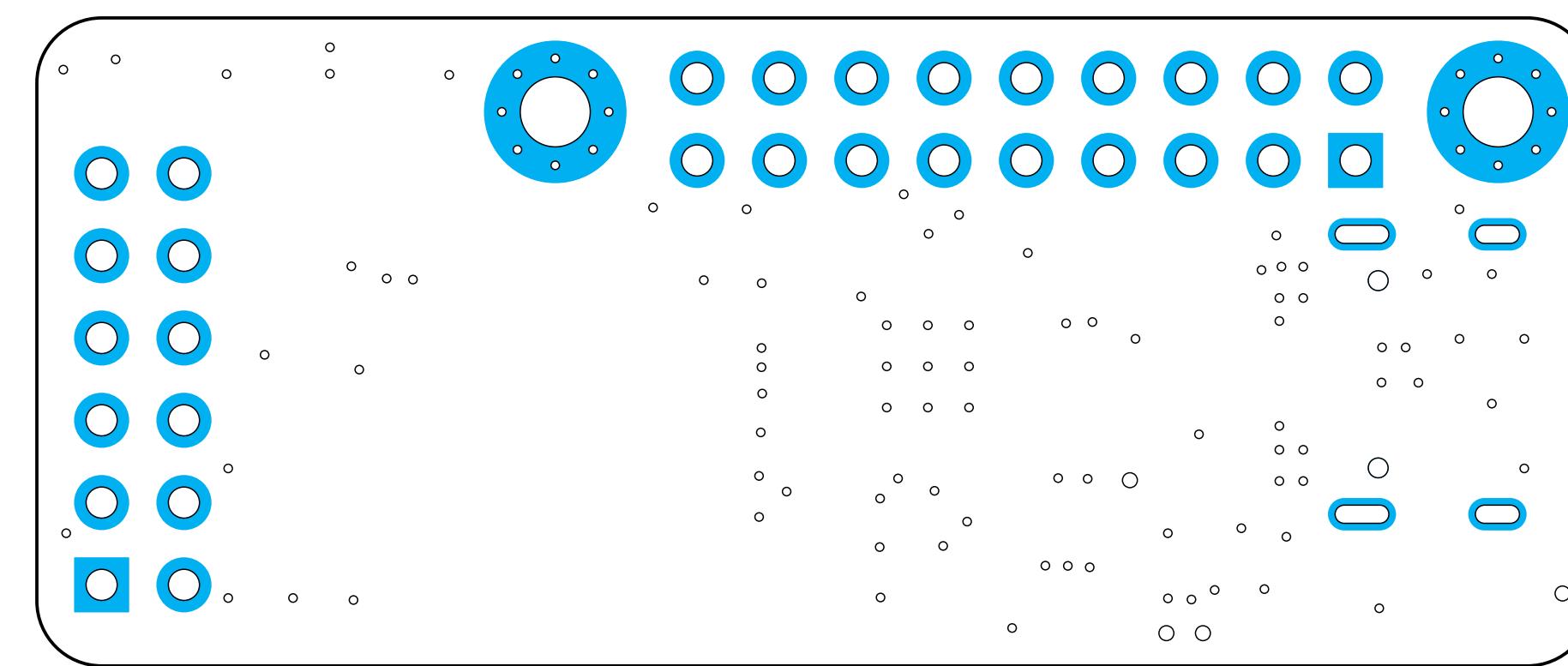
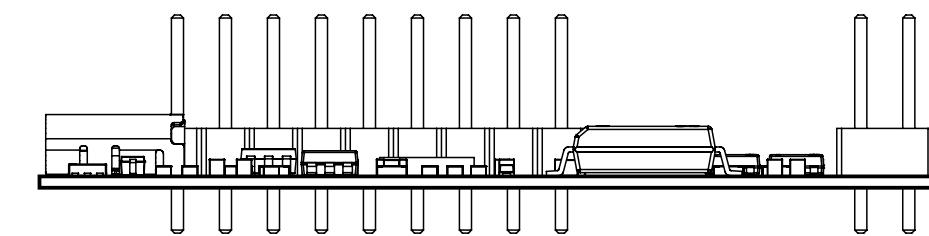
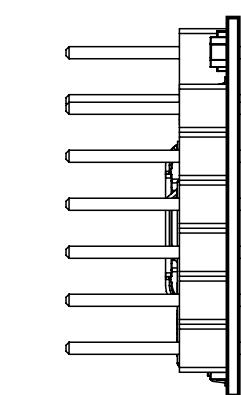
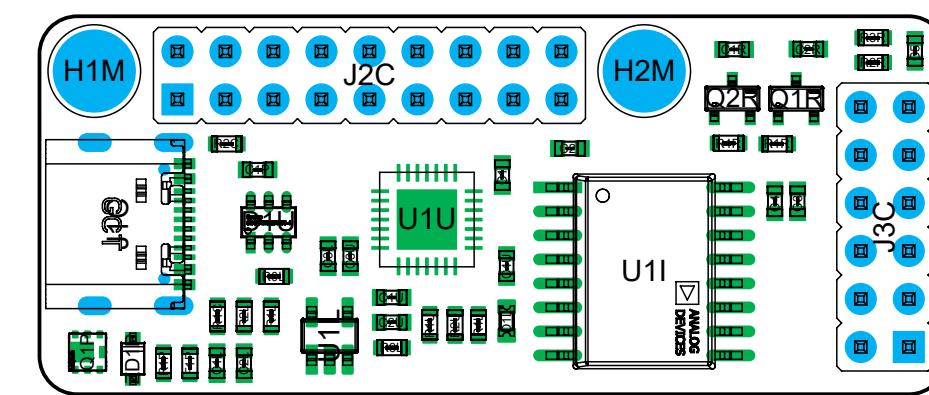
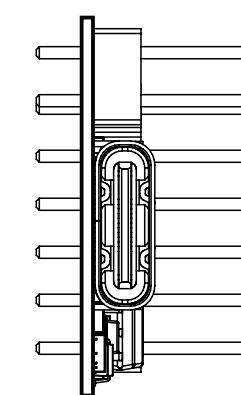
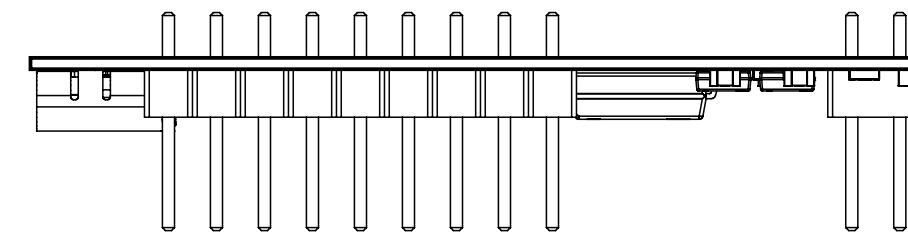
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Note:

- 1 Text element with square border.
- 2 Text element with no border
- 3 Text element with circle border

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AS A WHOLE WITHOUT THE
WRITTEN PERMISSION OF IS
PROPRIETARY AND CONFIDENTIAL

		UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES	NAME	DATE	TITLE
		TOLERANCES: FRACTIONAL: ± ANGULAR: MACH: ± BEND: ±	DRAWN	23-11-2024	
		TWO PLACE DECIMAL: ± THREE PLACE DECIMAL: ±	CHECKED		
		INTERPRET GEOMETRIC TOLERANCING PER:	ENG APPR.		
		MATERIAL	MFG APPR.		
	NEXT ASSY	USED ON	Q.A.		COMMENTS:
			MATERIAL		
			FINISH		
		APPLICATION	DO NOT SCALE DRAWING		SIZE DWG NO.
					SCALE: 1:1 WEIGHT: SHEET 1 OF 1

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PCB MANUFACTURING SPECIFICATIONS

"=ProjectTitle"

SPECIFICATIONS

NOTE #	NOTE
1	ALL SPECIFICATIONS REFERENCED ARE OF THE REVISION SPECIFIED IN THE TITLE BLOCK
2	SUPPLIER SHALL NOT MODIFY THE DESIGN OR APPROVED STACK-UP WITHOUT WRITTEN PERMISSION
3	ALL MATERIALS SHALL BE RoHS COMPLIANT AND FINAL PRODUCT SHALL BE ACCEPTABLE TO USE IN RoHS ASSEMBLY. RoHS LOGO SHALL BE MARKED IN SILKSCREEN INK BY THE SUPPLIER WHERE INDICATED BY THE TEXT "PLACE MARKINGS HERE"
4	COPPER FOIL: REFER TO LAYER STACK LEGEND FOR Cu THICKNESS DETAILS. ALL Cu THICKNESSES ARE FINISHED AND INCLUDE BASE FOIL PLUS Cu PLATING ON PLATED LAYERS
5	ELECTRICAL TEST: ALL PRINTED CIRCUITS SHALL BE 100% ELECTRICALLY TESTED FOR OPENS/SHORTS USING PROVIDED NETLIST. REJECTED PRINTED BOARDS MUST BE CLEARLY MARKED WITH NON-CONDUCTIVE, PERMANENT INK.
6	MARKINGS: VENDOR MARKING AND DATE/LOT CODES SHALL BE LOCATED ON THE BOARD IN THE RESERVED AREA AS SPECIFIED IN THE GERBER LAYER "PCBM_NOTES" BY THE TEXT "PLACE MARKINGS HERE".
7	MARKINGS: THE SIDE ONTO WHICH PLACE THE MARKINGS IS AT THE SUPPLIER DISCRETION UNLESS OTHERWISE NOTED ONTO THE LAYER "PCBM_NOTES"
8	SUPPLIER SHALL CHECK PCBM_NOTES LAYER BEFORE ASKING FOR CLARIFICATIONS
9	MANUFACTURE TENTED/PLUGGED VIAS AS SPECIFIED IN THE GERBER FILES

SPECIFICATIONS

LENGTH	20.00mm
WIDTH	48.00mm
LAYERS	2
MATERIAL	FR-4
MATERIAL MIN TG	130-140
TRACK WIDTH/CLEARANCE	10 mils / 10 mils
THICKNESS	0.6mm
COPPER THICKNESS	35um (1oz)
SOLDERMASK	YES, TOP AND BOTTOM
SOLDERMASK COLOR	GREEN
SILKSCREEN	YES, TOP AND BOTTOM
SILKSCREEN COLOR	WHITE
SURFACE FINISH	HASL LEAD FREE
GOLD FINGERS	NO
CHAMFERING	YES
IMPEDANCE CONTROL	YES
HALF-CUT/CASTELLATED HOLES	NO
BURIED/BLIND VIAS	NO
VIAS FILLED WITH RESIN	NO
CARBON MASK	NO
COUNTERSINKS/COUNTERBORES	NO
Z-AXIS MILLING	NO
PEELABLE SOLDERMASK	NO

Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
	Surface Material	0.02mm	Solder Resist	Solder Mask	GTS
Copper	Top Layer	0.04mm		Signal	GTL
	Core	0.50mm	FR-4	Dielectric	
Copper	Bottom Layer	0.04mm		Signal	GBL
	Surface Material	0.02mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.60mm

NON-COPPER LAYER THICKNESS FOR REFERENCE ONLY
LAYERS OF TYPE "INTERNAL PLANE" ARE NEGATIVE

Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 22-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 23-11-2024 03:04 AM	Sheet 1 of 3	Address Line 3
Git Hash:	SW version: 24.10.1.45	Address Line 4
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB MANUFACTURING_U		

[YOUR LOGO
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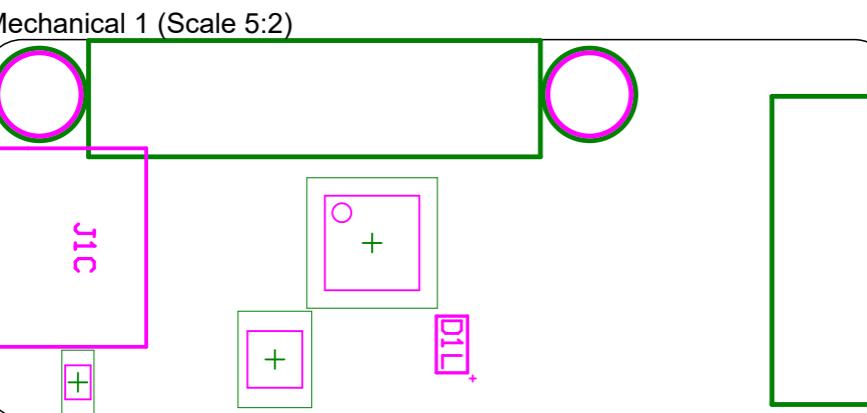
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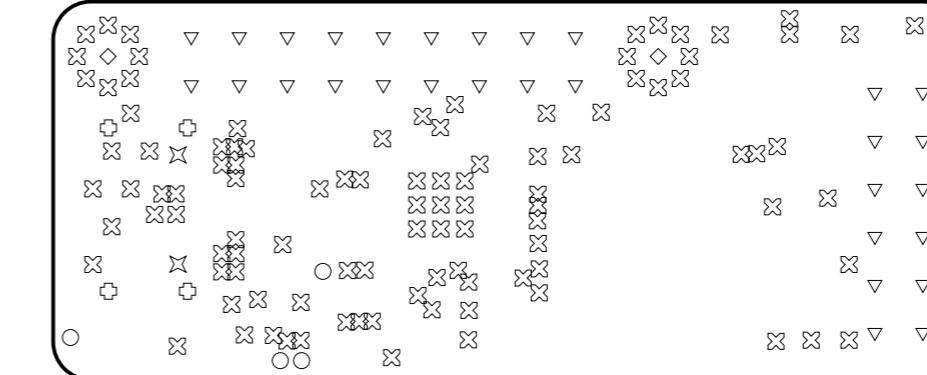
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2

Drill Drawing View (Scale 5:2)

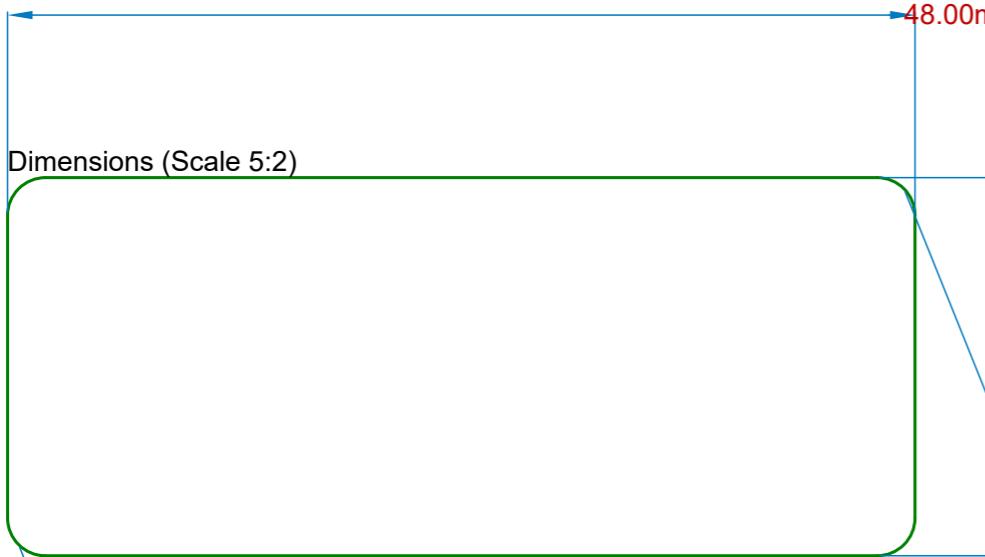


3

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
✗	105	0.30mm	Есть	
○	4	0.50mm	Есть	
✚	4	0.60mm	Есть	
☒	2	0.65mm	Нет	
▽	30	1.00mm	Есть	
◇	2	2.20mm	Есть	
147 Total				

4



**ALWAYS CAREFULLY READ
THE NOTES ON THIS LAYER!**

5

Title: =ProjectTitle	Author:	CONFIDENTIAL
Approved:		
Size: A3	Edited: 22-11-2024	
Prj: =ProjectTitle	Variant: [No Variations]	
Unit: mm	SW version: 24.10.1.45	
Date: 23-11-2024 03:04 AM	Sheet 2 of 3	
Git Hash: 431 [No modification]		
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB MANUFACTURING_US		

[YOUR LOGO
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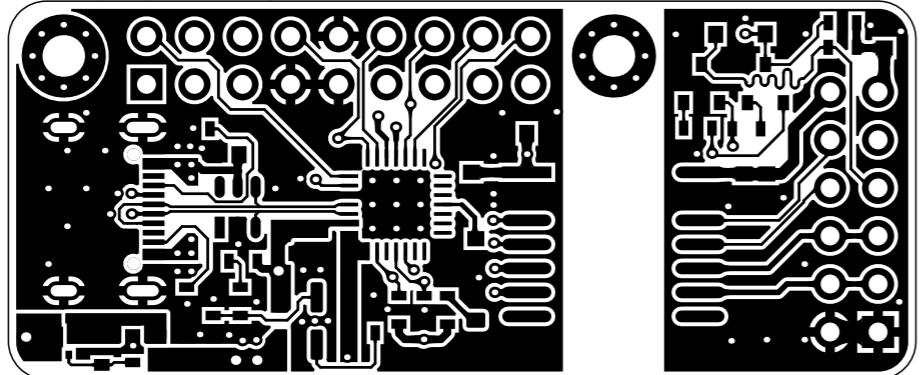
E

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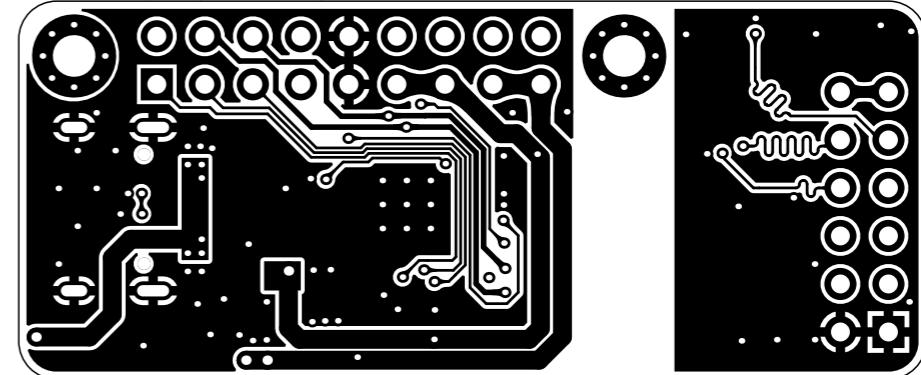
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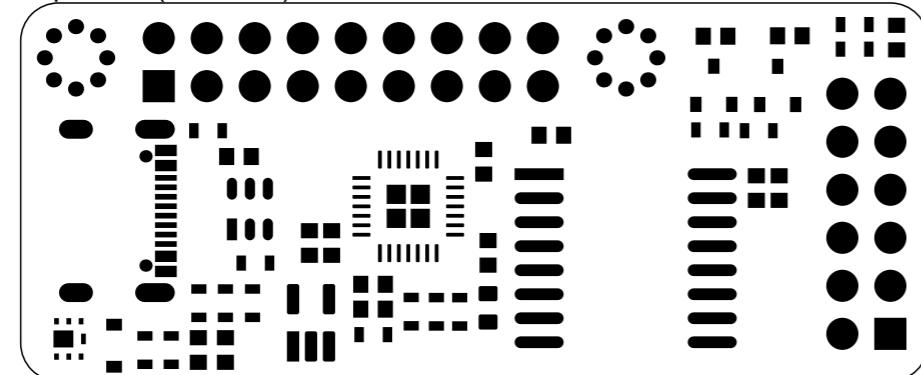
Top Layer (Scale 5:2)



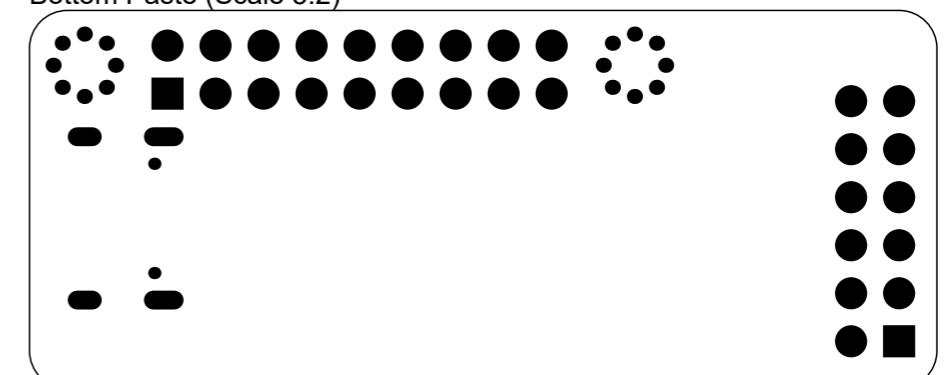
Bottom Layer (Scale 5:2)



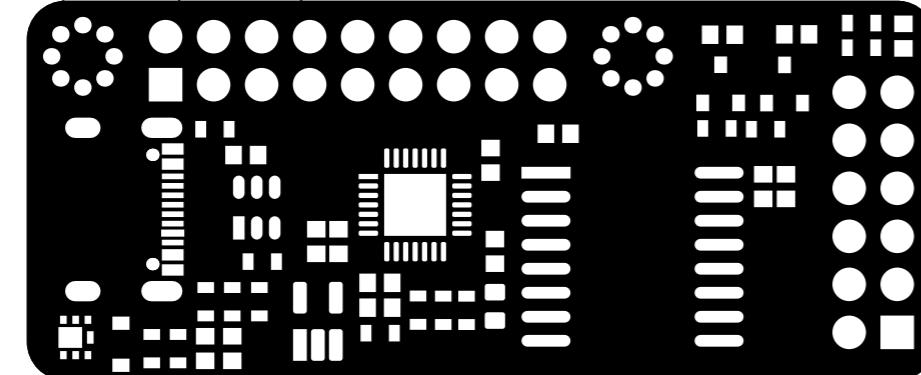
Top Paste (Scale 5:2)



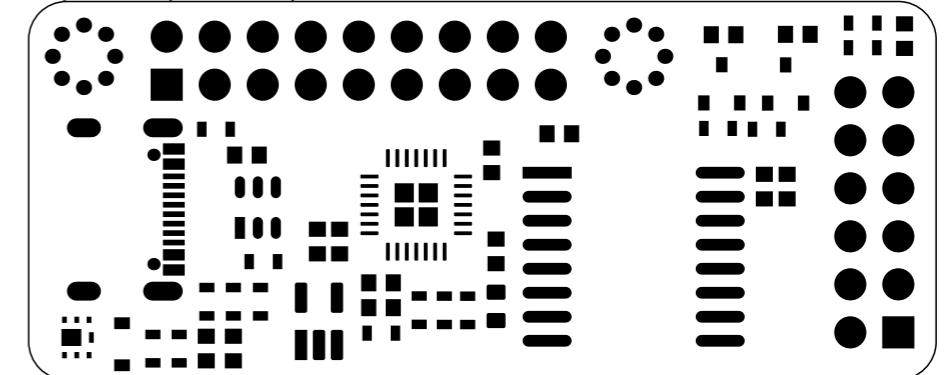
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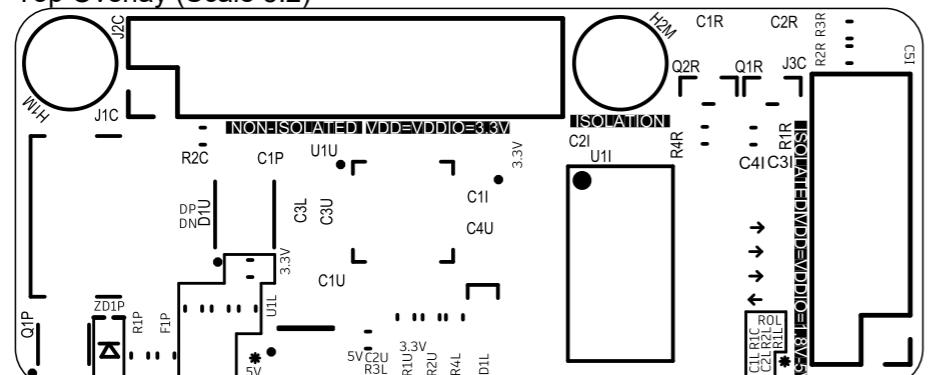
Top Solder (Scale 5:2)



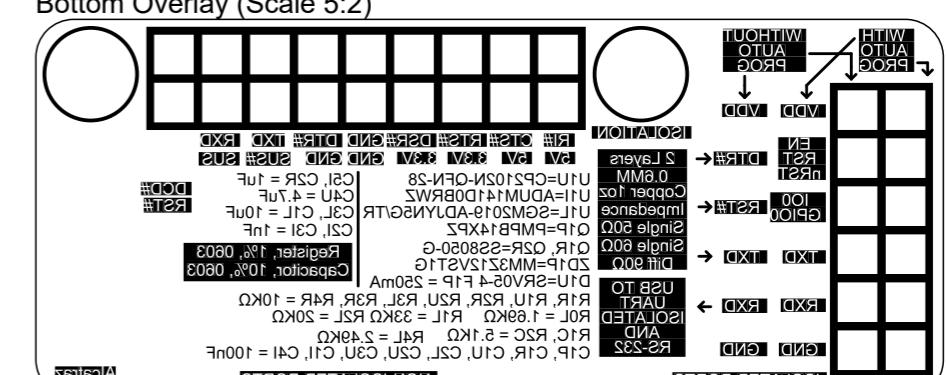
Top Paste (Scale 5:2)



Top Overlay (Scale 5:2)



Bottom Overlay (Scale 5:2)



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Size: A3	Approved:	
Unit: mm	Edited: 22-11-2024	
Prj: =ProjectTitle	Variant: [No Variations]	
Date: 23-11-2024 03:04 AM	Sheet: 3 of 3	SW version: 24.10.1.45
Git Hash: 431 [No modification]		
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[YOUR LOGO
HERE]

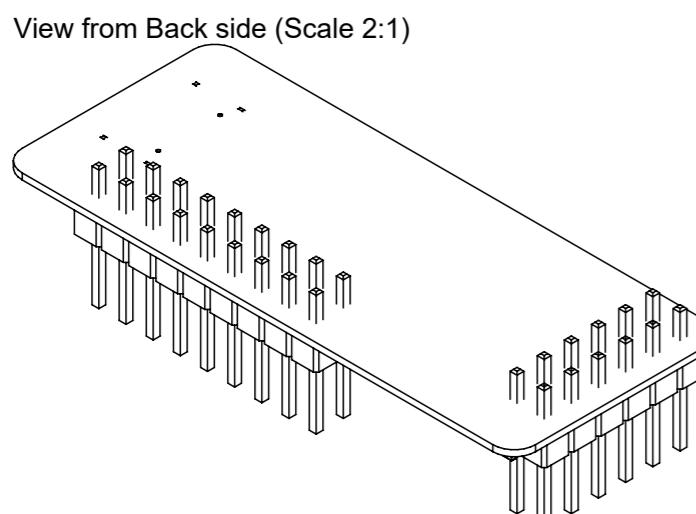
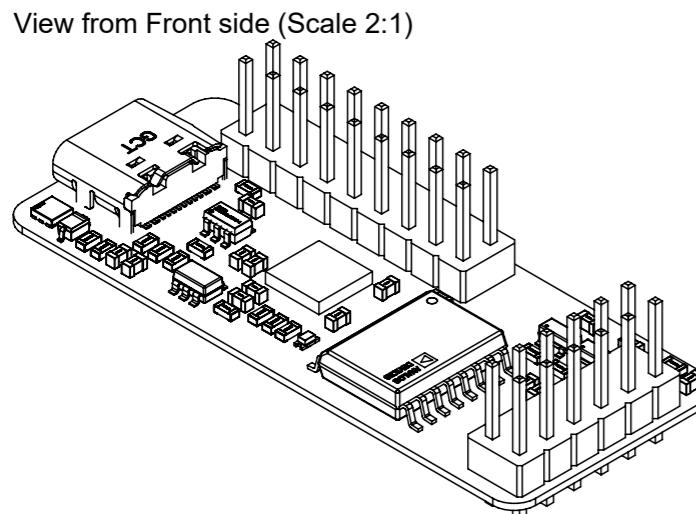
PCB ASSEMBLY SPECIFICATIONS

"=ProjectTitle"

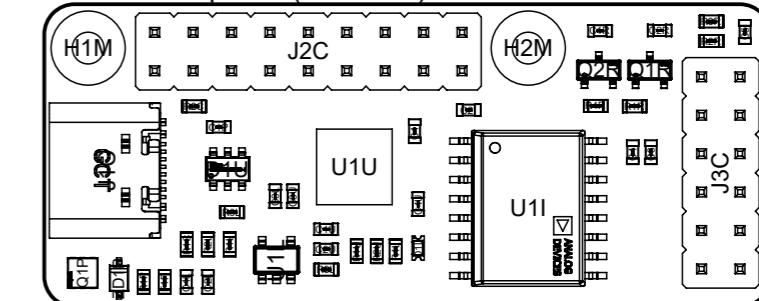
Variant: "[No Variations]"

SPECIFICATIONS

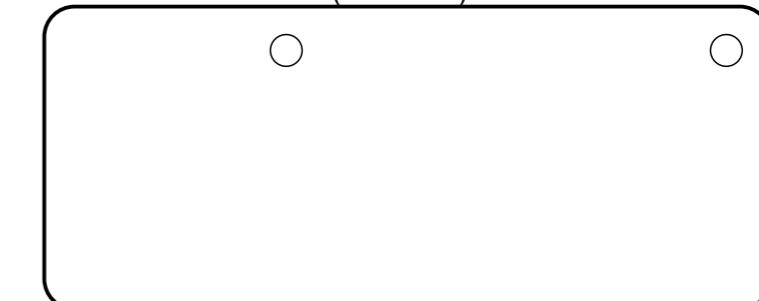
NOTE #	NOTE
1	ALL SPECIFICATIONS REFERENCED SHALL BE OF THE LATEST REVISION UNLESS OTHERWISE NOTED
2	SUPPLIER SHALL NOT MODIFY THE DESIGN WITHOUT WRITTEN PERMISSION
3	REFER TO EXCEL BOM FOR UP-TO-DATE INFORMATION
4	THE BOM IN THIS DOCUMENT IS PURELY AN AID TO ASSEMBLY OPERATIONS AND MAY NOT HAVE THE MOST UP-TO-DATE DATA OR ALL APPROVED COMPONENT ALTERNATIVE.



View from Top side (Scale 2:1)



View from Bottom side (Scale 2:1)



Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Prj: =ProjectTitle	Edited: 22-11-2024	Address Line 1
Unit: mm	Variant: [No Variations]	Address Line 2
Date: 23-11-2024 03:04 AM	Sheet 1 of 9	Address Line 3
Git Hash:	SW version: 24.10.1.45	Address Line 4
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_U\$B-UAR		[YOUR LOGO HERE]

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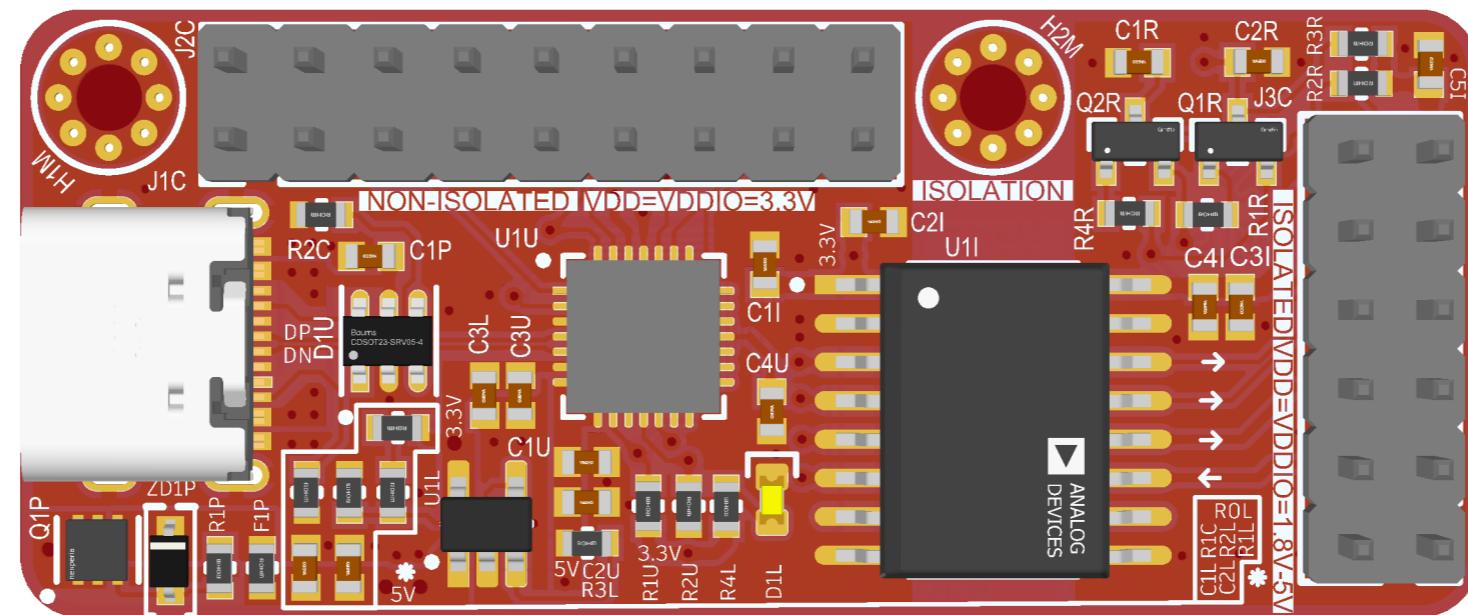
2

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Realistic View TOP



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Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 22-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 23-11-2024 03:04 AM	Sheet: 2 of 9	Address Line 3
Git Hash: 431 [No modification]	SW version: 24.10.1.45	Address Line 4
File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_USB-UAR		

[YOUR LOGO HERE]

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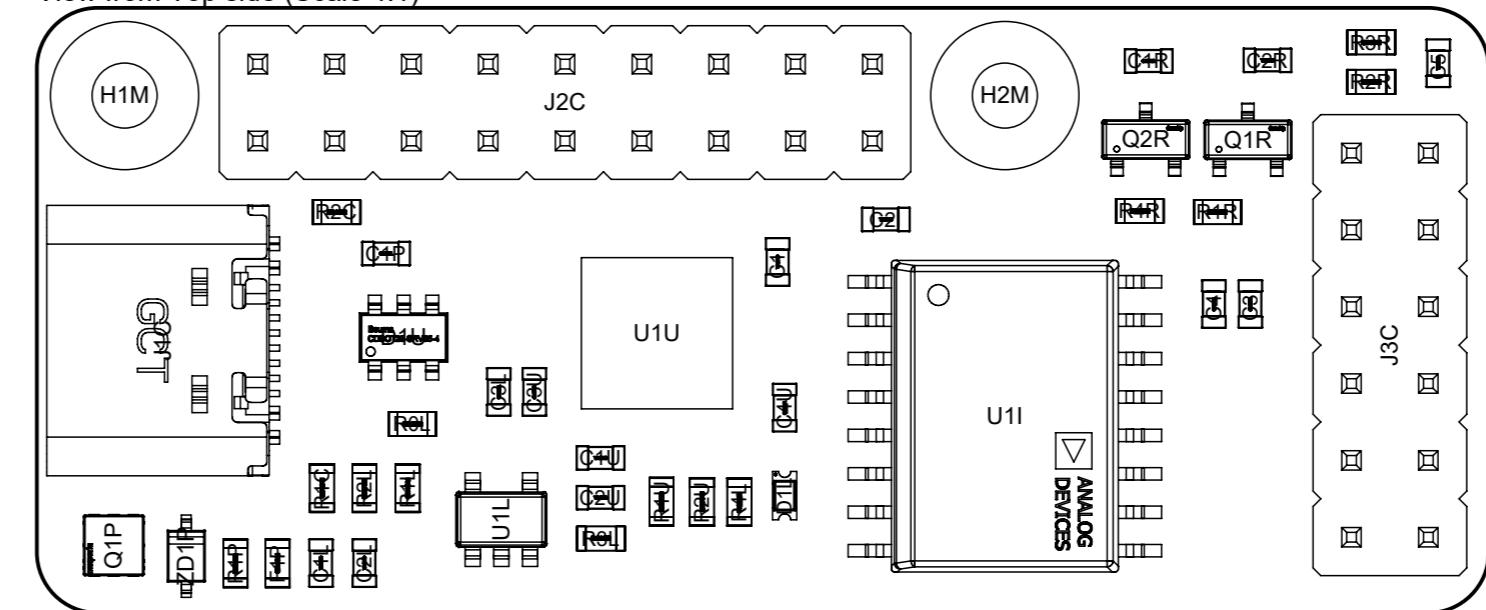
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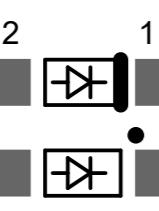
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6

View from Top side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ()



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

Title: =ProjectTitle

Author:

CONFIDENTIAL

Size: A3 Prj: =ProjectTitle

Approved: Edited: 22-11-2024

My Company

Unit: mm

Variant: [No Variations]

Address Line 1

Date: 23-11-2024 03:04 AM

Sheet 3 of 9 SW version: 24.10.1.45

Address Line 2

Git Hash: 431 [No modification]

Address Line 3

Address Line 4

File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_USB-UAR

[YOUR LOGO HERE]

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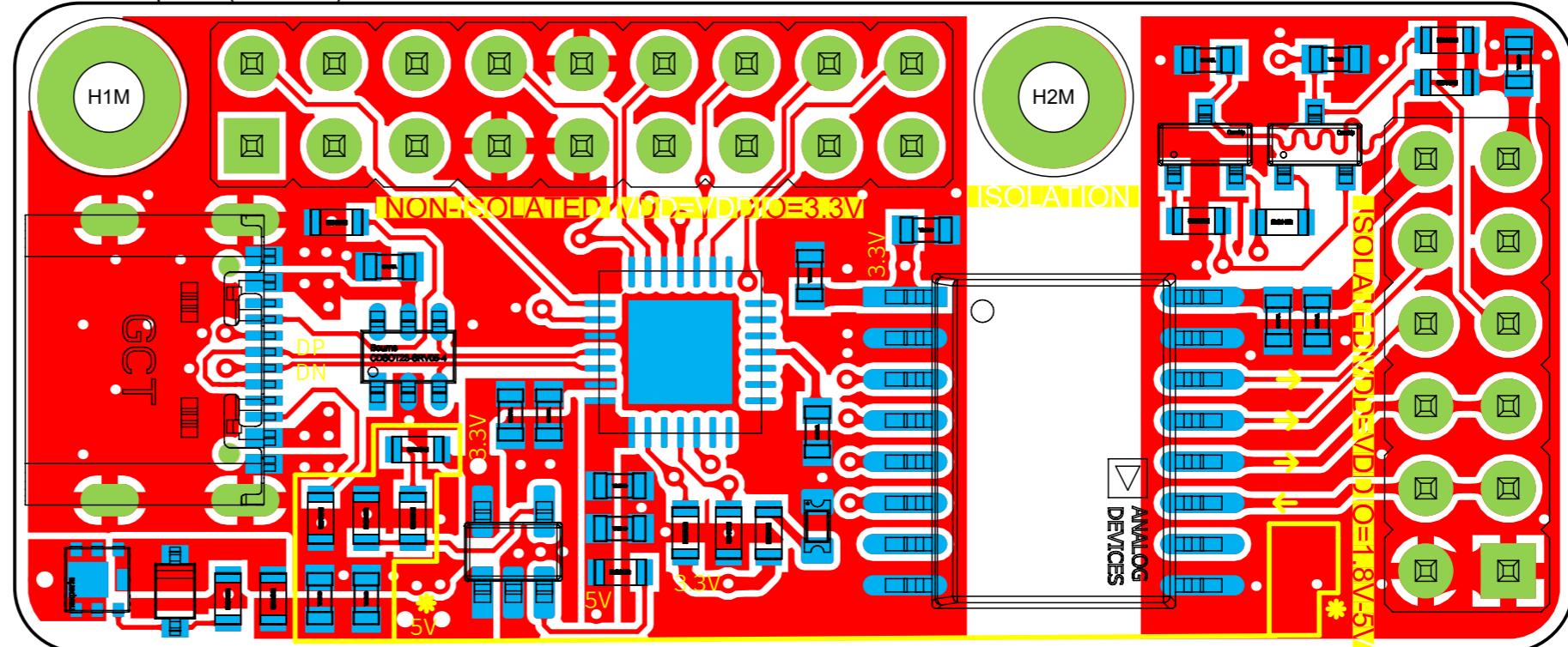
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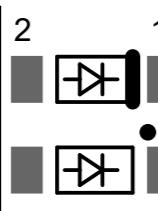
5

6

View from Top side (Scale 5:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ()



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

Title: =ProjectTitle

Author:

CONFIDENTIAL

Approved:

Edited: 22-11-2024

Size: A3 Prj: =ProjectTitle

Variant: [No Variations]

Unit: mm Date: 23-11-2024 03:04 AM

Sheet 4 of 9 SW version: 24.10.1.45

Git Hash: 431 [No modification]

File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_USB-UAR

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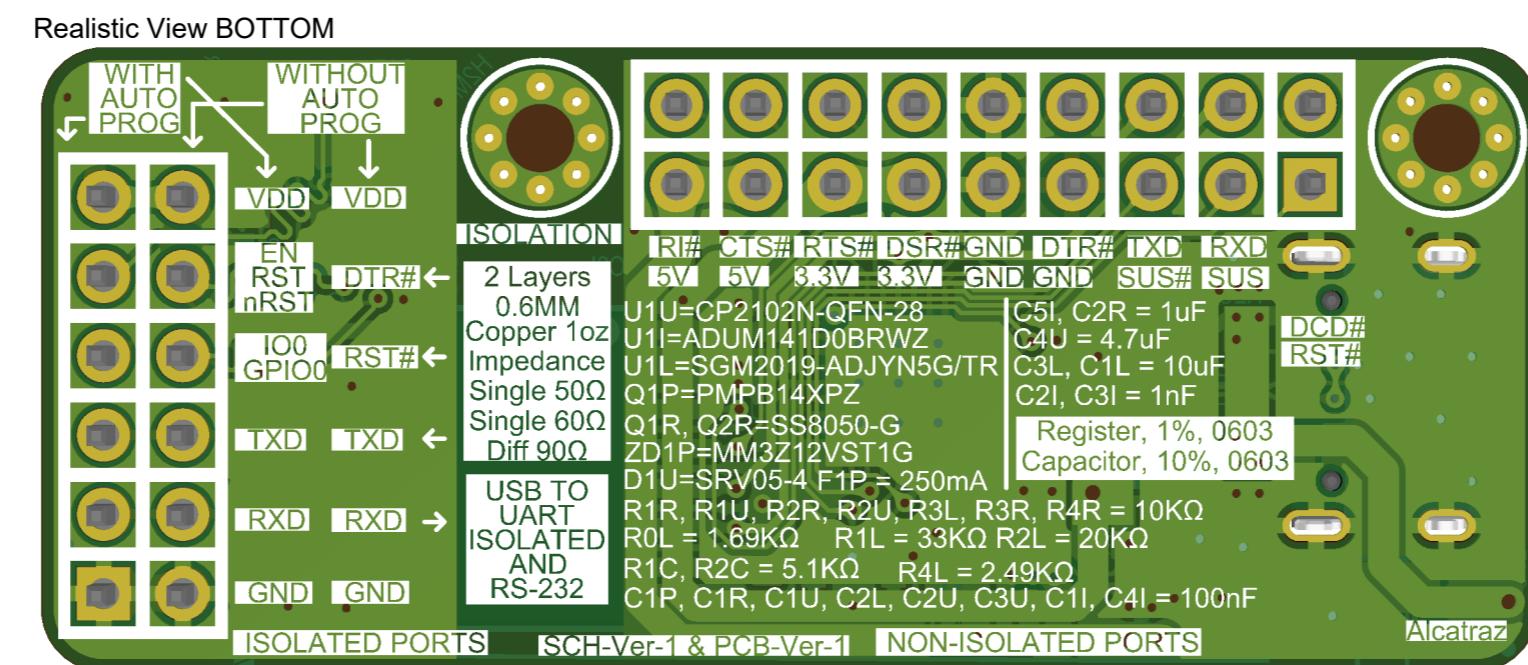
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Unit: mm	Edited: 22-11-2024	Address Line 1
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Date: 23-11-2024 03:04 AM	Sheet: 5 of 9	Address Line 3
Git Hash: 431 [No modification]	SW version: 24.10.1.45	Address Line 4
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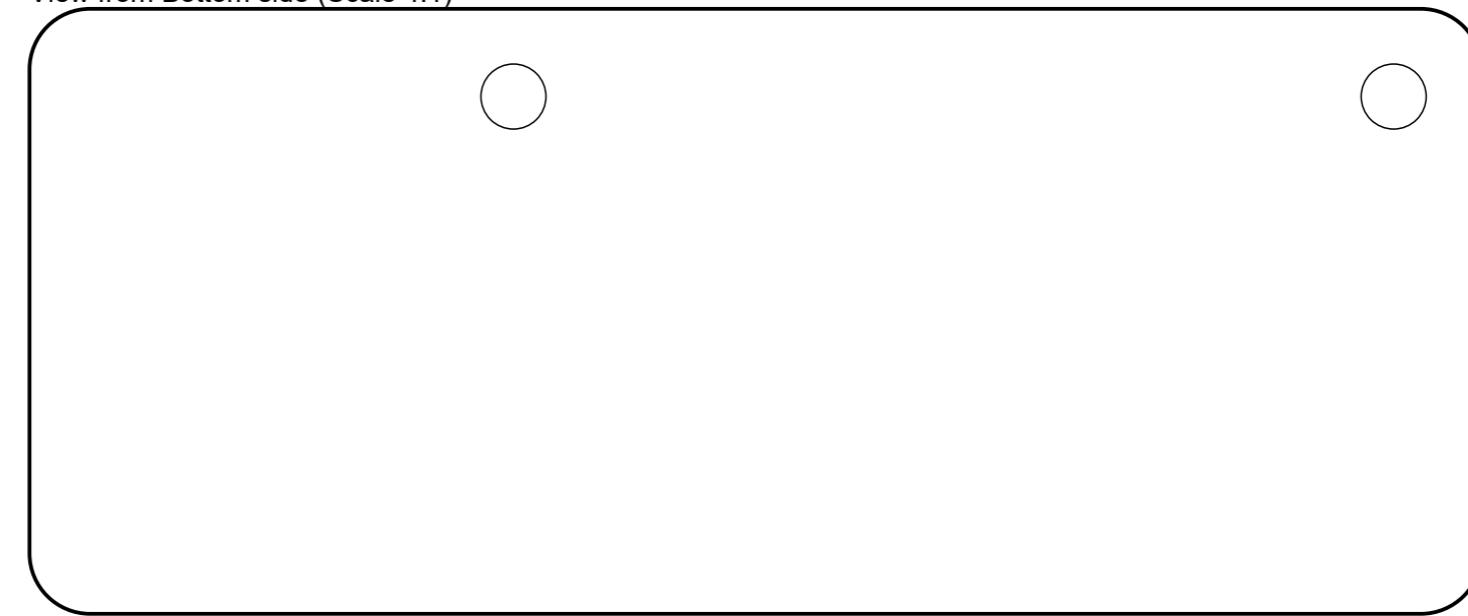
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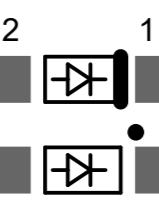
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View from Bottom side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ()



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (•)

Title: =ProjectTitle

Author:

CONFIDENTIAL

Size: A3 Prj: =ProjectTitle

Approved: 22-11-2024

My Company
Address Line 1
Address Line 2
Address Line 3
Address Line 4

Unit: mm Date: 23-11-2024 03:04 AM

Variant: [No Variations]
SW version: 24.10.1.45

Sheet 6 of 9

Git Hash: 431 [No modification]

File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_USB-UAR

YOUR LOGO
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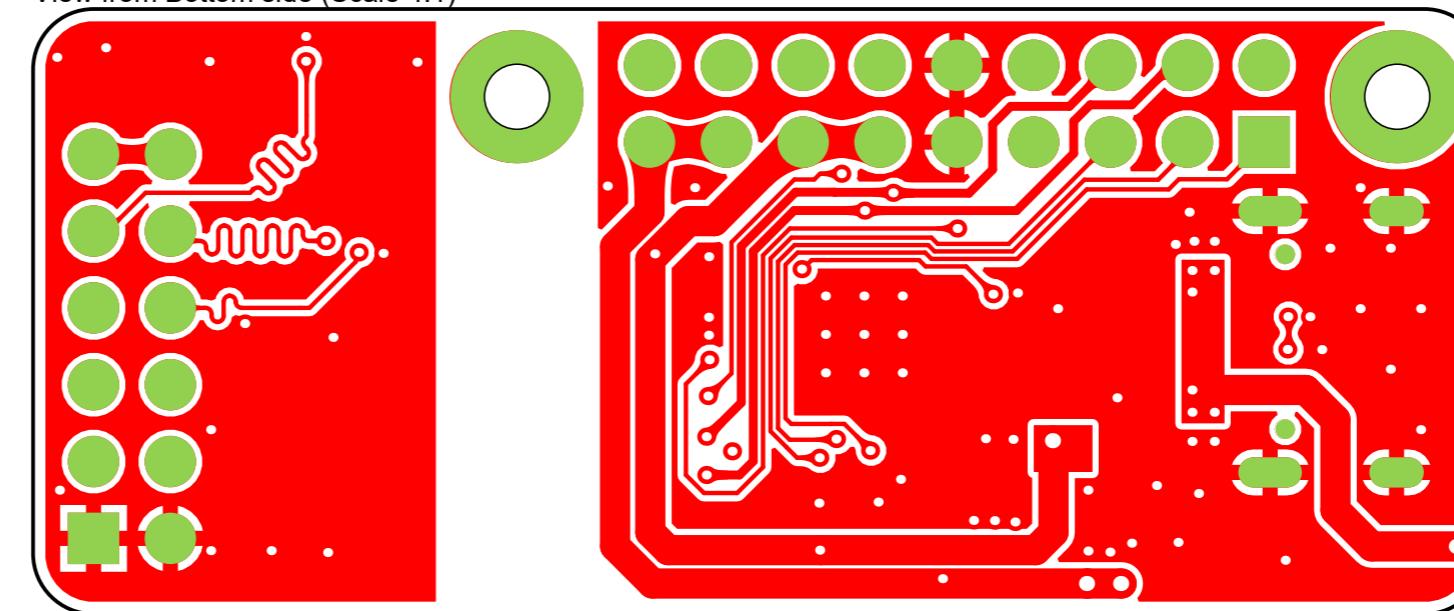
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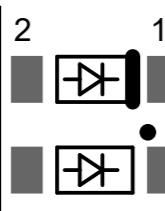
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View from Bottom side (Scale 4:1)

**DIODE ORIENTATION**

Name	ANODE
Short name	A
Pin number	2
Silkscreen	thin line
assembly view	no dot ()



Name	CATHODE
Short name	K
Pin number	1
Silkscreen	thick line / dot
assembly view	dot (*)

Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company
Unit: mm	Edited: 22-11-2024	Address Line 1
Prj: =ProjectTitle	Variant: [No Variations]	Address Line 2
Date: 23-11-2024 03:04 AM	Sheet 7 of 9	Address Line 3
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File: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\PCB_ASSEMBLY_USB-UAR		

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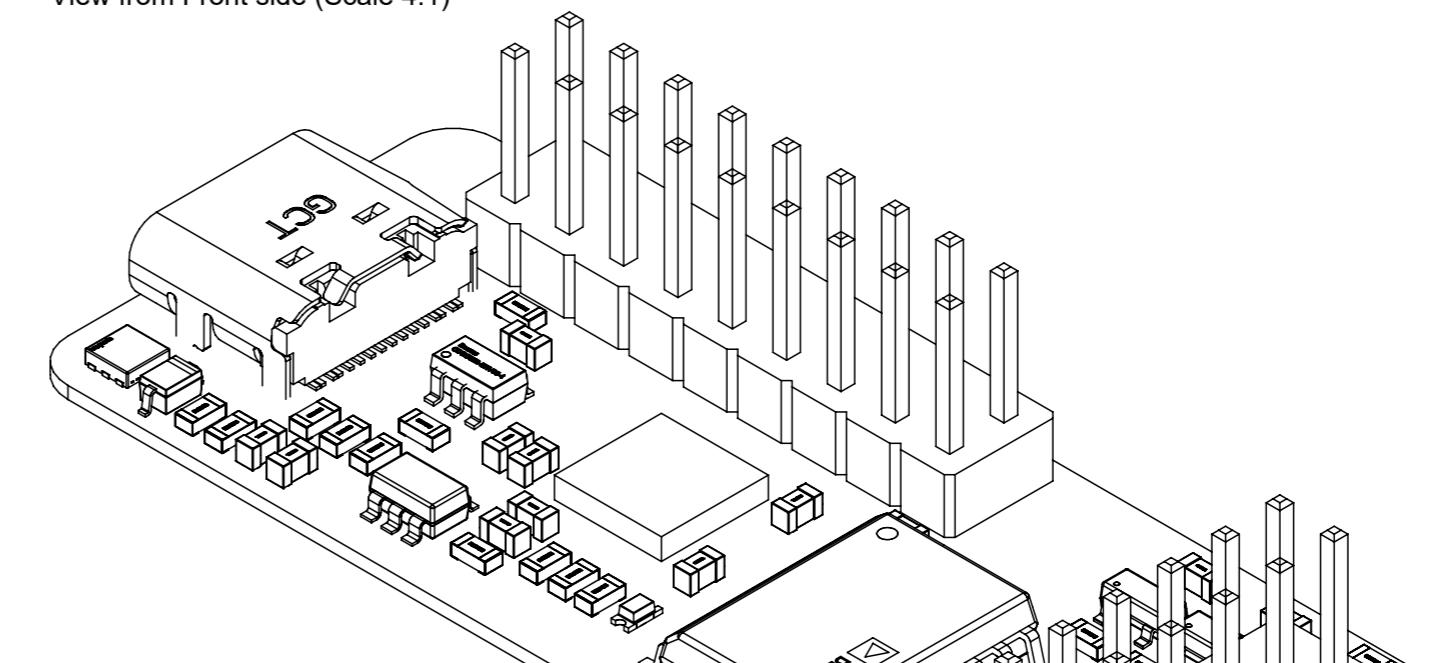
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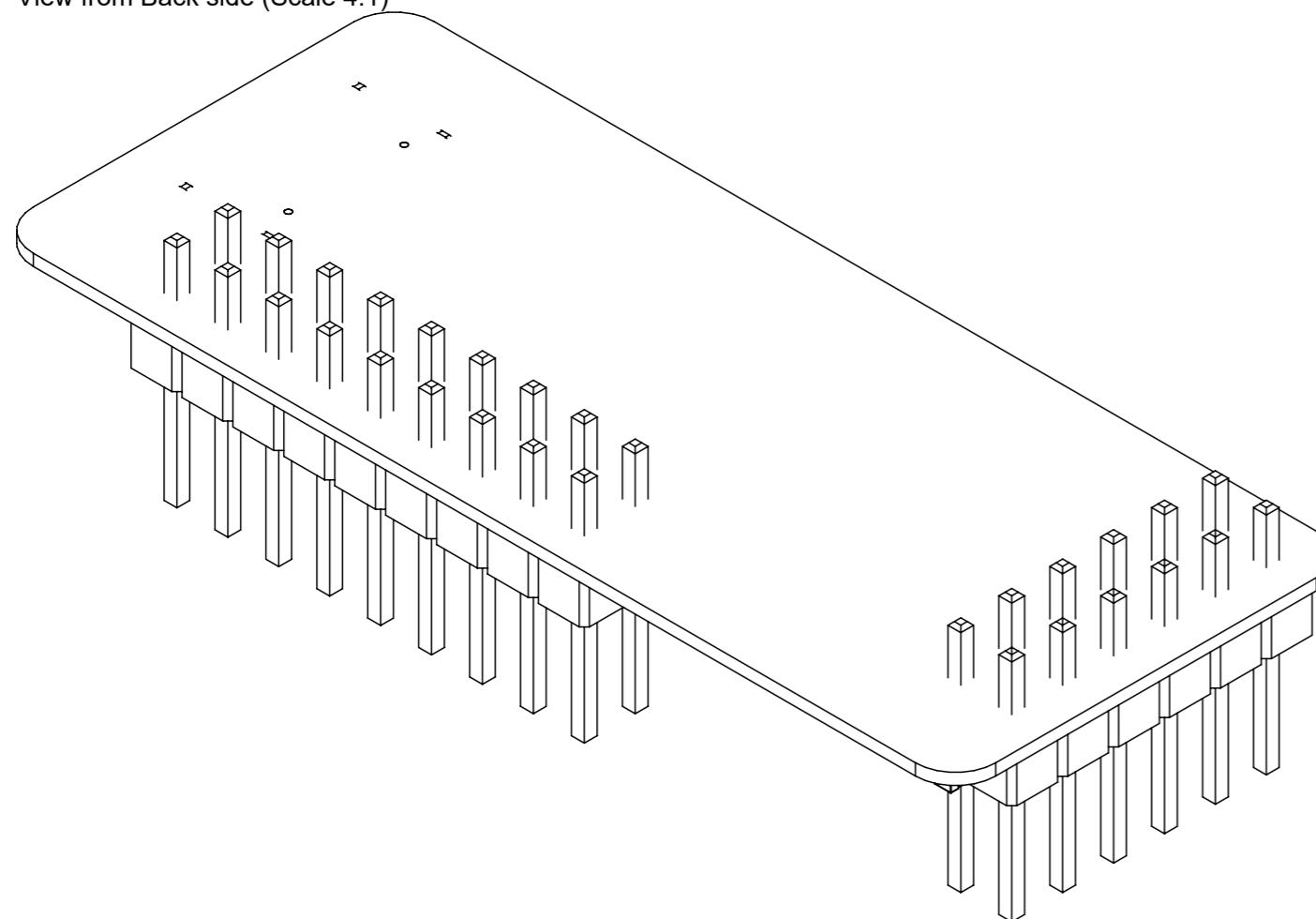
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View from Front side (Scale 4:1)



View from Back side (Scale 4:1)



Title: =ProjectTitle	Author:	CONFIDENTIAL
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Bill Of Materials

Line #	Description	Designator	Quantity	Manufacturer Part Number 1	Part Number	Layer
2	Cap Cer 0.1uF 6.3V X7R 0603	C1I, C1R, C3U	3	KGM15AR70J104KM		
	Multilayer Ceramic Capacitor, 10 uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C1L	1			
	Multilayer Ceramic Capacitor, 0.1 uF, 10 V, ± 10%, X7R, 0603 [1608 Metric]	C1P, C1U, C2L, C2U, C4I	5	C0603C104K8RAC7867		
	Cap Ceramic 0.001uF 6.3V COG 10% SMD 0603 125°C Paper T/R	C2I	1			
	Ceramic Capacitor, Multilayer, Ceramic, 10V, 10% +Tol, 10% -Tol, X5R, 15% TC, 1uF, 0603	C2R, C5I	2			
	Cap Ceramic 0.001uF 10V X7R 10% SMD 0603 125°C Paper T/R	C3I	1			
	Multilayer Ceramic Capacitor, 10 uF, 6.3 V, ± 10%, X5R, 0603 [1608 Metric]	C3L	1	CL10A106KQ8NNNC		
	Multilayer Ceramic Capacitor, 4.7 uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C4U	1	CL10A475KP8NNNC		
3	LED 0603 YELLOW SMD	D1L	1			
	TVS DIODE 5V 15V SOT23-6	D1U	1			
	Fuse PPTC SMD 0603	F1P	1			
	USB Connector Type C SMT 16 Pin (Power pins joints = 12 pins)	J1C	1			
		J2C	1			
		J3C	1			
	PMPB14XPZ	Q1P	1	PMPB14XPZ		
	Trans Gp Bjt NPN 25V 1.5A 300MW 3-PIN SOT-23 T/r	Q1R, Q2R	2	SS8050-G		
	Surface Mount Thick Film Chip Resistor 0603 Case 1.69K Ohms 1% Tolerance 100 PPM	R0L	1	MCR03EZPFX1691		
4	SMD Chip Resistor, 5.1 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1C, R2C	2	CRCW06035K10FKEA		
	Res Thick Film 0603 33K Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD Automotive T/R	R1L	1	ERJ-3EKF3302V		
	SMD Chip Resistor, 100 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1P	1	AC0603FR-07100KL		
	SMD Chip Resistor, 10 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1R, R1U, R2R, R2U, R3L, R3R, R4R	7	RC0603FR-0710KL		
	SMD Chip Resistor, 20 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R2L	1	CR0603-FX-2002ELF		
	Res Thick Film 0603 2.49K Ohm 1% 1/10W ±100ppm/°C Molded SMD SMD Paper T/R	R4L	1			
	DGTL ISO 3750VRMS 4CH GP 16SOIC	U1I	1			
	LDO U-Reg Adj 0, 3A SOT23-5	U1L	1			
5	Single-Chip USB to UART Bridge, 1024 Bytes EEPROM, -40 to 85 degC, 28-pin QFN, Tube	U1U	1			
	MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323 ON Semiconductor MM3Z12VST1G	ZD1P	1			

Please consider LCSC (立创商城) as our first supplier

BOM FOR REFERENCE ONLY

ALWAYS REFER TO THE LATEST EXCEL BOM PROVIDED

Title: =ProjectTitle	Author:	CONFIDENTIAL
Size: A3	Approved:	My Company Address Line 1 Address Line 2 Address Line 3 Address Line 4
Unit: mm	Edited: 22-11-2024	
Prj: =ProjectTitle	Variant: [No Variations]	
Date: 23-11-2024 03:04 AM	Sheet 9 of 9	
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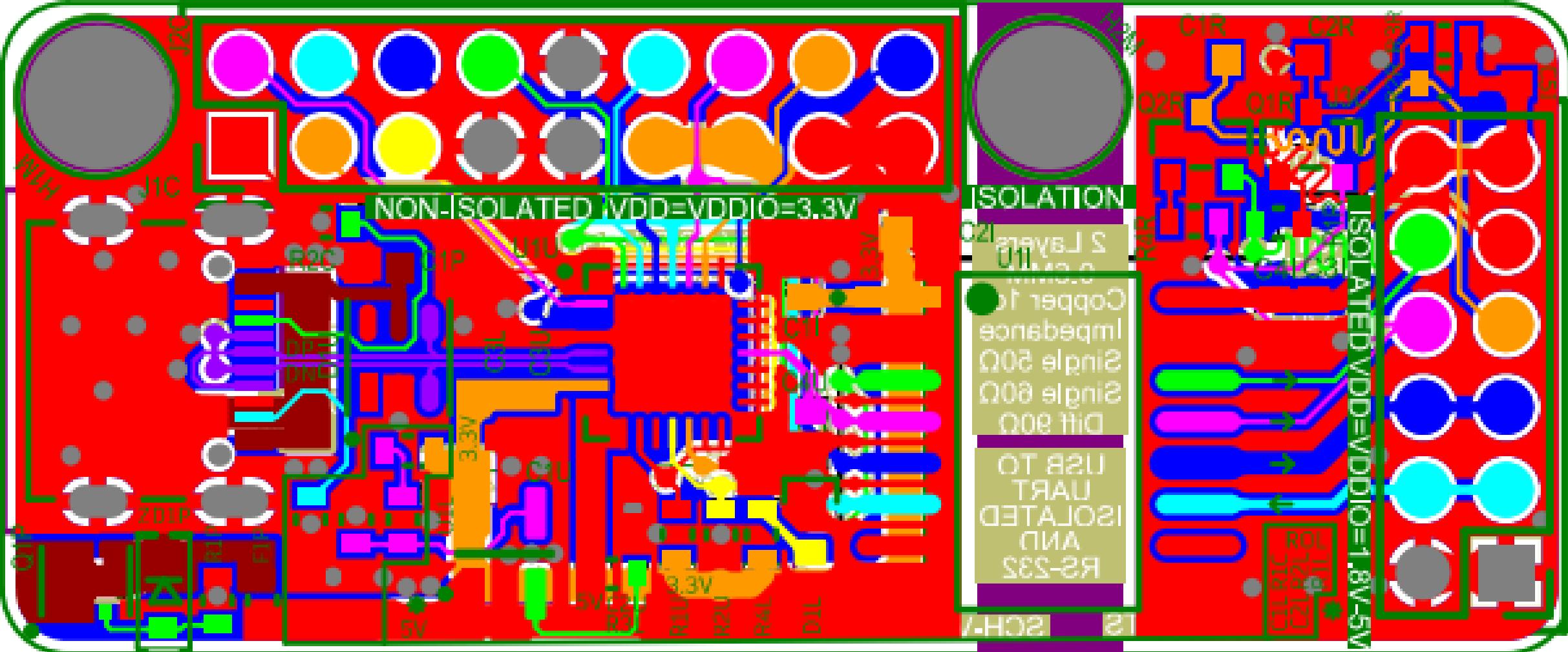
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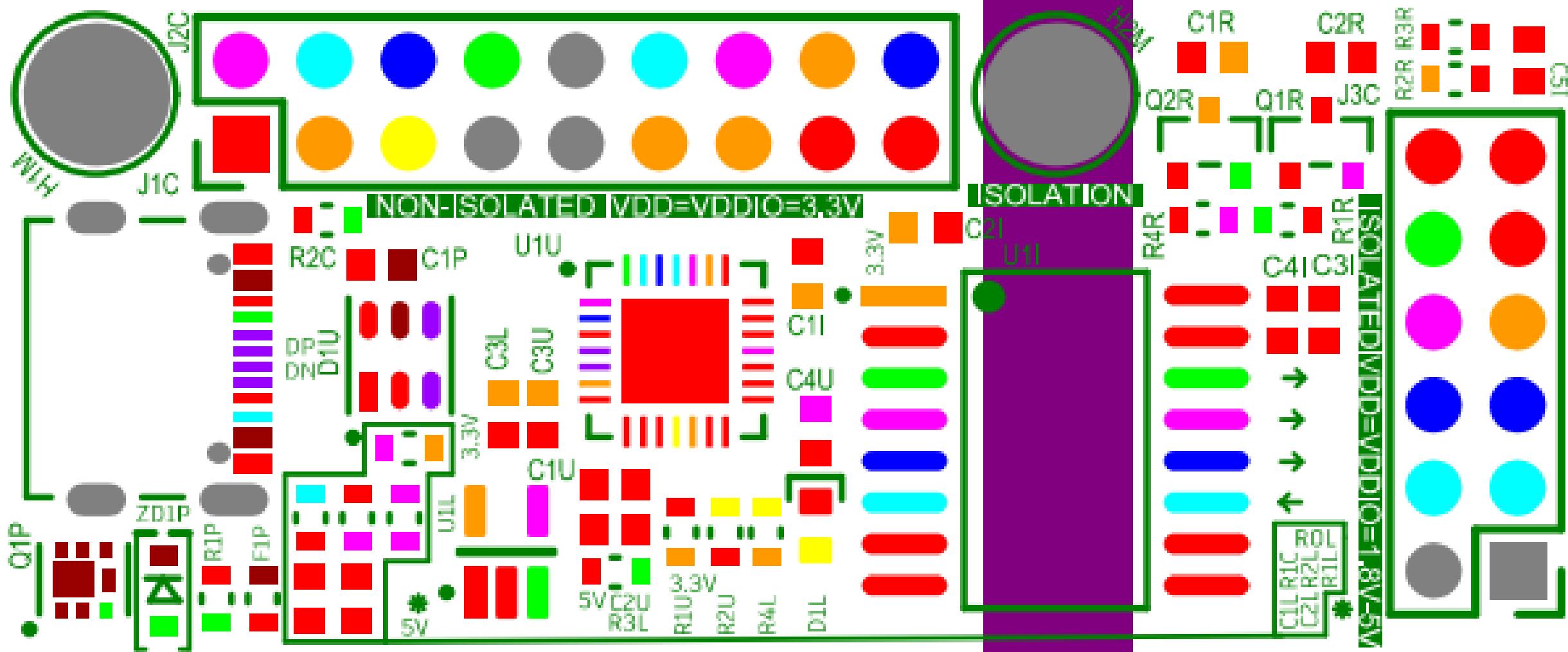
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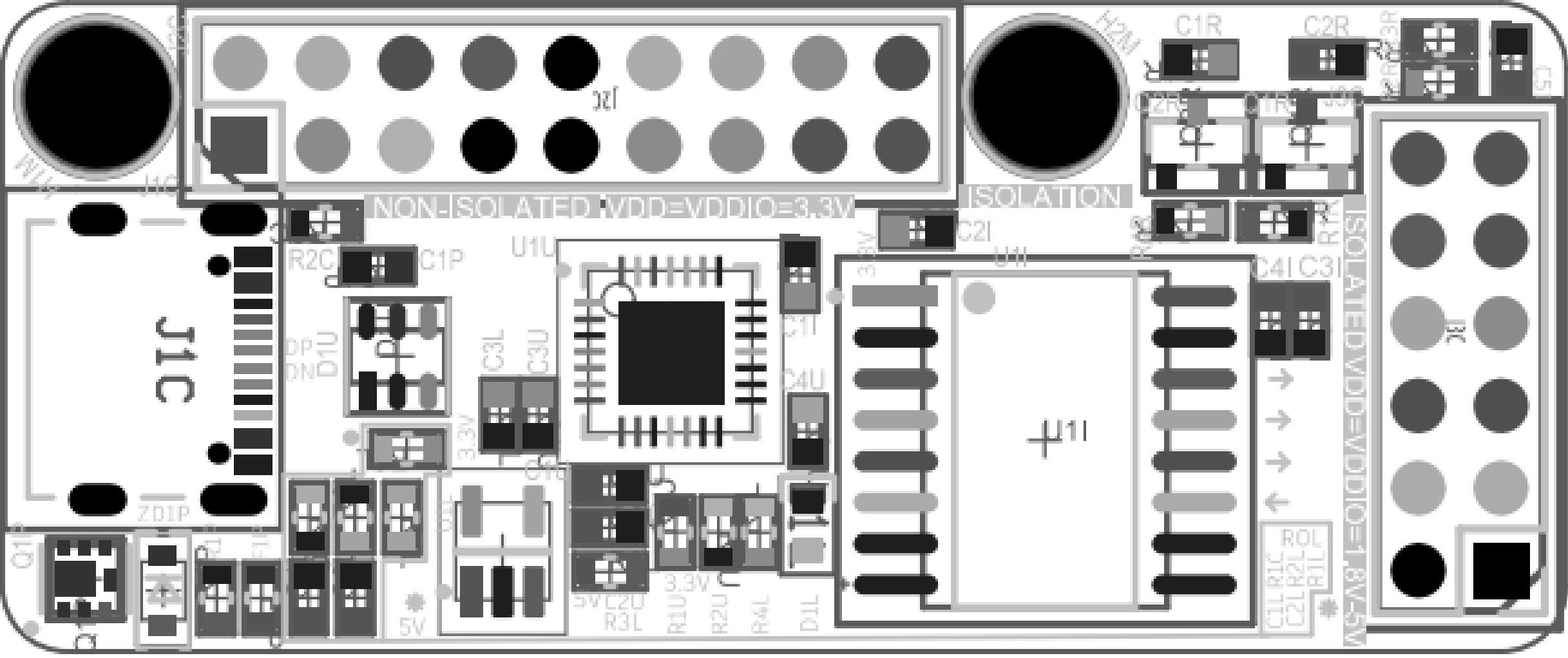
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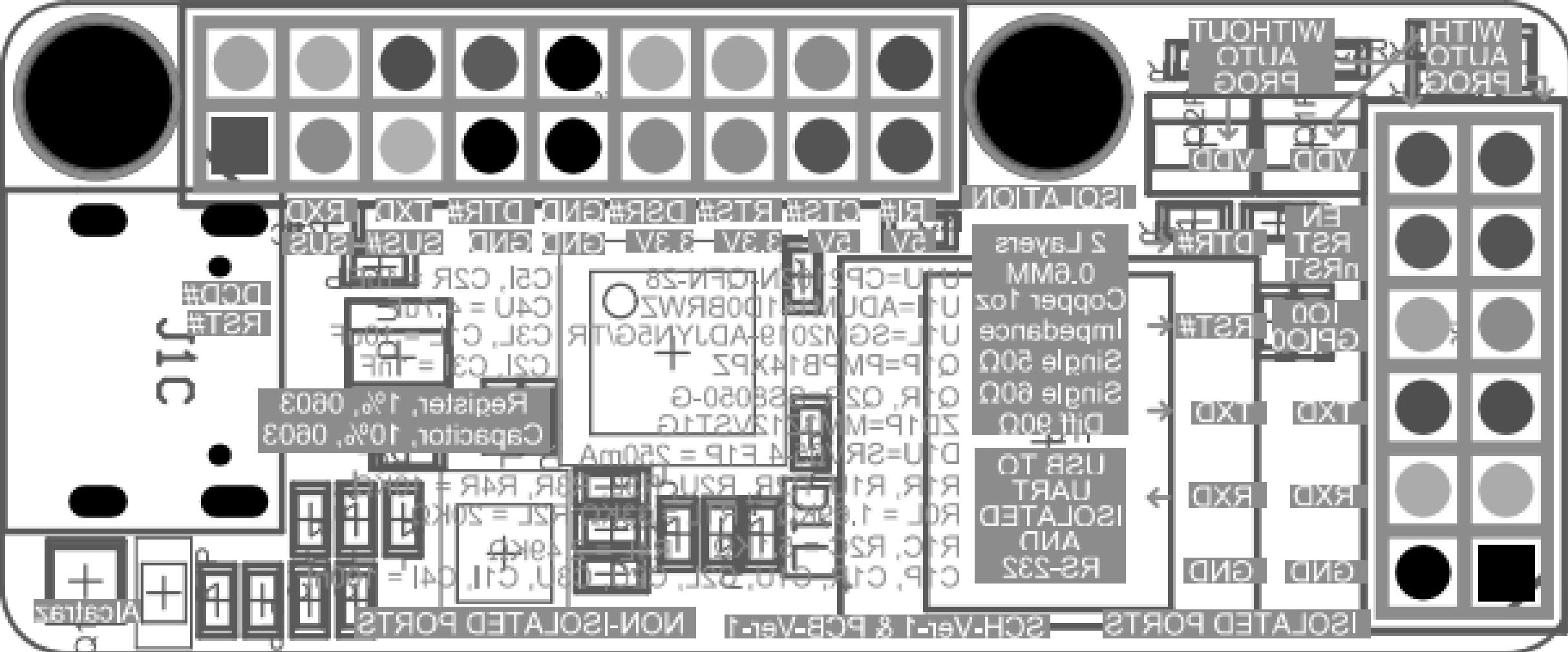
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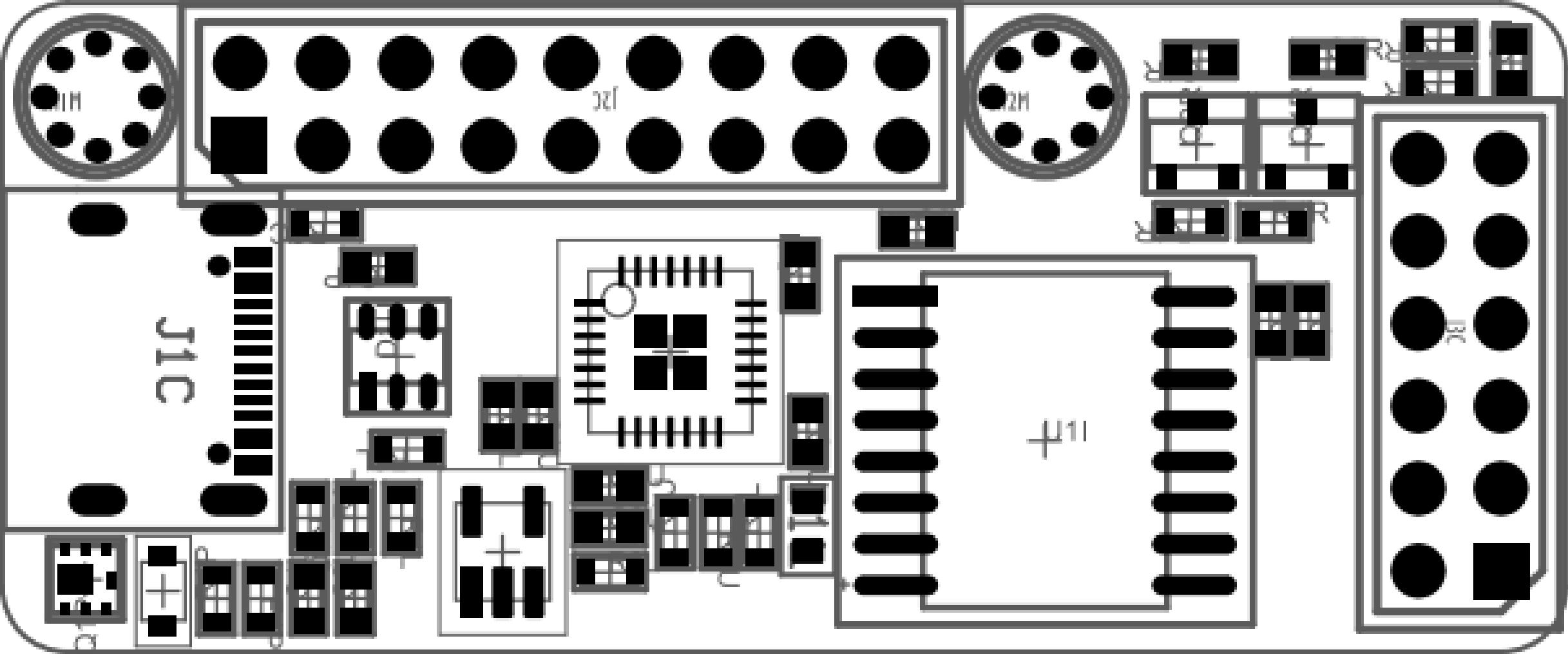


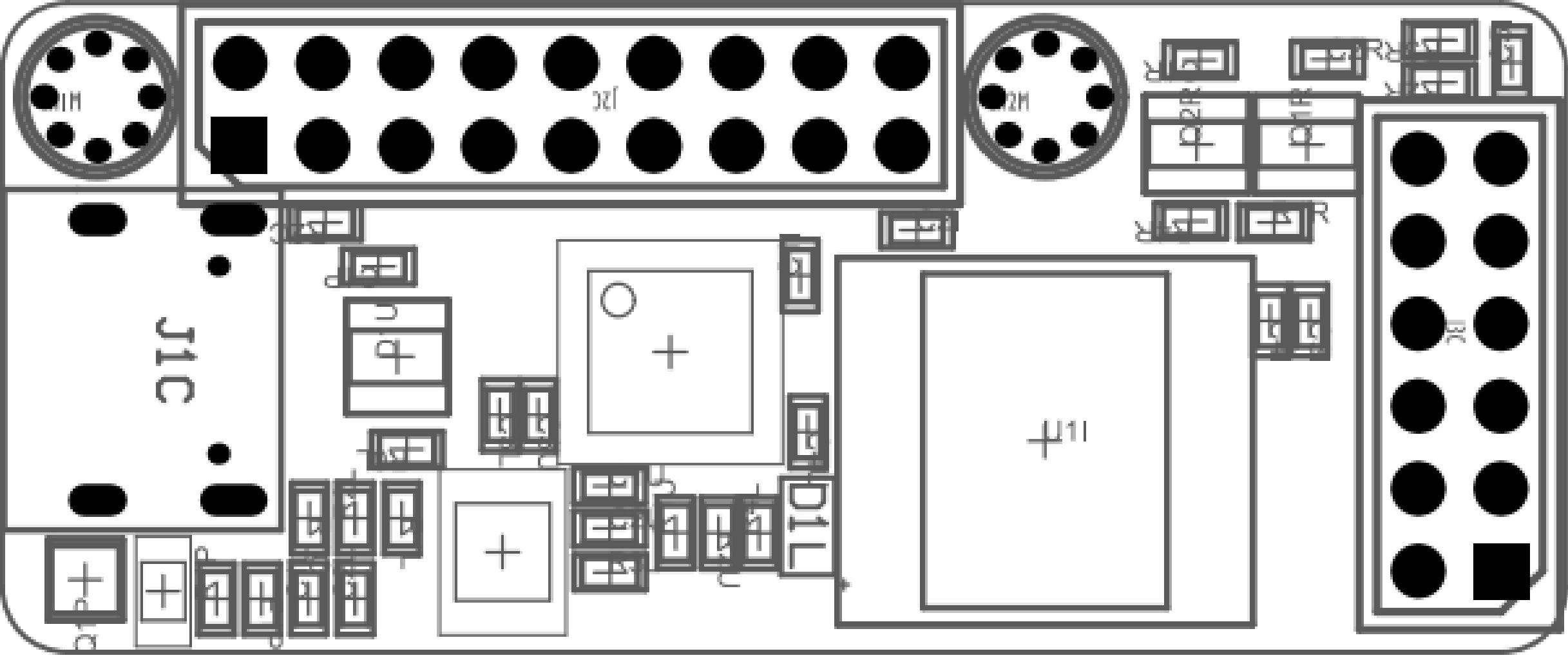


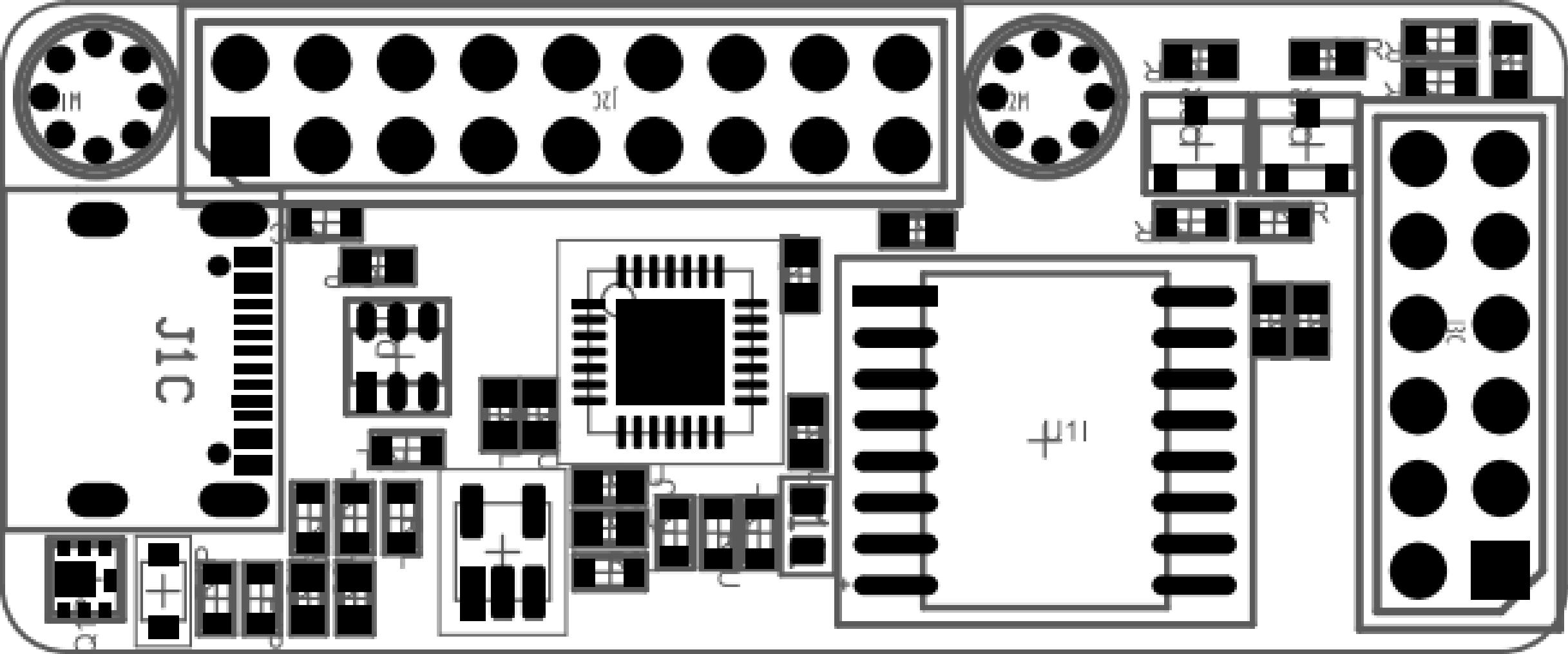


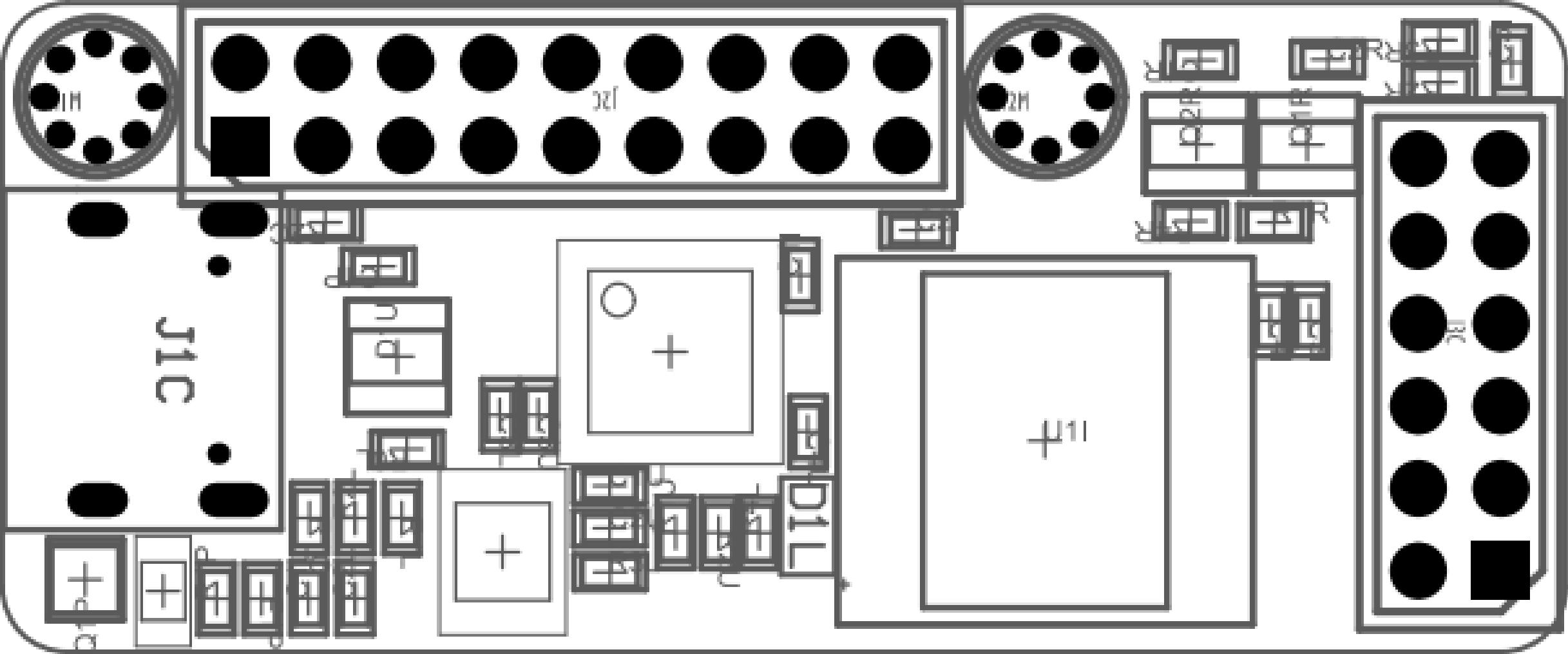


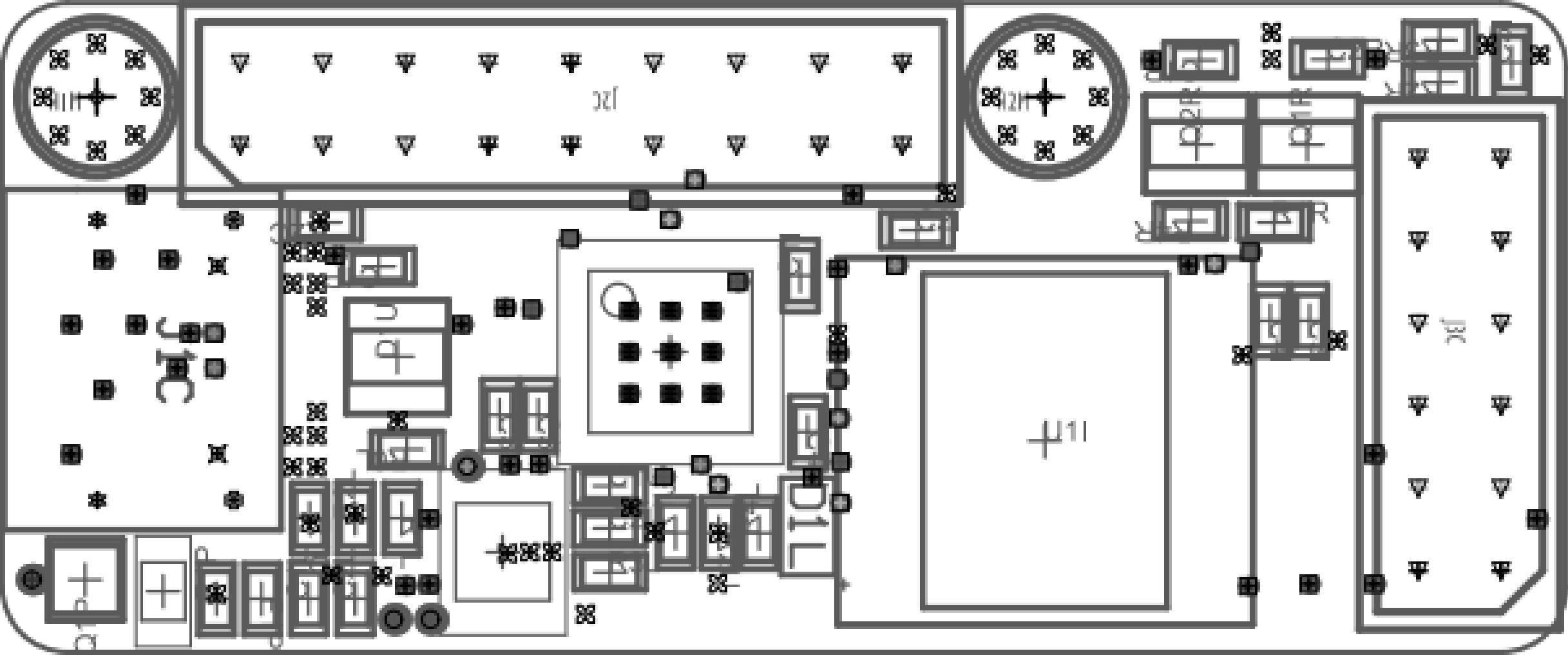


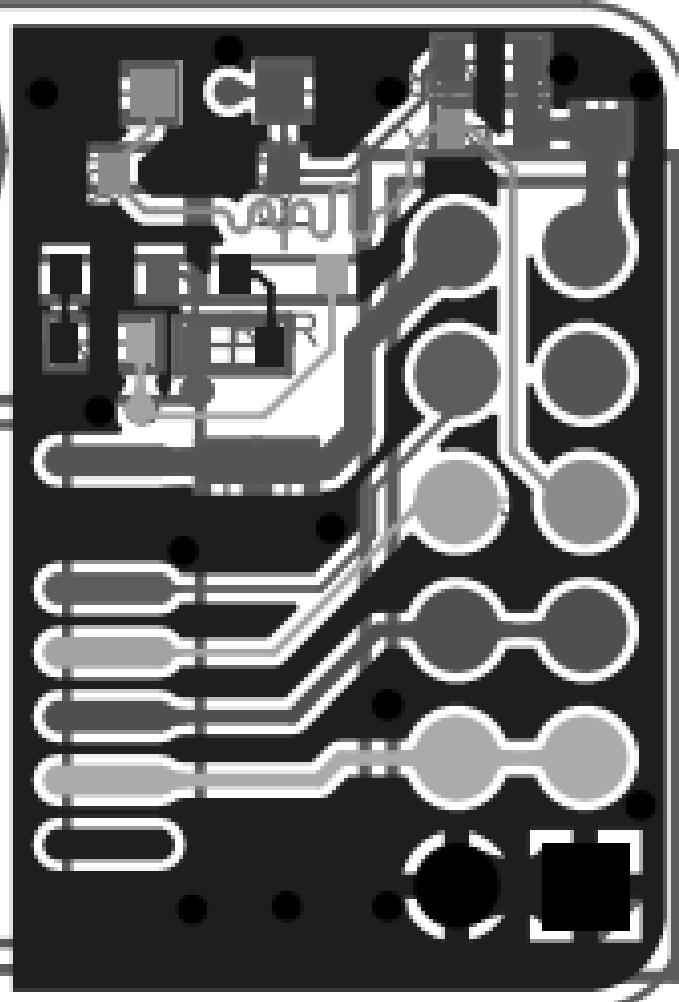
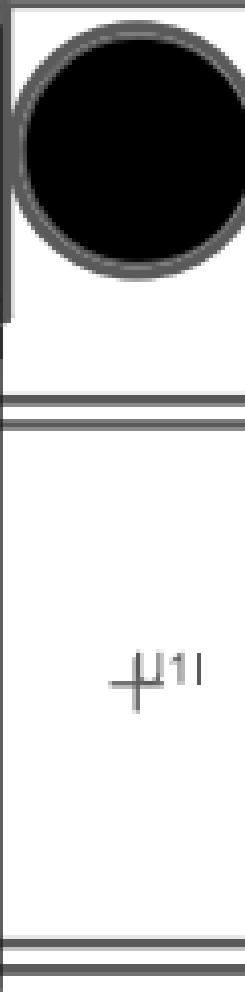
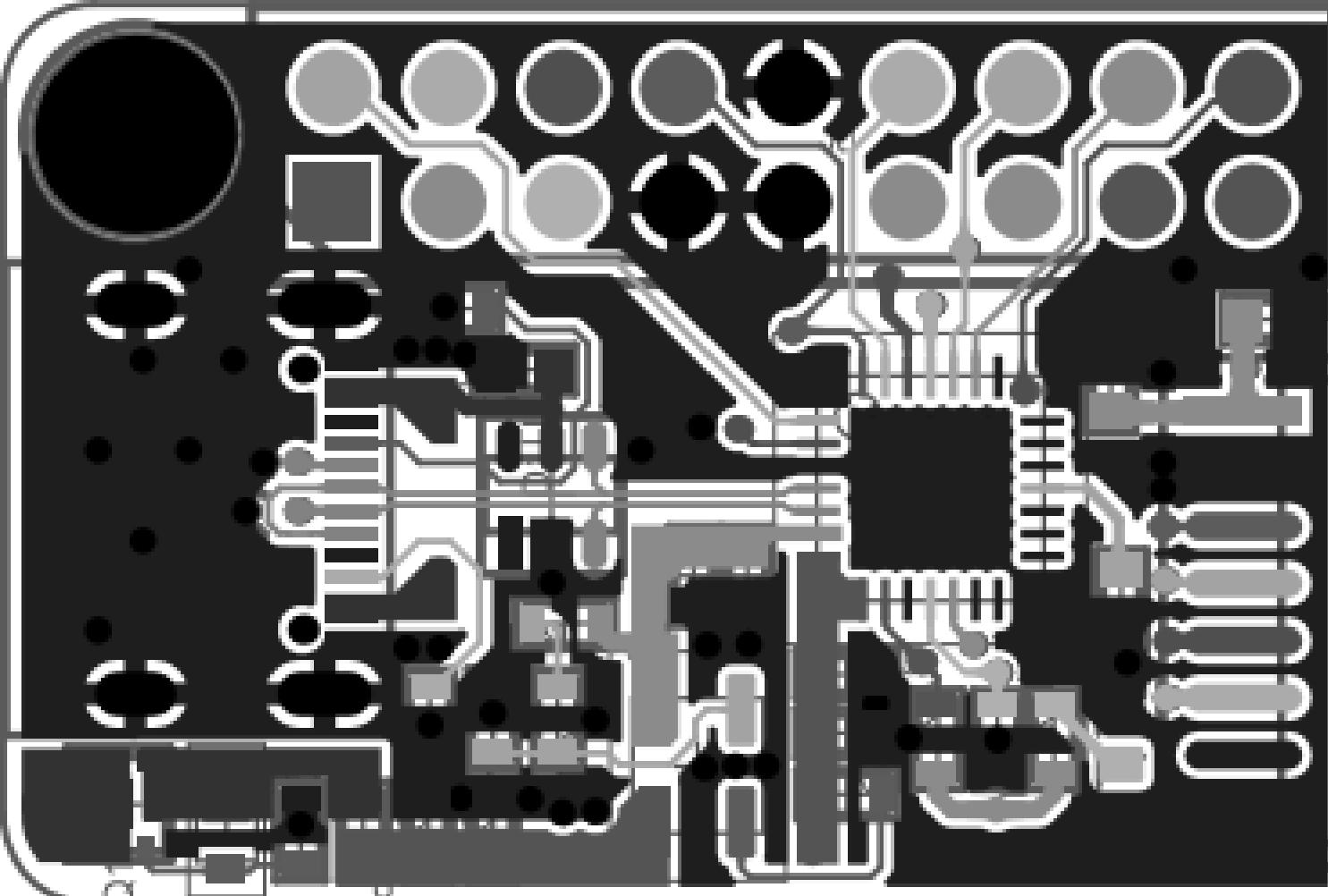


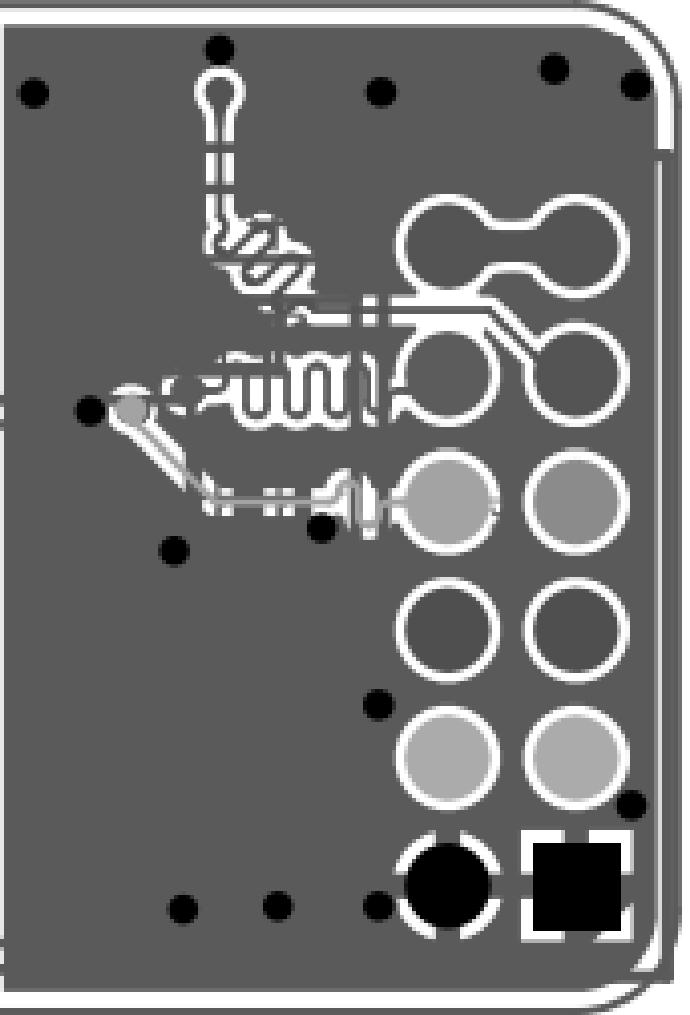
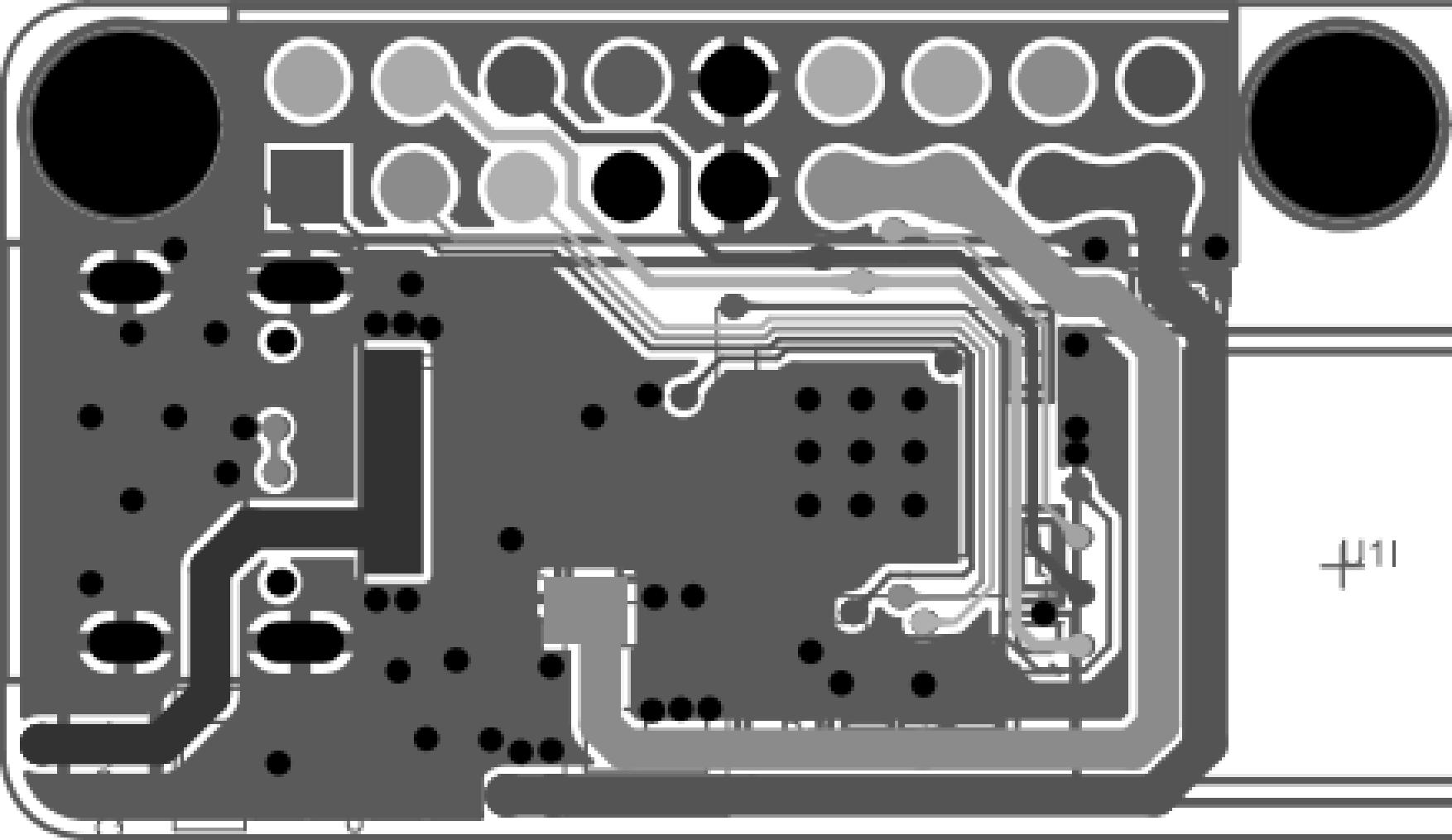


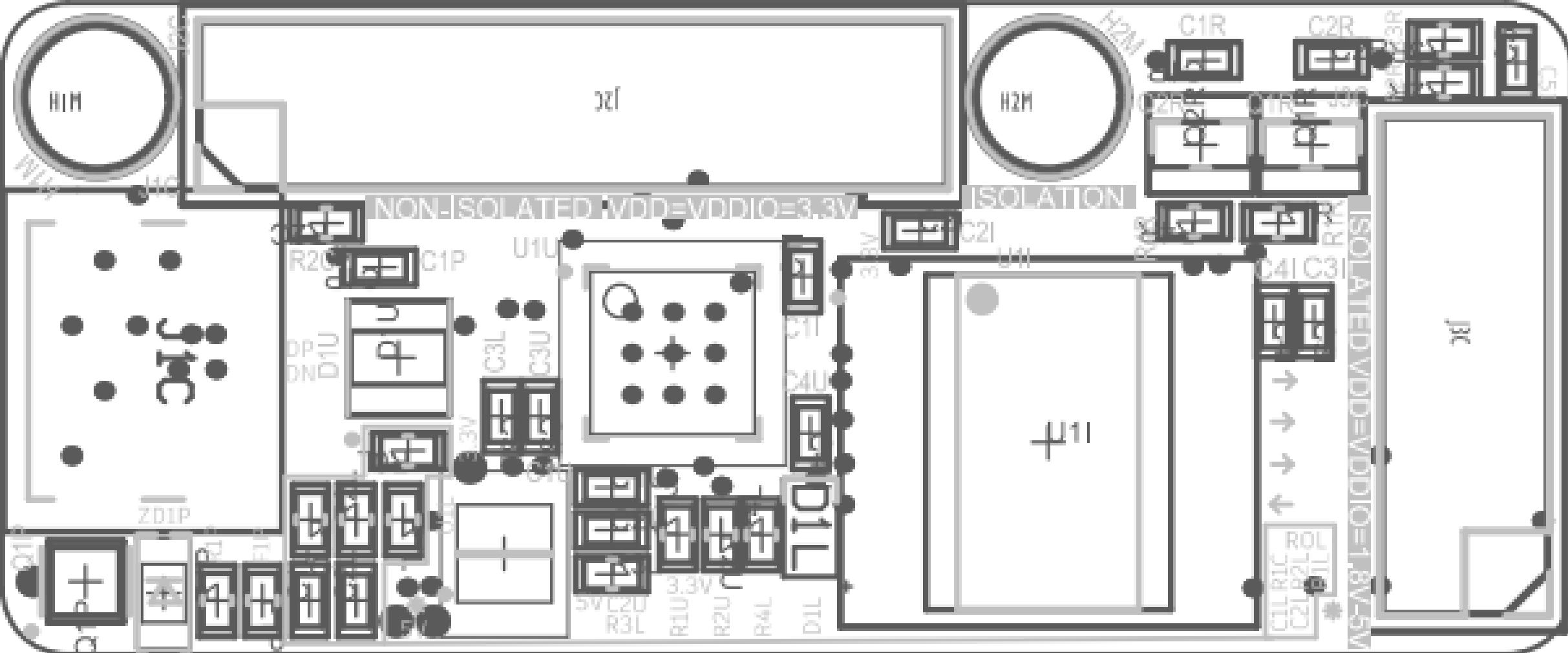


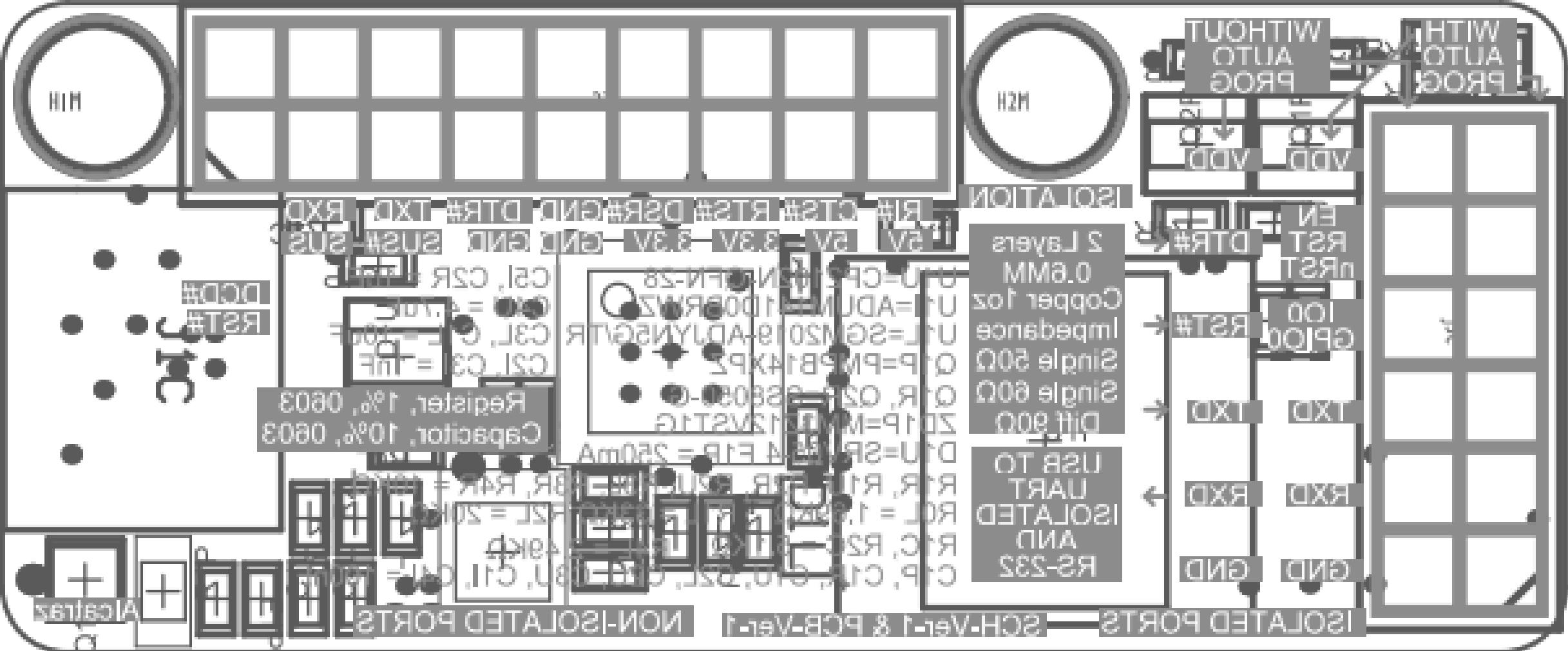


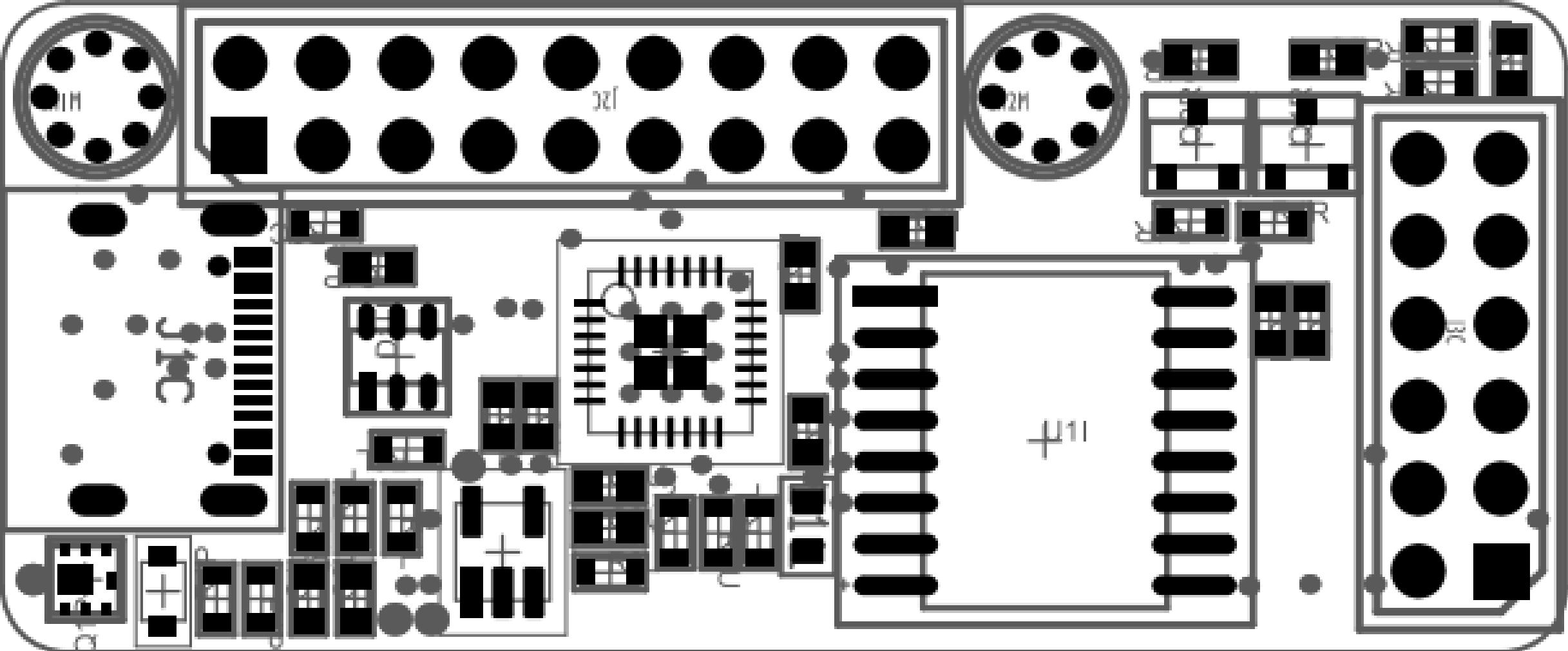


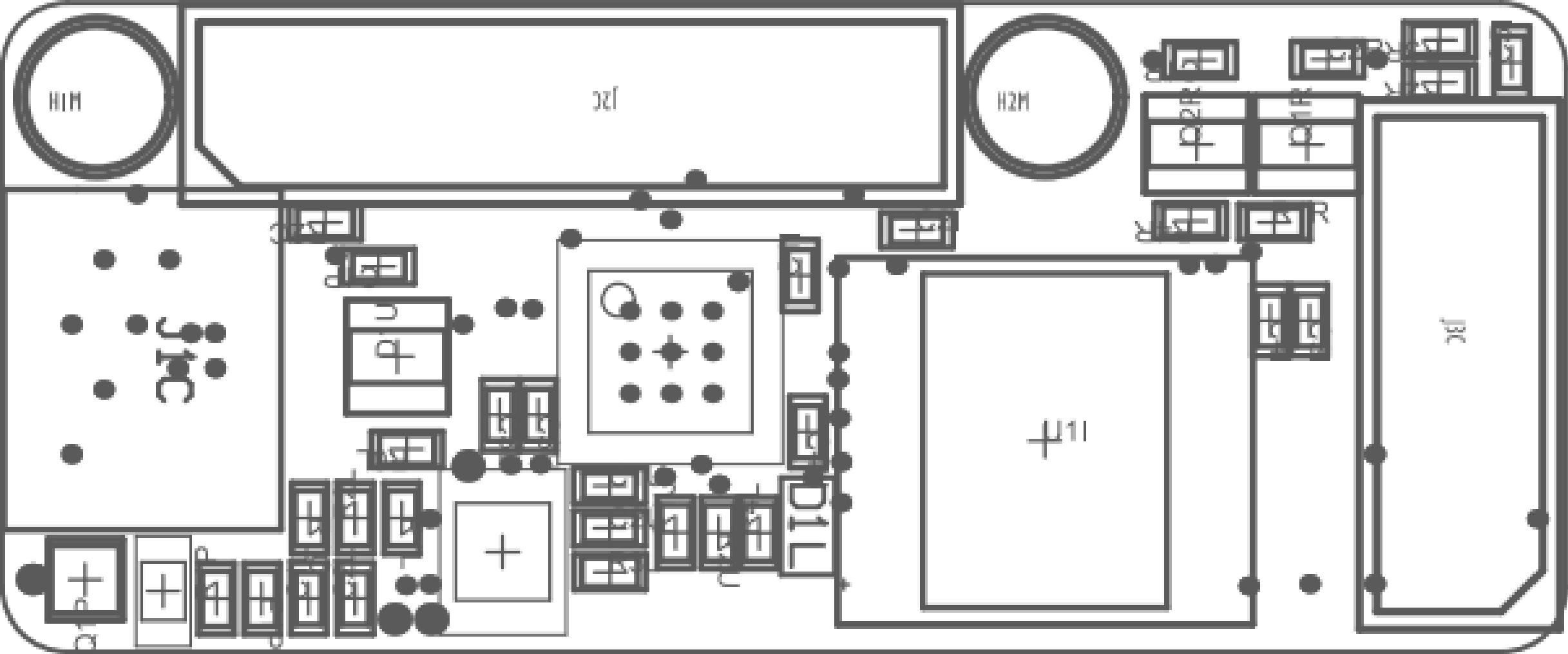


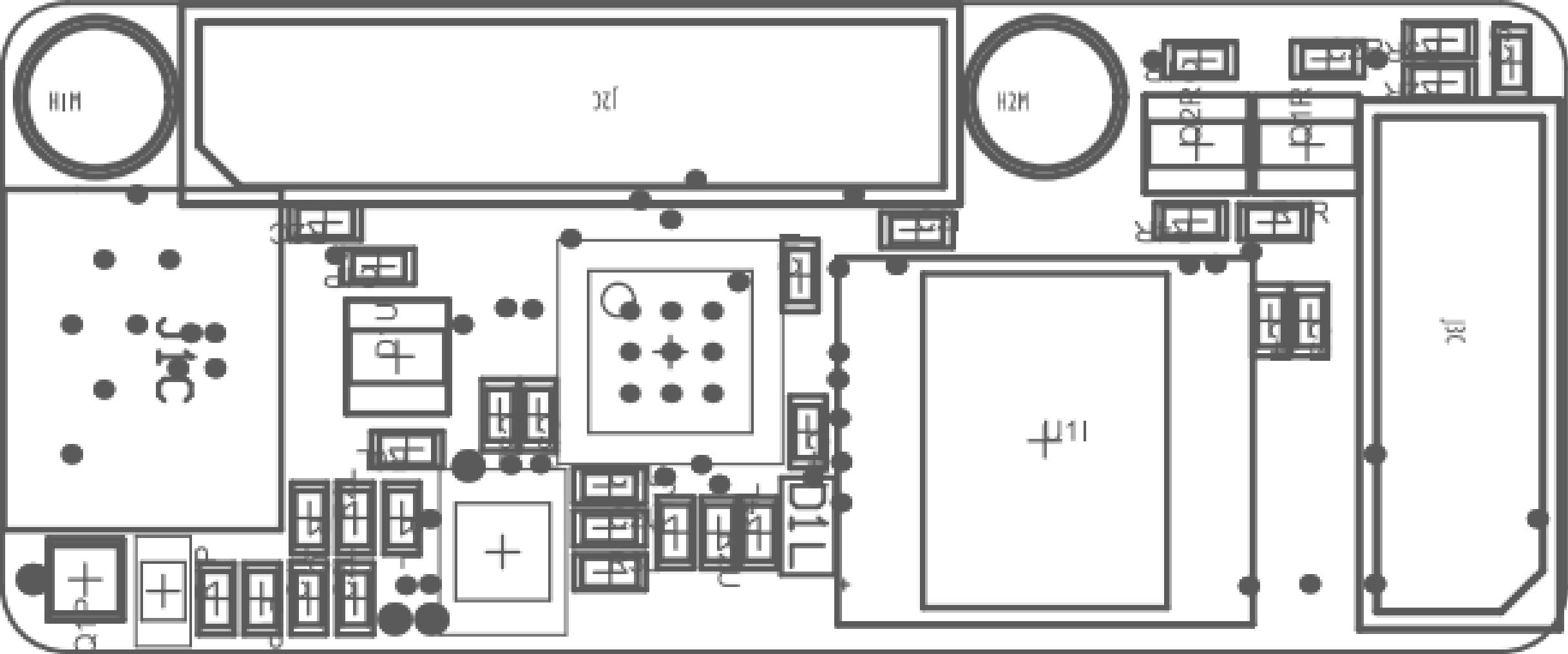


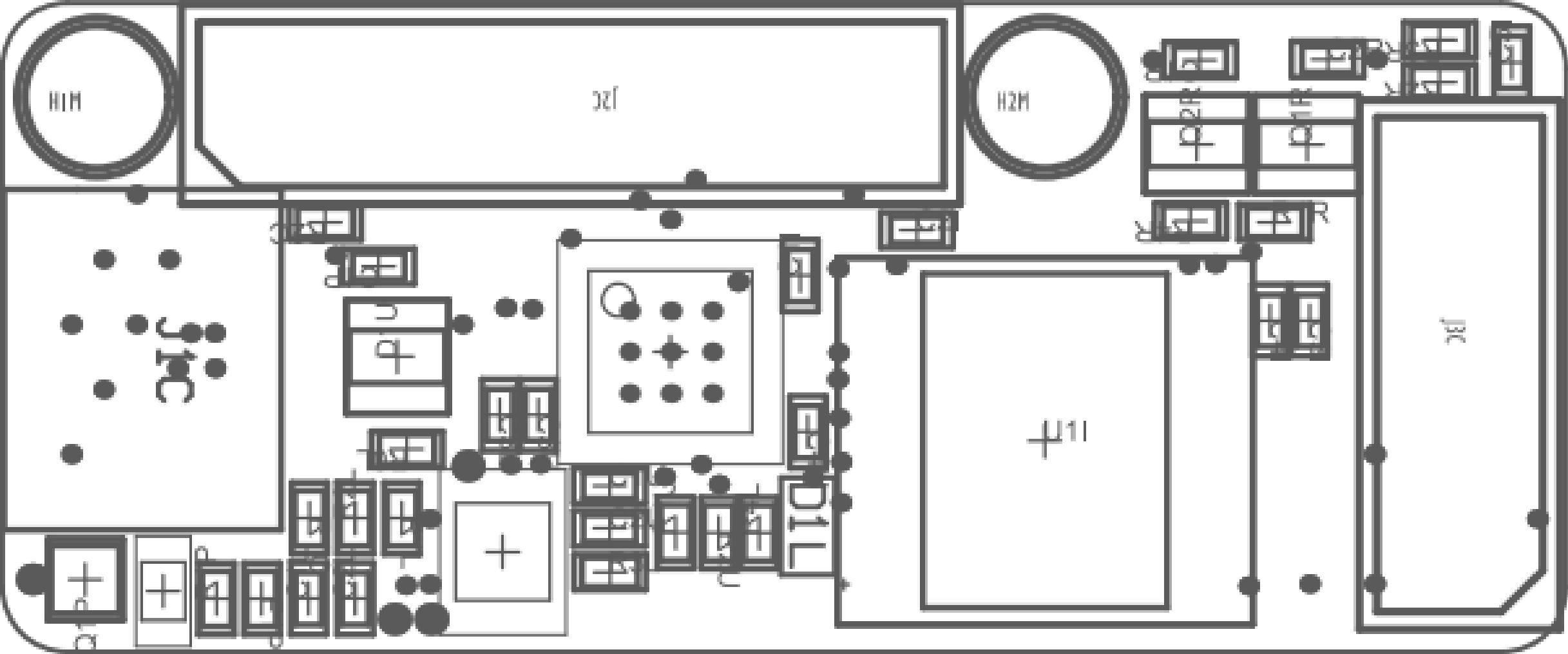


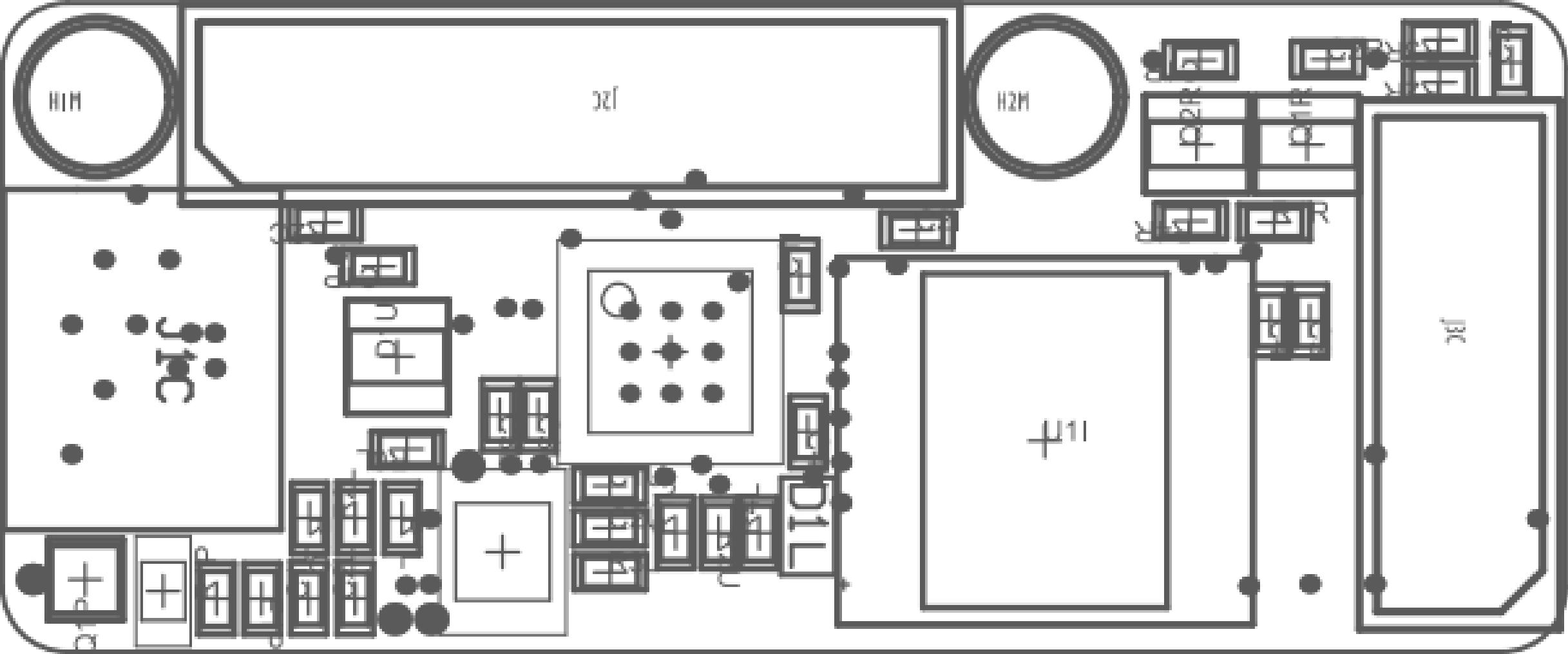


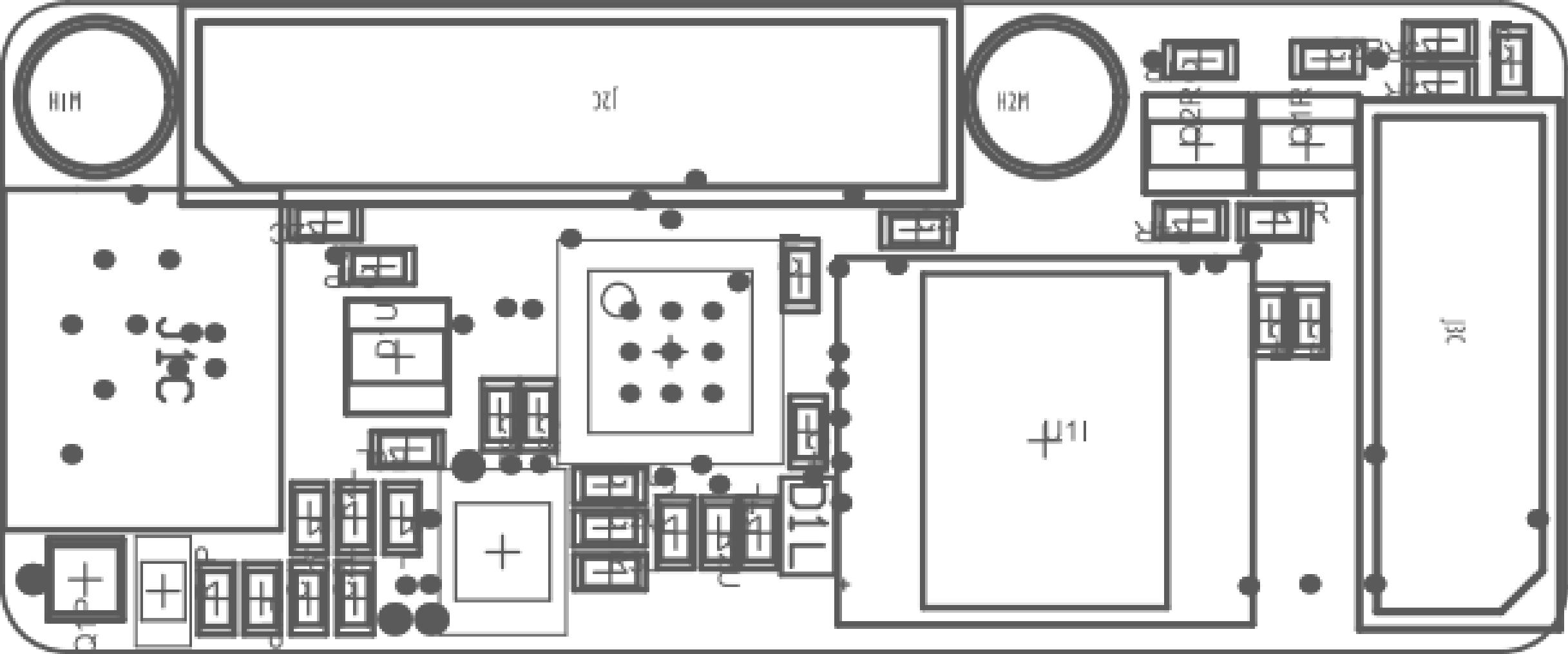


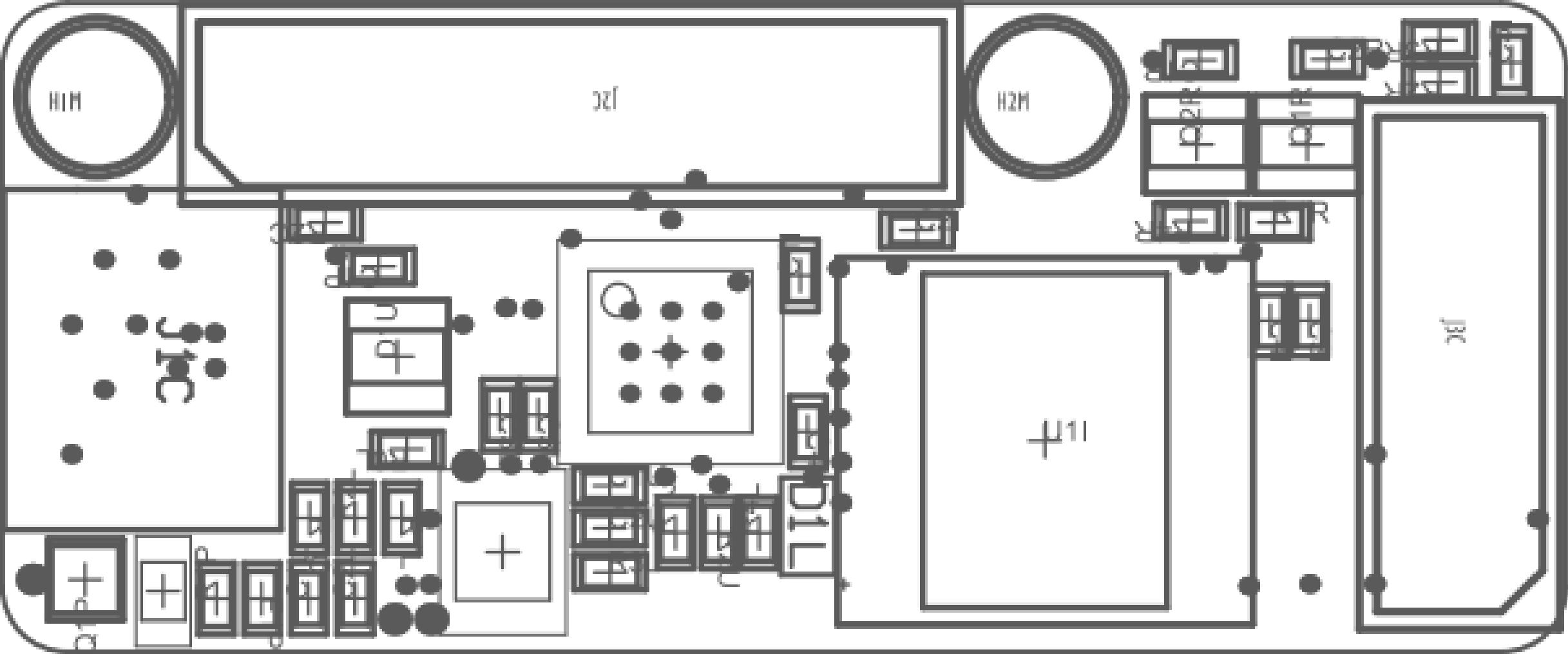


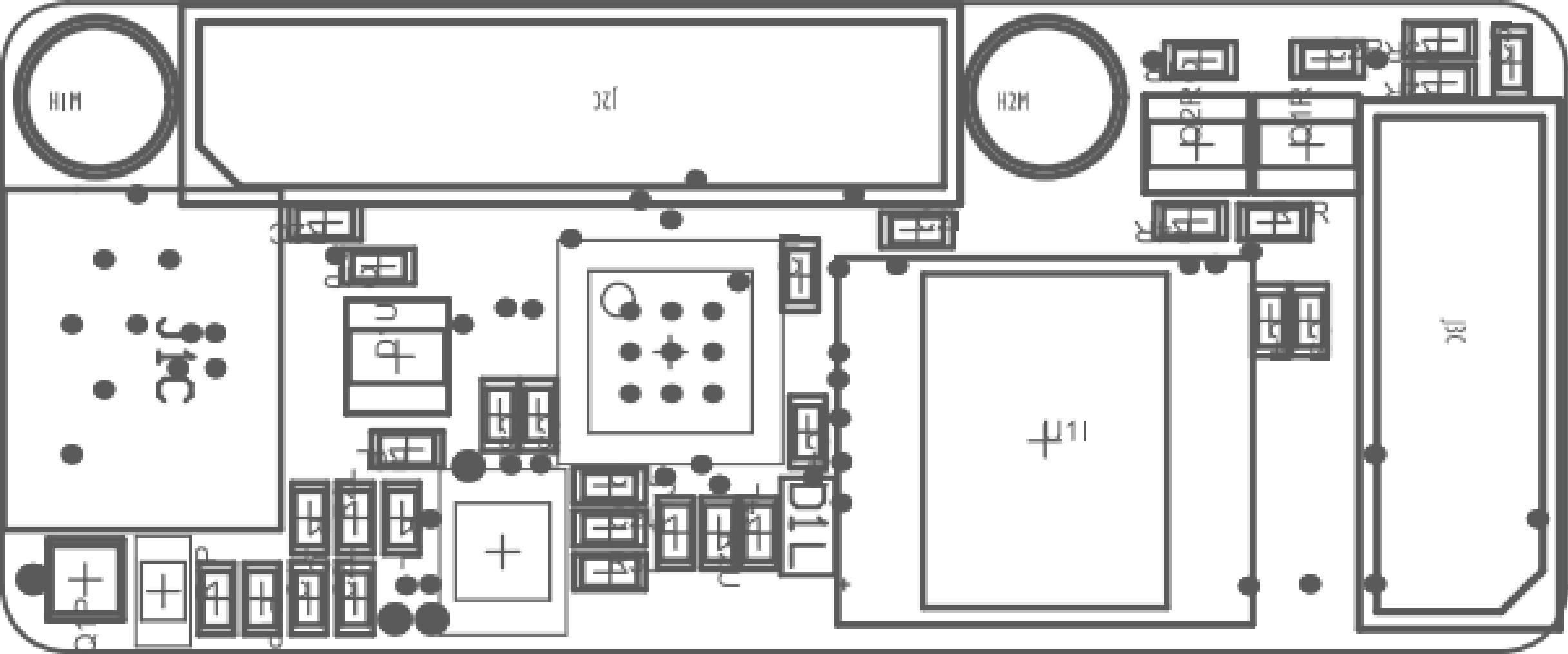


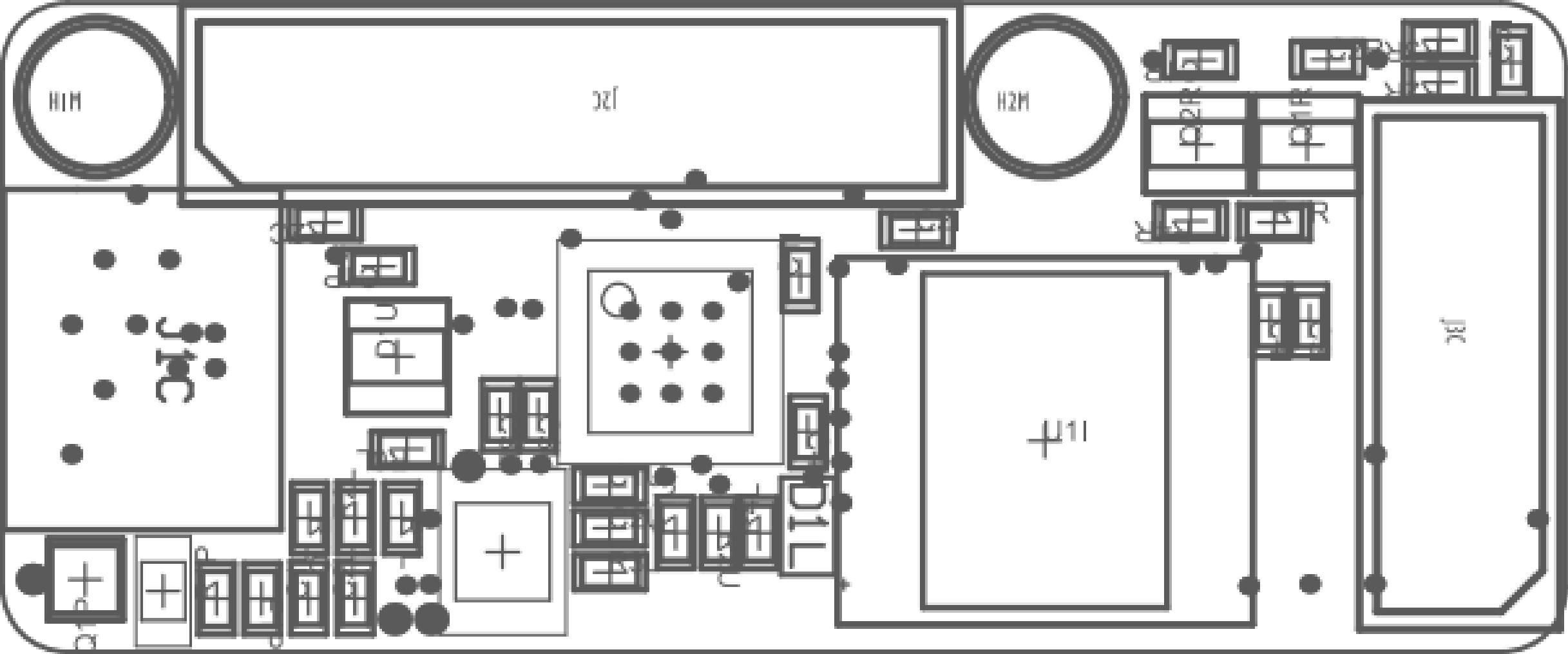


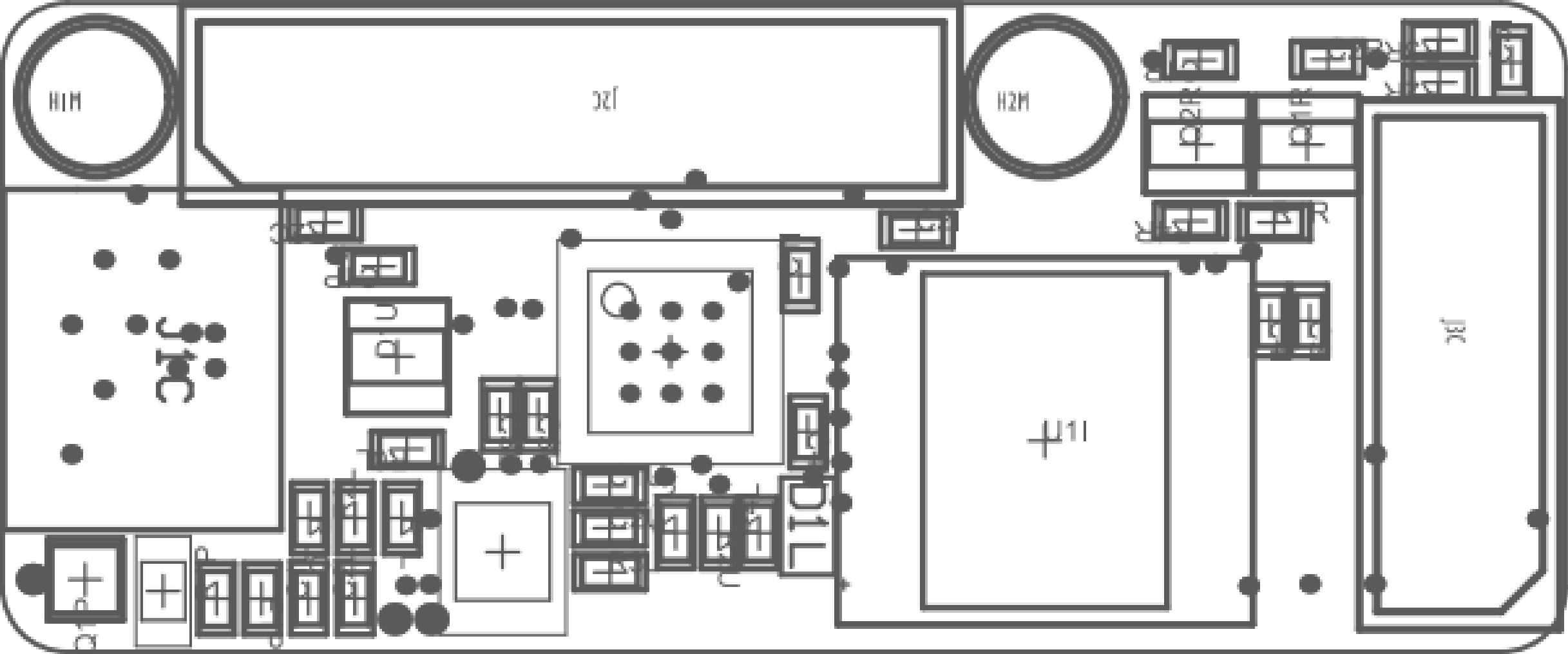


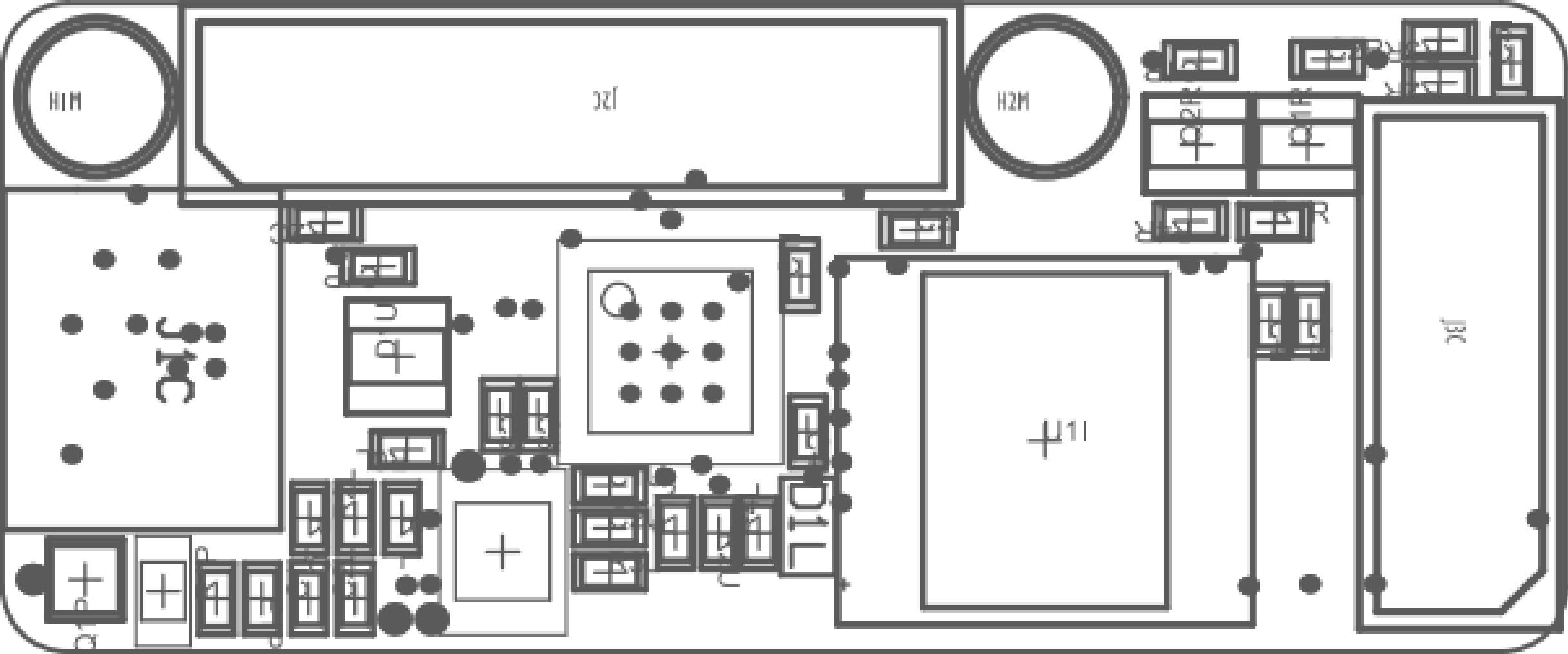


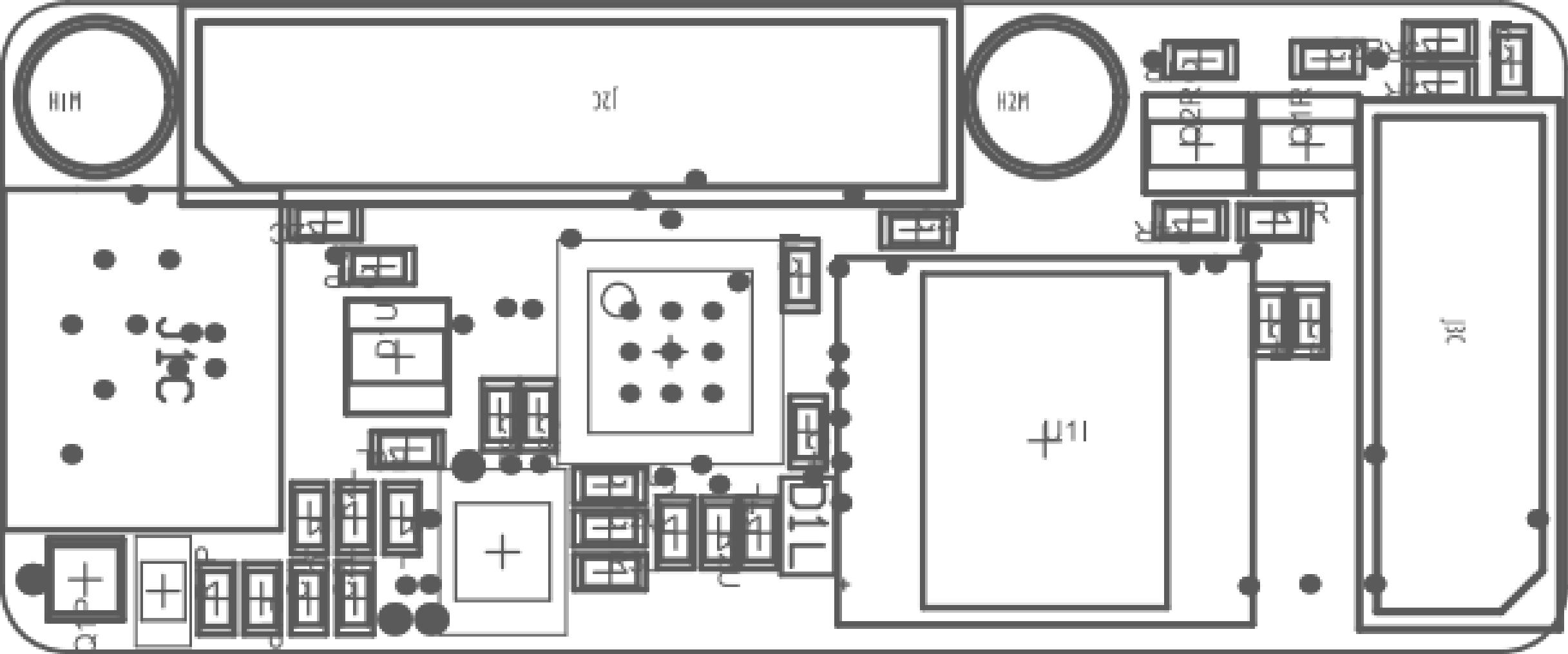


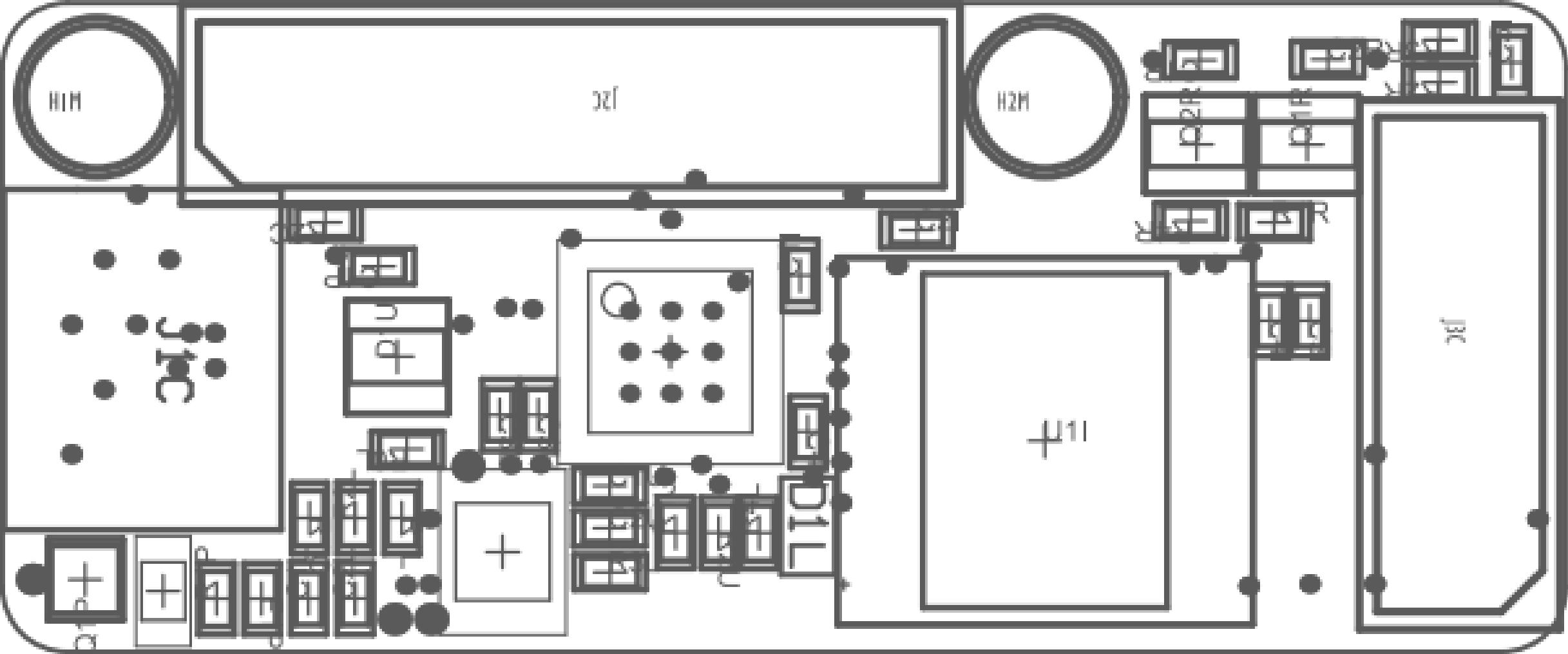


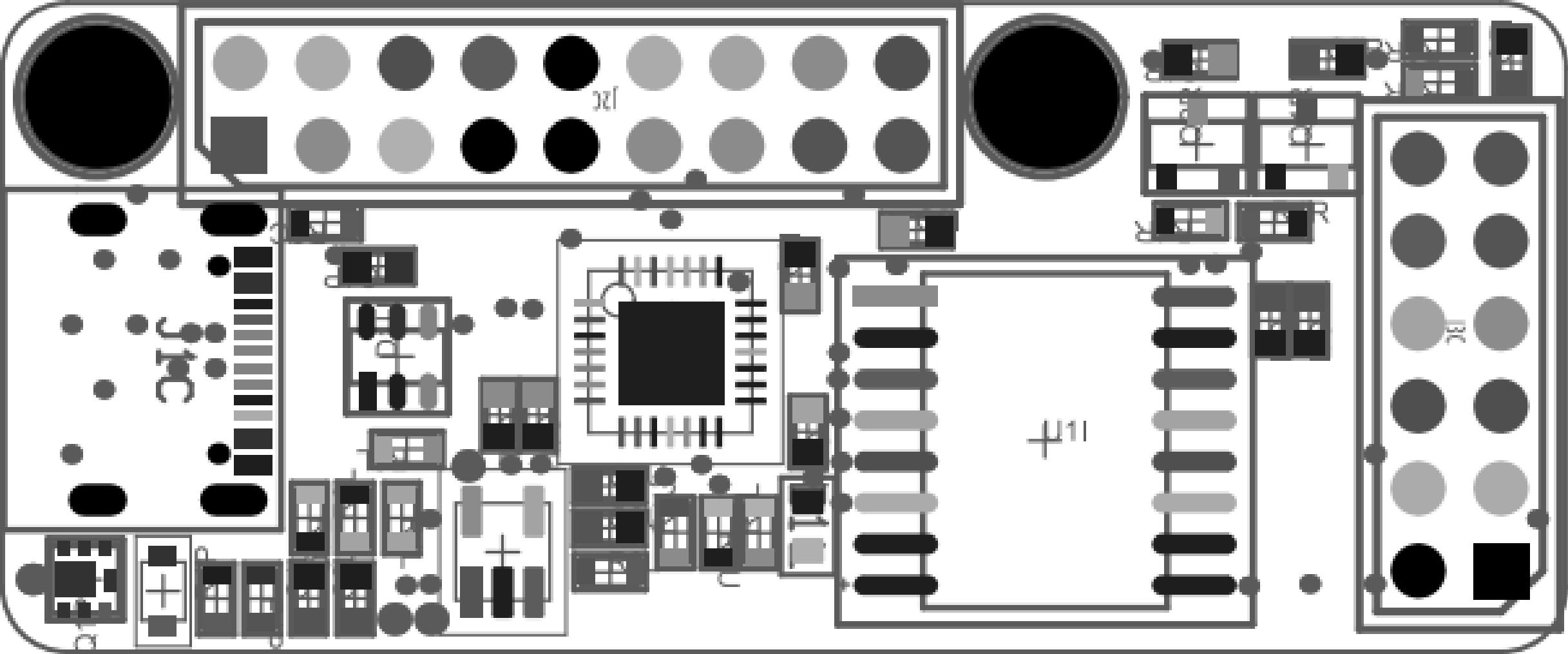


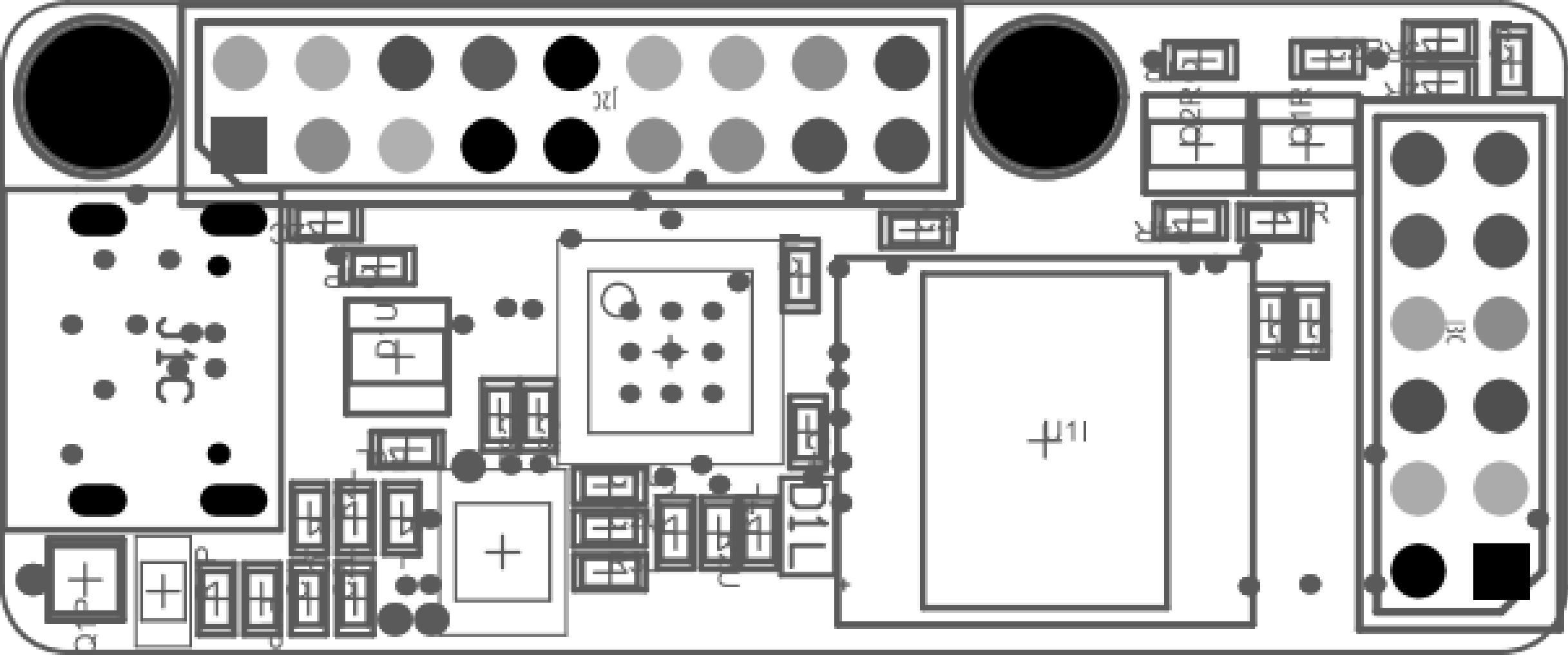


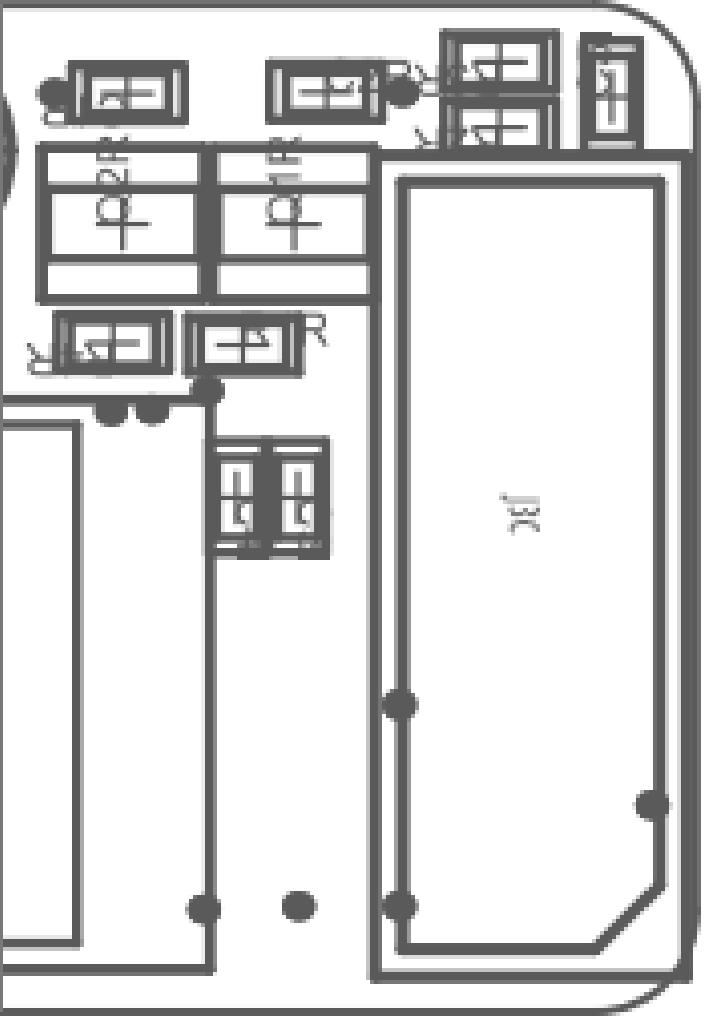
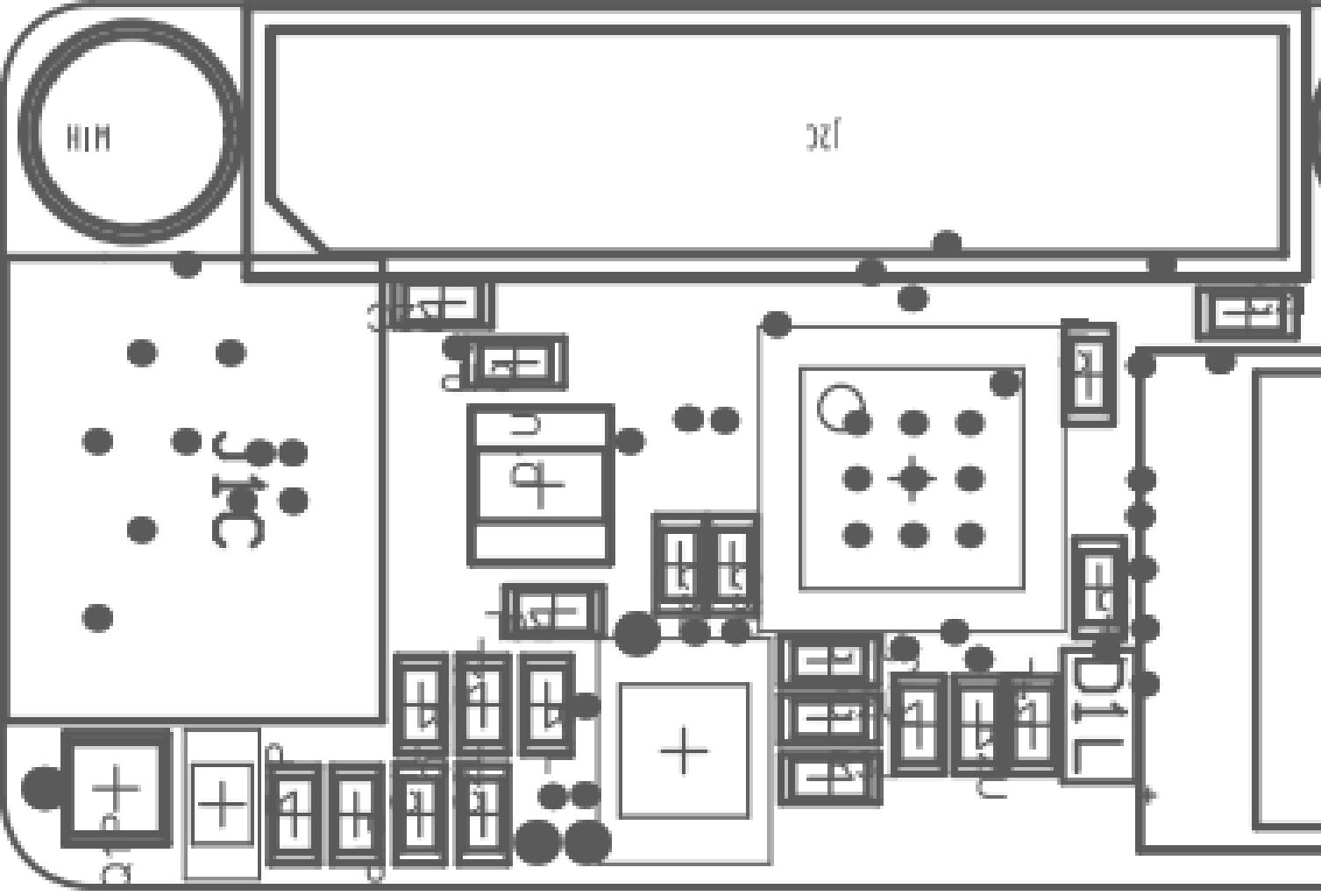


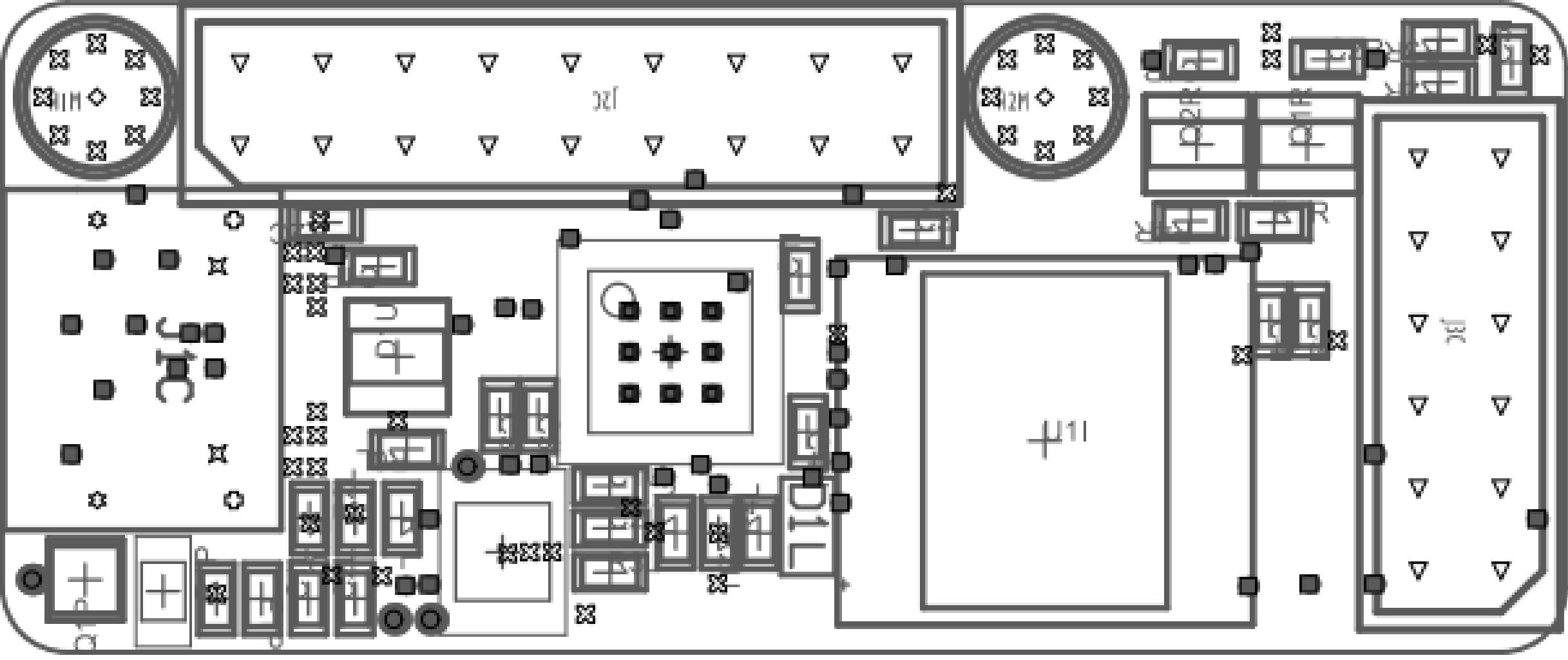


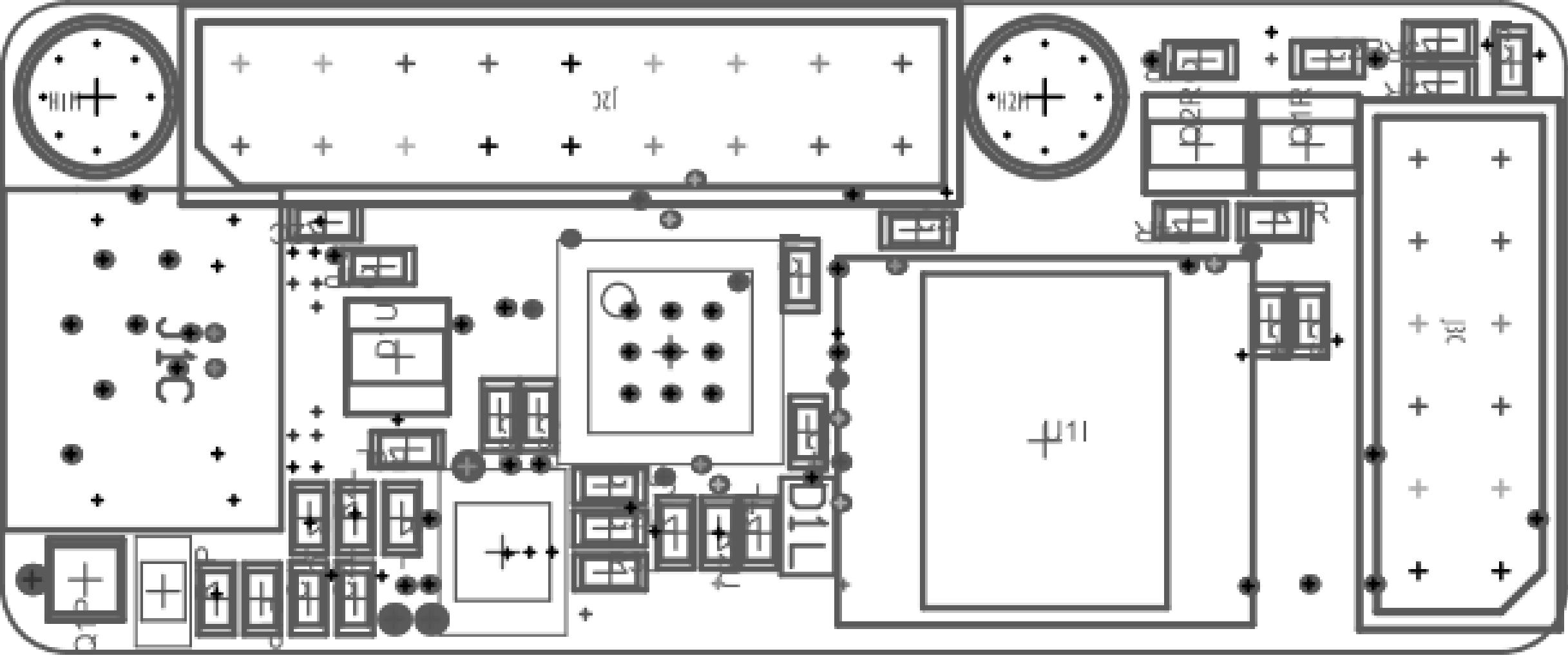


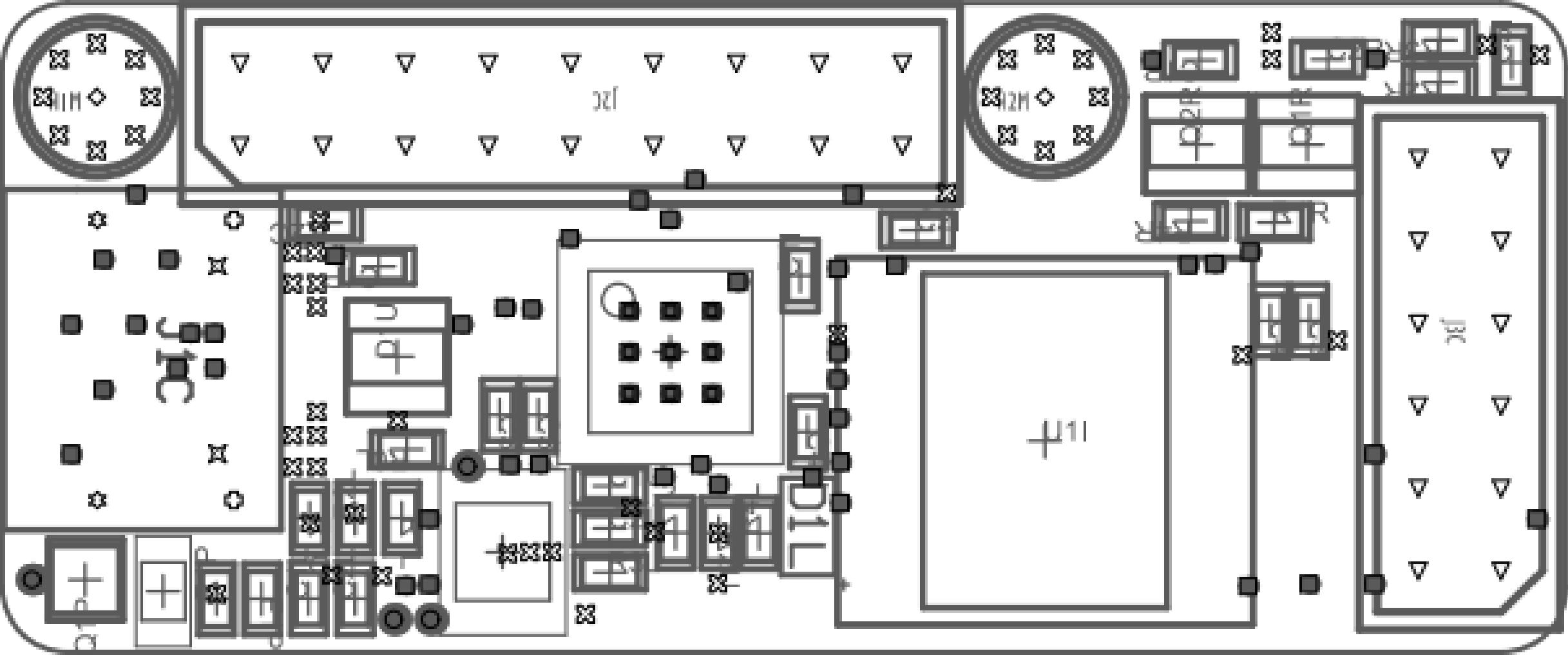


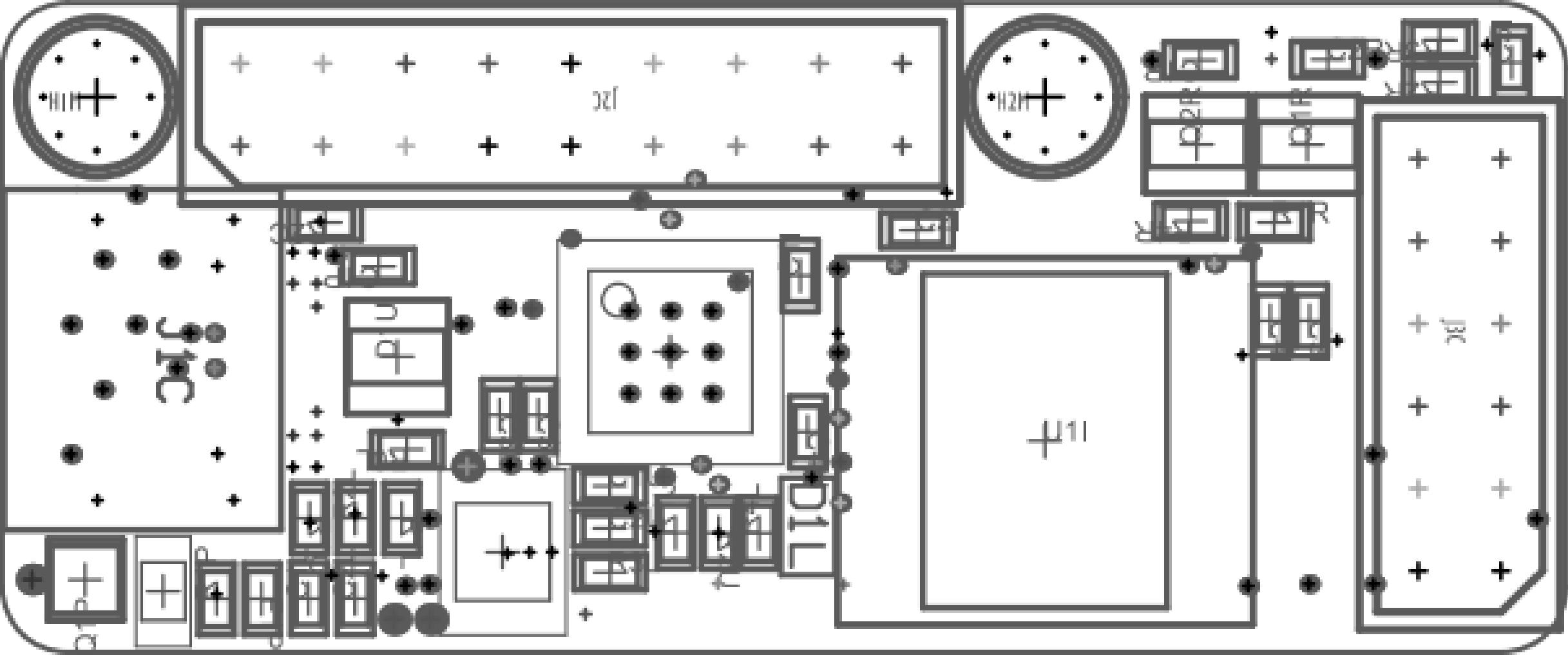












Comment	Description	Designator	Footprint	LibRef	Quantity	Manufacturer Part Number	Value	Tolerance	Voltage Rating
KGM15AR70J104KM XTR_0603	Cap Cer 0.1UF 6.3V	C1I, C1R, C3U	CO603-IPC_C_No_Silk	100nF_.6.3V	3	KGM15AR70J104K M	100nF		
C1608X5R1A106K080 AC	Multilayer Ceramic Capacitor, 10 uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C1L	CO603-IPC_C_No_Silk	10uF_10V	1	C1608X5R1A106K0 80AC	10uF	10%	10V
C0603C104K8RACTU	Multilayer Ceramic Capacitor, 0.1uf, 10 V, ± 10%, XTR, 0603 [1608 Metric]	C1P, C1U, C2L, C2U, C4I	CO603-IPC_C_No_Silk	100nF_10V	5	C0603C104K8RAC TU	100nF	10%	10V
06036A102KAT2A	Cap Ceramic 0.001uF 6.3V COG 10% SMD 0603 125°C Paper T/R	C2I	CO603-IPC_C_No_Silk	1nF_.6.3V	1	06036A102KAT2A	1nF	10%	6.3V
C0603C105K8PACTU	Ceramic Capacitor, Multilayer, Ceramic, 10V, 10% Tol, 10% -Tol, X5R, 15% TC, 1uF, 0603	C2R, C5I	CO603-IPC_C_No_Silk	1uF_10V	2	C0603C105K8PAC TU	1uF	10%	10V
CC0603KRX7R6BB102	Cap Ceramic 0.001uF 10V XTR 10% SMD 0603 125°C Paper T/R	C3I	CO603-IPC_C_No_Silk	1nF_10V	1	CC0603KRX7R6BB 102	1nF	10%	10V
CL10A106KQ8NNNC	Multilayer Ceramic Capacitor, 10uF, 6.3 V, ± 10%, X5R, 0603 [1608 Metric]	C3L	CO603-IPC_C_No_Silk	10uF_.6.3V	1	CL10A106KQ8NN NC	10uF	10%	6.3V
CL10A475KP8NNNC	Multilayer Ceramic Capacitor, 4.7uF, 10 V, ± 10%, X5R, 0603 [1608 Metric]	C4U	CO603-IPC_C_No_Silk	4.7uF_10V	1	CL10A475KP8NN NC	4.7uF	10%	10V
YELLOW	LED 0603 YELLOW SMD	D1L	LED_0603_YELLOW	LED_0603_YELLOW	1				
CDSOT23-SRV05-4	TVS DIODE 5V 15V SOT23-6	D1U	SOT23-6-IPC_C	SRV05-4	1	CDSOT23-SRV05-4			
F0603	Fuse PPTC SMD 0603	F1P	R0603-MFG	FUSE_PPTC_0603	1		250mA		
USB4105-GF-A-060	USB Connector Type C SMT 16 Pin (Power pins joints = 12 pins)	J1C	USB-Type-C-16-Pin-SMT	USB-Type-C-16-Pin-SMT	1	USB4105-GF-A-060			
2X09		J2C	PinHeader_2x09_P2.5_4mm_Vertical	PinHeader_2X09 DU	1				
2X06		J3C	Pinheader_2x06_P2.5_4mm_Vertical	UART_2x06_P2.54mm_V2	1				
PMPB14XPZ	PMPB14XPZ	Q1P	DFN2020MD-MFG	PMPB14XPZ	1	PMPB14XPZ			
SS8050-G	Trans Gp 8jt NPN 25V 1.5A 300mW 3-PIN SOT-23T/r	Q1R, Q2R	SOT-23-3-MFG	SS8050-G	2	SS8050-G			
MCR03EZPFX1691	Surface Mount Thick Film Chip Resistor 0603 Case 1.69K Ohms 1% Tolerance 100 PPM	R0L	R0603-MFG	1.69K	1	MCR03EZPFX1691	1.69K	1%	
CRCW06035K10FKEA	SMD Chip Resistor, 5.1kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1C, R2C	R0603-MFG	5.1K	2	CRCW06035K10F EA	5.1kR	1%	75V
ERJ-3EKF3302V	Res Thick Film 0603 33K Ohm 1% 0.1W(1/10W) ±100ppm/C Pad SMD Automotive 1/T	R1L	R0603-MFG	33K	1	ERJ-3EKF3302V	33kR	1%	75V
AC0603FR-07100KL	SMD Chip Resistor, 100kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1P	R0603-MFG	100K	1	AC0603FR-07100KL	100kR	1%	50V
RC0603FR-0710KL	SMD Chip Resistor, 10 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R1R, R1U, R2R, R2U, R3L, R3R, R4R	R0603-MFG	10K	7	RC0603FR-0710KL	10kR	1%	75V
CR0603-FX-2002ELF	SMD Chip Resistor, 20 kOhm, ± 1%, 100 mW, 0603 [1608 Metric], Thick Film, General Purpose	R2L	R0603-MFG	20K	1	CR0603-FX-2002ELF	20kR	1%	50V
MCR03EZPFX2491	Res Thick Film 0603 2.49K Ohm 1% 1/10W ±100ppm/°C Molded SMD Paper T/R	R4L	R0603-MFG	2.49K	1	MCR03EZPFX2491	2.49kR	1%	
ADUM141D0BRWZ	DGTl ISO 3750VRMS 4CH GP 16SIC	U1I	SOIC-W-16-IPC_A	ADUM141D0BRWZ	1				
SGM2019-ADJYN5G/TR	DDO U-Reg Adj 0, 3A SOT23-5	U1L	TSOT-23-5-IPC_A	SGM2019-ADJYN5G/TR	1	SGM2019-ADJYN5G/TR			
CP2102N-QFN-28	Single-Chip USB to UART Bridge, 1024 Bytes EEPROM, -40 to 85 degC, 28-pin QFN, Tube	U1U	OFN28_IPC_A	CP2102N-QFN-28	1				
MM3Z12VST1G	MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323 ON Semiconductor MM3Z12VST1G	ZD1P	SOD-323	MM3Z12VST1G	1	MM3Z12VST1G		2%	

Design Rules Verification Report

Filename : C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\USB-UART-ISO-CP2102-V-` Warnings 0
Rule Violations 0

Warnings
Total 0

Rule Violations	
Clearance Constraint (Gap=4mm) (InNetClass('PowerRails_HighVoltage_AC') Or	0
Clearance Constraint (Gap=0.254mm) (InComponentClass('Via_Plugged')), (IsPad)	0
Clearance Constraint (Gap=0.2mm) (All), (All)	0
Short-Circuit Constraint (Allowed=No) (All), (not IsBoardCutoutRegion)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.18mm) (Max=0.4mm) (Preferred=0.254mm) (InNetClass('Power_Signal'))	0
Width Constraint (Min=0.18mm) (Max=0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))	0
Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.4mm) (InNetClass('GND'))	0
Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.146mm) (InNetClass('Signal'))	0
Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass('PowerRails_LowVoltage_DC'))	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Preferred=0.102mm)	0
SMD To Corner (Distance=0.102mm) (NOT InNetClass('PowerRails_LowVoltage_DC') AND NOT	0
SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.074mm) (IsVia)	0
Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass('7_MountingHoles'))	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)	0
Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)	0
Silk To Solder Mask (Clearance=0.15mm) (All), (All)	0
Silk to Silk (Clearance=0.102mm) (All), (All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer')))	0
Height Constraint (Min=0mm) (Max=1816.048mm) (Preferred=12.7mm) (All)	0
Total	0

Electrical Rules Check Report

Class	Document	Message
Error	3_USB_TO_UART.SchDoc	Net CTS# contains multiple Input Ports (Port CTS#, Port CTS#).
Error	3_USB_TO_UART.SchDoc	Net DCD# contains multiple Input Ports (Port DCD#, Port DCD#).
Error	3_USB_TO_UART.SchDoc	Net DSR# contains multiple Input Ports (Port DSR#, Port DSR#).
Error	3_USB_TO_UART.SchDoc	Net RI# contains multiple Input Ports (Port RI#, Port RI#).
Error	3_USB_TO_UART.SchDoc	Net RXD contains multiple Input Ports (Port RXD, Port RXD).
Error	6_Connector.SchDoc	Net RXD_ISO contains multiple Input Ports (Port RXD_ISO, Port RXD_ISO, Port RXD_ISO).

Different Descriptions
Schematic Object

MM3Z12VST1G Zener Diode, 12V 2% 200 mW SMT 2-Pin SOD-323

PCB Object

ON Semiconductor MM3Z12VST1G [ZD1P]