**Design Rules Verification Report**Filename: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-UART-ISO-CP2102\USB-UART-ISO-CP2102\V-'

Warnings 0 Rule Violations 0

Warnings Total

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Clearance Constraint (Gap-0 25-tmm) (Investigate) (ProverRails, Light/orlate)—AC) Or Clearance Constraint (Gap-0 25-tmm) (Inition (Gap-0 25-tmm) (Inition (Gap-0 25-tmm) (All), (All)	Rule Violations	
Clearance Constraint (Gap-0.254mm) (InComponent Class(Via_Plugped)), (Is-Pad)		0
Clearance Constraint (Gap-0.2mm) (All) (All)   Short-Circuit Constraint (Gap-0.2mm) (All) (All)   Short-Circuit Constraint (Gap-0.2mm) (All) (All)   Short-Circuit Constraint (All-Circuit Constraint Constraint (All-Circuit Constraint Constraint (All-Circuit Constraint Constraint (All-Circuit Constraint Constraint Constraint Constraint (All-Circuit Constraint Constraint (All-Circuit (All-Circuit Constraint (All-Circuit (All-Circuit (All-		0
Un-Rouled Net Constraint ((All)         0           Modified Polygon (Allow modified: No), (Allow shelved: No)         0           Modified Polygon (Allow modified: No), (Allow shelved: No)         0           Width Constraint (Min-0.18mm) (Max-0.4mm) (Preferred-0.254mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.18mm) (Max-0.25mm) (Preferred-0.295mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.18mm) (Max-25.4mm) (Preferred-0.4mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.18mm) (Max-25.4mm) (Preferred-0.3mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.15mm) (Max-25.4mm) (Preferred-0.3mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.15mm) (Max-25.4mm) (Preferred-0.3mm) (InNetClass("Signal_50.chm"))         0           Width Constraint (Min-0.15mm) (Max-25.4mm) (Preferred-0.3mm) (InNetClass("Signal_50.chm"))         0           Rouling Layers(All)         0           Rouling Layers(All)         0           Rouling Layers(All)         0           Sold Discontine (Min-0.15mm) (Max-0.15mm) (Preferred-0.3mm) (MinWidth-0.45mm)         0           SMD To Corner (Distance-0.102mm) (NOT InNetClass("PowerPalls LowVollage_DC") AND NOT         0           SMD To Corner (Distance-0.102mm) (NOT InNetClass("PowerPalls LowVollage_DC") AND NOT         0           SMD Entry (Sidie = Allowed) (Corner = Allowe		0
Modified Polygon (Allow modified: No), (Allow shelved: No)         0           Width Constraint (Min=-0.18mm) (Max=0.4mm) (Preferred-0.295mm) (InNetClass(Signal_50_phm))         0           Width Constraint (Min=-0.18mm) (Max=0.295mm) (Preferred-0.295mm) (InNetClass(Signal_50_phm))         0           Width Constraint (Min=-0.18mm) (Max=0.454mm) (Preferred-0.295mm) (InNetClass(Signal_50_phm))         0           Width Constraint (Min=-0.15mm) (Max=0.46mm) (Preferred-0.146mm) (InNetClass(Signal_7))         0           Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred-0.146mm) (InNetClass(Signal_7))         0           Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred-0.146mm) (InNetClass(Signal_7))         0           Routing Layer(All)         0           Routing Layer(All)         0           Routing Layer(All)         0           Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.3mm) (MaxHoleWidth=0.3mm) (MinWidth=0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min=-0.102mm) (Max=-0.102mm) (Max=-0.102mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRals_Low Vollage_DC') AND NOT         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRals_Low Vollage_DC') AND NOT         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Grooner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.588mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	Short-Circuit Constraint (Allowed=No) (All), (not IsBoardCutoutRegion)	0
Width Constraint (Min-0.18mm) (Max -0.4mm) (Preferred-0.25fmm) (InNetClass(Power_Signal))         0           Width Constraint (Min-0.18mm) (Max -0.25fmm) (Preferred-0.25fmm) (InNetClass(Signal_S0_ohm))         0           Width Constraint (Min-0.11mm) (Max -0.25fmm) (Preferred-0.25fmm) (InNetClass(St0D))         0           Width Constraint (Min-0.1146mm) (Max -0.146mm) (Preferred-0.146mm) (InNetClass(St0D))         0           Width Constraint (Min-0.15mm) (Max -0.25fmm) (Preferred-0.146mm) (InNetClass(St0D))         0           Width Constraint (Min-0.15mm) (Max -0.25fmm) (Preferred-0.146mm) (InNetClass(St0D))         0           Width Constraint (Min-0.15mm) (Max -0.25fmm) (Preferred-0.146mm) (InNetClass(PowerRails_LowVollage_DC))         0           Routing Layers(All)         0           Routing Use (Min-HoleWidth-0.3mm) (Max HoleWidth-0.3mm) (MinWidth-0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max -0.102mm) (Preferred-0.102mm)         0           SMD To Comer (Dislance-0.102mm) (NOT InNetClass(PowerRails_LowVollage_DC) AND NOT         0           SMD To Comer (Percent-90%) (not Is Estpoin)         0           SMD Entry (Side - Allowed) (Corner - Allowed) (Any Angle - Not Allowed) (Ignore First Corner - Allowed)         0           Power Plane Connect Risk(Difered Connect) (Expansion-0.598mm) (Conductor Width-0.254mm) (Air Gap-0.254mm) (Air Gap-0.254mm	Un-Routed Net Constraint ( (All) )	0
Width Constraint (Min-0.18mm) (Max = 0.295mm) (Preferred - 0.295mm) (InNetClass("Signal_50_ohm"))         0           Width Constraint (Min-0.15mm) (Max = 2.54mm) (Preferred - 0.4mm) (InNetClass("Signal"))         0           Width Constraint (Min-0.15mm) (Max = 0.146mm) (Preferred - 0.146mm) (InNetClass("Signal"))         0           Width Constraint (Min-0.15mm) (Max = 0.146mm) (Preferred - 0.146mm) (InNetClass("Signal"))         0           Routing Layers(All)         0           Routing Layers(All)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.12mm) (Max = 0.102mm) (Max = 0.102mm) (Max = 0.102mm) (Max = 0.102mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass("PowerRails_LowVollage_DC") AND NOT         0           SMD Entry (Side = Allowed) (Corner = NoteClass("PowerRails_LowVollage_DC") AND NOT         0           SMD Entry (Side = Allowed) (Corner = NoteClass("Cyaparsion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annutar Ring (Minimum=0.074mm) (IsThruPin and not InComponentClass("T_MountingHoles))         0           Moure Plane Connect (Rine) (Mine—0.2mm) (Max = 6.300m) (All)         0           Hole Size Constraint (Min=0.3mm) (Max = 6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Note Size (Capa-0.4mm) (spad), (SPad)         0           Note Clearance (Gap=0.13mm) (All), (All)         0	Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min0.15mm) (Max-25.4mm) (Preferred-0.4mm) (InNetClass(*GND*))         0           Width Constraint (Min0.15mm) (Max-25.4mm) (Preferred-0.34mm) (InNetClass(*Signal*))         0           Width Constraint (Min0.15mm) (Max-25.4mm) (Preferred-0.3mm) (InNetClass(*Signal*))         0           Routing Lay ex/All)         0           Routing Via (MinH-oleWidth-0.3mm) (Max HoleWidth-0.5mm) (Preferred-0.45mm) (MinWidth-0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max-0.102mm) (MinWidth-0.45mm)         0           SMD To Corner (Distance-0.102mm) (NOT InNetClass(*PowerRails_LowVoltage_DC*) AND NOT         0           SMD Neck-Down Constraint (Percent-90%) (not is Testpoin)         0           SMD Enry (Side - Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion-0.508mm) (Conductor Width-0.254mm) (Air Gap-0.254mm)         0           Minimum Annutar Ring (Minimum-0.074mm) (Istria) (Sivia)         0           Minimum Annutar Ring (Minimum-0.074mm) (Istria) (Sivia)         0           Acute Angle Constraint (Min-0.3mm) (Max -6.3mm) (All)         0           Pads and Vias to foliow the Drill pairs settings         0           Hole To Hole Clearance (Gap-0.13mm) (All), (All)         0           Sik to Sik (Clearance-0.10mm) (All), (All)         0           Sik to Sik (	Width Constraint (Min=0.18mm) (Max=0.4mm) (Preferred=0.254mm) (InNetClass('Power_Signal'))	0
Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.34mm) (InNetClass(Signaf))         0           Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass(PowerRails_LowVoltage_DC*))         0           Routing Lay ers(All)         0           Routing Lay ers(All)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (MinWidth=0.45mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC*) AND NOT         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC*) AND NOT         0           SMD Enrity (Side = Allowed) (Corner = Allowed) (Allowed) (Ignore First Corner = Allowed)         0           SMD Enrity (Side = Allowed) (Corner = Allowed) (Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annutar Ring (Minimum=0.07mm) (IsTrurplin and not InComponentClass(7_MountingHoles*))         0           Acute Angle Constraint (Tiracts Only) (Minimum=45.000) (All)         0           Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Pads and Vias to follow the Drill pairs sellings         0           Hole To Hole Clearance (Gap=0.13mm) (All),(All)         0           Silk to Solder Mask (Clearance (Gap=0.13mm) (All),(All)         0           <	Width Constraint (Min=0.18mm) (Max=0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))	0
Width Constraint (Min-0.15mm) (Max=25.4mm) (Prefered-0.3mm) (InNelClass(PowerRails_LowVoltage_DC'))         0           Routing Layers(All)         0           Routing Layers(All)         0           Routing Using MinholeWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferedHoleWidth=0.3mm) (MinWidth=0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Prefered=0.102mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNelClass(PowerRails_LowVoltage_DC') AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoin)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsTruch) in and not InC componentClass(7_MountingHoles*))         0           Minimum Annular Ring (Minimum=0.074mm) (IsTruch's Only) (Minimum=45.000) (All)         0           Hole Size Constraint (Tiracks Only) (Minimum=45.000) (All)         0           Hole Size Constraint (Min=0.mm) (Min=0.3mm) (Min=0.3mm) (All), (All)         0           Bilk To Solder Mask (Clearance (Gap=0.4mm) (spad), (SPad)         0           Minimum Solder Mask Silver (Gap=0.13mm) (All), (All)         0           Silk to Solder Mask (Clearance=0.15mm) (All), (All)         0	Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.4mm) (InNetClass('GND'))	0
Routing Layers(All)         0           Routing Via (MinI+toleWidth=0.3mm) (Max HoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Preferred=0.102mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC') AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoin)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Cornect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsTruPin and not InC omponentClass(7_MountingHoles))         0           Mcute Angle Constraint (Tracks Only) (Minimum=45.000) (All)         0           Hole Size Constraint (Win=0.3mm) (Max =6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.4mm) (spad),(IsPad)         0           Minimum Solder Mask Silver (Gap=0.13mm) (All),(All)         0           Silk To Solder Mask (Clearance=0.15mm) (All),(All)         0           Silk (Is Carance Contrictaint (Gap=0mm) (All),(All)         0           Bead Clearance Cornstraint (Gap=0mm) ((InLayer(Top Layer) OR OnLayer(Bottom Layer)))         0           Height Constraint	Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.146mm) (InNetClass('Signal'))	0
Rouling Via (MinHoleWidth=0.3mm) (Max HoleWidth=0.5mm) (PreferedHoleWidth=0.3mm) (MinWidth=0.45mm)   Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max=0.102mm) (Prefered=0.102mm)   OSMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC') AND NOT   OSMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)   OSMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)   OSMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)   OSMD Neck-Down Constraint (Percent=90%) (Any Angle = Not Allowed) (gnore First Corner = Allowed)   Osmer = Allowed) (Corner = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (gnore First Corner = Allowed)   Osmer Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)   Osminimum Annular Ring (Minimum=0.074mm) (IsTruPin and not InComponentClass(7_MountingHoles))   Osminimum Annular Ring (Minimum=0.074mm) (IsTruPin and not InComponentClass(7_MountingHoles))   Osminimum Annular Ring (Minimum=0.07mm) (Minimum=0.074mm) (Mini	Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass('PowerRails_LowVoltage_DC'))	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Prefered=0.102mm) (Prefered=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC) AND NOT	Routing Layers(All)	0
SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC') AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsVia)         0           Minimum Annular Ring (Minimum=0.074mm) (IsThruPin and not InComponentClass(7_MountingHoles'))         0           Acute Angle Constraint (Min=0.3mm) (Max =6.3mm) (All)         0           Hole Size Constraint (Min=0.3mm) (Max =6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.4mm) (spad), (IsPad)         0           Minimum Solder Mask (Clearance (Gap=0.13mm) (All), (All)         0           Silk To Solder Mask (Clearance=0.15mm) (All), (All)         0           Silk to Silk (Clearance=0.10mm) (All), (All)         0           Board Clearance (Tolerance=0mm) (All), (All)         0           Board Clearance (Constraint (Min=0mm) (Max =1816.048mm) (Prefered=12.7mm) (All)         0	Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)	0
SMD Neck-Down Constraint (Percent-90%) (not IsTestpoint)  SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)  Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)  Minimum Annular Ring (Minimum=0.074mm) (IsTvia)  Minimum Annular Ring (Minimum=0.2mm) (IsTrnuPin and not InComponentClass(7_MountingHoles))  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad), (IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  O Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)       0         Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)       0         Minimum Annular Ring (Minimum=0.074mm) (IsVia)       0         Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles*))       0         Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)       0         Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)       0         Pads and Vias to follow the Drill pairs settings       0         Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)       0         Minimum Solder Mask Silver (Gap=0.13mm) (All),(All)       0         Silk To Solder Mask (Clearance=0.15mm) (All),(All)       0         Silk to Silk (Clearance=0.102mm) (All),(All)       0         Silk to Silk (Clearance=0.102mm) (All),(All)       0         Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))       0         Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)       0		0
Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm) (Dispansion=0.508mm) (Isvia)		0
Minimum Annular Ring (Minimum=0.074mm) (IsVia)  Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles'))  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  O  Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)  Silk To Solder Mask (Clearance=0.15mm) (All),(All)  Silk to Silk (Clearance=0.102mm) (All),(All)  O  Net Antennae (Tolerance=0mm) (All),  Board Clearance Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)  O  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InC omponentClass(7_MountingHoles))  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (AII)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (AII)  Pads and Vias to follow the Drill pairs settings  OHole To Hole Clearance (Gap=0.4mm) (ispad), (IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (AII), (AII)  Silk To Solder Mask (Clearance=0.15mm) (AII), (AII)  Silk to Silk (Clearance=0.102mm) (AII), (AII)  OHet Antennae (Tolerance=0.0mm) (AII)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer)))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (AII)		0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad), (IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  ONE Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad), (isPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)  Silk To Solder Mask (Clearance=0.15mm) (All),(All)  Silk to Silk (Clearance=0.102mm) (All),(All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Hole To Hole Clearance (Gap=0.4mm) (spad), (IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All) Silk To Solder Mask (Clearance=0.15mm) (All), (All) Silk to Silk (Clearance=0.102mm) (All), (All) Net Antennae (Tolerance=0mm) (All) Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') )) Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Silk To Solder Mask (Clearance=0.15mm) (AII),(AII)  Silk to Silk (Clearance=0.102mm) (AII),(AII)  Net Antennae (Tolerance=0mm) (AII)  Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (AII)		0
Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	· · · · · · · · · · · · · · · · · · ·	0
Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)		0
Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Net Antennae (Tolerance=0mm) (All)	0
· · · · · · · · · · · · · · · · · · ·	Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))	0
Total 0	Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	0
	Total	0

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