**Design Rules Verification Report**Filename: C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Devlopment\USB-UART-ISO-CP2102\USB-UART-ISO-CP2102\V-2

Warnings 0 Rule Violations 0

Warnings Total

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Clearance Constraint (Gap-0.25mm) (InfoClibass(PaverRains, 14jp)Moltage, AC) Or Clearance Constraint (Gap-0.25mm) (InfoComponent Class(Via_Plugged)) (IsPad)	Rule Violations	
Clearance Constraint (Gap-0.254mm) (InComponent Class (Via_Plugged)), (Is-Pad)		0
Clearance Constraint (Gap-0.2mm) (All), (All)   Short-Circuit Constraint (Allowed-No) (All), (All) (All Short-Circuit Constraint (Allowed-No) (All), (All) (All Short-Circuit Constraint (Allowed-No) (All), (All) (All Short-Circuit Constraint (Allowed-No) (Allow shelved: No)   Ol Modified Polygon (Allow modified: No), (Allow shelved: No)   Ol Width Constraint (Min-0.18mm) (Max -0.25mm) (Preferred-0.25mm) (InNeClass(*Cond'))   Ol Width Constraint (Min-0.18mm) (Max -0.25mm) (Preferred-0.3mm) (InNeClass(*Cond'))   Ol Width Constraint (Min-0.15mm) (Max -0.25mm) (Preferred-0.3mm) (InNeClass(*Cond'))   Ol Width Constraint (Min-0.15mm) (Max -0.25mm) (Preferred-0.3mm) (InNeClass(*Cond'))   Ol Width Constraint (Min-0.15mm) (Max -0.25mm) (Max		0
Short-Circuit Constraint (Alloweds-No) (All), (not Is BoardCutoutRegion)		0
Un-Rouled Net Constraint ((All)		0
Width Constraint (Min-0.18mm) (Max-0.4mm) (Prefered-0.25fmm) (inNetClass(Power_Signal))         0           Width Constraint (Min-0.18mm) (Max-0.279mm) (Prefered-0.25fmm) (inNetClass(Signal_So_Johm'))         0           Width Constraint (Min-0.18mm) (Max-0.28fmm) (Prefered-0.25fmm) (inNetClass(Signal_SO_Johm'))         0           Width Constraint (Min-0.18mm) (Max-0.146mm) (Prefered-0.146mm) (InNetClass(Signal_SO_Johm'))         0           Width Constraint (Min-0.18mm) (Max-0.254mm) (Prefered-0.146mm) (InNetClass(Signal_SO_John'))         0           Width Constraint (Min-0.18mm) (Max-0.254mm) (Prefered-0.146mm) (InNetClass(PowerRails_LowVollage_DC'))         0           Routing Layers(Ali)         0           Routing Layers(Ali)         0           Routing Via (MinHoleWidth-0.3mm) (Max-HoleWidth-0.3mm) (MinWidth-0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max-0.102mm) (Max-0.102mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max-0.102mm) (Max-0.102mm) (Prefered-0.102mm)         0           SMD Neck-Down Constraint (Percent-90%) (not IsTestpoin)         0           SMD Neck-Down Constraint (Percent-90%) (not IsTestpoin)         0           SMD Entry (Side - Allowed) (Corner - Allowed) (Ingone First Corner - Allowed)         0           Power Paine Connect Rule(Direct Connect) (Expansion-0.508mm) (Conductor Width-0.254mm) (Ali Gap-0.254mm) (Ali Gap-0.254mm) (Ali Gap-0.254mm) (Ali Gap-0.254mm) (	Un-Routed Net Constraint ( (All) )	0
Width Constraint (Min-0.18mm) (Max – 0.295mm) (Preferred – 0.295mm) (InNetClass('Signal_5O_ohm'))         0           Width Constraint (Min-0.15mm) (Max – 0.25mm) (Preferred – 0.4mm) (InNetClass('Signal'))         0           Width Constraint (Min-0.15mm) (Max – 0.146mm) (Preferred – 0.4mm) (InNetClass('Signal'))         0           Width Constraint (Min-0.15mm) (Max – 0.146mm) (Preferred – 0.14mm) (InNetClass('Signal'))         0           Routing Layers(All)         0           Routing Layers(All)         0           Routing Layers(All)         0           Differential Pairs Uncoupled Length using the Cap Constraints (Min-0.10mm) (Max – 0.102mm) (M	Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min-o. 15mm) (Max - 25.4mm) (Preferred-0.4mm) (InNetClass(*GND*))         0           Width Constraint (Min-o. 15mm) (Max - 25.4mm) (Preferred-0.146mm) (InNetClass(*Signaf*))         0           Routing Layers(Ali)         0           Routing Via (MinH-0.15mm) (Max - 25.4mm) (Preferred-0.3mm) (InNetClass(*PowerRails_LowVoltage_DC*))         0           Routing Via (MinH-0.15mm) (Max - 25.4mm) (Preferred-0.3mm) (InNetClass(*PowerRails_LowVoltage_DC*))         0           Routing Via (MinH-0.15mm) (Max - 25.4mm) (Preferred-0.3mm) (MinWitth-0.3mm) (MinWitth-0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max - 0.102mm) (Max - 0.102mm)         0           SMD To Corner (Distance-0.102mm) (NOT inNetClass(*PowerRails_LowVoltage_DC*) AND NOT         0           SMD Neck-Down Constraint (Percent-90%) (not IsTestpoint)         0           SMD Entry (Side - Allowed) (Corner - Allowed) (Any Angle - Not Allowed) (Ignore First Corner - Allowed)         0           Power Plane Cornect Rule(Direct Connect) (Expansion-0.50mm) (Conductor Width-0.254mm) (Air Gap-0.254mm)         0           Minimum Annutar Ring (Minimum-0.074mm) (IsTruPin and not InComponentClass(*7_MountingHoles*))         0           Acute Angle Constraint (Tiracks Only) (Minimum-45.000) (All)         0           Hole Size Constraint (Min-0.3mm) (Max - 6.100mm) (All) (All)         0           Pads and Vias to foliow the Drill pairs settings         0	Width Constraint (Min=0.18mm) (Max=0.4mm) (Preferred=0.254mm) (InNetClass('Power_Signal'))	0
Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.34mm) (InNetClass(Signaf))         0           Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass(PowerRails_LowVoltage_DC))         0           Routing Lay ers(All)         0           Routing Lay ers(All)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (MinWidth=0.45mm)         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC) AND NOT         0           SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC) AND NOT         0           SMD Enrity (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           SMD Enrity (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.598mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annutar Ring (Minimum=0.07mm) (IsTruPin and not InC omponentClass(7_MountingHoles*))         0           Acute Angle Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.13mm) (All),(All)         0           Silk to Solder Mask (Clearance (Gap=0.13mm) (All),(All)         0 <td>Width Constraint (Min=0.18mm) (Max=0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))</td> <td>0</td>	Width Constraint (Min=0.18mm) (Max=0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))	0
Width Constraint (Min-0.15mm) (Max=25.4mm) (Prefered-0.3mm) (InNetClass(PowerRails_LowVoltage_DC7))         0           Rouling Layers(All)         0           Rouling Layers(All)         0           Rouling Via (MinholeWidth-0.3mm) (Max HoleWidth-0.5mm) (Prefered-HoleWidth-0.3mm) (MinWidth-0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max -0.102mm) (Prefered-0.102mm)         0           SMD To Corner (Distance-0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC*) AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoin)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Ali Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsSVa)         0           Minimum Annular Ring (Minimum=0.074mm) (IsSVa)         0           Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InC componentClass(7_MountingHoles))         0           Acute Angle Constraint (Tiracks Only) (Minimum=45.000) (All)         0           Hole Size Constraint (Min-0.3mm) (Min	Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.4mm) (InNetClass('GND'))	0
Routing Layers(All)   Routing Layers(All)   Routing Via (MinHoleWidth=0.3mm) (Max HoleWidth=0.5mm) (PreferedHoleWidth=0.45mm)   O	Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.146mm) (InNetClass('Signal'))	0
Rouling Via (MinHoleWidth=0.3mm) (Max HoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)         0           Differential Pairs Uncoupled Length using the Gap Constraints (Min-0.102mm) (Max=0.102mm) (Preferred=0.102mm)         0           SMD To Corner (Distance=-0.102mm) (NOT InNeClass(PowerRails_LowVoltage_DC') AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annutar Ring (Minimum=0.074mm) (IsThruPin and not InComponentClass(*7_MountingHoles*))         0           Acute Angle Constraint (Tracks Only (Minimum=45.000) (All)         0           Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.4mm) (ispad), (isPad)         0           Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)         0           Silk To Solder Mask (Clearance=0.15mm) (All), (All)         0           Silk To Solder Mask Clearance=0.15mm) (All), (All)         0           Bead Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Boltom Layer'))         0           Bead Clearance Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)         <	Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass('PowerRails_LowVoltage_DC'))	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Prefered=0.102mm) (OT InNetClass('PowerRails_LowVollage_DC') AND NOT OSMD Nock-Down Constraint (Percent=90%) (not IsTestpoint) 0 SMD Nock-Down Constraint (Percent=90%) (not IsTestpoint) 0 SMD Entry (Side = Allowed) (Corner = Allowed) (Innet = Al	Routing Layers(All)	0
SMD To Corner (Distance=0.102mm) (NOT InNetClass(PowerRails_LowVoltage_DC') AND NOT         0           SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsThruPin and not InComponentClass(7_MountingHoles*))         0           Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles*))         0           Acute Angle Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.4mm) (ispad),(ispad)         0           Minimum Solder Mask (Clearance=0.15mm) (All),(All)         0           Silk To Solder Mask (Clearance=0.15mm) (All),(All)         0           Silk to Silk (Clearance=0.10mm) (All),(All)         0           Board Clearance (Tolerance=0mm) (All)         0           Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)         0	Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)	0
SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)         0           SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)         0           Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)         0           Minimum Annular Ring (Minimum=0.074mm) (IsTruPin and not InComponentClass(7_MountingHoles'))         0           Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)         0           Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)         0           Pads and Vias to follow the Drill pairs settings         0           Hole To Hole Clearance (Gap=0.4mm) (ispad) (IsPad)         0           Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)         0           Slik To Solder Mask (Clearance=0.15mm) (All), (All)         0           Slik to Silk (Clearance=0.102mm) (All), (All)         0           Net Antennae (Tolerance=0mm) (All)         0           Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))         0           Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)         0	Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Prefered=0.102mm)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)       0         Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)       0         Minimum Annular Ring (Minimum=0.074mm) (IsVia)       0         Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles'))       0         Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)       0         Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)       0         Pads and Vias to follow the Drill pairs settings       0         Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)       0         Minimum Solder Mask Silver (Gap=0.13mm) (All),(All)       0         Silk To Solder Mask (Clearance=0.15mm) (All),(All)       0         Silk to Silk (Clearance=0.102mm) (All),(All)       0         Silk to Silk (Clearance=0.102mm) (All),(All)       0         Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))       0         Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)       0	SMD To Corner (Distance=0.102mm) (NOT InNetClass('PowerRails_LowVoltage_DC') AND NOT	0
Power Plane Connect Rule(Direct Connect) (Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)  Minimum Annular Ring (Minimum=0.074mm) (IsVia)  Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles'))  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  OHole To Hole Clearance (Gap=0.4mm) (spad), (IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)  OHeight Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)	0
Minimum Annular Ring (Minimum=0.074mm) (IsVia)       0         Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles))       0         Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)       0         Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)       0         Pads and Vias to follow the Drill pairs settings       0         Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)       0         Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)       0         Silk To Solder Mask (Clearance=0.15mm) (All),(All)       0         Silk to Silk (Clearance=0.102mm) (All),(All)       0         Net Antennae (Tolerance=0mm) (All)       0         Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))       0         Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)       0	SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)	0
Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass(7_MountingHoles'))  Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)  Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  Deads and Vias to follow the Drill pairs settings  Minimum Solder Mask Sliver (Gap=0.4mm) (spad),(IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)  Silk To Solder Mask (Clearance=0.15mm) (All),(All)  Silk to Silk (Clearance=0.102mm) (All),(All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer)))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Power Plane Connect Rule(Direct Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All) Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All) Pads and Vias to follow the Drill pairs settings Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad) Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All) Silk To Solder Mask (Clearance=0.15mm) (All),(All) Silk To Solder Mask (Clearance=0.15mm) (All),(All) Silk to Silk (Clearance=0.102mm) (All),(All) OR Antennae (Tolerance=0mm) (All) Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer))) Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Minimum Annular Ring (Minimum=0.074mm) (IsVia)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)  Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad), (isPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer)))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass('7_MountingHoles'))	0
Pads and Vias to follow the Drill pairs settings  Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)  Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)  Silk To Solder Mask (Clearance=0.15mm) (All),(All)  Silk to Silk (Clearance=0.102mm) (All),(All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole To Hole Clearance (Gap=0.4mm) (ispad), (IsPad) Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All) Silk To Solder Mask (Clearance=0.15mm) (All), (All) Silk to Silk (Clearance=0.102mm) (All), (All) Net Antennae (Tolerance=0mm) (All) Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer))) Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Minimum Solder Mask Sliver (Gap=0.13mm) (All), (All)  Silk To Solder Mask (Clearance=0.15mm) (All), (All)  Silk to Silk (Clearance=0.102mm) (All), (All)  Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer) OR OnLayer(Bottom Layer)))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Pads and Vias to follow the Drill pairs settings	0
Silk To Solder Mask (Clearance=0.15mm) (AII),(AII)  Silk To Solder Mask (Clearance=0.15mm) (AII),(AII)  Silk to Silk (Clearance=0.102mm) (AII),(AII)  Net Antennae (Tolerance=0mm) (AII)  Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (AII)	Hole To Hole Clearance (Gap=0.4mm) (ispad), (IsPad)	0
Silk to Silk (Clearance=0.102mm) (AII), (AII)  Net Antennae (Tolerance=0mm) (AII)  Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (AII)	Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)  Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Silk To Solder Mask (Clearance=0.15mm) (All),(All)	0
Board Clearance Constraint (Gap=0mm) ((OnLayer(Top Layer') OR OnLayer(Bottom Layer')))  Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Silk to Silk (Clearance=0.102mm) (All),(All)	0
Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	Net Antennae (Tolerance=0mm) (All)	0
· · · · · · · · · · · · · · · · · · ·	Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer') ))	0
	Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	0
	Total	0

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