Design Rules Verification Report

Filename : C:\Users\desktop\Documents\Project Files\Altium\Projects\Project - Development\USB-UART-ISO-CP2102\USB-UART-ISO-CP2102-V-2

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=4mm) (InNetClass('PowerRails_HighVoltage_AC') Or	0
Clearance Constraint (Gap=0.254mm) (InComponentClass('Via_Plugged')),(IsPad)	0
Clearance Constraint (Gap=0.2mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(not IsBoardCutoutRegion)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.18mm) (Max=0.4mm) (Preferred=0.254mm) (InNetClass('Power_Signal'))	0
Width Constraint (Min=0.18mm) (Max=0.295mm) (Preferred=0.295mm) (InNetClass('Signal_50_ohm'))	0
Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.4mm) (InNetClass('GND'))	0
Width Constraint (Min=0.146mm) (Max=0.146mm) (Preferred=0.146mm) (InNetClass('Signal'))	0
Width Constraint (Min=0.15mm) (Max=25.4mm) (Preferred=0.3mm) (InNetClass('PowerRails_LowVoltage_DC'))	0
Routing Layers(All)	0
Routing Via (MinHoleWidth=0.3mm) (MaxHoleWidth=0.5mm) (PreferredHoleWidth=0.3mm) (MinWidth=0.45mm)	0
Differential Pairs Uncoupled Length using the Gap Constraints (Min=0.102mm) (Max=0.102mm) (Prefered=0.102mm)	0
SMD To Corner (Distance=0.102mm) (NOT InNetClass('PowerRails_LowVoltage_DC') AND NOT	0
SMD Neck-Down Constraint (Percent=90%) (not IsTestpoint)	0
SMD Entry (Side = Allowed) (Corner = Allowed) (Any Angle = Not Allowed) (Ignore First Corner = Allowed)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.074mm) (IsVia)	0
Minimum Annular Ring (Minimum=0.2mm) (IsThruPin and not InComponentClass('7_MountingHoles'))	0
Acute Angle Constraint [Tracks Only] (Minimum=45.000) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Pads and Vias to follow the Drill pairs settings	0
Hole To Hole Clearance (Gap=0.4mm) (ispad),(IsPad)	0
Minimum Solder Mask Sliver (Gap=0.13mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.15mm) (All),(All)	0
Silk to Silk (Clearance=0.102mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) ((OnLayer('Top Layer') OR OnLayer('Bottom Layer')))	0
Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	0
Total	0