ASSIGNMENT – 03

DIGITAL CIRCUIT DESIGN AND IMPLEMENTION

EC4010 - DIGITAL DESIGN

GROUP NAME : A2

REGISTRATION NO. : 2019/E/011

2019/E/021

2019/E/023

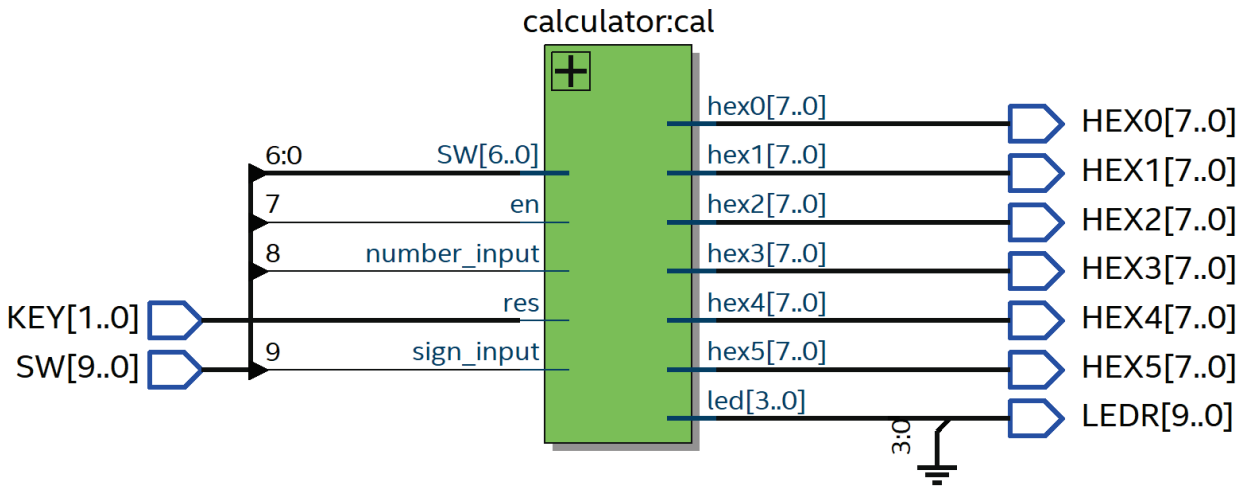
DATE ASSIGNED : 30 JUNE 2022

CONTRIBUTION CHART :

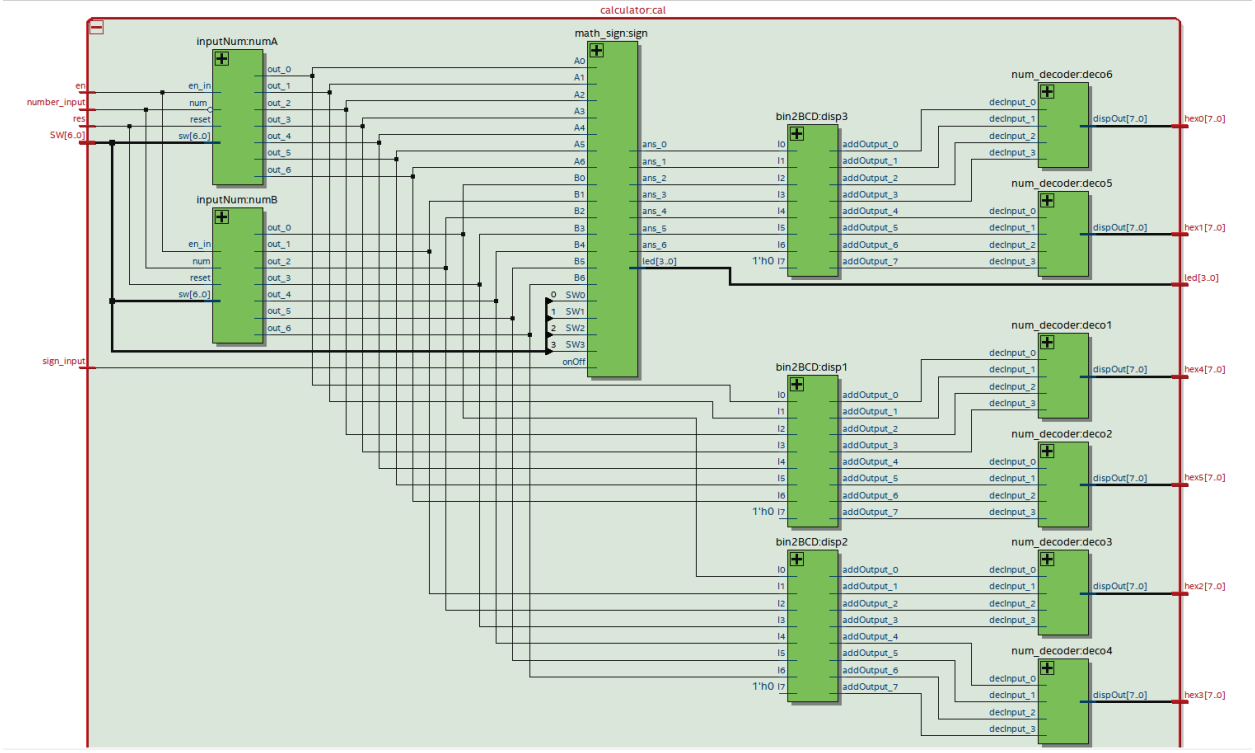
GROUP MEMBERS' NAME & E-NUM	CONTRIBUTION
ASHFA A.G.F. (2019/E/011)	Divider Module
BANDARANAYAKE H.A.C.S. (2019/E/021)	Multiplier Module
CHANDRASIRI H.V.B.L. (2019/E/023)	All base Modules and Adder/Subtractor Module

BLOCK DIAGRAMS OF ALL MODULES:

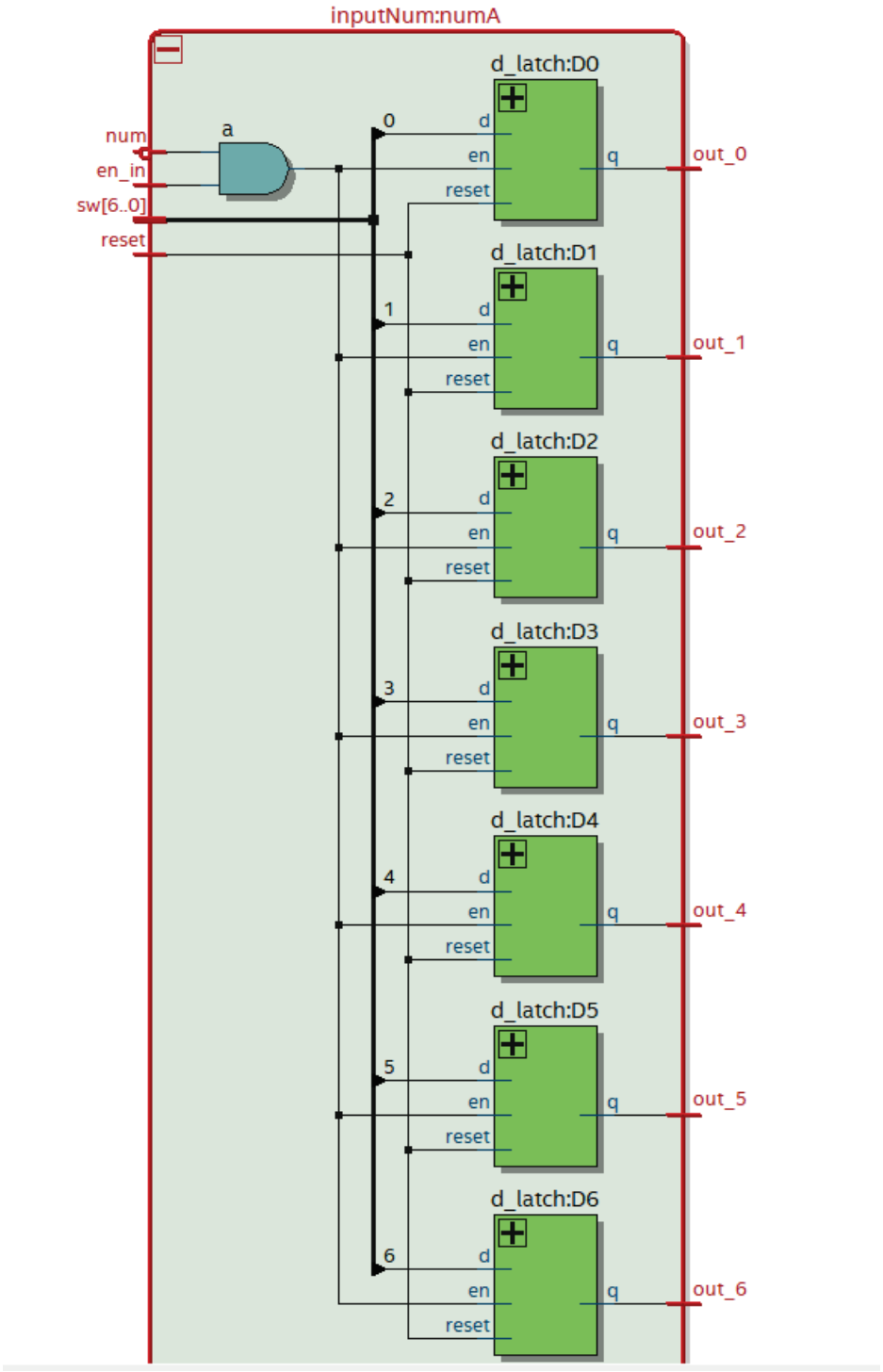
1. Golden Top Module:



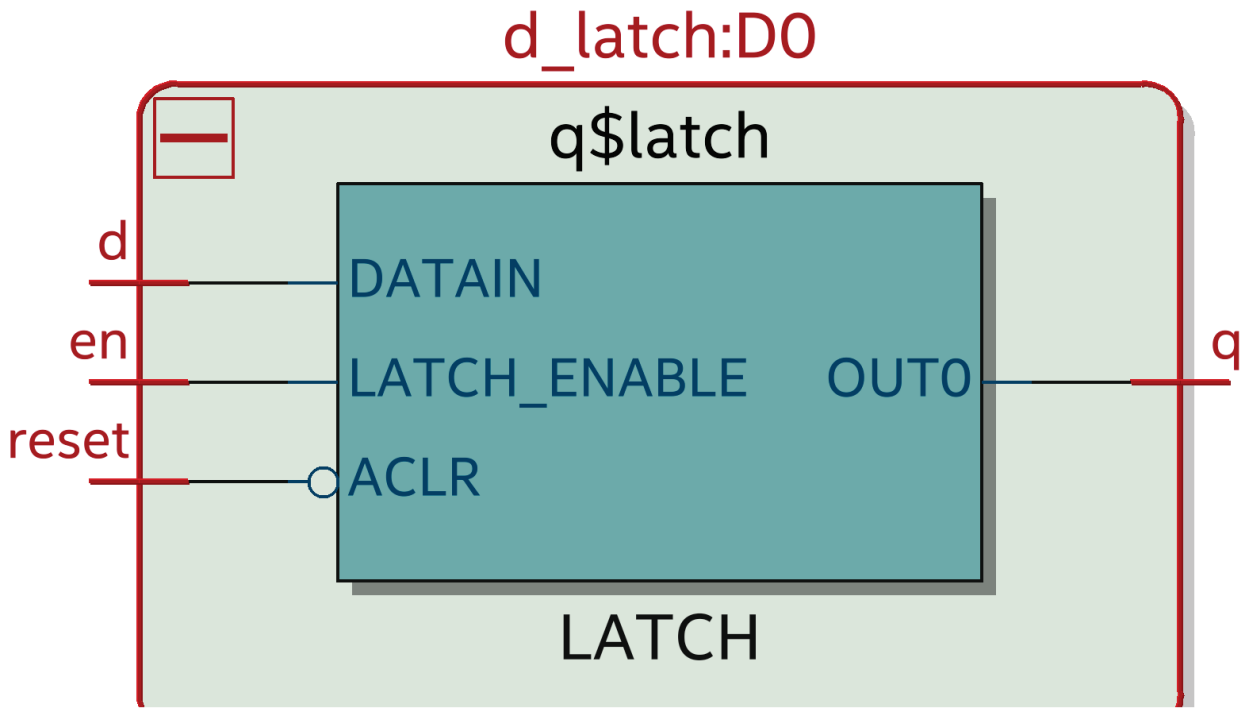
2. Calculator Module:



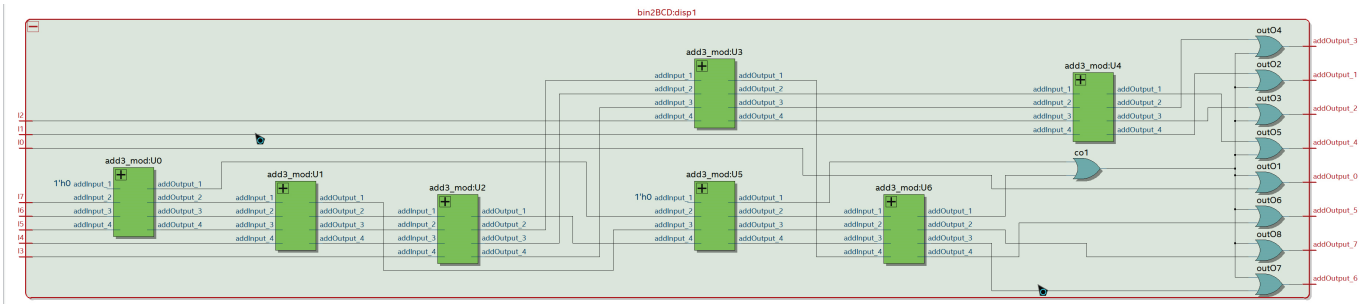
3. Number Input Module:



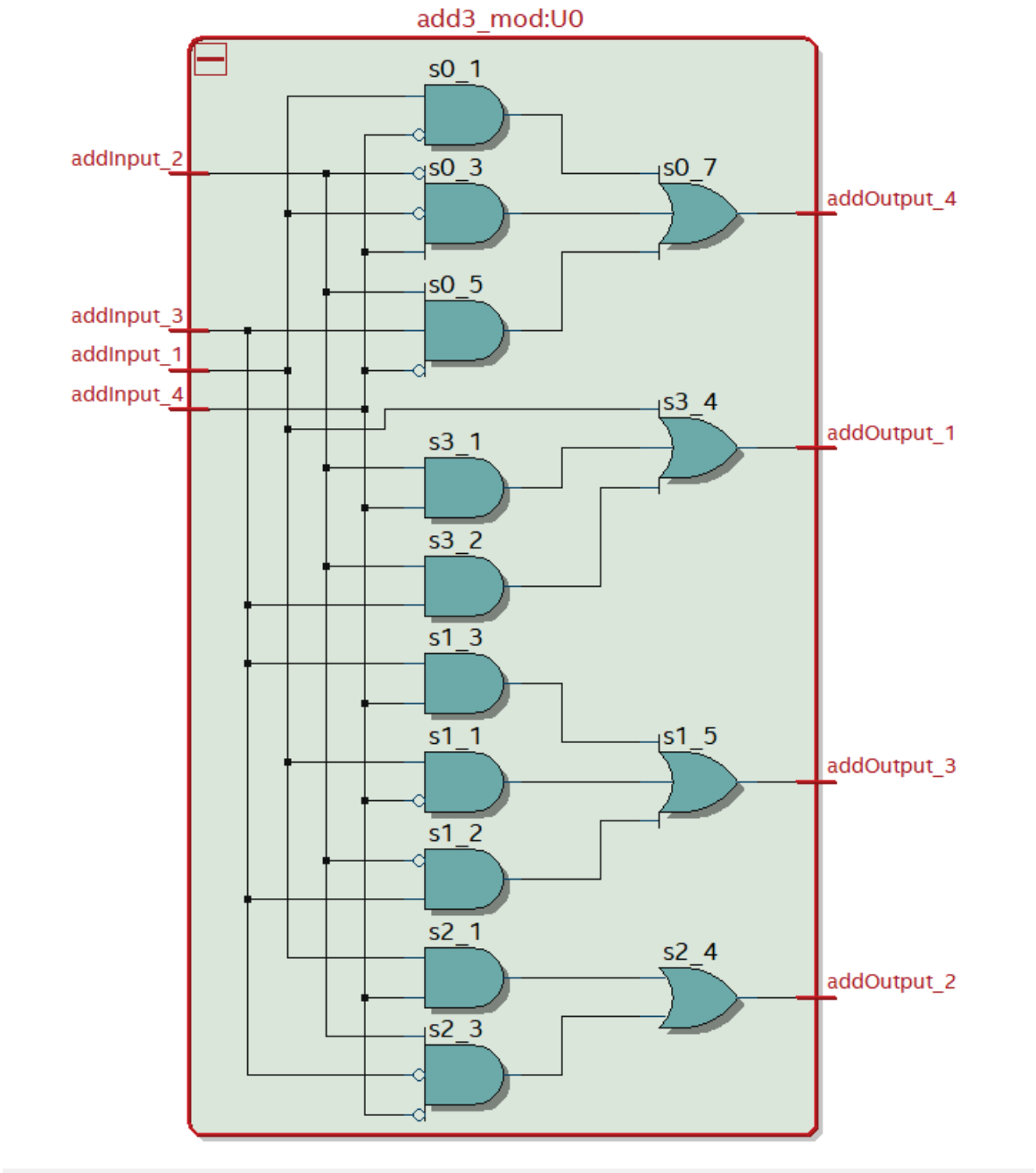
4. D Latch Module:



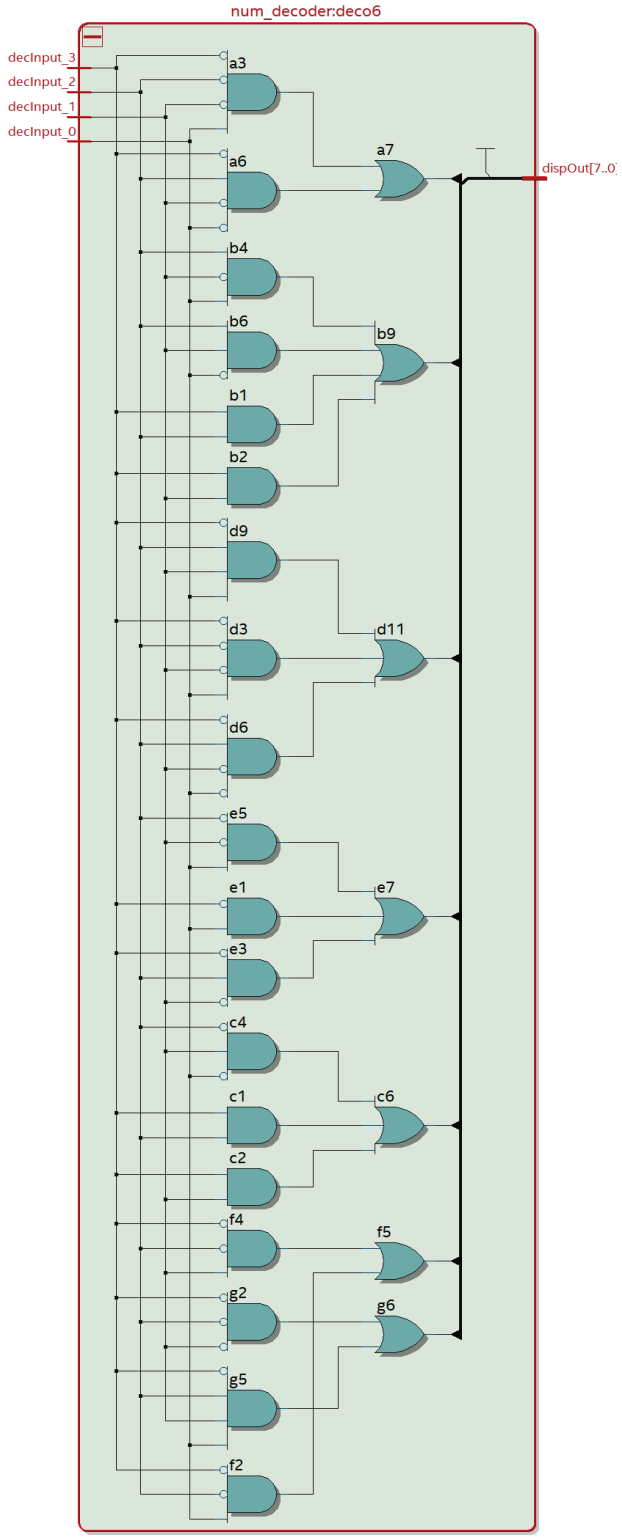
5. Binary to BCD Converter Module:



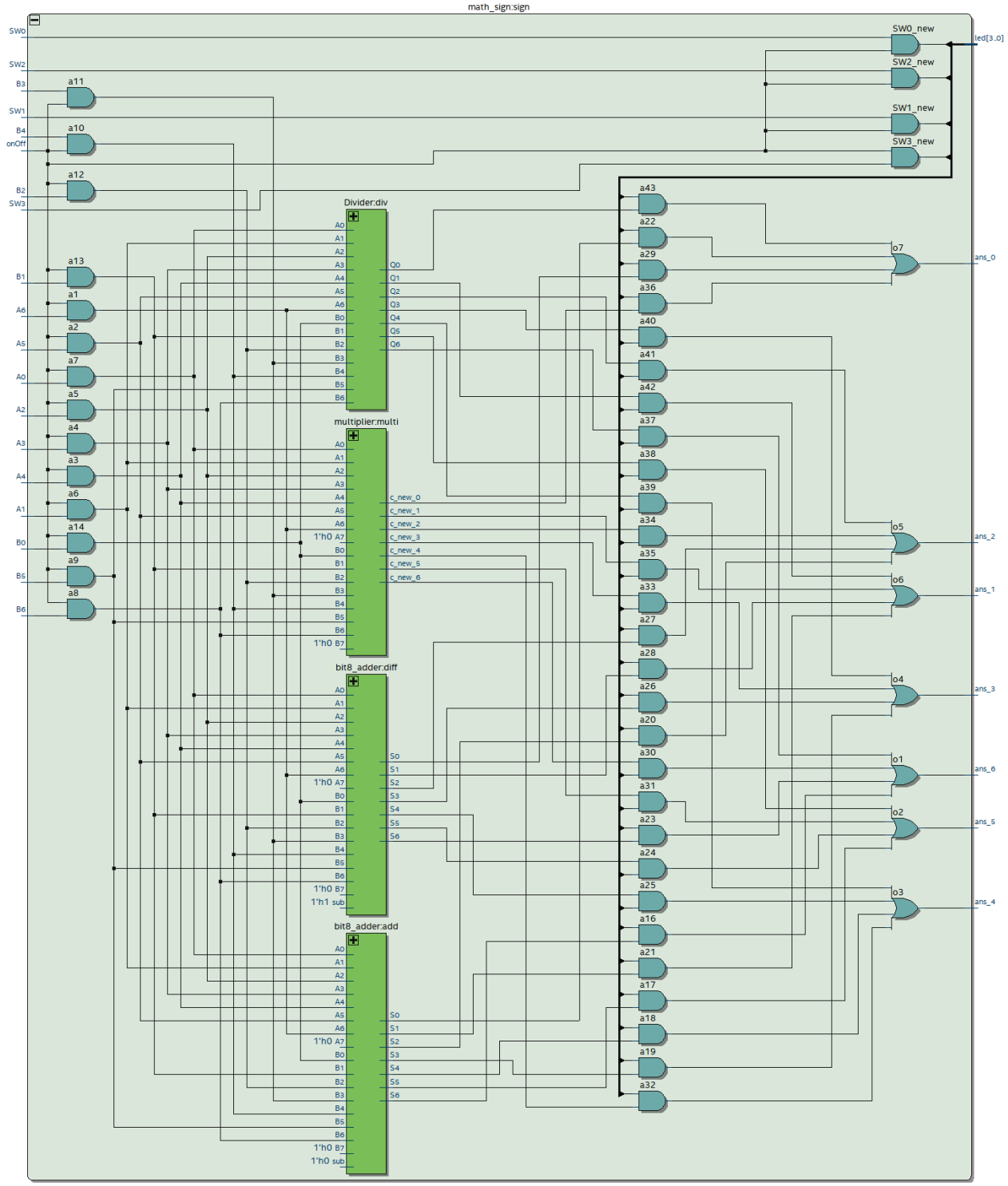
6. ADD-3 Module:



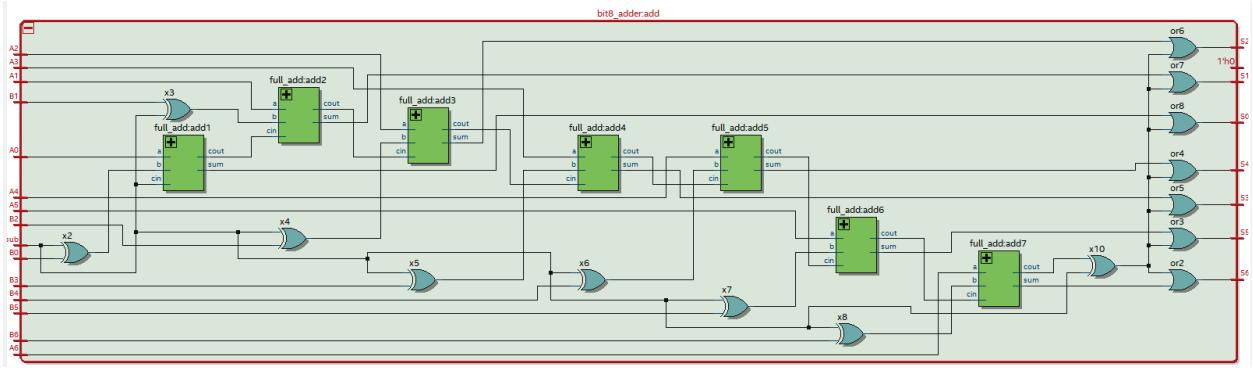
7. Decoder Module:



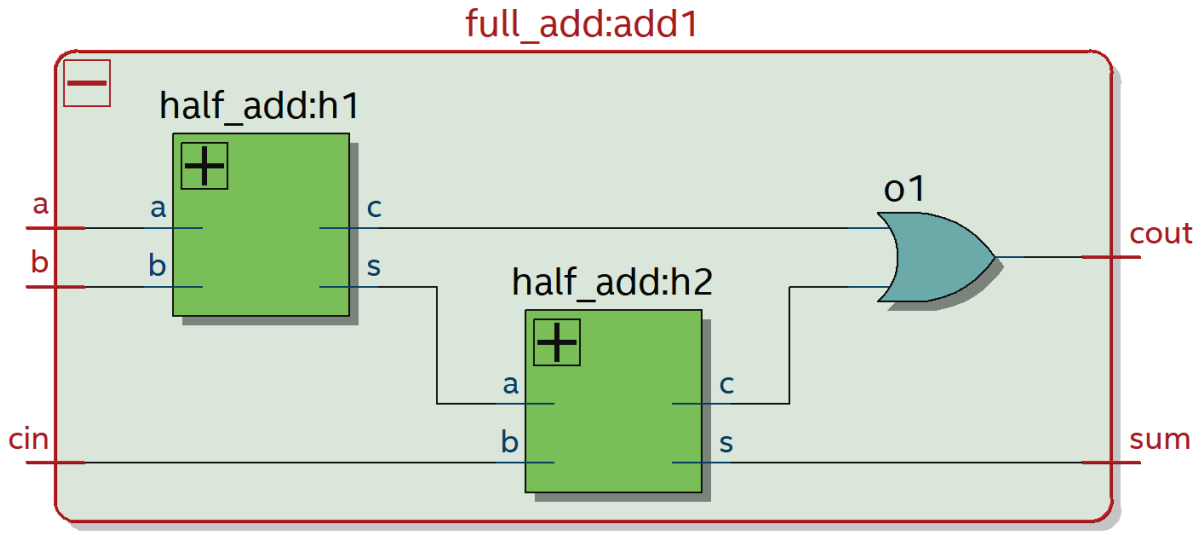
8. Operation Module:



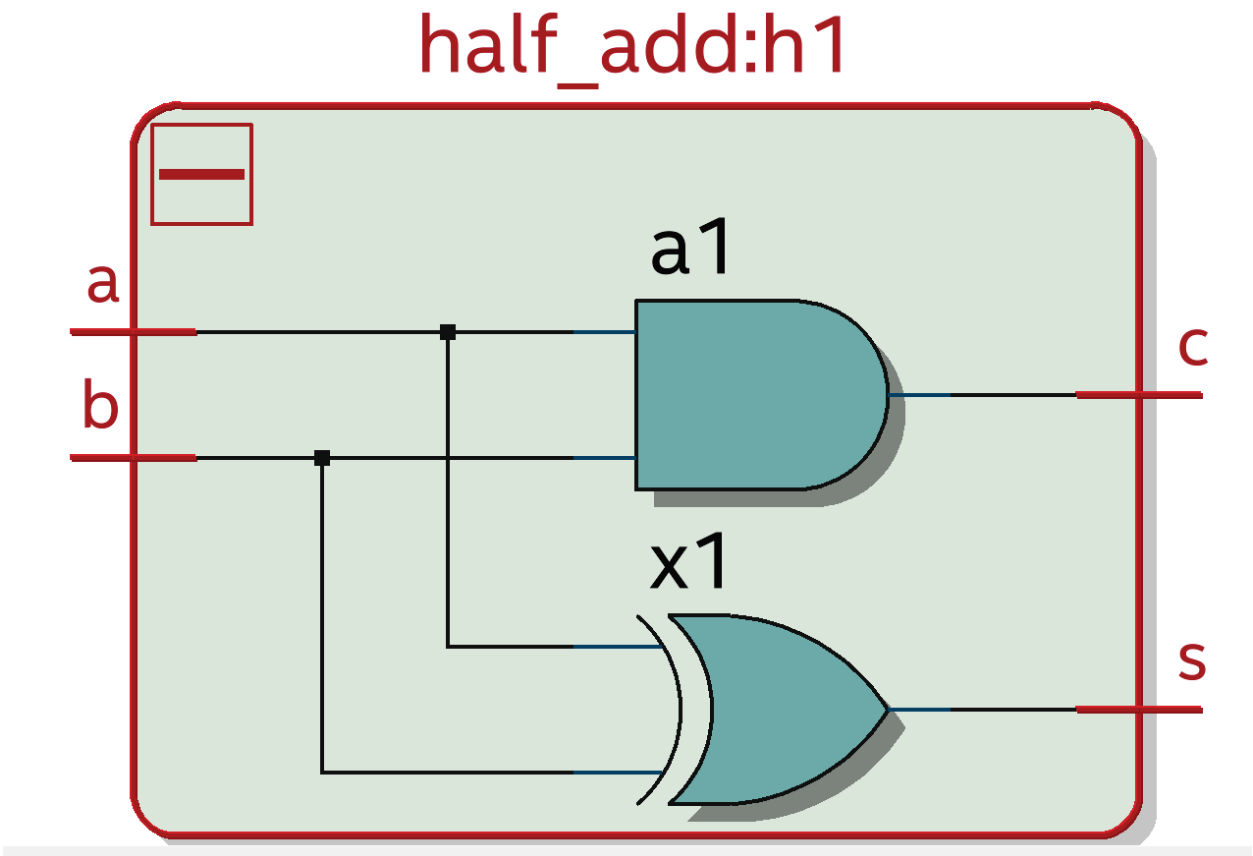
9. Adder/Subtractor Module:



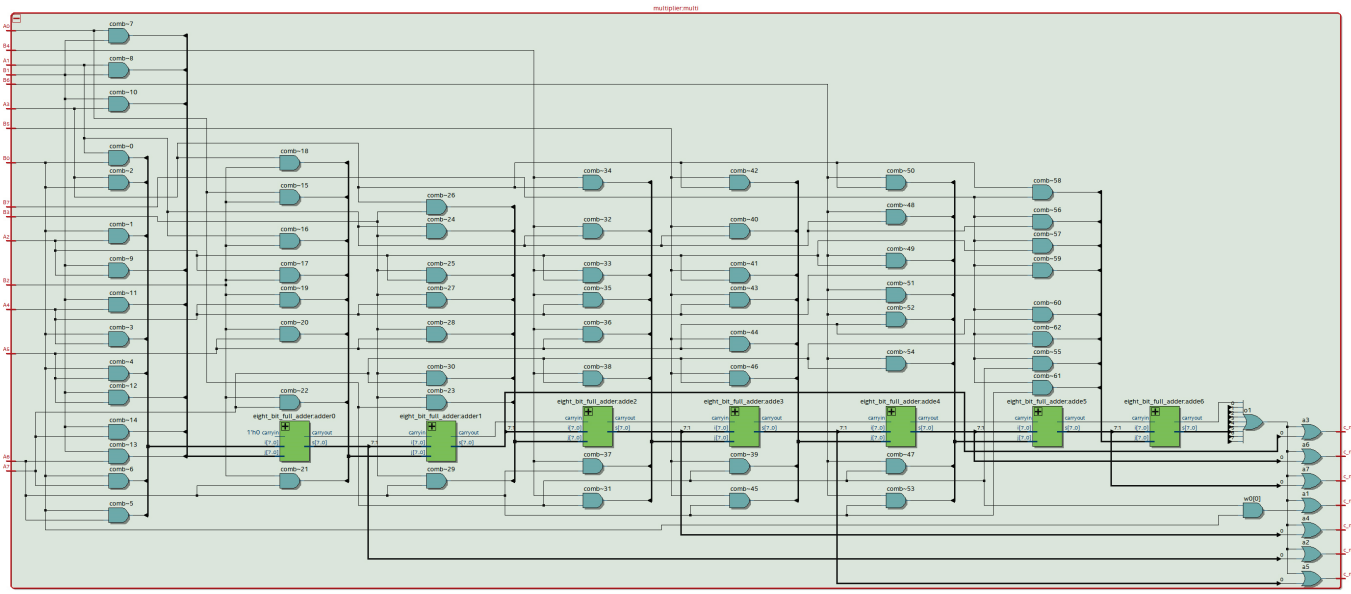
10. Full Adder module:



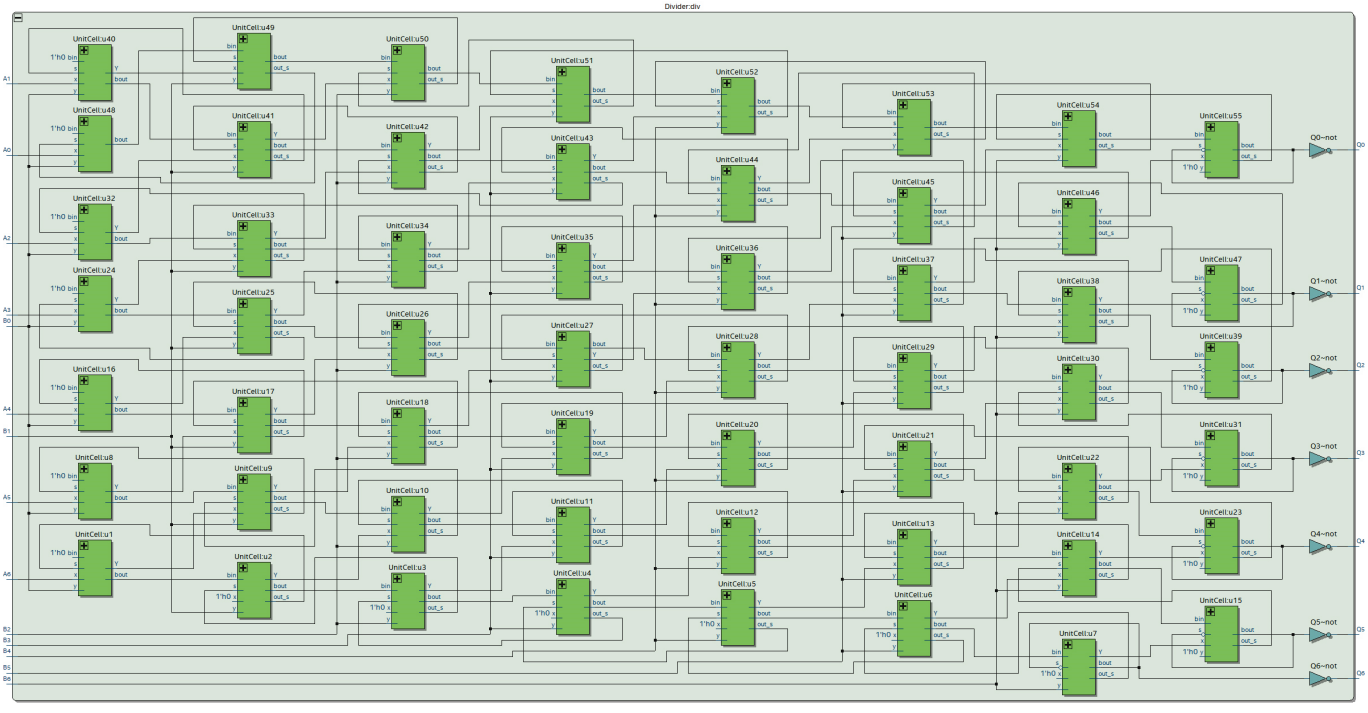
11. Half Adder Module:



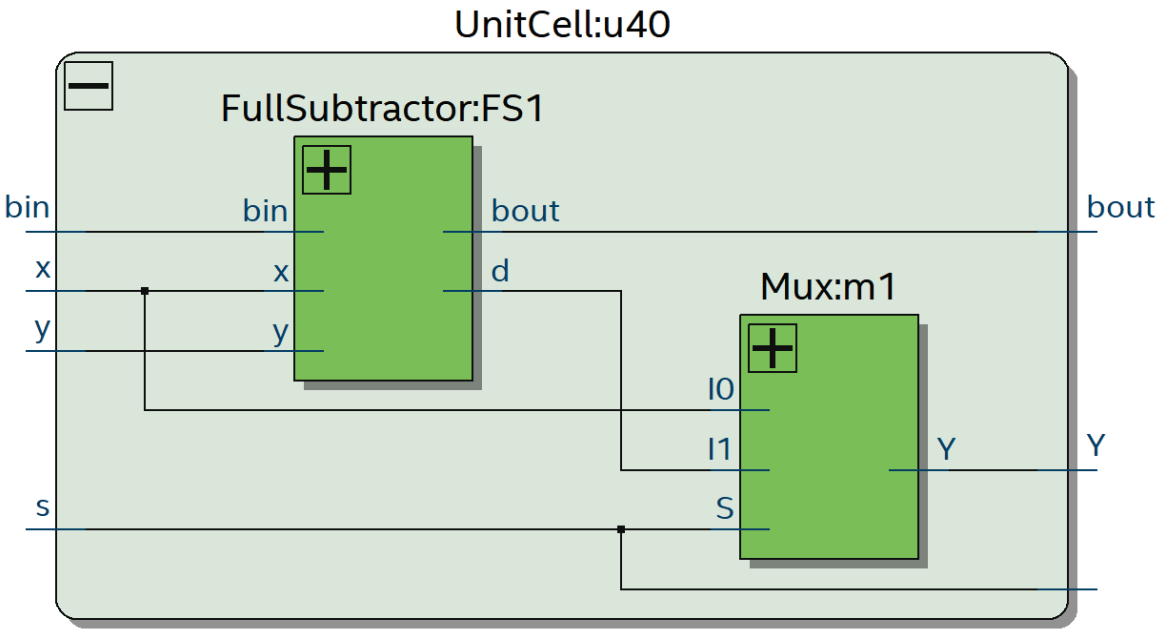
12. Multiplier Module:



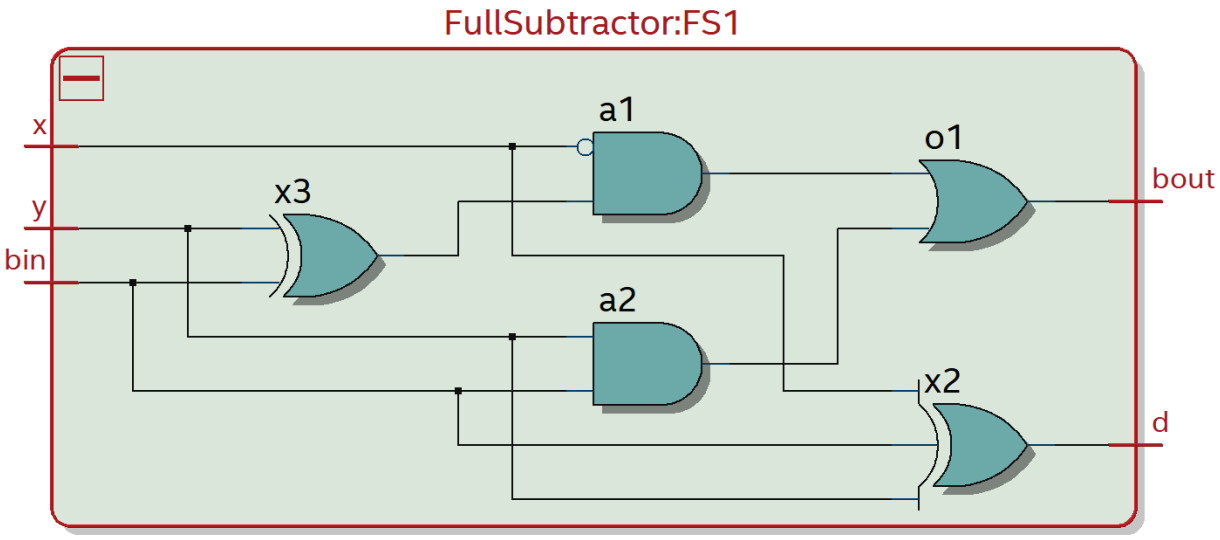
13. Divider Module:



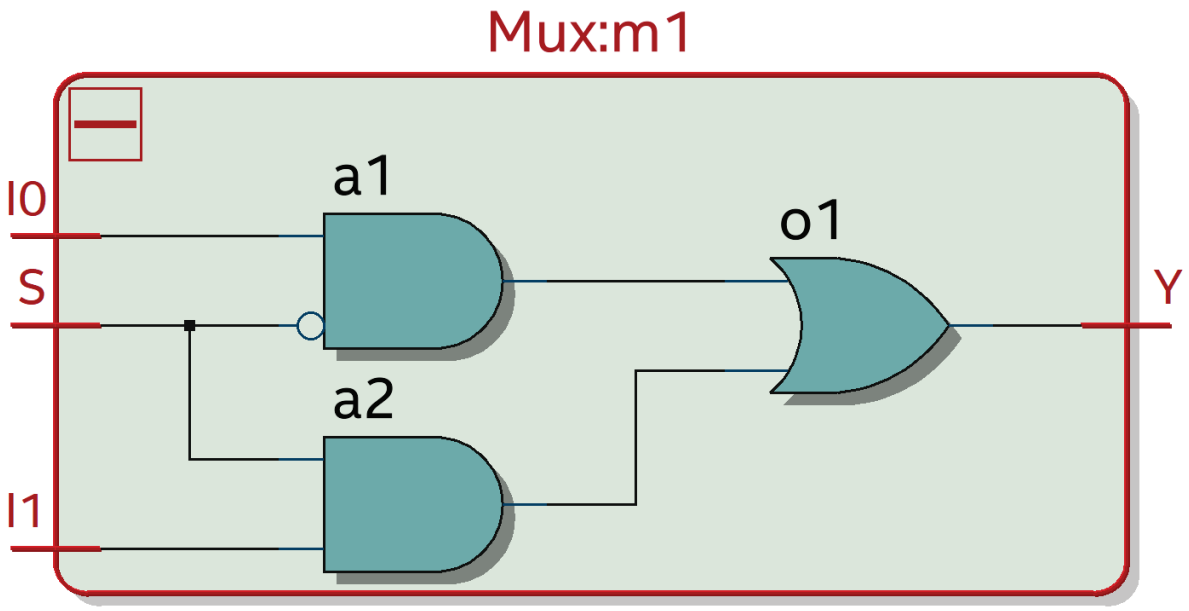
14. Unit Cell Module:



15. Full Subtractor Module:



16. Multiplexer Module:



7- SEGMENT DISPLAY DECODER K-MAPS AND EQUATION

DC \ BA	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	0	0	0	0

10	0	0	0	0

F_a= B'AD'C'+B'A'D'C

DC \ BA	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	1	1	1
10	0	0	1	1

F_b= DC+BD+BA'C+B'AC

DC \ BA	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

F_c= DC+BD+BA'C'

DC \ BA	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	0	0
10	0	0	0	0

F_d= B'AD'C'+B'A'D'C+BAD'C

DC \ BA	00	01	11	10
00	0	1	1	0

01	1	1	1	0
11	0	0	0	0
10	0	1	0	0

F_e= AD'+B'AC'+B'D'C

BA / DC	00	01	11	10
00	0	1	1	1
01	0	0	0	0
11	0	0	0	0
10	0	0	0	0

F_f= AD'C'+BD'C'

BA / DC	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	0	0	0	0
10	0	0	0	0

F_g= B'D'C'+BAD'C

D-LATCH STATE DIAGRAM, STATE TABLE AND STATE EQUATION

State Truth Table:

Q	Q_{next}	D
0	0	0
0	1	1
1	0	0
1	1	1

State Table:

Q \ D	0	1
0	0	1
1	0	1

State Equation:
$Q(t+1) = Q_{next} = D$

State Diagram: