实验四预习

用 VHDL 语言编写 SM

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_unsigned.all;
4
5   entity zjw_SM is
6       port(EN: in std_logic;
7            clk: in std_logic;
8            SM: out std_logic);
9   end zjw_SM;
10
11  architecture behavioral of zjw_SM is
12  signal d: std_logic:='0';
13  begin
14      process(clk)
15      begin
16      if (clk='0' and clk'event and EN='1') then
17          d <= not d;
18      else d <= d;
19      end if;
20      end process;
21      SM <= d;
22  end behavioral;
```

用 VHDL 语言编写程序计数器 PC

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.std_logic_unsigned.all;
4
5  entity zjw_PCjishuqi is
6      port(CIN: in std_logic_vector(7 downto 0);
7           IN_PC, LD_PC: in std_logic;
8           Reset,clk,NOP: in std_logic;
9           PC: out std_logic_vector(7 downto 0));
10 end zjw_PCjishuqi;
11
12 architecture behavioral of zjw_PCjishuqi is
13 signal d: std_logic_vector(7 downto 0):="00000000";
14 begin
15     process(LD_PC,Reset,clk,NOP)
16     begin
17     if Reset='1' then
18         d <= "00000000";
19     elsif clk='0' and clk'event then
20         if NOP='1' or (LD_PC='1' and IN_PC='1') then
21             d<=d+1;
22         elsif LD_PC='1' and IN_PC='0'then
23             d<=CIN;
24         end if;
25     end if;
26     end process;
27     PC <= d;
28 end behavioral;
```

用 VHDL 语言编写寄存器组

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3
4   entity zjw_jicunqizu is
5       port(CIN: in std_logic_vector(7 downto 0);
6       RAA, RWBA: in std_logic_vector(1 downto 0);
7       N_WE,rst,clk: in std_logic;
8       A_OUT, B_OUT: out std_logic_vector(7 downto 0));
9   end zjw_jicunqizu;
10
11  architecture behavorial of zjw_jicunqizu is
12  signal A,B,C: std_logic_vector(7 downto 0):="00000000";
13  begin
14      A_OUT<=A when RAA="00" else
15              B when RAA="01" else
16              C when RAA="10" or RAA="11";
17      B_OUT<=A when RWBA="00" else
18              B when RWBA="01" else
19              C when RWBA="10" or RWBA="11";
20      process(rst,N_WE,RWBA,RAA,clk)
21      begin
22      if rst = '1' then
23          A <= "00000000";
24          B <= "00000000";
25          C <= "00000000";
26      elsif N_WE='0' then
27          if clk'event and clk = '0' then
28              if(RWBA="00") then
29                  A<=CIN;
30              elsif(RWBA="01") then
31                  B<=CIN;
32              elsif(RWBA="10") then
33                  C<=CIN;
34              end if;
35          end if;
36      end if;
37      end process;
38  end;
```

采用 LPM_RAM_IO 定制