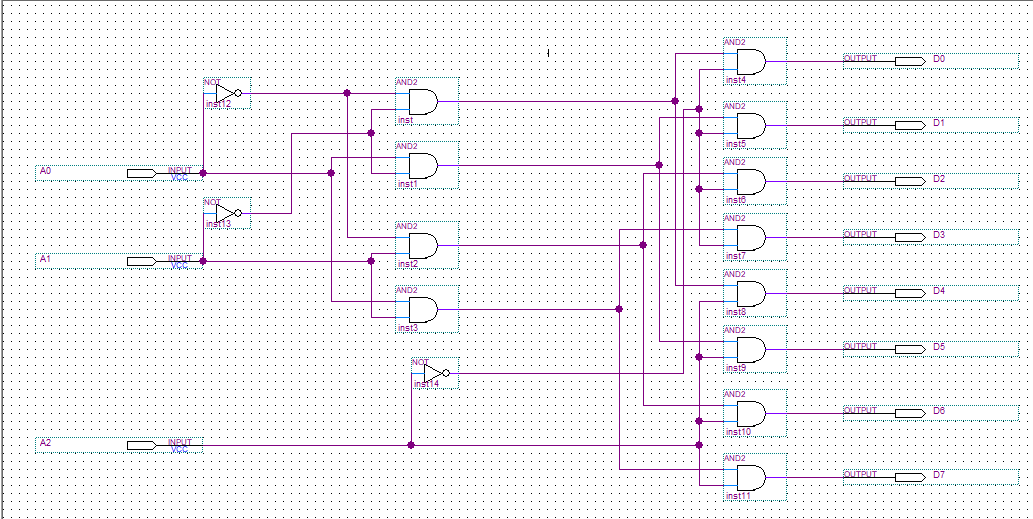
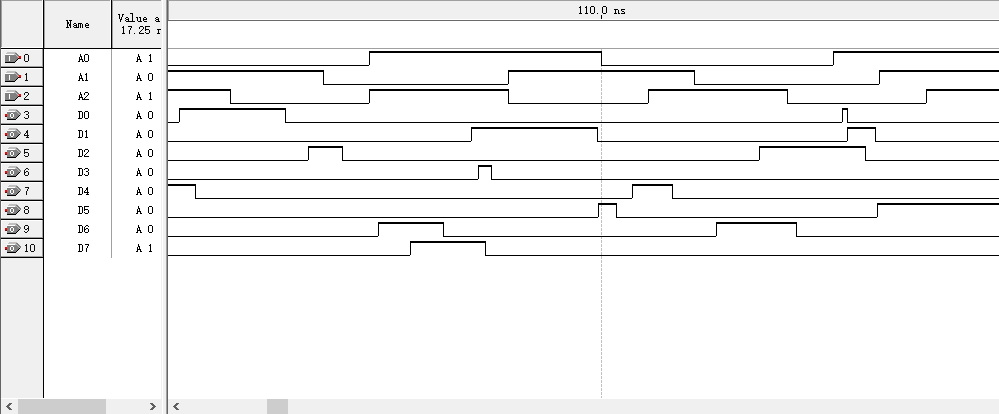
# 3-8译码器的原理图



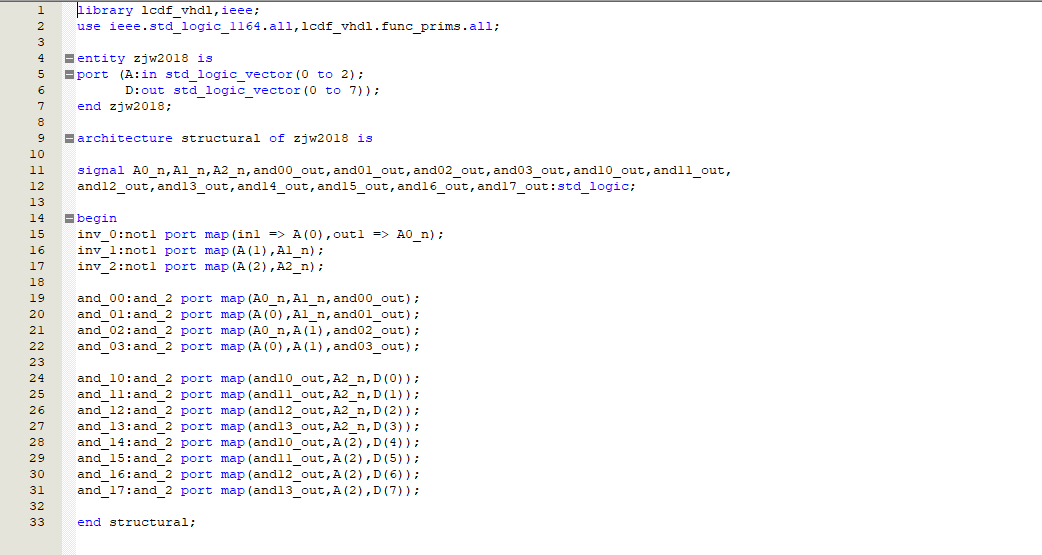
**输入：A0,A1,A2**

**输出：D0,D1,D2,D3,D4,D5,D6,D7**

**仿真结果：**

****

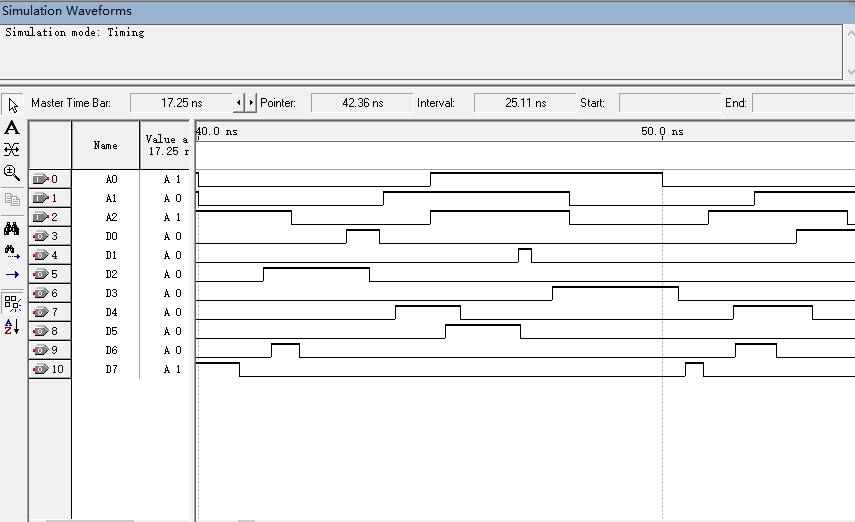
# 3-8译码器VHDL程序



**输入：A0,A1,A2**

**输出：D0,D1,D2,D3,D4,D5,D6,D7**

**仿真结果：**

****

# 模型机指令译码器的VHDL程序

