SOC Design Report

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***Abstract*—Abstract goes here. Use this latex template as our report template.**

I. Outline

II. NAND logic gate

In this exercise the design of the NAND gate was expected to have minimum area while to have high fanout output(fanout =8). In order to find the delay time between input and output of the NAND gate, the Elmore Delay model **?** was used in the design.

A. Design and Optimization

As shown in the Figure 1, NAND gate is constructed by two parallel connected PMOS transistors and two serial connected NMOS transistors.

Although transistors have complicate current-voltage behaviour, turned on transistors can be assumed as resistors, a chain of transistors can be represented as an RC ladder, as shown in Figure 2. Therefore the Elmore delay model can estimate the delay of this RC ladder in terms of the path resistance and capacitance of a node on the ladder and the supply:

$$t_{\text{pd}} = \sum_i Rn{-}iCi \tag{1}$$

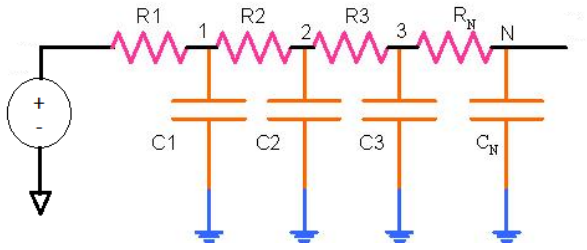


Figure 2. Simple Elmore delay model

Therefore it is possible to use this method as the reference to calculate the width of logic gate, since the propagation delay is dependent to it and the capacitance of the load.
Typically in the logic gate, for parallel connected transistors, the total resistance is lower when they are all on. In many gates, the worst-case delay is usually because only on the parallel transistor is on **?**. So when applying the Elmore delay model in the NAND design, one of input is connected to vdd while the other one is connected in the path, as shown in Figure 3.

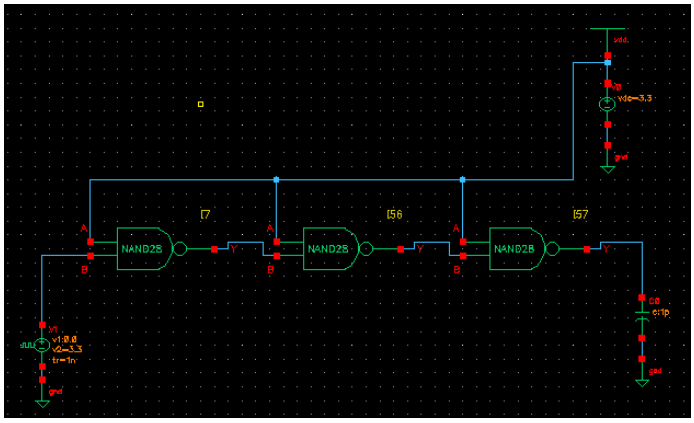


Figure 3. NAND Elmore delay model

While deceasing the width of NMOS and increasing the width of PMOS, the propagation delays, which is the maximum time from input to output crossing 50%, of the rising edge and falling edge are also changing. When the certain ratio between the width of PMOS and NMOS is reached, the propagation delay between rising edge and falling edge of logic gate will become similar. In another word, the signal rise and fall at the output of logic gate will become almost identical to the input, only with amount of delay. In the design, the ratio between PMOS and NMOS is 2.3, as found in the Figure 4. Design and Optimisation

III. NAND

IV. NOR2

V. XOR2

VI. DFF

The design goal for the DFF was high speed. Initially it was designed using a standard circuit composed of NAND gates. However then the option of Transmission gates was considered and found to be superior. Using transmission gates a master slave style flip plot was produced as shown in figure 5. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology

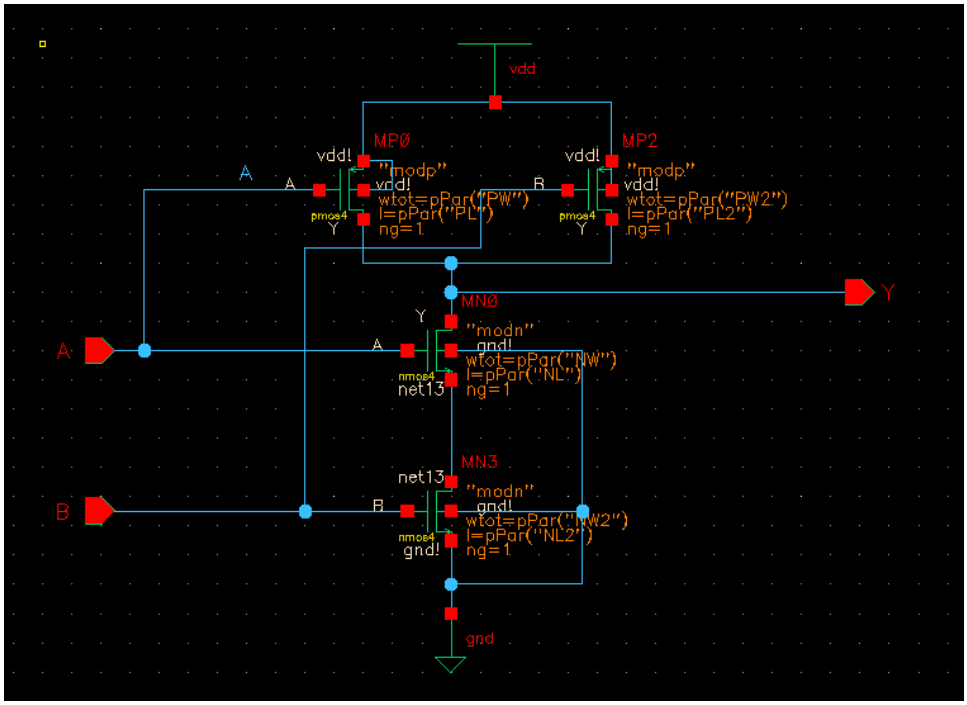


Figure 1. NAND gate schematic

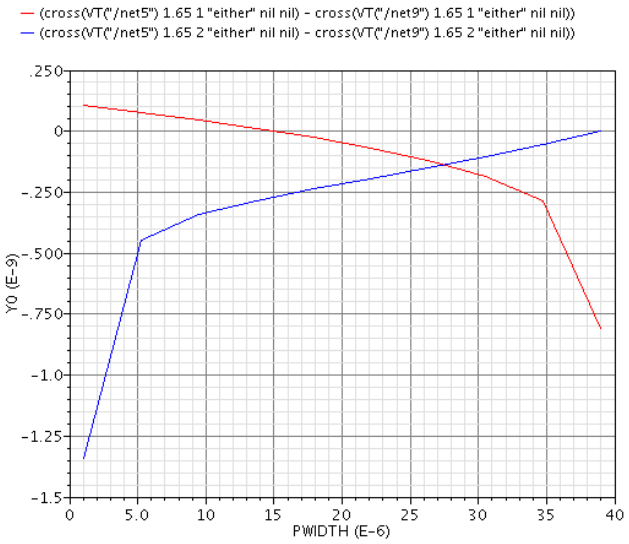


Figure 4. Ratio of width of PMOS and NMOS in NAND gate

used the only parameter used is NWIDTH for each gate as PWIDTH is simply 3 times that.

In terms of transistor sizes the Transmission gate and the Inverters were considered as separate parameters although there was only one size for each family This may have been a bad decision in terms of the inverter creating CLKN as it has to drive 4 components where as the maximum of any other gate was only 2, However in this situation it was not much of a problem as the relatively large transistor sizes chosen to deliver high speed negated much of this effect.

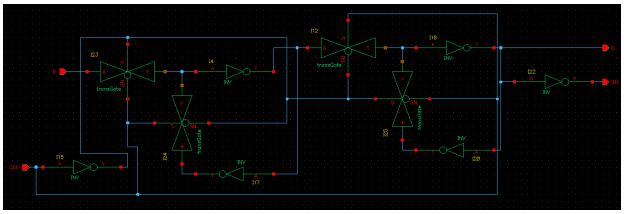
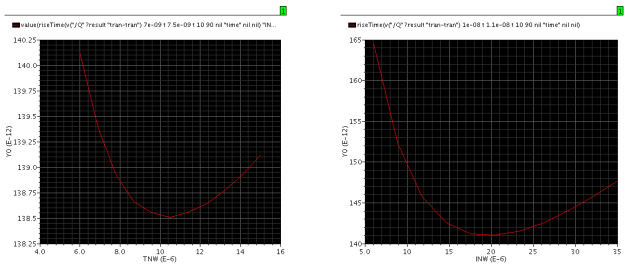


Figure 5. DFF Schematic.

By using the rise times, as shown in figure 6, among other metrics when measured in the test circuit Values for NMOS and PMOS widths were chosen based on giving maximum performance. These turned out to be a 11μm for the transmission gate and 17.5 μm for the inverter. This is quite large but as the only restriction on the design is that it must be high speed regardless of area.



(a) Inverter N Width (b) Transmission gate N Width

Figure 6. Transistor size effect on rise time.

One point of note is that the QN output is created via a separate inverter rather than taking the signal from either side

of the left most transmission gate. This was because large capacitive loads on QN caused incorrect circuit behaviour as this effected the transition time across the transmission gate which incorrect circuit behaviour on extreme loads where the slave circuit wouldn't latch new master value.

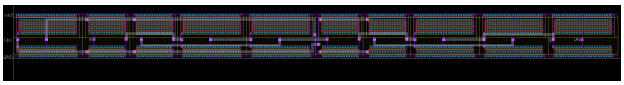


Figure 7. DFF Layout.

Due to the large transistor size layout was not particularly difficult as there was a lot of space for gate interconnects. When laying out the gates were placed in an order such as to minimise local process variations however with such large gates this is not particularly effective. A future layout revision could increase robustness by splitting the transistors into 2 or 3 smaller transistors of equal total size and interleaving them.

VII. Duel Edge Triggered Flip Flop

The Dual Edge Triggered Flip Flop (DETFF) was designed using transmission gates as this allows the design to contain a minimum of 20 transistors (18 if there is no requirement for QN). Figure 8 shows the schematic produced. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is 3 times that.

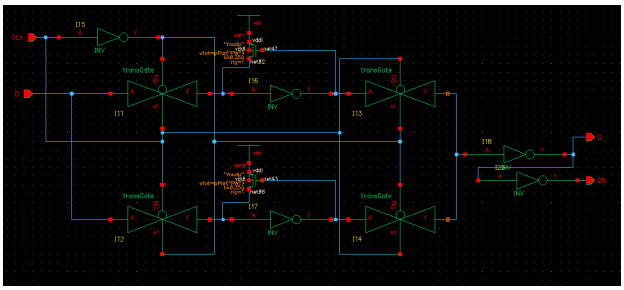


Figure 8. DETFF Schematic.

The size of the gates where considered in terms of Transmission gates NMOS Width, Inverters NMOS Width and the 2 PMOS pull up transistors width. These parameters were brought to minimum values of 1.2μm 2μm and 4μm (Trans NW,Inv NW,Pwidth respectively) before correct operation ceased. However these values were found to be to small for effective layout without enough space for interconnects and routing to fit due to DRC constraints, they also gave speed performance deemed unacceptable. The sizes were increased until sensible routing and speed was achieved at values of 2.4μm 3.2μm and 4.7μm (Trans NW,Inv NW,Pwidth respectively).

Figure 9 shows the final layout of the DETFF its easily visible that this is towards the limit of gate size for the given layout in particular in crowded areas such as the between gates 6 and 7. The option of using MET3 in this area was considered

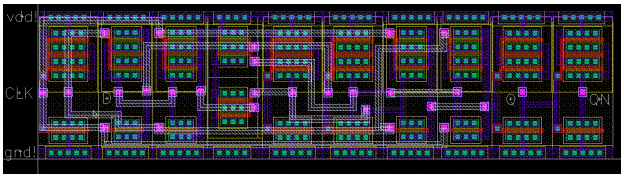


Figure 9. DETFF Layout.

but it was not specified this layer was available for use also as a consideration to real world manufacture having to add another metal layer because of a single gate when a 2 layer design is possible would not be viable.

The layout of the design initial versions of the Transmission and inverter were lain out at the minimum possible width and copied to populate the design and as interconnects were placed some of them had the wells expanded to allow for interconnect spacing.The pull-up PMOS are stacked vertically so as to not waste horizontal space as the rail distance is fixed meaning total area is effected by the width of the entire gate.

VIII. C Element

IX. Dual Rail AND

The design goal for the Dual Rail AND was small area. The design was chosen based on its simplicity and the fact that the C-Element had the same goal of small area. This fact allowed us to simply reuse the C-Element with fixed parameters and reuse its layout saving substantial amounts of work in layout. there is a disparity between the Required fan-outs however as the fanout of the c-element is two and the AND has a fanout of one meaning the extra area gained is not too great.

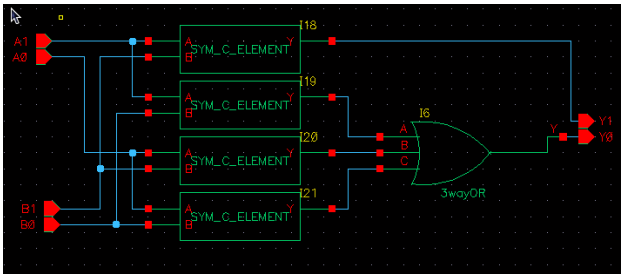


Figure 10. Dual Rail AND Schematic.

The only element in this design that required optimisation in design was the 3 input OR gate. This was constructed from a 3 input NOR gate and an inverter on the output. The PMOS and NMOS ratio was set at 3 and the characteristics matched to that of the output of the C-element meaning there should be minimum disparity between the Y0 and Y1 signals. The Nwidth was finalised at 4μm This is slightly larger than is strictly necessary but helps reduce the propagation disparity between the outputs.

X. 1-bit Subtractor

XI. 2-to-1 Multiplexor

XII. Mutex Element

Testing

XIII. NAND

XIV. NOR2

XV. XOR2

XVI. DFF

TEST CIRCUIT
FUNCTIONALITY TESTING
SPEED TESTING
LAYOUT VS SCHEMATIC
ERRONIOUS BEHAVIOUR

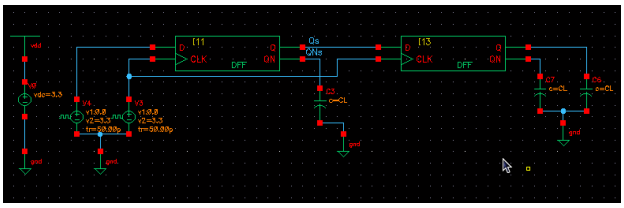


Figure 11. DFF Test Circuit Schematic.

XVII. Duel Edge Triggered Flip Flop

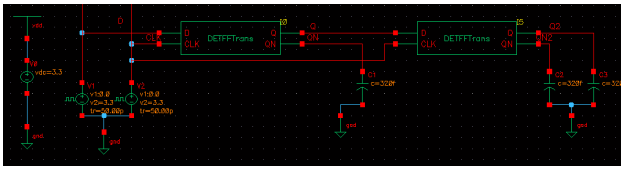


Figure 12. DETFF Test Circuit Schematic.

XVIII. C Element

XIX. Dual Rail AND

TEST CIRCUIT

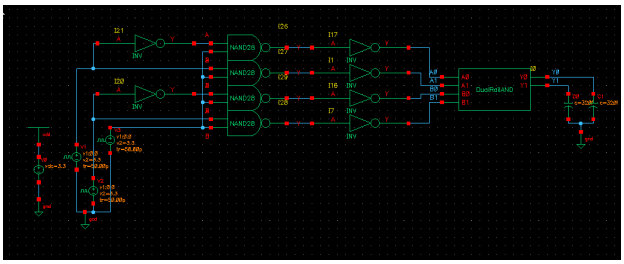


Figure 13. Dual Rail AND Test Schematic.

FUNCTIONALITY TESTING
SPEED TESTING
LAYOUT VS SCHEMATIC
ERRONIOUS BEHAVIOUR

XX. 1-bit Subtractor

XXI. 2-to-1 Multiplexor

XXII. Mutex Element

Impact of Variablility

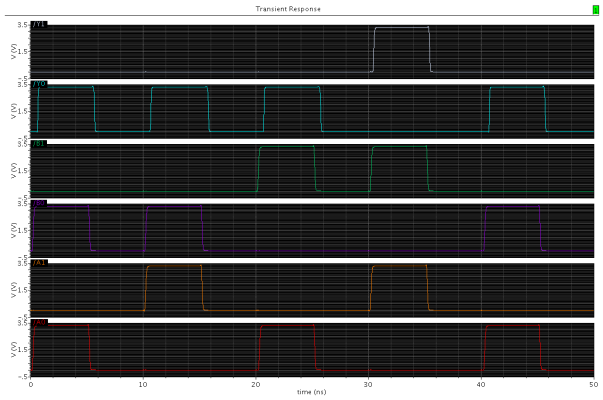


Figure 14. Dual Rail AND Simulation showing correct operation.

XXIII. NAND

XXIV. NOR2

XXV. XOR2

XXVI. DFF

VDD
TEMP

XXVII. Duel Edge Triggered Flip Flop

VDD
TEMP

XXVIII. C Element

XXIX. Dual Rail AND

XXX. 1-bit Subtractor

XXXI. 2-to-1 Multiplexor

XXXII. Mutex Element

Conclusions

References