# SOC Design Report

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***Abstract*—Abstract goes here. Use this latex template as our report template.**

## I. Outline

## II. Design and Optimisation

### A. NAND

### B. NOR2

### C. XOR2

### D. DFF

The design goal for the DFF was high speed. Initially it was designed using a standard circuit composed of NAND gates. However then the option of Transmission gates was considered and found to be superior. Using transmission gates a master slave style flip plot was produced as shown in figure 1. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As $0.35\mu$ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is simply 3 times that.

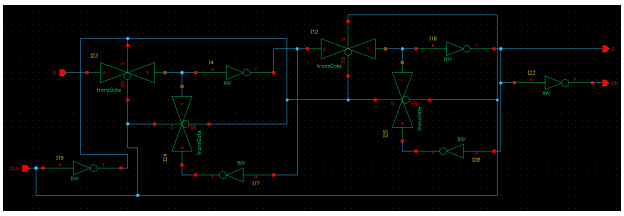
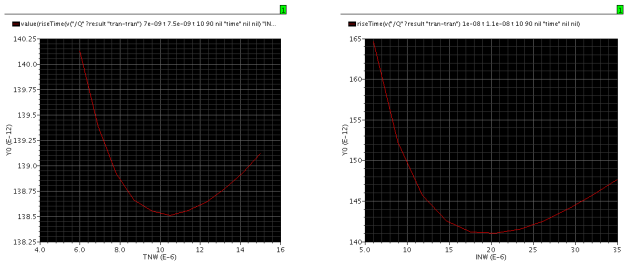


Figure 1. DFF Schematic.

In terms of transistor sizes the Transmission gate and the Inverters were considered as separate parameters although there was only one size for each family This may have been a bad decision in terms of the inverter creating CLKN as it has to drive 4 components where as the maximum of any other gate was only 2, However in this situation it was not much of a problem as the relatively large transistor sizes chosen to deliver high speed negated much of this effect.

By using the rise times, as shown in figure 2, among other metrics when measured in the test circuit Values for NMOS and PMOS widths were chosen based on giving maximum performance. These turned out to be a $11\mu$m for the transmission gate and 17.5 $\mu$m for the inverter. This is quite large but as the only restriction on the design is that it must be high speed regardless of area.



(a) Inverter N Width (b) Transmission gate N Width

Figure 2. Transistor size effect on rise time.

One point of note is that the QN output is created via a separate inverter rather than taking the signal from either side of the left most transmission gate. This was because large capacitive loads on QN caused incorrect circuit behaviour as this effected the transition time across the transmission gate which incorrect circuit behaviour on extreme loads where the slave circuit wouldn't latch new master value.

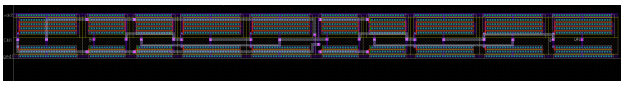


Figure 3. DFF Layout.

Due to the large transistor size layout was not particularly difficult as there was a lot of space for gate interconnects. When laying out the gates were placed in an order such as to minimise local process variations however with such large gates this is not particularly effective. A future layout revision could increase robustness by splitting the transistors into 2 or 3 smaller transistors of equal total size and interleaving them.

### E. Dual Edge Triggered Flip Flop

The Dual Edge Triggered Flip Flop (DETFF) was designed using transmission gates as this allows the design to contain a minimum of 20 transistors (18 if there is no requirement for QN). Figure 4 shows the schematic produced. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As $0.35\mu$ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is 3 times that.

The size of the gates where considered in terms of Transmission gates NMOS Width, Inverters NMOS Width and the

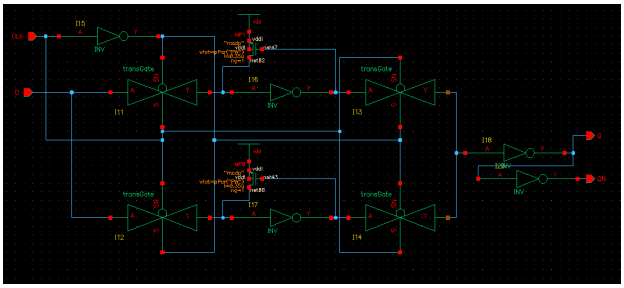


Figure 4. DETFF Schematic.

2 PMOS pull up transistors width. These parameters were brought to minimum values of 1.2$\mu$m 2$\mu$m and 4$\mu$m (Trans NW,Inv NW,Pwidth respectively) before correct operation ceased. However these values were found to be to small for effective layout without enough space for interconnects and routing to fit due to DRC constraints, they also gave speed performance deemed unacceptable. The sizes were increased until sensible routing and speed was achieved at values of 2.4$\mu$m 3.2$\mu$m and 4.7$\mu$m (Trans NW,Inv NW,Pwidth respectively).

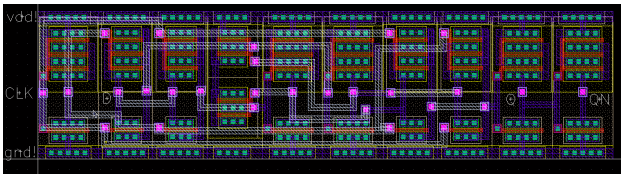



Figure 5. DETFF Layout.

Figure 5 shows the final layout of the DETFF its easily visible that this is towards the limit of gate size for the given layout in particular in crowded areas such as the between gates 6 and 7. The option of using MET3 in this area was considered but it was not specified this layer was available for use also as a consideration to real world manufacture having to add another metal layer because of a single gate when a 2 layer design is possible would not be viable.

The layout of the design initial versions of the Transmission and inverter were lain out at the minimum possible width and copied to populate the design and as interconnects were placed some of them had the wells expanded to allow for interconnect spacing.The pull-up PMOS are stacked vertically so as to not waste horizontal space as the rail distance is fixed meaning total area is effected by the width of the entire gate.

### *F. C Element*

### *G. Dual Rail AND*

The design goal for the Dual Rail AND was small area. The design was chosen based on its simplicity and the fact that the C-Element had the same goal of small area. This fact allowed us to simply reuse the C-Element with fixed parameters and reuse its layout saving substantial amounts of work in layout. As the C-Element fan out is two this works well as the Y1 signal must drive 2 C Elements inside a subsequent AND giving an effective fanout of 1 which meets specification.

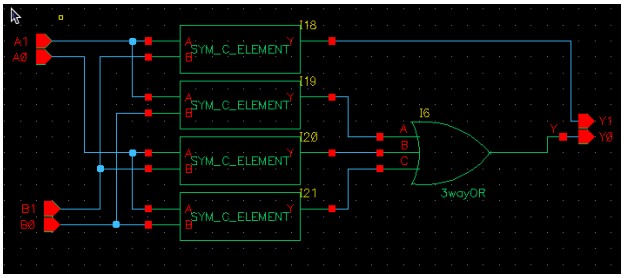



Figure 6. Dual Rail AND Schematic.

The only element in this design that required optimisation in design was the 3 input OR gate. This was constructed from a 3 input NOR gate and an inverter on the output. The PMOS and NMOS ratio was set at 3 and the characteristics matched to that of the output of the C-element meaning there should be minimum disparity between the Y0 and Y1 signals. The Nwidth was finalised at 4$\mu$m This is slightly larger than is strictly necessary but helps reduce the propagation disparity between the outputs.

### *H. 1-bit Subtractor*

### *I. 2-to-1 Multiplexor*

### *J. Mutex Element*

## III. Testing

### *A. NAND*

### *B. NOR2*

### *C. XOR2*

### *D. DFF*

Figure 7 shows the test circuit used to test the DFF.The vpulse elements allow generation of a clock and an alternating D signal using correct timing and phase. By connecting the Q of the first gate to that of the second it also is useful for demonstrating the required fanout of 1. By choosing suitable values for CLK D and load capacitance a variety of situations can be simulated.

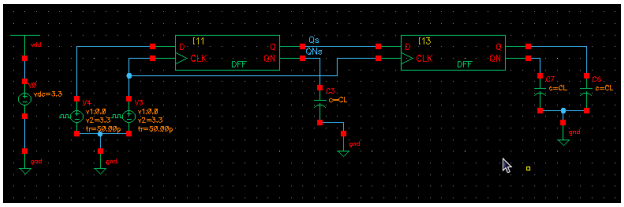



Figure 7. DFF Test Circuit Schematic.

Figure 8 shows the output of a simulation using the above circuit. The load is set to 320 fF to represent a relatively high load case. As is shown the output Q does not change until the positive clock edge and holds its data until subsequent positive edges. The input D also propagates correctly through both flip flops.

SPEED TESTING

Figure 9 shows a zoomed in section of the output of the simulation. This shows a Q rise time of 0.21 ns and a fall

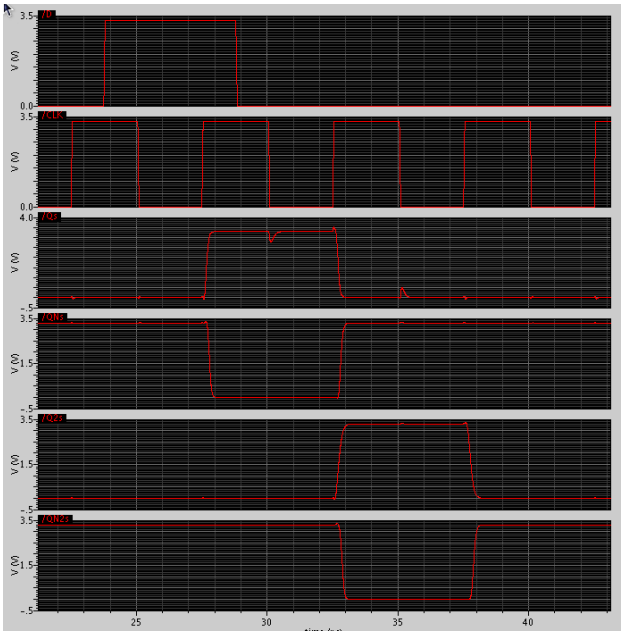


Figure 8. DFF Functionality Test.

time of 0.22 ns which for a 320pF load is quite fast. However the design does suffer slightly from its large transistors which although deliver good rise time the propagation delay is 0.36 ns.

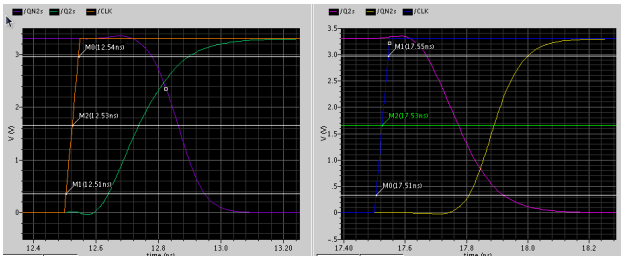


Figure 9. DFF Speed Test.

The disruption in the Q signal connected to the input of the second gate when the clock pulses as seen at 30ns in figure 8 is caused by the transmission gates switching on the clock edge and latching the data for the usbsequent edge. As this is below the threshold of 10 percent it should not cause any problems as part of a asynchronous or synchronous design.

### *E. Dual Edge Triggered Flip Flop*

Figure 10 shows the test circuit used to test the DFF.The vpulse elements allow generation of a clock and an alternating D signal using correct timing and phase. By connecting the Q of the first gate to that of the second it also is useful for demonstrating the required fanout of 1. By choosing suitable values for CLK D and load capacitance a variety of situations can be simulated.

Figure 11 shows the output of a simulation using the above circuit. The load is set to 320 fF to represent a relatively high load case. As is shown the output Q does not change until the positive clock edge and holds its data until subsequent clock

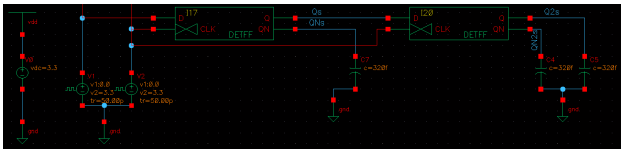


Figure 10. DETFF Test Circuit Schematic.

edges. The input D also propagates correctly through both flip flops.

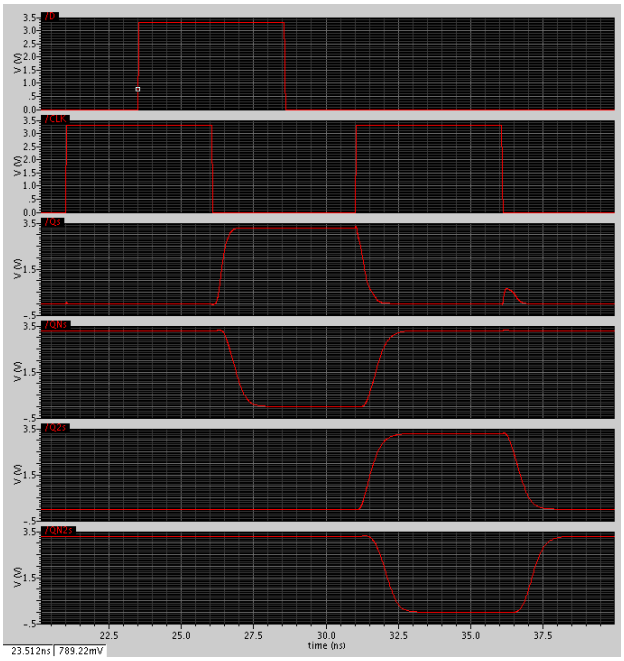


Figure 11. DETFF Functionality Test.

Figure 12 shows a zoomed in section of the output of the simulation. This shows a Q rise time of 0.8 ns and a fall time of 0.65 ns which for a 320pF load is reasonable for this gate. The disparity between the times suggest a different PMOS/Nmos ratio could be beneficial.

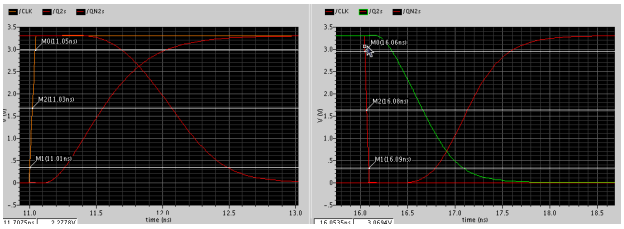


Figure 12. DETFF Speed Test.

The disruption in the Q signal connected to the input of the second gate when the clock pulses as seen at 30ns in figure 8 is caused by the transmission gates switching on the clock edge and latching the data for the subsequent edge. As this is below the threshold of 10 percent it should not cause any problems as part of a asynchronous or synchronous design.

### F. C Element

### G. Dual Rail AND

Figure 13 shows the test circuit for the Dual Rail AND (DRAND) there are 2 clocks for data generation one set at half the frequency of the other allowing for all 4 data states to be modelled. The outpus of the clocks are connected to the A/B 1 connections and also go through an inverter to create the relevant A/B 0 signal. The third clock is used in conjunction with the AND structure to add the '00' spacer state to reset the C Elements between data.

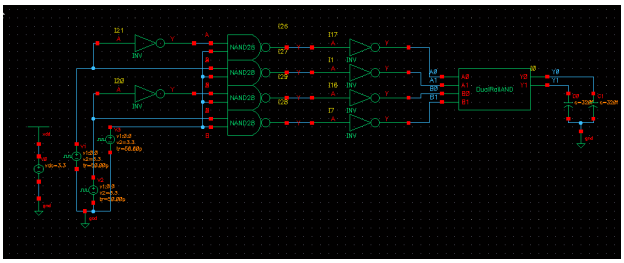


Figure 13. Dual Rail AND Test Schematic.

Figure 14 shows the output of a simulation using the above circuit. As you can see this the output Y0 goes low and Y1 goes high only when both A1 and B1 are asserted it also correctly transmits the '00' spacer behaviour.

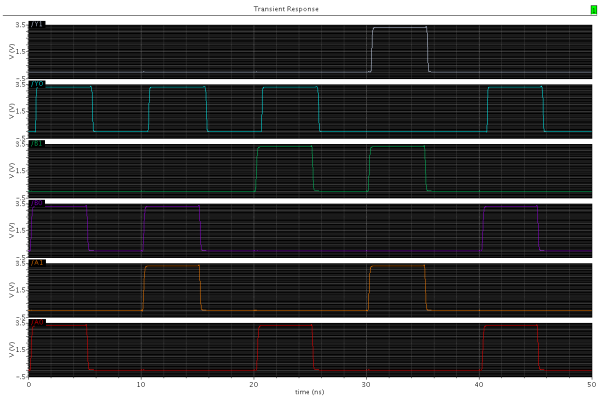



Figure 14. Dual Rail AND Simulation showing correct operation.

### H. 1-bit Subtractor

### I. 2-to-1 Multiplexor

### J. Mutex Element

TEST CIRCUIT FUNCTIONALITY TESTING SPEED TESTING LAYOUT VS SCHEMATIC ERRONIOUS BEHAVIOUR

## IV. Impact of Variablility

### A. NAND

### B. NOR2

### C. XOR2

### D. DFF

TEMP

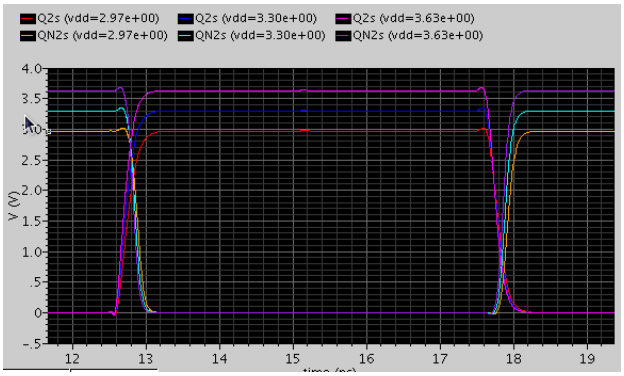



Figure 15. DFF effects of vdd.

### E. Dual Edge Triggered Flip Flop

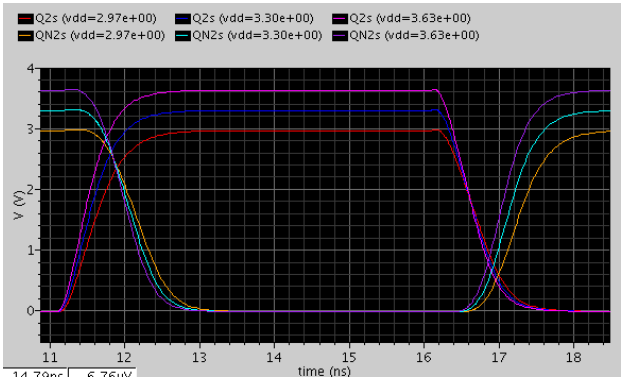



Figure 16. DETFF effects of vdd.

TEMP

### F. C Element

### G. Dual Rail AND

### H. 1-bit Subtractor

### I. 2-to-1 Multiplexor

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## V. Conclusions