

SOC Design Report

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Abstract—Abstract goes here. Use this latex template as our report template.

Outline

Design and Optimisation

- I. NAND
- II. NOR2
- III. XOR2
- IV. DFF

The design goal for the DFF was high speed. Initially it was designed using a standard circuit composed of NAND gates. However then the option of Transmission gates was considered and found to be superior. Using transmission gates a master slave style flip flop was produced as shown in figure 1. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is simply 3 times that.

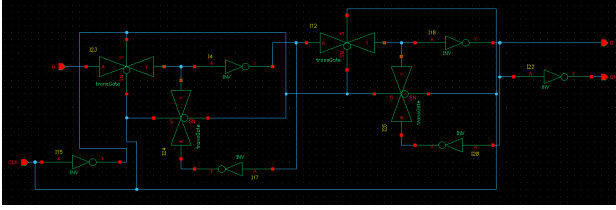


Figure 1. DFF Schematic.

In terms of transistor sizes the Transmission gate and the Inverters were considered as separate parameters although there was only one size for each family. This may have been a bad decision in terms of the inverter creating CLKIN as it has to drive 4 components whereas the maximum of any other gate was only 2. However in this situation it was not much of a problem as the relatively large transistor sizes chosen to deliver high speed negated much of this effect.

By using the rise times, as shown in figure 2, among other metrics when measured in the test circuit. Values for NMOS and PMOS widths were chosen based on giving maximum performance. These turned out to be a $11\mu\text{m}$ for the transmission gate and $17.5\mu\text{m}$ for the inverter. This is quite large but as the only restriction on the design is that it must be high speed regardless of area.

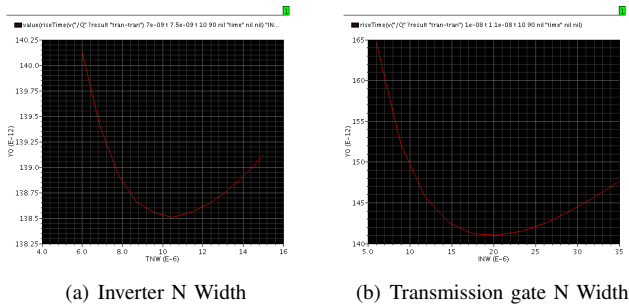


Figure 2. Transistor size effect on rise time.

One point of note is that the QN output is created via a separate inverter rather than taking the signal from either side

of the left most transmission gate. This was because large capacitive loads on QN caused incorrect circuit behaviour as this effected the transition time across the transmission gate which incorrect circuit behaviour on extreme loads where the slave circuit wouldn't latch new master value.

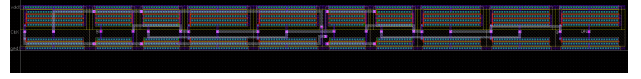


Figure 3. DFF Layout.

Due to the large transistor size layout was not particularly difficult as there was a lot of space for gate interconnects. When laying out the gates were placed in an order such as to minimise local process variations however with such large gates this is not particularly effective. A future layout revision could increase robustness by splitting the transistors into 2 or 3 smaller transistors of equal total size and interleaving them.

V. DUEL EDGE TRIGGERED FLIP FLOP

The Dual Edge Triggered Flip Flop (DETFF) was designed using transmission gates as this allows the design to contain a minimum of 20 transistors (18 if there is no requirement for QN). Figure 4 shows the schematic produced. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is 3 times that.

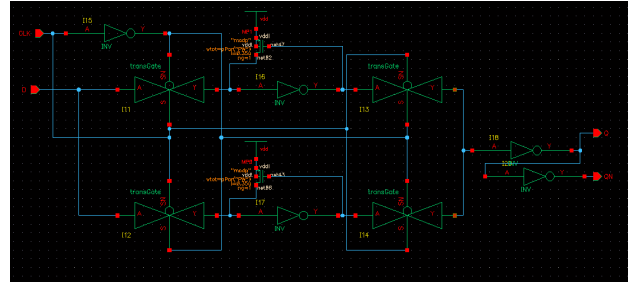


Figure 4. DETFF Schematic.

The size of the gates were considered in terms of Transmission gates NMOS Width, Inverters NMOS Width and the 2 PMOS pull up transistors width. These parameters were brought to minimum values of $1.2\mu\text{m}$, $2\mu\text{m}$ and $4\mu\text{m}$ (Trans NW, Inv NW, Pwidth respectively) before correct operation ceased. However these values were found to be too small for effective layout without enough space for interconnects and routing to fit due to DRC constraints, they also gave speed performance deemed unacceptable. The sizes were increased until sensible routing and speed was achieved at values of $2.4\mu\text{m}$, $3.2\mu\text{m}$ and $4.7\mu\text{m}$ (Trans NW, Inv NW, Pwidth respectively).

Figure 5 shows the final layout of the DETFF its easily visible that this is towards the limit of gate size for the given layout in particular in crowded areas such as the between gates 6 and 7. The option of using MET3 in this area was considered

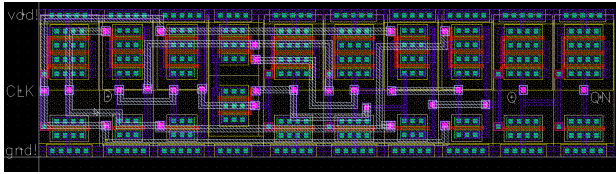


Figure 5. DETFF Layout.

but it was not specified this layer was available for use also as a consideration to real world manufacture having to add another metal layer because of a single gate when a 2 layer design is possible would not be viable.

The layout of the design initial versions of the Transmission and inverter were laid out at the minimum possible width and copied to populate the design and as interconnects were placed some of them had the wells expanded to allow for interconnect spacing. The pull-up PMOS are stacked vertically so as to not waste horizontal space as the rail distance is fixed meaning total area is effected by the width of the entire gate.

VI. C ELEMENT

VII. DUAL RAIL AND

The design goal for the Dual Rail AND was small area. The design was chosen based on its simplicity and the fact that the C-Element had the same goal of small area. This fact allowed us to simply reuse the C-Element with fixed parameters and reuse its layout saving substantial amounts of work in layout. there is a disparity between the Required fan-outs however as the fanout of the c-element is two and the AND has a fanout of one meaning the extra area gained is not too great.

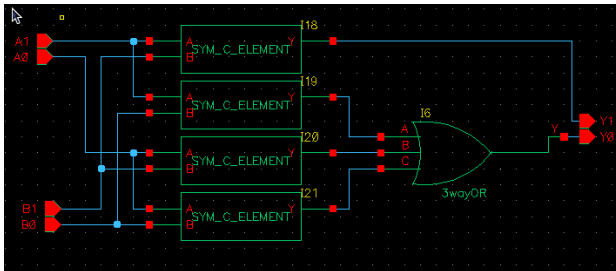


Figure 6. Dual Rail AND Schematic.

The only element in this design that required optimisation in design was the 3 input OR gate. This was constructed from a 3 input NOR gate and an inverter on the output. The PMOS and NMOS ratio was set at 3 and the characteristics matched to that of the output of the C-element meaning there should be minimum disparity between the Y0 and Y1 signals. The Nwidth was finalised at $4\mu\text{m}$ This is slightly larger than is strictly necessary but helps reduce the propagation disparity between the outputs.

VIII. 1-BIT SUBTRACTOR

IX. 2-TO-1 MULTIPLEXOR

X. MUTEX ELEMENT

Testing

- XI. NAND
- XII. NOR2
- XIII. XOR2
- XIV. DFF

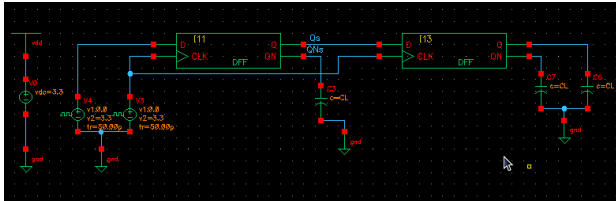


Figure 7. DFF Test Circuit Schematic.

XV. DUEL EDGE TRIGGERED FLIP FLOP

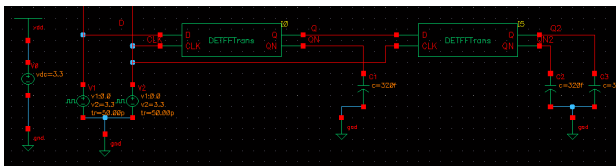


Figure 8. DETFF Test Circuit Schematic.

- XVI. C ELEMENT
- XVII. DUAL RAIL AND

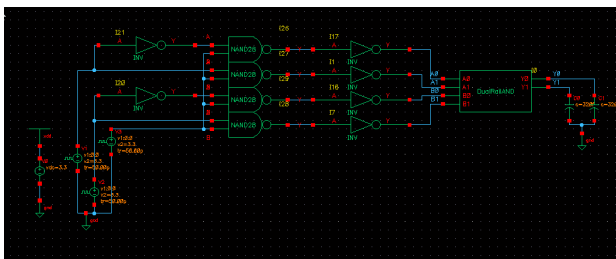


Figure 9. Dual Rail AND Test Schematic.

- XVIII. 1-BIT SUBTRACTOR
- XIX. 2-TO-1 MULTIPLEXOR
- XX. MUTEX ELEMENT

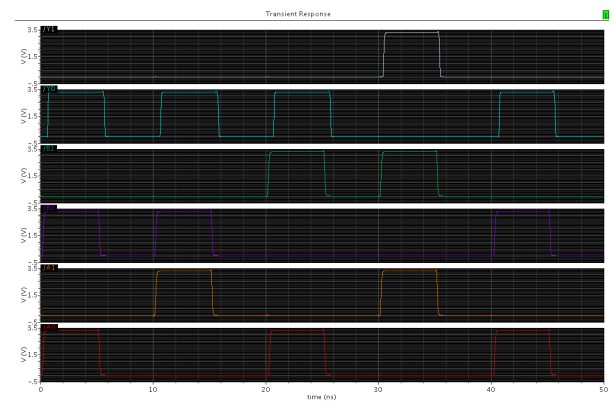


Figure 10. Dual Rail AND Simulation showing correct operation.

Impact of Variability

XXI. NAND

XXII. NOR2

XXIII. XOR2

XXIV. DFF

XXV. DUEL EDGE TRIGGERED FLIP FLOP

XXVI. C ELEMENT

XXVII. DUAL RAIL AND

XXVIII. 1-BIT SUBTRACTOR

XXIX. 2-TO-1 MULTIPLEXOR

XXX. MUTEX ELEMENT

Conclusions