Custom IC Design Assignment 1

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***Abstract*—Abstract goes here. Use this latex template as our report template.**

Outline

I. NAND LOGIC GATE

In this exercise the design of the NAND gate was expected to have minimum area while to have high fanout output(fanout =8). In order to find the delay time between input and output of the NAND gate, the Elmore Delay model **?** was used in the design.

A. Design and Optimization

As shown in the Figure 1, NAND gate is constructed by two parallel connected PMOS transistors and two serial connected NMOS transistors.

Although transistors have complicate current-voltage behaviour, turned on transistors can be assumed as resistors, a chain of transistors can be represented as an RC ladder, as shown in Figure 2. Therefore the Elmore delay model can estimate the delay of this RC ladder in terms of the path resistance and capacitance of a node on the ladder and the supply:

$$t_{\text{pd}} = \sum_i Rn{-}iCi \tag{1}$$

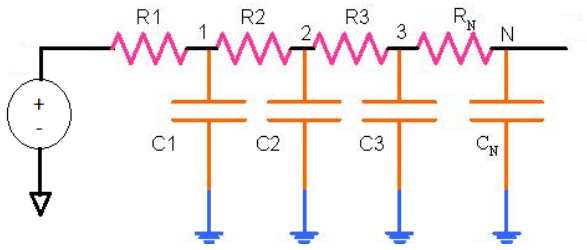


Figure 2. Simple Elmore delay model

Therefore it is possible to use this method as the reference to calculate the width of logic gate, since the propagation delay is dependent to it and the capacitance of the load.
Typically in the logic gate, for parallel connected transistors, the total resistance is lower when they are all on. In many gates, the worst-case delay is usually because only on the parallel transistor is on **?**. So when applying the Elmore delay model in the NAND design, one of input is connected to vdd while the other one is connected in the path, as shown in Figure 3.

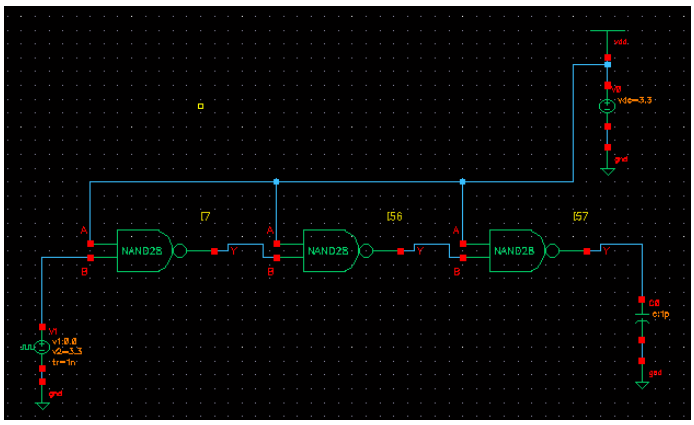


Figure 3. NAND Elmore delay model

While deceasing the width of NMOS and increasing the width of PMOS, the propagation delays, which is the maximum time from input to output crossing 50%, of the rising edge and falling edge are also changing. When the certain ratio between the width of PMOS and NMOS is reached, the propagation delay between rising edge and falling edge of logic gate will become similar. In another word, the signal slope at the output of logic gate will become quite identical to the input, only with an amount of delay.
In this design, the ratio between PMOS and NMOS is at 2.3, as found in the Figure 4.

If a gate can drive n copies of itself, then it is said to have a fanout or electrical effort of n. When multiple gates are chain connected together, they could form a multi-stage logic network, the logical effort of logic gate is independent of size of next connected gate but the electrical effort is not. Therefore the ratio between size of PMOS and NMOS found previously is still legitimate for the design, but it is possible to find the speed of logic gate with fanout by using the multi-stage logic network gate.
A multi-stage logic network can be easily converted into a ring oscillator, which is often used as a process monitor to judge if a logic gate is fast or not. As shown in the Figure 5, the NAND gate is connected in serial to construct a ring oscillator, with 8 fanout gate attached to each stage.

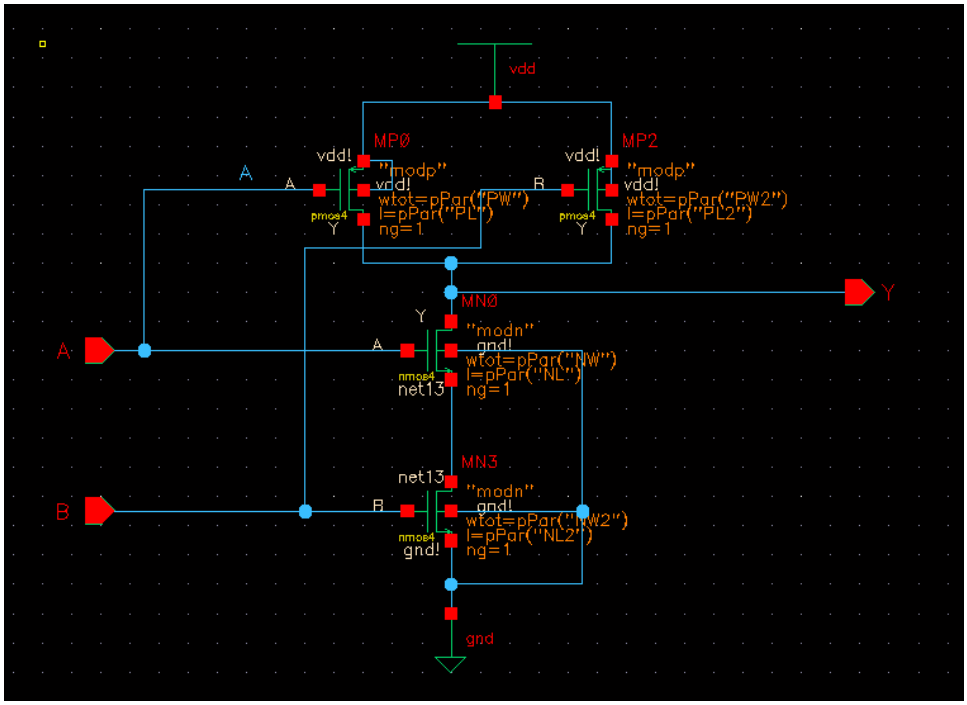


Figure 1. NAND gate schematic

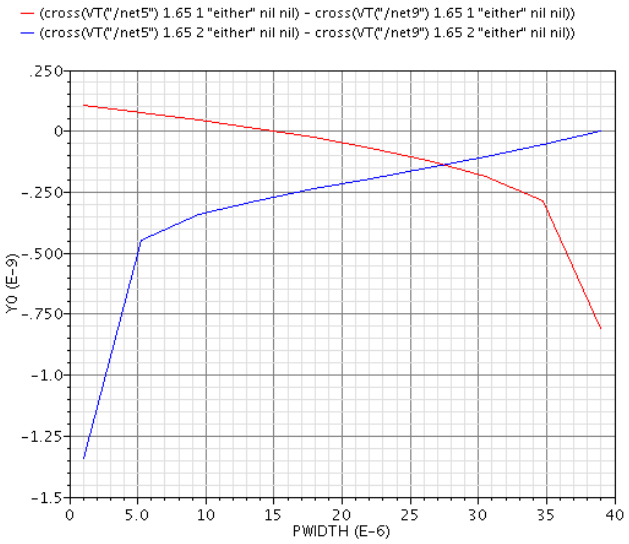


Figure 4. Ratio of width of PMOS and NMOS in NAND gate

According to the frequency diagram obtained in Figure 6, the width of NMOS is set at 2.4um to achieve small area design without too much performance degradation.

B. Testing

To the functionality of the design, two vpulse sources were used. One of input pulses has twice the period than another one so all possible input combinations can be generated, as shown in the Figure 7

The result (Figure 8) shows that the NAND gate design is functioning properly with input signal at 100Mhz. The rise up time is approximate 8ns, which is similar to general manufactured NANDs in the industry . Further decreasing the width of transistors will cause output signal fail to reach the voltage level on time, as shown in Figure 9

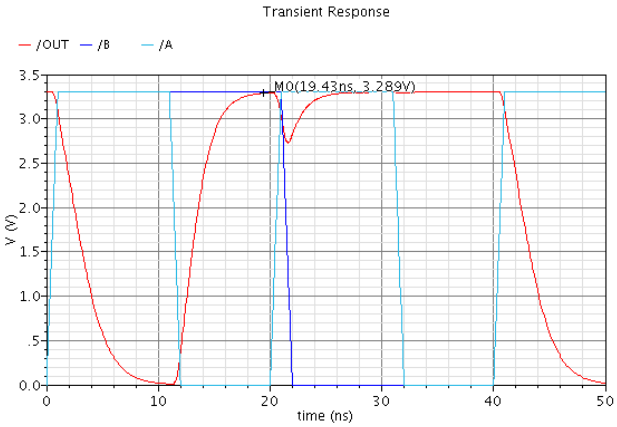


Figure 8. Correct function of NAND gate

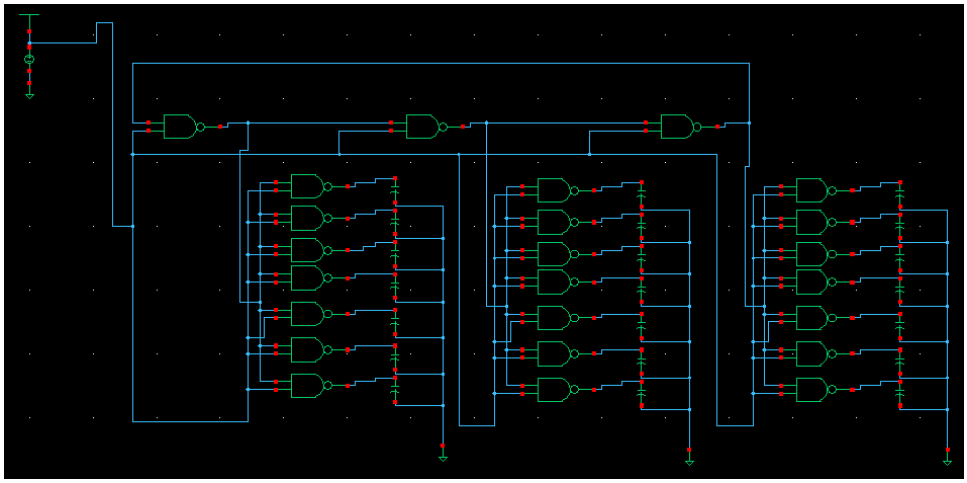


Figure 5. NAND ring oscillator with fanout 8

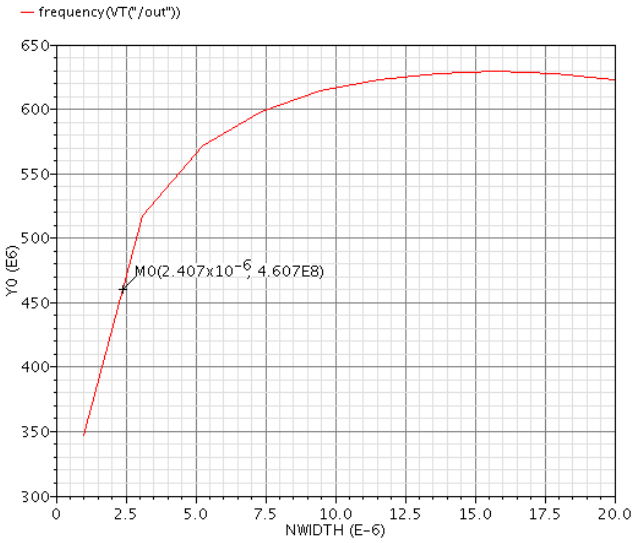


Figure 6. Frequency of NAND gate in the Ring Oscillator

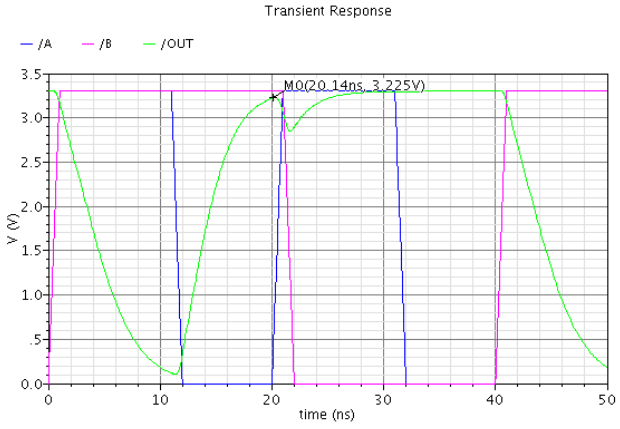


Figure 9. NAND gate is too slow

Design and Optimisation

II. NAND

III. NOR2

IV. XOR2

V. DFF

The design goal for the DFF was high speed. Initially it was designed using a standard circuit composed of NAND gates. However then the option of Transmission gates was considered and found to be superior. Using transmission gates a master slave style flip plot was produced as shown in figure 10. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is simply 3 times that.

In terms of transistor sizes the Transmission gate and the Inverters were considered as separate parameters although there was only one size for each family This may have been a bad decision in terms of the inverter creating CLKN as it has to drive 4 components where as the maximum of any other gate was only 2, However in this situation it was not much of a problem as the relatively large transistor sizes chosen to deliver high speed negated much of this effect.

By using the rise times, as shown in figure 11, among other metrics when measured in the test circuit Values for NMOS and PMOS widths were chosen based on giving maximum performance. These turned out to be a 11μm for the transmission gate and 17.5 μm for the inverter. This is quite large but as the only restriction on the design is that it must be high speed regardless of area.

One point of note is that the QN output is created via a separate inverter rather than taking the signal from either side of the left most transmission gate. This was because large capacitive loads on QN caused incorrect circuit behaviour as this effected the transition time across the transmission gate which incorrect circuit behaviour on extreme loads where the slave circuit wouldn't latch new master value.

Due to the large transistor size layout was not particularly difficult as there was a lot of space for gate interconnects.

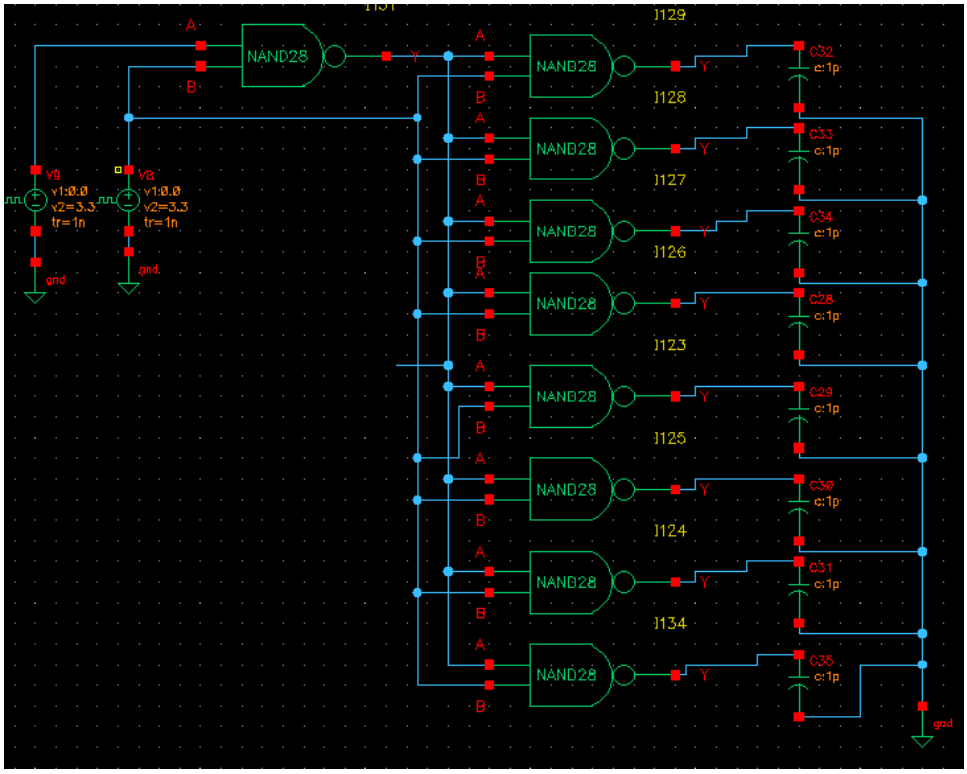


Figure 7. NAND28 test circuit

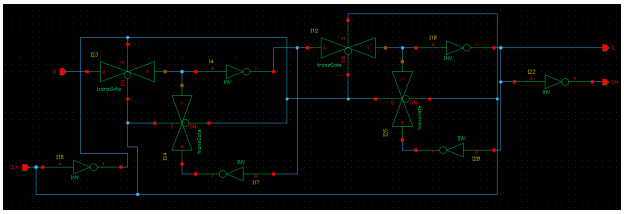
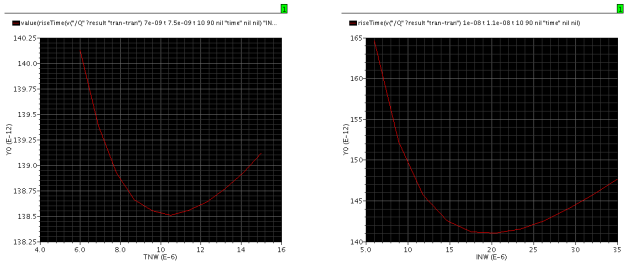


Figure 10. DFF Schematic.



(a) Inverter N Width (b) Transmission gate N Width

Figure 11. Transistor size effect on rise time.

When laying out the gates were placed in an order such as to minimise local process variations however with such large gates this is not particularly effective. A future layout revision could increase robustness by splitting the transistors into 2 or 3 smaller transistors of equal total size and interleaving them.

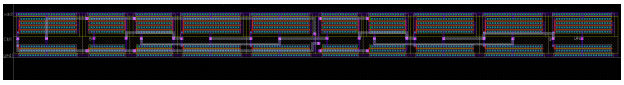


Figure 12. DFF Layout.

VI. Duel Edge Triggered Flip Flop

The Dual Edge Triggered Flip Flop (DETFF) was designed using transmission gates as this allows the design to contain a minimum of 20 transistors (18 if there is no requirement for QN). Figure 13 shows the schematic produced. A ratio between PMOS and NMOS of 3 was chosen as it is the integer ratio which produced the best results for rise and fall time matching. As 0.35μ is the length set by the technology used the only parameter used is NWIDTH for each gate as PWIDTH is 3 times that.

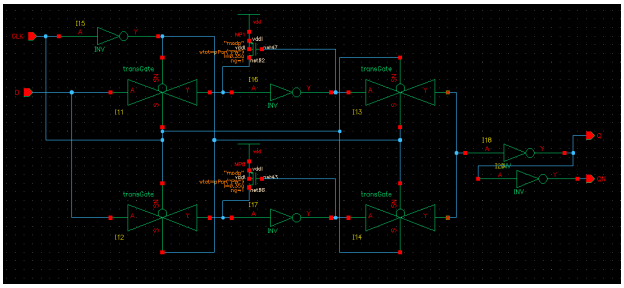


Figure 13. DETFF Schematic.

The size of the gates where considered in terms of Transmission gates NMOS Width, Inverters NMOS Width and the

2 PMOS pull up transistors width. These parameters were brought to minimum values of 1.2μm 2μm and 4μm (Trans NW,Inv NW,Pwidth respectively) before correct operation ceased. However these values were found to be to small for effective layout without enough space for interconnects and routing to fit due to DRC constraints, they also gave speed performance deemed unacceptable. The sizes were increased until sensible routing and speed was achieved at values of 2.4μm 3.2μm and 4.7μm (Trans NW,Inv NW,Pwidth respectively).

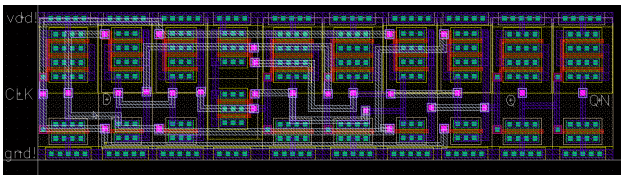


Figure 14. DETFF Layout.

Figure 14 shows the final layout of the DETFF its easily visible that this is towards the limit of gate size for the given layout in particular in crowded areas such as the between gates 6 and 7. The option of using MET3 in this area was considered but it was not specified this layer was available for use also as a consideration to real world manufacture having to add another metal layer because of a single gate when a 2 layer design is possible would not be viable.

The layout of the design initial versions of the Transmission and inverter were lain out at the minimum possible width and copied to populate the design and as interconnects were placed some of them had the wells expanded to allow for interconnect spacing.The pull-up PMOS are stacked vertically so as to not waste horizontal space as the rail distance is fixed meaning total area is effected by the width of the entire gate.

VII. C Element

VIII. Dual Rail AND

The design goal for the Dual Rail AND was small area. The design was chosen based on its simplicity and the fact that the C-Element had the same goal of small area. This fact allowed us to simply reuse the C-Element with fixed parameters and reuse its layout saving substantial amounts of work in layout. there is a disparity between the Required fan-outs however as the fanout of the c-element is two and the AND has a fanout of one meaning the extra area gained is not too great.

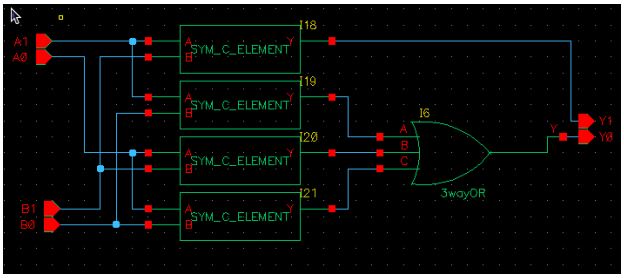


Figure 15. Dual Rail AND Schematic.

The only element in this design that required optimisation in design was the 3 input OR gate. This was constructed from a 3 input NOR gate and an inverter on the output. The PMOS and NMOS ratio was set at 3 and the characteristics matched to that of the output of the C-element meaning there should be minimum disparity between the Y0 and Y1 signals. The Nwidth was finalised at 4μm This is slightly larger than is strictly necessary but helps reduce the propagation disparity between the outputs.

IX. 1-bit Subtractor

X. 2-to-1 Multiplexor

XI. Mutex Element

Testing

XII. NAND

XIII. NOR2

XIV. XOR2

XV. DFF

TEST CIRCUIT
FUNCTIONALITY TESTING
SPEED TESTING
LAYOUT VS SCHEMATIC
ERRONIOUS BEHAVIOUR

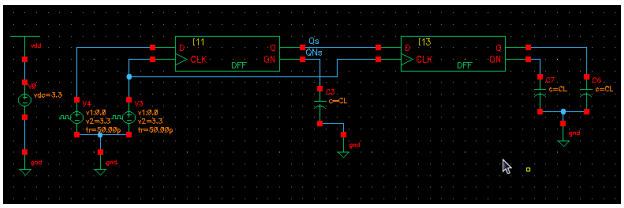


Figure 16. DFF Test Circuit Schematic.

XVI. Duel Edge Triggered Flip Flop

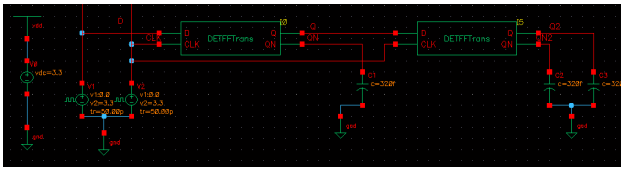


Figure 17. DETFF Test Circuit Schematic.

XVII. C Element

XVIII. Dual Rail AND

TEST CIRCUIT
FUNCTIONALITY TESTING
SPEED TESTING
LAYOUT VS SCHEMATIC
ERRONIOUS BEHAVIOUR

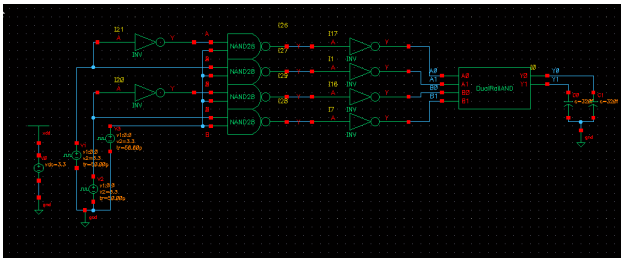


Figure 18. Dual Rail AND Test Schematic.

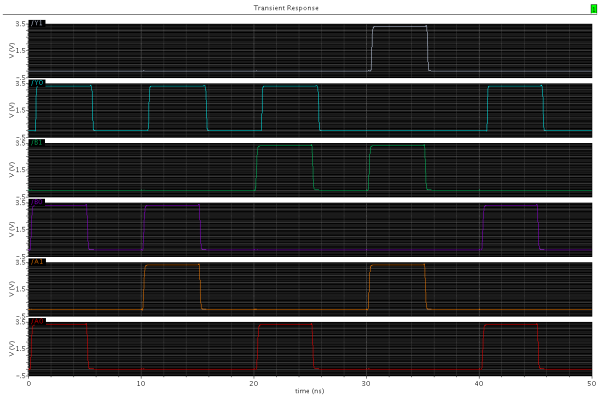


Figure 19. Dual Rail AND Simulation showing correct operation.

XIX. 1-bit Subtractor

XX. 2-to-1 Multiplexor

XXI. Mutex Element

Impact of Variablility

XXII. NAND

XXIII. NOR2

XXIV. XOR2

XXV. DFF

VDD
TEMP

XXVI. Duel Edge Triggered Flip Flop

VDD
TEMP

XXVII. C Element

XXVIII. Dual Rail AND

XXIX. 1-bit Subtractor

XXX. 2-to-1 Multiplexor

XXXI. Mutex Element

Conclusions

References