# Design

The design goal for the Mutex Element (Arbiter) is high speed. The schematic of the design is shown in the figure 1 below. The implementation, as shown in the figure, involves a pair of cross coupled NAND gates and a metastability filter. One input is enabled while the other input is blocked considering the operation of NAND. When both inputs are asserted high at the same time, the circuit becomes metastable as two outputs of the NAND gates stick halfway between supply and ground. These undefined values would be prevented from propagating to the outputs by the metastability filter.



Figure Schematic for MUTEX

The ratio between width of PMOS and NMOS is chosen by swapping the ratio to achieve the best results for rise and fall time matching. The configuring method and the results are in the figures below. And the ratio of 4 is chosen as an integer value is more reliable in design.



Figure Test circuit to find out ratio

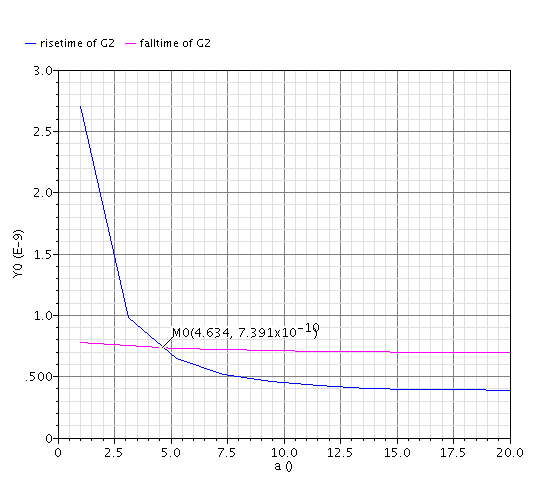


Figure Test results for the ratio

To find out the value of NWIDTH to achieve the design goal of high speed, a transient test with fan out of 2 is taken on one output with fall time and rise time against the change of NWIDTH. The test circuits and results are shown below.



Figure Test curcuit to find NWIDTH

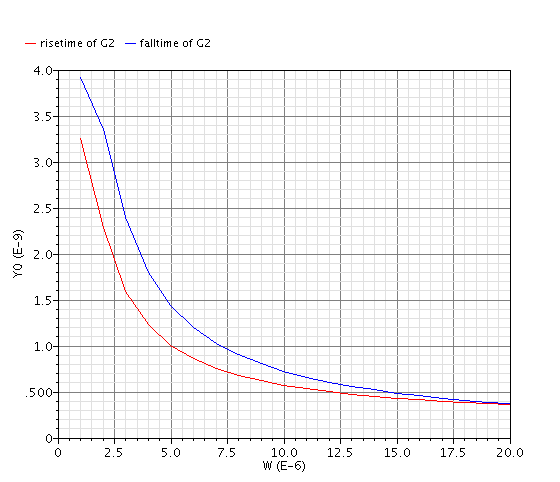


Figure Test results for NWIDTH

As can be seen from the test results, the slope of fall and rise time is initially sharp in the range of NWIDTH smaller than 5um and goes flat after NWIDTH is larger than 5um. Therefore, the value of 5um can be taken as the critical point which balances the area of the design as well as keeps the high speed property of the design. The NWIDTH is chosen as 5um and the PWIDTH is of 20um as 3 times the value. The final layout of MUTEX is then produced as following Figure.



Figure Layout of MUTEX

# Testing

For testing the function of both schematic and layout, transient analysis is launched and the results are stick in the figures below. For MUTEX, the task of it is to pass the inputs to the corresponding outputs (like R1 to G1) that at most one output is active at any given time. If only one input request arrives the operation is trivial. If one input request arrives before the other, the front request has a higher property and the latter request is blocked till the front one is de-asserted. The output signals and input signals in Figure 7 shows the operation of design element exactly meet the operation of MUTEX indicating the schematic of the MUTEX design has the correct function. Also, the output in Figure 8 suggests little difference between the layout output and the correct schematic output which indicates a good design of layout. This design can be further improved with adding buffer onto the outputs.

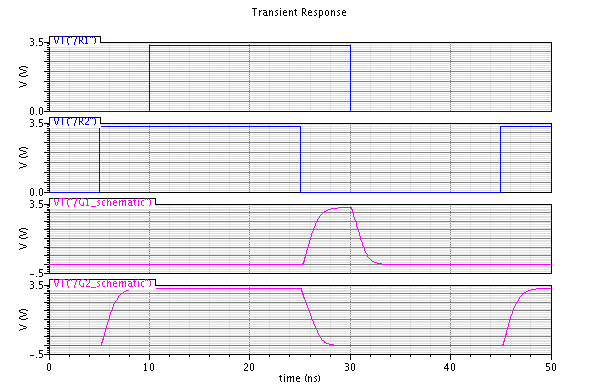


Figure MUTEX Schematic Simulation

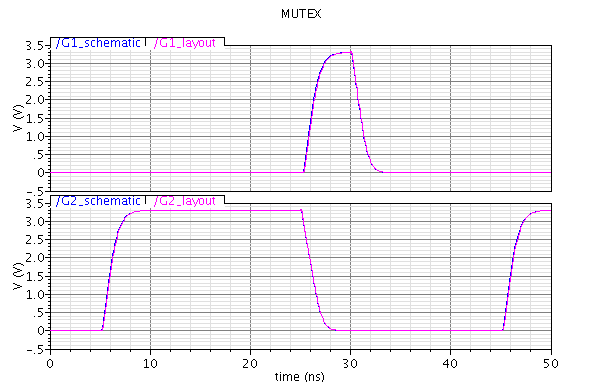


Figure MUTEX Layout Simulation

# Impact of Variability

## Temperature Variations

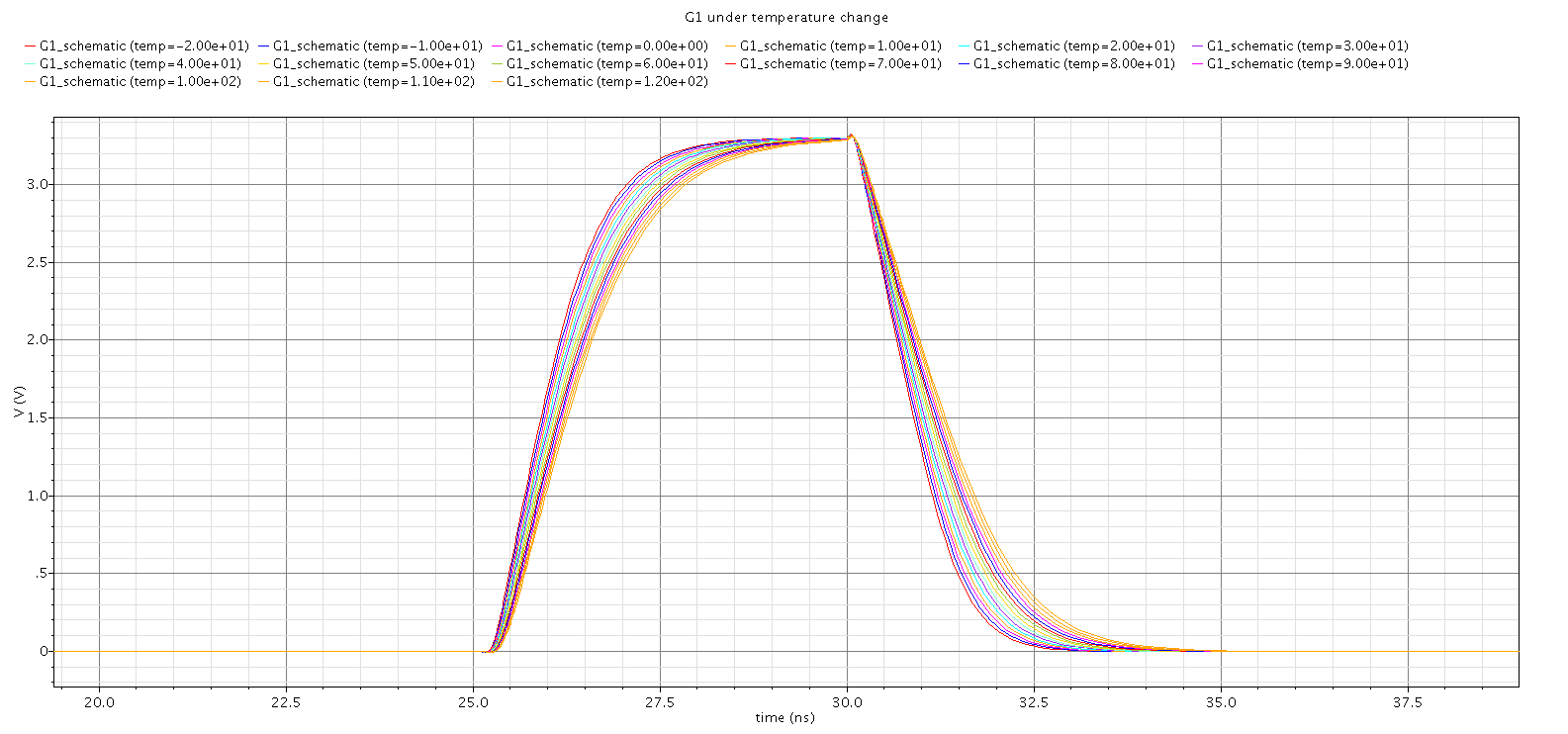


Figure 9 Transient Simulation with Temperature Swapping for MUTEX

This Figure indicates the rise and fall time of the output differs under different temperature. It is indicated that with a higher temperature the rise time and fall time increases leading to a longer propagation delay.

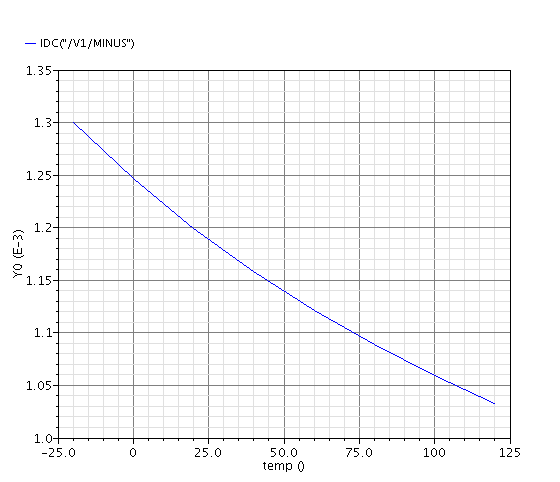


Figure 10 DC simulation with Temperature Swapping for MUTEX

This Figure shows that the current supply drops linearly when the temperature increases. The possible reason is that when both inputs are asserted, the MUTEX enters a metastable state.

## Power supply Variations

As the design requirement is high speed, the difference of supply voltage will not influence the performance of the design as is described in the previous XOR design. The change of power supply influences significantly the current supply of the circuit as can been seen in the figure below that the current supply increases linearly with the increase of power supply.

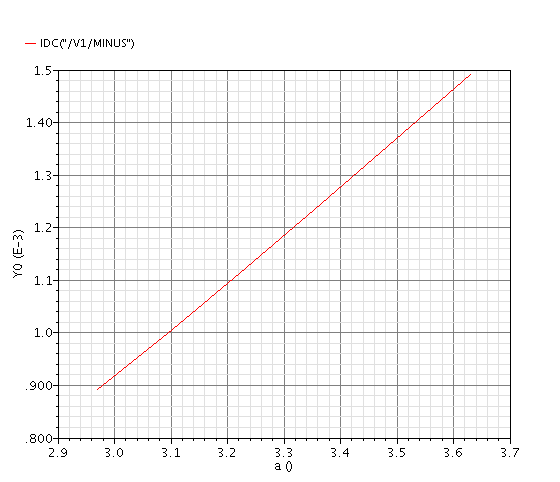


Figure 11 DC simulation with VDD Swapping for MUTEX